20th CSEC – Past Year Paper Solution (2017 – 2018 Sem 1)
CE/CZ1006 – Computer Organisation and Architecture

Question 1

a) Note that the **C flag is set** in the initial contents of SR. Therefore, the C flag will remain set after executing operations such as MOV, which cannot affect the C flag. Refer to the instruction chart for what flags are affected by each instruction.

i. MOV R0, #0xFFB
R0 = 0XFFB SR = 0x005

ii. MOV RO, [R1]
RO = 0x000 SR = 0x003

iii. AND RO, [R2 +2]
R0 = 0x602 SR = 0x001

iv. ADD R0, R3
R0 = 0x8E1 SR = 0x00C

v. RRC R0
R0 = 0xB89 SR = 0x004

b) The following table shows the step-by-step execution of the instructions in Figure Q1b. Any changes in register/memory content are shown in **bold**.

Instruction	R0	R2	SR	PC	[0x052]
MOV R2, #0x050	0x000	**0x050**	0x000	**0x002**	0x000
MOV R0, #1	**0x001**	0x050	0x000	**0x004**	0x000
ADD R0, [R2+0]	**0x004**	0x050	0x000	**0x006**	0x000
CMP R0, [0X051]	0x004	0x050	**0x004**	**0x008**	0x000
JGE EXIT	0x004	0x050	0x004	**0x009**	0x000
MOV PC, #0x004	0x004	0x050	0x004	**0x004**	0x000
ADD R0, [R2+0]	**0x007**	0x050	**0x000**	**0x006**	0x000
CMP R0, [0X051]	0x007	0x050	**0x004**	**0x008**	0x000
JGE Exit	0x007	0x050	0x004	**0x009**	0x000
MOV PC, #0x004	0x007	0x050	0x004	**0x004**	0x000
ADD R0, [R2+0]	**0x00A**	0x050	0x004	**0x006**	0x000
CMP R0, [0X051]	0x00A	0x050	**0x001**	**0x008**	0x000
JGE Exit	0x00A	0x050	0x001	**0x00B**	0x000
MOV [R2+2], R0	0x00A	0x050	0x001	**0x00D**	**0x00A**

c) We can create a position independent version by making use of PC- related addressing.

```
Start   MOV R2, [PC + 0x04E]
        MOV R0, #1
        ADD R0, [R2+0]
        CMP R0, [R2+1]
        JLT -5
Exit    MOV [R2+2], R0
```

Question 2

a) (I1) PSHM 7
(I2) MOV R1, [SP+5]
(I3) MOV R2, [SP+4]
(I4) ADD SP, #2
(I5) POPM 7
(I6) RET

b) R0 = 0x005, PC = 0x00C, SP = 0xFFD, RESULT = 0x009
We can immediately deduce the content of PC, R0 and SP without tracing the program.
The contents of all the registers used in subroutine SubA have been restored upon returning to the main program, hence R0 will contain its initial content of 0x005.
As the instruction on the label Done has yet to be executed, PC will point at the start address of Done, which is 0x00C.
Currently, the parameters pushed before calling the subroutine have yet to be removed. As SP initially points at 0xFFF and 2 parameters were pushed, SP will point at 0xFFD.
The subroutine will calculate the sum of all the odd numbers between 0 and X (inclusive) and store in the memory variable RESULT. Since X is 5, the operation will be 5 + 3 + 1 = 9.

c)

```
Begin   MOV SP, # 0xFFF
        PSH #5
        MOVS [0X200], #0
        CALL SubA
Done    :
SubA    PSHM 3
        MOV R1, [SP+3]
        MOV R0, R1
        AND R0, #0x001
Skip1   DEC R1
        JEQ Skip2
        PSH R1
        CALL SubA
        ADD SP, #1
Skip2   POPM 3
        RET
```

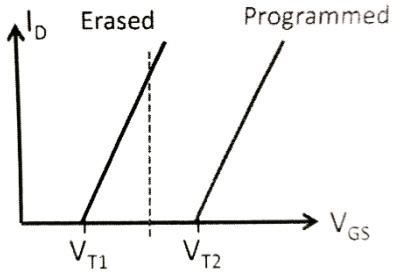
Question 3

a) Main Storage Memory for Commercial Company's Data Centre
Memory Type: Magnetic HDD
Reason: Magnetic HDDs can support high storage capacity in a more affordable price, making it good for commercial use. Its infinite amount of erasure cycles also allows the data to be updated regularly according to the company's needs.

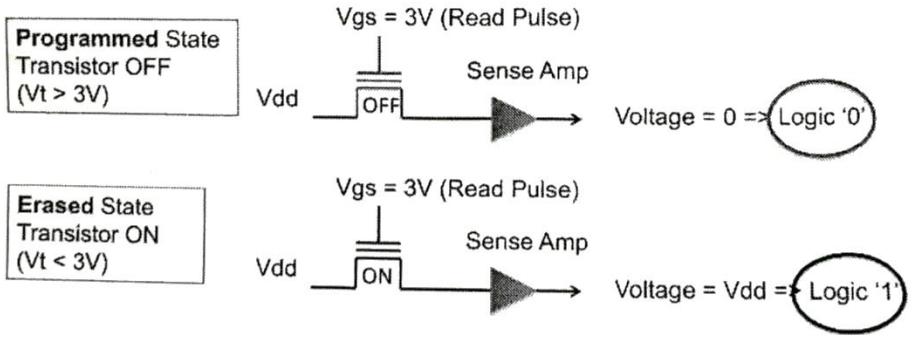
External System Memory for a processor that does not have any internal (on-chip) memory. Product powers on/off weekly.
Memory Type: NOR Flash
Reason: As the processor does not have any internal memory, we will require some space in the external memory to store instructions/programs. Using NOR Flash is suitable for this as it supports XIP (Execute in Place) so that program code can be executed directly. It also behaves similarly to an SRAM during read operation.

Very High Speed internal memory of a high end processor
Memory Type: DRAM
Reason: DRAM is more commonly used as main memory as compared to SRAM. While SRAM is faster, it is significantly more expensive than DRAM hence it is only implemented in limited sizes such as cache memory.

b) At any point in time, a Floating Gate Transistor can only be either in the Erased state or Programmed state. In both states, the transistor has a certain threshold voltage (Vt) in which the Gate-Source Voltage (Vgs) must surpass Vt to allow current to flow through the transistor. Vt Programmed state > Vt Erased State.



Thus, we can apply Vgs that lies between the Erased state threshold voltage and Programmed state threshold voltage to determine the current state of the transistor. This is the Read pulse. If the transistor is on Erased state, it will be enabled and the Sense Amplifier will detect an electrical conduction, indicating a logic'1'. Instead, if t is in Programmed state, no electrical conduction will be found, indicating a logic '0'.



(images are taken from lecture notes)

c) SPI is a synchronous data transfer protocol while UART is asynchronous. SPI is able to transfer any number of bits in a continuous stream without any interruption. UART transfers data in packets instead, each containing a fixed number if bits, including data overhead that will interrupt the transmission. When transferring data of the same size, using UART protocol requires transferring a greater number of bits than SPI due to necessary data overhead. All this limits the maximum transfer rate that can be achieved using UART, making it significantly lower than SPI.

d) This statement can be valid for when both laptops are used to run the exact same programs, hence executing the exact same instructions, requiring the same number of clock cycles. In this case, the laptop with higher clock frequency will take less time for every clock cycle and the program will run faster.

However, this statement may also not be valid because execution time, and ultimately the laptop's performance, does not solely depend on clock frequency. Different programs will have instruction with different complexity and average number of clock cycles. In addition, other factors, such as run time issues (cache miss, branching/looping) need to be considered.

e)

Data transmitted by COMP-B		
Start	Data (LSB to MSB)	Stop
0	1011 0000	1
Data transmitted by COMP-A		
Start	Data (LSB to MSB)	Stop
0	0011 1000	1

We can observe that every bit transferred by COMP-B is oversampled by COMP-A by 3 times. Therefore, the baud rate of COMP-A must be 3 times that of COMP-B.
So, the baud rate of COMP-B is 115200/3 = 38400.

Question 4

a) The purpose of Cache memory is to improve system performance by storing recently used data closer to the CPU so that it can be accessed faster, By the Locality of Space principle, Code/Data that is close to each other is likely to be accessed together. Thus, when the CPU requires a particular byte, there is a high chance that the bytes nearby (those in the same cache block) will soon be needed as well, so the entire cache block is transferred.

b) Main Memory Size = 1Mbyte = 2^{20} bytes, so the MM address is 20 bits long.
Cache Block Size = 32 bytes = 2^5bytes, so last 5 bits of MM address will indicate Offset.
Cache Size = 256 bytes, so the number of Cache Blocks = 256/32 = 8 Blocks:
Hence 3 bits will be used to indicate Block value, and the remaining bits will indicate the Tag value. The TAG-BLOCK-OFFSET format is 11-3-5.

MM address 0x00999 = 0000000001001 100 11001
It will map the Block 0x100 while the Tag value is 0x009.

c) Fixed Point Representation
- Advantage: Fixed precision within the entire range of representable numbers.
- Disadvantage: As the number of bits allocated for both integers and fractional values are fixed, some of the bits may not be fully utilized when certain values are being represented.

Floating Point Representation

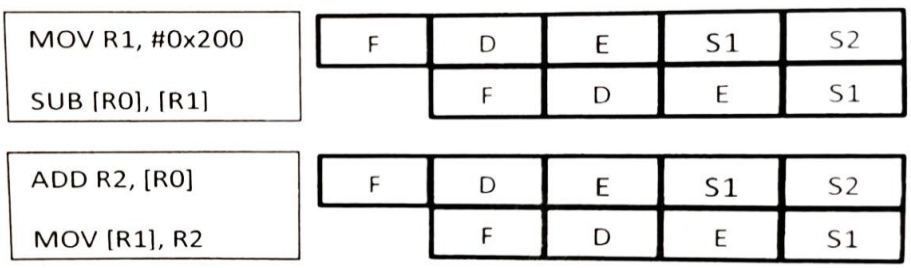
- Advantage: Provide a very large range of representable numbers by sacrificing precision for larger numbers
- Disadvantage: Rounding error may occur especially for computation using larger numbers

d)

i) Between I3 and I4 (R1 as the destination operand of I3 and source operand of I4)
Between I7 and I8 (R2 as the destination operand of I7 and source operand of I8)

ii) There are two possible modifications:
- Inserting a NOP instruction between I3 and I4 and between I7 and I8.
- Adding hardware circuitry that will stall the pipeline when data dependency is detected.

iii) R1 will be updated on stage S1 of I3, where at the same time I4 reaches stage E. Likewise, R2 will be updated on stage S1 of I7, where at the same tie I8 reaches stage E. Hence, the data dependencies still exit.



==End of Answers==

Solver: Emmanuelle Vania

Email Address: emma0006@e.ntu.edu .sg