CE2003 Digital Systems Design 17/18 Sem 2

Solutions

1a)

**Synthesis**: Behavioural description will be translated into hardware blocks, logic will be minimized, hardware structures such as multiplexers and memories are identified by the tool. Netlist, a representation using basic logic blocks will be produced.

**Mapping**: Netlist is mapped. Combinational logic is converted into LUTs, Synchronous components are mapped to registers inside CLBs, Memories are mapped to Block RAMs.

**Place and Route**: The mapped netlist will be assigned to locations on the FPGA/tool, connections will be set up between blocks. This process will be repeated internally to optimize timing/performance.

b) (i) $C_3 = g_2 \mid p_2 \,\&\, C_2$

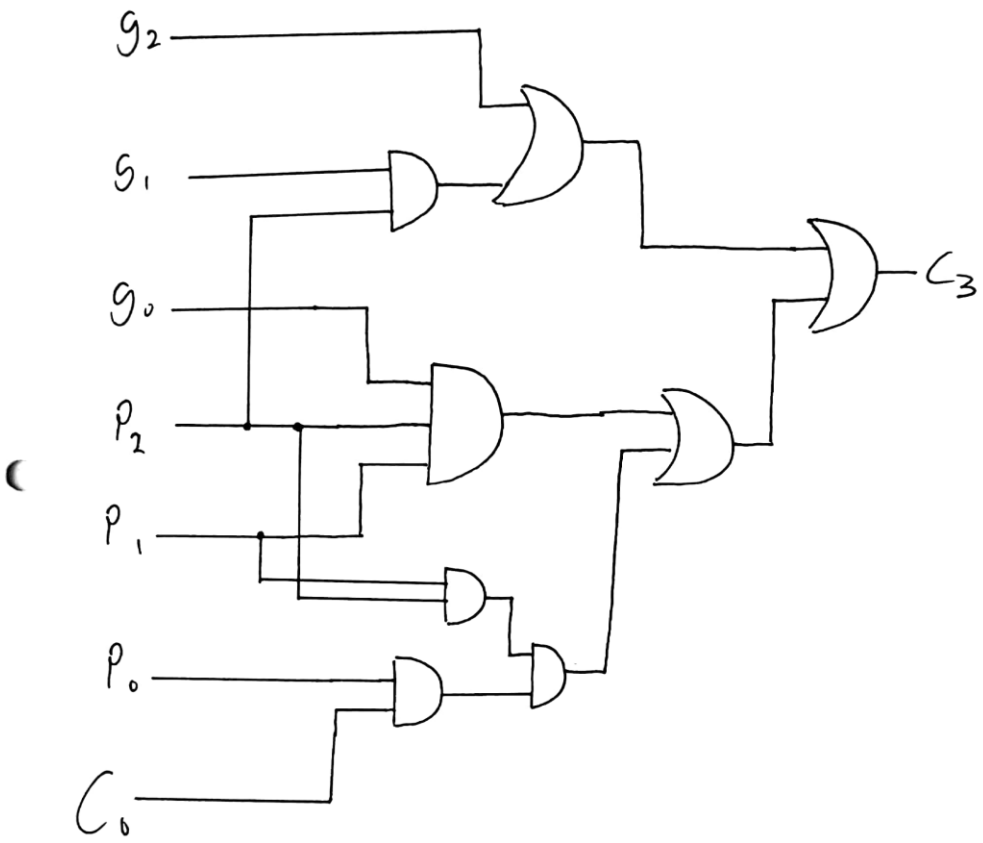
$= g_2 \mid p_2 \,\&\, (g_1 \mid p_1 \,\&\, C_1)$

$= g_2 \mid p_2 \,\&\, (g_1 \mid p_1 \,\&\, (g_0 \mid p_0 \,\&\, C_0))$

$= g_2 \mid p_2 \,\&\, (g_1 \mid p_1 \,\&\, g_0 \mid p_1 \,\&\, p_0 \,\&\, C_0)$

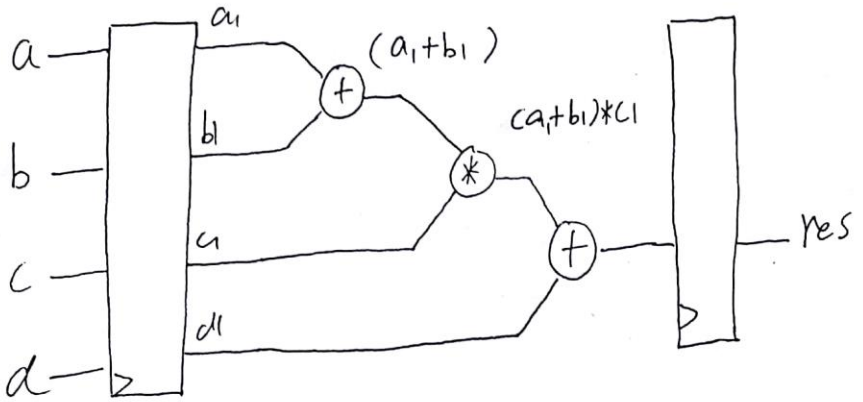
$= g_2 \mid p_2 \,\&\, g_1 \mid p_2 \,\&\, p_1 \,\&\, g_0 \mid p_2 \,\&\, p_1 \,\&\, p_0 \,\&\, C_0$

1 b)(ii)

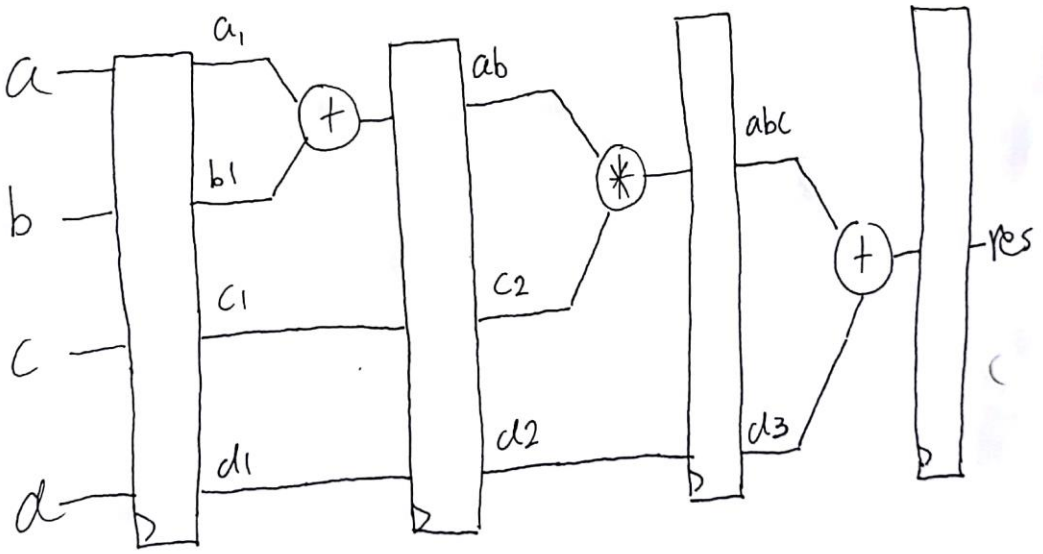



(iii) In a CLA, unlike standard ripple adder, carry out bits are determined by the inputs, then, each section of addition does not need to wait for the previous section to finish computation to propagate a carry bit. This will be very efficient when computing large numbers. Not applicable to FPGA because it uses hard blocks for logic implementation.

2a)


a
b
c
d
a1
b1
c1
d1
(a1+b1)
(a1+b1)*c1
res

b)


a
b
c
d
a1
b1
c1
d1
ab
c2
d2
abc
d3
res

```
always @ (posedge clk) begin
        if (rst) begin
        ‟
        ‟
        end else begin
                a1 <= a; b1<= b;
                c1 <= c; d1<= d;
                ab<= (a1 + b1); c2 <= c1; d2 <= d1;
                abc <= (ab * c2); d3 <= d2;
                res <= (abc + d2);
        end
end
```

c) (i)

Original Cct:

Max Freq = 1 / 5ns = 200 Mhz

Mod cct:

Max Freq = 1 / 3ns = 333.3 Mhz

(ii) Latency of Mod cct : 3 clock cycles , 9ns

(iii) $T_{min}$ = 0.6ns + 0.3ns + 0.1ns + 3ns = 4ns

Max Freq = 1 / 4ns = 250 Mhz

d)

ab : (3 int . 9 frac) + (3 int . 9 frac) + 1 int for overflow

4 int . 9 frac

ab * c2 : (4 int . 9 frac) * (5 int. 7 frac)

9 int . 16 frac

abc + d3: (9 int . 16 frac) + 1 int for overflow (since d3 is suitably aligned)

10 int . 16 frac

Keep 16 bits: 10 int . 6 frac

Range = $-2^{10-1}$ to $2^{10-1} - 2^{-6}$

= -512 to 511.984

e) The DSP block because it supports cumulative operation at high speed and saves space for other computational blocks.

3a)

**first bgt**: $1 = #0; $3 = #0; $2 = #0

**second bgt**: $1 = #0; $3 = #0; $2 = #1

**third bgt**: $1 = #0; $3 = #0; $2 = #3

**fourth bgt**: $1 = #0; $3 = #1; $2 = #7

$1 = #1; $3 = #4; $2 = #7;

**bgt** was executed 4 times

b)

**first bgt**: $1 = #0; $3 = #0; $2 = #0

**second bgt**: $1 = #0; $3 = #0; $2 = #1

**third bgt**: $1 = #0; $3 = #1; $2 = #3

**lli**: $3 = #4

$1 = #1; $3 = #4; $2 = #7

**bgt** was executed 3 times

4 a)

$$y_1^+ = y_1 \cdot \bar{w}_2 + w_1 \cdot \bar{w}_2 + y_2 \cdot y_1 \cdot \bar{w}_1$$

$$y_2^+ = w_2 + y_2 \cdot w_1 + y_1 \cdot \bar{w}_1$$

$z = y_2$

for $y_1^+$

| $y_2y_1$ \ $w_2w_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 0 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 |

for $y_2^+$

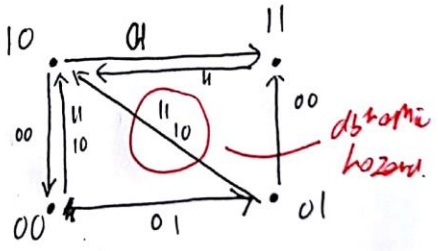
| $y_2y_1$ \ $w_2w_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 1 |
| 01 | 1 | 0 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 |

static hazard

We can see that not all prime implicands are included for $y_2^+$. Hence, a static hazard. (rectangular box was not covered at first.)

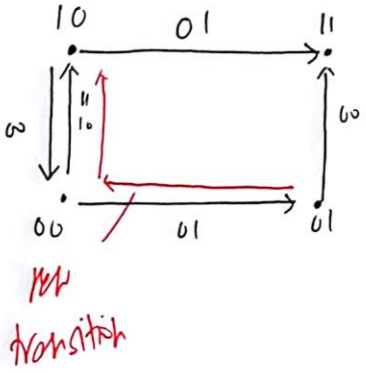
Next state $y_2^+ y_1^+$

| present state $y_2y_1$ \ input: $w_2w_1$ | 00 | 01 | 11 | 10 | z |
|---|---|---|---|---|---|
| 00 | 00 | 01 | 10 | 10 | 0 |
| 01 | 11 | 01 | 10 | 10 | 0 |
| 11 | 11 | 11 | 10 | 11 | 1 |
| 10 | 00 | 11 | 10 | 10 | 1 |




Unwanted state change, dynamic hazard.

4b) Basically rectify all hazards found.
(DO note that trying to rectify the static hazard first will / might create another hazard, hence determine the hazard free excitation table first)




we get:

| present state $y_2y_1$ | input: $w_2w_1$ 00 | 01 | 11 | 10 | output z |
|---|---|---|---|---|---|
| | $Y_2^+Y_1^+$ | $Y_2^+Y_1^+$ | $Y_2^+Y_1^+$ | $Y_2^+Y_1^+$ | |
| 00 | 00 | 01 | 10 | 10 | 0 |
| 01 | 11 | 01 | 00 | 00 | 0 |
| 11 | 11 | 11 | 10 | 11 | 1 |
| 10 | 00 | 11 | 10 | 10 | 1 |

✱

then,

for $y_2^+$:

| $y_2y_1$ \ $w_2w_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 1 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 |

(include ALL prime implicants)

$$y_2^+ = y_2y_1 + y_2w_1 + y_1w_2 + \bar{y}_1 \cdot w_2 + y_1 \cdot \bar{w}_2 \cdot \bar{w}_1$$

***Solution done by: Alfred Huang***