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1. (a) 8-bit processors matches byte-size data naturally, memories are usually byte-addressable. Typically uses 16-bit address bus to provide sufficient memory space for practical applications. Low cost and power consumptions.

   (b)

   (i) Vector table contains addresses, not instructions, that point to their respective exception handlers (except the first address, which contains the initial stack point.). It contains the address of the main stack pointer, and a reset handler address for the processor to go to if a reset/startup is required. The others on the vector table will be the fault handler.

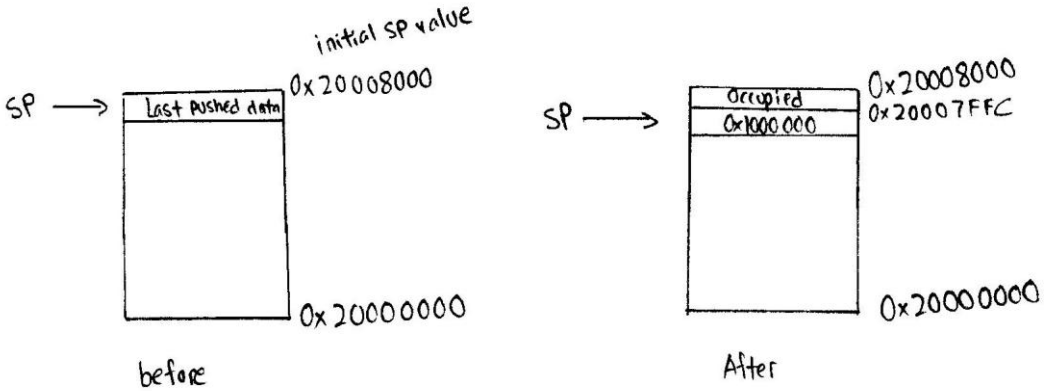
0x00	DCD Top_of_Stack	;Top of stack
0x04	DCD Reset_Handler	;Reset handler
0x08	DCD NMI_Handler	;NMI handler
0x0C	DCD HardFault_Handler	;Hard fault handler

   (ii) Upon starting up, processor read the first word at location 0x00 to 0x03, which contains the initial stack memory address. The value is copied into R13, SP_main the default stack pointer. Subsequently, processor reads the next word at location 0x04, which contains the reset vector address. The value is copied into R15, the Program Counter Register.

   (c)

   (i) Line 1: Declared as Stack, can be read and write, data size is half word (16 bits).
   Line 2: Declare the stack size as 0x120
   Line 3: Define as Stack memory with size declared at line 2.
   Line 4: Function declared as TOP_STACK

   (ii) Initially after initialization, the SP is pointing at the last pushed data at 0x20008000 location. After line 14, Push {R0}, it pushed 0x10000000 into the location 0x20007FFC.

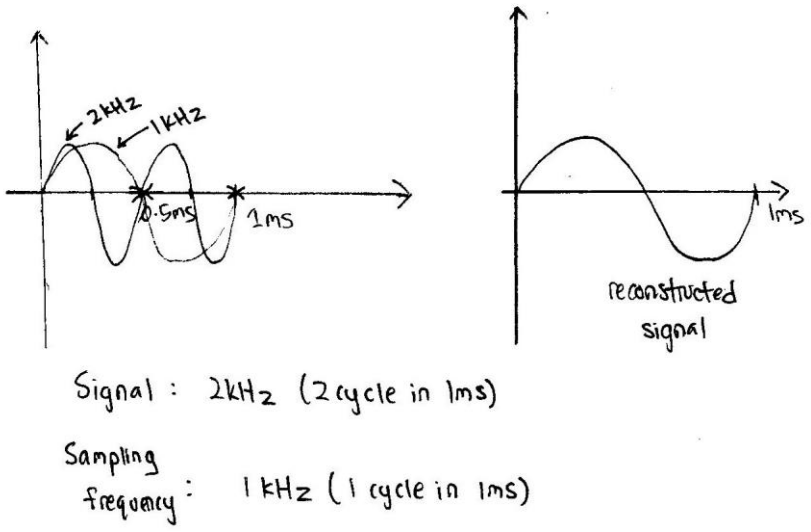


(d) Advantage: Use 1 microcontroller will do, if never use multiplexed row/column, not enough pins to connect to DRAM.

Disadvantage: Need memory controller to issue commands, multiplexed row/column address and issue refresh cycles.

2. (a)

(i) Reconstruction from acquired signal samples of 2khz introduces distortion.



(ii) Aliasing effect can be avoided by having the sampling frequency at least 2 times of the highest frequency component of the signal (Nyquist Rate).

(b)

(i) Period of Clock = 1 / 80MHz
= 12.5 ns

Period of interrupt = 1 / 25 KHz

= 40 us

Value to be written into timer register = 40 us / 12.5 ns

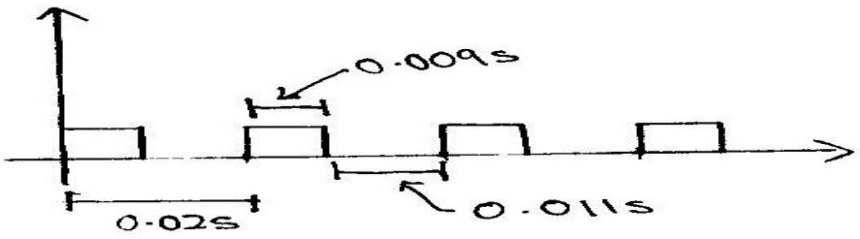
= 3200

(ii) Period of the 50 Hz waveform = 1 / 50

= 0.02 seconds

45% of high = 0.45 x 0.02 = 0.009

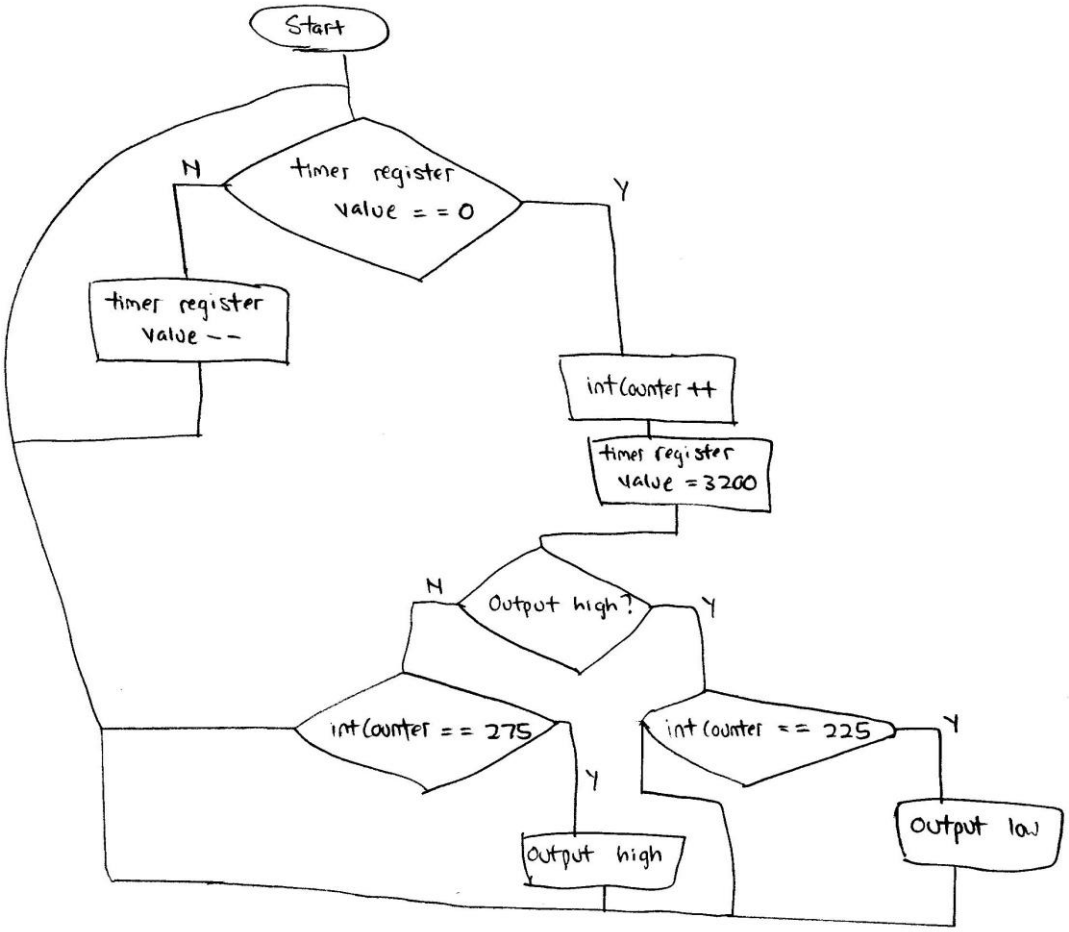
55% of low = 0.55 x 0.02 = 0.011



(iii) No. of interrupt to reach 0.009s: 0.009 / 40 us = 225 times

No. of interrupt to reach 0.011s: 0.011 / 40 us = 275 times

Assumption made: Output is initially high.

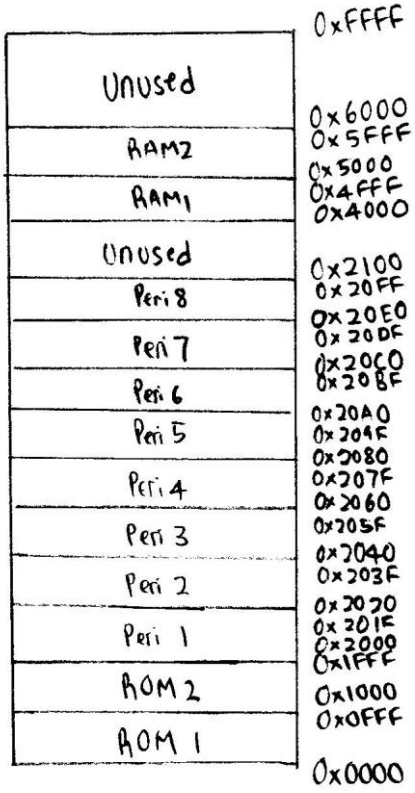


(c) Using PWM techniques for motor allows us to manipulate with the power supplied to the motor instead of using just discrete logics.

2. (a)

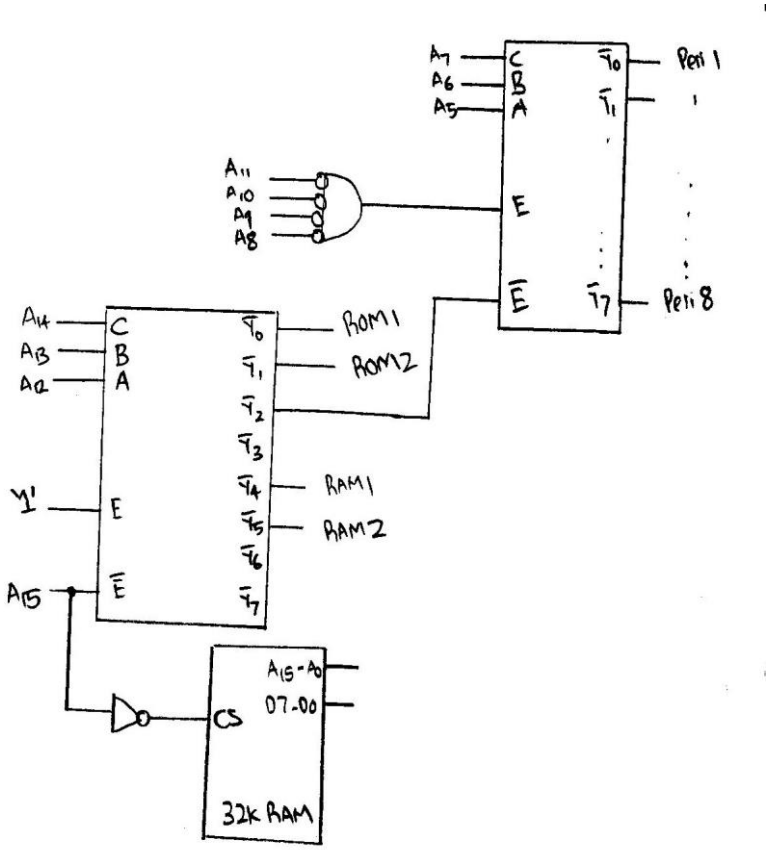
(i) A15 must be '0' to enable the 3 to 8 decoder
A11 – A8 must be '0' to enable the 3 to 8 decoder
A14 – A12 must be '010' to select Y2

Devices	A15 – A0	Start Add	End Add
ROM1	0000 xxxx xxxx xxxx	0x0000	0x0FFF
ROM2	0001 xxxx xxxx xxxx	0x1000	0x1FFF
RAM1	0100 xxxx xxxx xxxx	0x4000	0x4FFF
RAM2	0101 xxxx xxxx xxxx	0x5000	0x5FFF
Peri 1	0010 0000 000x xxxx	0x2000	0x201F
Peri 2	0010 0000 001x xxxx	0x2020	0x203F
Peri 3	0010 0000 010x xxxx	0x2040	0x205F
Peri 4	0010 0000 011x xxxx	0x2060	0x207F
Peri 5	0010 0000 100x xxxx	0x2080	0x209F
Peri 6	0010 0000 101x xxxx	0x20A0	0x20BF
Peri 7	0010 0000 110x xxxx	0x20C0	0x20DF
Peri 8	0010 0000 111x xxxx	0x20E0	0x20FF



(ii) Full-Address decoder must be used for peripheral device, because A14 – A12 must be '010' in order to select Y2 to enable the second 3 to 8 decoder. And A11 – A8 must be logic '0' in order to output a logic '1' from the NAND gate to enable the second 3 to 8 decoder. A14 – A8 must be in a fixed logic, therefore partial address decoding cannot be used.

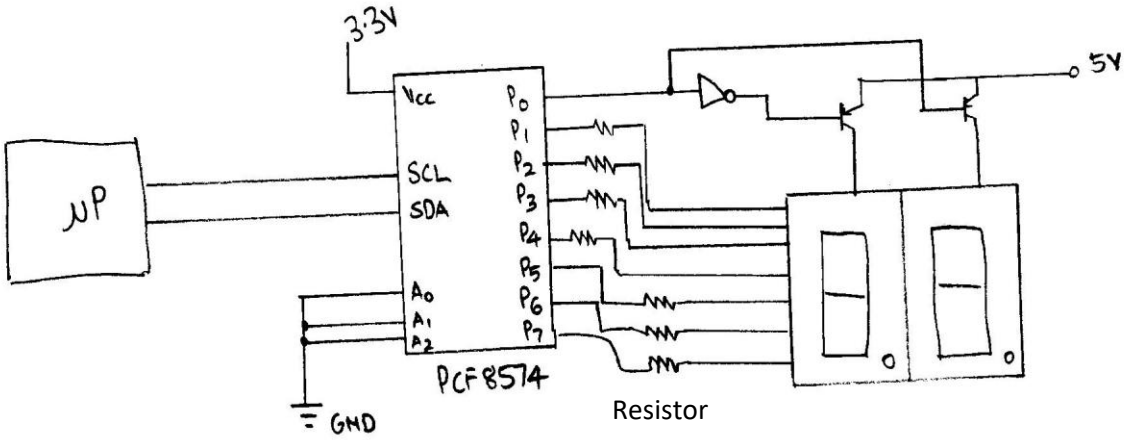
(iii) Add an invertor to the pin A15.



(iv) Starting Address: 0x6000, Ending Address: 0xFFFF

(b) Allows the output port to assume a High Impedance (Hi-Z) state in addition to Logic '0' and '1'. It also allows multiple circuits to share the same output line/lines, such as a bus and thus, effectively removes the devices influence on the rest of the circuit.

4. (a)
   (i) Resistor is used to limit the current flowing through to the SSD. The conduction of transistors is controlled by P0.



Resistor

   (ii) Since P0 is used to control the SSD, P0 must be '1' when displaying 8 and '0' when displaying '1'.
   Display '1': 0x06 (0'b00000110)
   Display '8': 0xFF (0'b11111111)

```
int main()
{
   1. i2c_init();
   2. i2c_start(0xA0);
   3. while(1)
   4. {
   5. i2c_write(0x06); //Switch display by controlling P0.
   6. i2c_write(0xFF);
   7. }
}
```

   (iii) I2C clock stretching. It allows receiver to have more time to process, during an SCL low phase, any I2C device on the bus may additionally hold down SCL to prevent it rising high again.

(b) Use JTAG, hardware instruction breakpoint. Set a breakpoint at the memory location 0xA0008000, and see which part of the code/instruction enter here.

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