CSEC 20th – Past Year Paper Solution 2016-2017 Sem2

CE/CZ1006 – Computer Organisation and Architecture

Question 1

1)

a)

R2	SR
0xFFD	0x004
0x000	0x002
0xC78	0x004
0xC72	0x00C
0xA39	0x005

b)

```
START  PSHM  3                    Avoid using R2, R3, push fewer registers
       MOVS  R1, #0                Reduce instruction cycle
       MOV   AR, #16               Use AR register for looping
LOOP   ADD   R1, AR
       JDAR  LOOP
       MOV   [0x100], R1
       POPM  3
```

The following code realize the addition from 16 to 0 and save the result into memory address 0x100. As 0 does not have impact to the result, therefore, we only need to add from 16 to 1. In this case, AR register is involved. In each loop cycle, AR is added into the result and then self-deduct by 1.

JDAR is the instruction that use the self-reducer AR as the condition for jump.

JDAR is equivalent to

```
AR -= 1
if AR == 0: BREAK
else:
     Go to loop label
```

The optimized instructions are above.

c) First, we look for PC. PC points to 0x082. We want to find out what is the mnemonics start from 0x082:

address	content
0x081	0x432
0x082	0x40D
0x083	0xFFD
0x084	0xBFC
:	:

We convert the machine code into mnemonics, which will be:

```
ADD R3, R2          ; R3 = R3 + R2
ADD R0, [0xFFD]     ; add R0 by 4
JMP -4              ; PC = PC - 4
```

After the execution of JMP -4, PC should point to 0x085. However, the instruction says PC = PC – 4, which means PC is 0x081 after the execution of JMP. Therefore, there is infinite loop between 0x081 and 0x084. In each loop,

R0	R3	SR	PC
0x473	0x7FE	0x001	0x082
0x477	0x7FE	0x000	0x082 -> 0x083 -> 0x085 -> 0x081
0x47B	0x880	0x00C -> 0x000	:
:	:	0x004 -> 0x000	:

Question 2

2)

a)

```
MOV  R0,[SP+6]

MOV R0,[R0]

MOV  R1,  [SP  +  5]
```

See what is the Stack at this point

SP–>	Base - 6	R0
+1	Base - 5	R1
+2	Base - 4	R2
+3	Base - 3	R3
+4	Base - 2	Return address
+5	Base - 1	Address of Var_B
+6	Base	Address of Var_A

First, we get the address of Var_A, then find the content in that address. We can directly get the address of Var_B.

b)

```
POPM 15
RET
```

c)

```
SubZ   PSHM 15          Save R0 ~ R3
       MOV R0, [SP+ 6]  R0 = 0x100
       MOV R0, [R0]     R0 = 0x003
```

	MOV R1, [SP + 5]		
Loop	MOV R2, [R1]	R2 = 0x111	
	MOV R3, #3	R3 = 0x003	
Nxt1	CMP R2, #0	Compare R2 and 0	
	JPL Nxt2	R2 >= 0, jump to Nxt2	R2 >= 0, jump to Nxt2
	NEG R2		
	JMP Nxt3		
Nxt2	ADD R2, R2	R2 = 0x222	R2 = 0x444
Nxt3	SUB R3, #1	R3 = 0x002	R3 = 0x001
	JNE Nxt1	Jump Nxt1	Jump to Nxt1
:		:	:

:			:
	Nxt1 CMP R2, #0		
	JPL Nxt2		R2 >= 0, jump to Nxt2
	NEG R2		
	JMP Nxt3		
	Nxt2 ADD R2, R2		R2 = 0x888
	Nxt3 SUB R3, #1		R3 = 0x000
	JNE Nxt1		Not jump
	MOV [R1], R2		[0x101] = 0x888
	ADD R1, #1		R1 = 0x102
	SUB R0, #1		R0 = 0x002
	JNE Loop		Jump back to loop
	POPM 15		
	RET		

For each element of Var_B, Var_C, Var_D, the following function is applied:

```
for ( R = 3, R3 > 0; R3 --){
        if (R2 >= 0)
                R2 *= 2;
        else
                R2 = -R2;
}
```

Therefore, it is easy to calculate: Var_A = 0x003, Var_B = 0x888, Var_C = 0x004, Var_D = 0x322, Var_E isn't changed.

d)

```
Var3 = 3;
   do {
      if (Var2 >= 0)
            Var2 = 2;
      else
            Var2 = -Var2;
      Var3--;
```

Question 3

3)

a)

(1) NAND Flash.

The memory of a recording pen should have the following properties: light, nonvolatile, and large capacity (around 500MiB - 2GiB). Therefore, NAND flash is suitable.

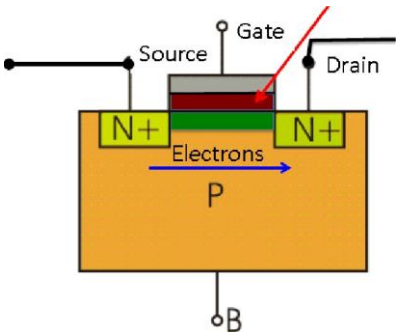
(2) Magnetic HDD.

Video recorder (DVD reader) is a large device and is able to use magnetic HDD as its storage memory. 7 days of HD video should take few hundreds GiB, NAND flash and NOR flash will cause a lot of money to have such capacity.

(3) DRAM

System memory for a high performance graphic card is usually few GiB. It needs high speed I/O while not so expensive. Therefore, DRAM is a better choice than SRAM.

b) Flash memory uses floating gate transistor to store electrons as information. When a large programming voltage is applied, it is able to 'write' electrons into the floating gate. When the voltage is removed, electrons are trapped inside. Hence, it stores the information.



c)

1. Eliminate signal skew

Multiple signal lines take different time to reach the receiver due to the difference in propagation delay. The propagation delay is influenced by resistance and capacitance in the PCB trace. The wavy traces are used to ensure all signals take approximately same amount of time to reach the receiver.

2. Avoid crosstalk

Crosstalk is undesired coupling of signals in different circuit. The close the placement, the greater the crosstalk. The wavy trace increases the distance between two high speed traces, thus reduce the effect of crosstalk.

d)

i) Bits per data packet = 1 + 8 + 1 + 1 = 1lbits
Cps = 9600bps / 11 bit = 872.73 cps > 200cps
The system can support a typist with a typing speed of 200 cps.

ii) By using a configuration with 1 start bit, 8 data bits, 1 stop bit. This can reduce data overhead, thus increase the data transfer rate.
However, there is no error detection if we remove the parity bit. This may cause the integrity of the received data.

iii) It is an error detection scheme that ensures the total number of 1s in the data bits plus the parity bit is an even number.

Question 4

4)

a) Wearing levelling is a method used by SSD to write data in different blocks. SSD has limited number of erase cycles, writing data evenly throughout the whole disk can avoid frequently erase a certain block, thus extend the life of an SSD.
External RAM buffer is a buffering mechanism that reduces the number of writes into SSD.

b) EAT = 5 x 90% + (5 + 100) x 10% = 15ns

c) '2n'
It is because when two n bits number multiplies, the maximum result would be 2n bits.

'+1':

It is designed for carry bit. The highest bit would produce a carry which can be used to detect overflow.

d)

i) For instructions other than branch:
If there are n instructions, the #cycles = n + 3.
For each branch instruction, the #cyc1e need to add 2 if the target is not taken. The number of loops = 5, therefore, total #cyc1es = 5 x 3 + 5 (total number of instructions) + 2 x 4 (4 branch instructions that target is not taken) + 3 (additional 3 from n +3) = 31 cycle.

ii) #cycles = 5 + 3 x 5 = 20 cycles

iii) Pipeline fully utilized the CPU resources, which will decrease the total amount of time of execution. Though the number of cycles needed by pipeline machine is more than the number needed by none-pipeline one, the time for execute 1 cycle is usually smaller. However, the penalty for branch is heavy if the target is not taken. It will slow down the pipeline machine significantly.

== End of Answers ==

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