ECSE 323 — Group 47 Lab 3 Report

Junyoung Shin id. 260499663
Timothee Flichy id. 260557686

March 17, 2016

Design and simulation of a 0-to-25 Counter Circuit

We desiged a 0-to-25 counter with inputs clock, asynchronous reset, and count_enable.The counter gives an output of a 5bit which counts up avery clock cycle while count_enable is high and reset is high. The count will add 1bit every clock cycle until it reaches the max value of ”11001”.The count_enable and count are trigered at the rising edge of the clock. When reset goes low, the count goes to ”00000”. If count_enable is not set high, the count is will at the value it was not until count_enable goes high. To test our code, we created a clock pulse of 50ns and tested the VHDL code. The data of the test cana be seen on figure 2.

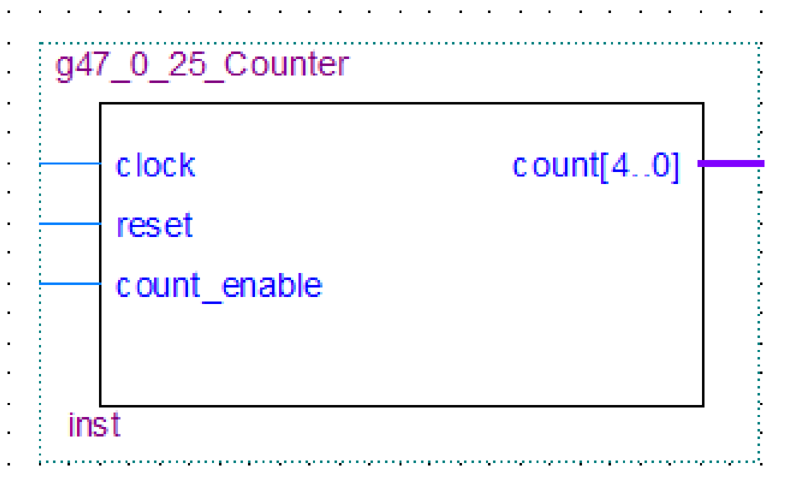

Figure 1: 0-to-25 counter driver pins.

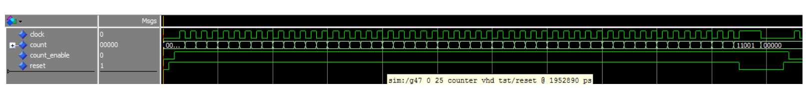

Figure 2: Simulation of the 0-to-25 counter.

Testing the 7-segment LED decoder on the Altera Board

The Altera DE1 development board is equiped with 4 7-segment LED display and 10 simple switches are controlled and received by the FPG. Our goal was to make a test bed to make the LED to display letters in the alphabet when playing with 5 of the switches availabe on the board. The lettering configuration was as followed on table 1. To decode the binary numbers being put in by the swtiches, we used the 7_segment_decoder to show the letters according to the table 1. The second step was to make a testbed circuit which combined all the components we have made so far including: 26_5_encoder, 5_26_decoder, 0_25_counter, pulse_generator, 26_barrelshift, and 7_segment_decoder.

Table 1: Alphabetical value accoding to the 5bit code.

Code	**Letter**
00000	A
00001	B
00010	C
00011	D
00100	E
00101	F
00110	G
00111	H
01000	I
01001	J
01010	K
01011	L
01100	M
01101	N
01110	O
01111	P
10000	Q
10001	R
10010	S
10011	T
10100	U
10101	V
10110	W
10111	X
11000	Y
11001	Z

The testbed use 5 switches to set the inital shift amount then shifts up using the 26_barrelshift circuit. A pulse generator is used to create a 2Hz pulse that acts as a 0_25_counter enable signal. This is due to the FPGA's clock being 50MHz which is too quick for human perception. There is also a reset button used to reset the counter. The counter acts as our barrelshift input. For our circuit, using the Altera EP2C20F484C7N fast model hold (FMH) slack time is 0.357ns, slow model setup (SMS) slack value is 14.167ns, and the slow model Fmax (SMFm) is 185.77MHz. If we changed to the cheaper Altera 5CSEMA5F31C6 having a FMH slack time of 0.259, a SMS slack value of 13.923, and a SMFm of 164.55MHz, we can see that the chaper model still has its SMFm higher then 50MHz clock cycle. Meaning changing to the Altera 5CSEMA5F31C6 would save to company buying 100,000 units a total of 1.557 million dollar.