

# ECSE 323 — Group 47 Lab 4 Report Permutation

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April 1, 2016

## 1 Permutation

The permutation is used to both encode and decode the input letter. To do so, we were given a table which depicts the character encryption list given in the figure 1. We were told to implement the first 4 rotor types. To make the permutation circuit, we need 2 input and 2 outputs. The inputs will receive a 2 bit rotor\_type and the second input is a 5-bit input\_code (letter) that must be encrypted. The outputs are a 5 bit output\_code which outputs the encrypted version of the input bits determined by the rotor position and the second input is the inv\_output\_code giving the inverted or decrypted 5 bit code. This is given by the figure 2. We tested out vhdl code on the ModelSim

INPUT	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
Rotor I	E	K	M	F	L	G	D	Q	V	Z	N	T	O	W	Y	H	X	U	S	P	A	I	B	R	C	J
Rotor II	A	J	D	K	S	I	R	U	X	B	L	H	W	T	M	C	Q	G	Z	N	P	Y	F	V	O	E
Rotor III	B	D	F	H	J	L	C	P	R	T	X	V	Z	N	Y	E	I	W	G	A	K	M	U	S	Q	O
Rotor IV	E	S	O	V	P	Z	J	A	Y	Q	U	I	R	H	X	L	N	F	T	G	K	D	C	M	W	B

Figure 1: Permutation graph.

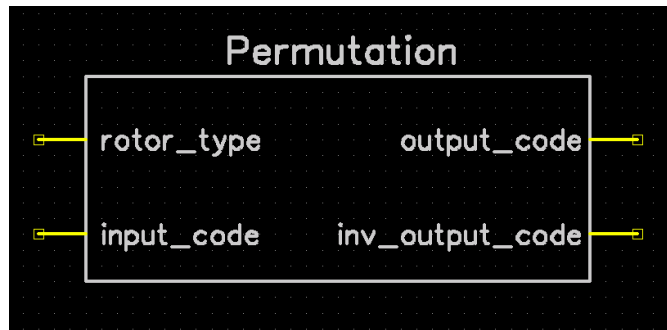


Figure 2: Permutation symbol.

and got what we were expected to get from the permutation graph as you can see from the figures 3, 4, 5, 6, and 7.

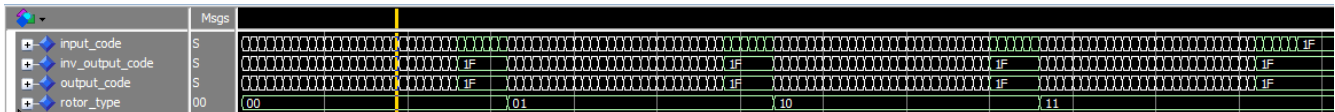


Figure 3: Tested circuit on ModelSim

		Msgs																																
+	input_code	S	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	1A	1B	1C	1D	1E	1F
+	inv_output_code	S	U	W	Y	G	A	D	F	P	V	Z	B	E	C	K	M	T	H	X	S	L	R	I	N	O	Q	J	1F					
+	output_code	S	E	K	M	F	L	G	D	O	V	Z	N	T	O	W	Y	H	X	U	S	P	A	I	B	R	C	J	1F					
+	rotor_type	00	00																															

Figure 4: With rotor I.

	Msgs	J F J E A B C D E F G H I J K L M N O P Q R S T U V W X Y Z JA JB JC JD JE JF
input_code	S	J F J E A B C D E F G H I J K L M N O P Q R S T U V W X Y Z JA JB JC JD JE JF
inv_output_code	S	J F J E A B C D E F G H I J K L M N O P Q R S T U V W X Y Z JA JB JC JD JE JF
output_code	S	J F J E A B C D E F G H I J K L M N O P Q R S T U V W X Y Z JA JB JC JD JE JF
rotor_type	00	00 01

Figure 5: With rotor II.

	Msgs	
input_code	S	J F A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 1A 1B 1C 1D 1E
inv_output_code	S	J F T A G B P C S D O E U F V N Z H Y I X J W L R K O M 1F
output_code	S	J F B D F H J L C P R T X V Z N Y E I W G A K M U S Q O 1F
rotor_type	00	01 10

Figure 6: With rotor III.

		Msgs																																																
+	input_code	S																																																
+	inv_output_code	S																																																
+	output_code	S																																																
+	rotor_type	00																																																

Figure 7: With rotor V.

## 2 fsm

For the FSM also known as Finite State Machine, we had build a circuit that work at a specific sequence mentioned on the lab sheet. The states are as following shown in the figure 8. To make this work, we wrote a FSM where we

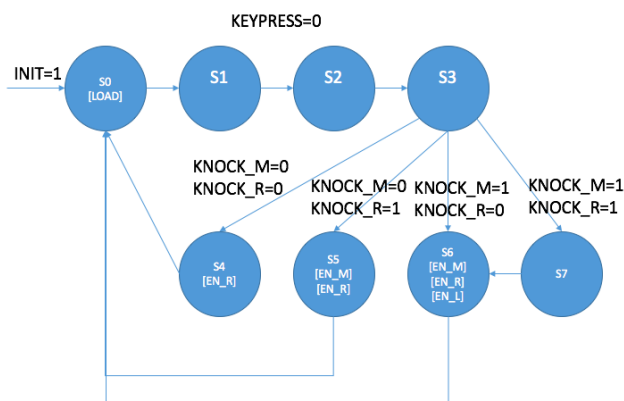


Figure 8: State Diagram.

have 5 inputs and 4 outputs as shown in the figure 9. Circuit goes as follows. The circuit check for the INIT to go high. When INIT is high, the LOAD will go high. After this, it waits for the KEYPRESS to go low in the case of the Altera board is active high. Next it checks the KNOCK\_M and KNOCK\_R. When both KNOCK are low, then only the EN\_R is set high. When only KNOCK\_R is high, then the EN\_R and EN\_M is set high. When only KNOCK\_M is high, the all EN is go high. When both KNOCK's are high, is will go to the state where all EN are high. After the states where EN are set, it will return to state 1 and start over again. At this, point, the INIT does not need to be checked. The figure 10 shows the circuit in a simulated environment.

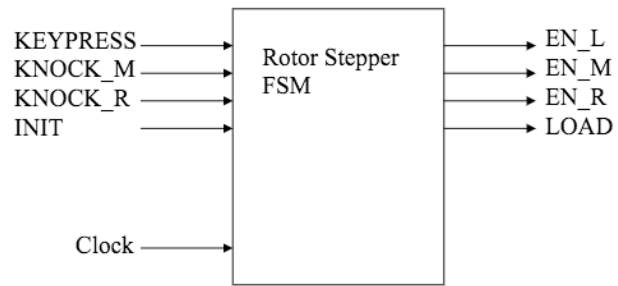


Figure 9: FSM symbol.

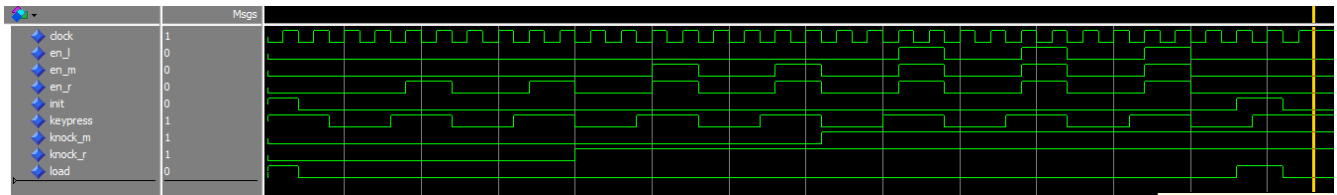


Figure 10: FSM symbol.

### 3 fsm\_testbed