计算机组成原理与接口技术
——基于 MIPS 架构

REVIEW

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信息工程系

- **Computer Architecture**
  - Von Neumann Architecture
  - Harvard Architecture
  - Modified Harvard Architecture
  - General Purpose Computer
  - Memory
    - Register, Cache, ROM, RAM, Virture Memory
    - Byte Address
    - Data Type
  - I/O Port
  - Processor
    - RISC
    - CISC

- **Computer Information Representation**
  - Data Storage Format
    - Bits Ordering (MSB, LSB)
    - Byte Ordering (Big-Endian, Little-Endian)
  - Binary Text (ASCII)
  - Number Systems
    - Base-R
      - Radix (Base), Weight
      - Conversion
    - Complement
    - Signed Binary Numbers
    - Fixed-Point Numbers
      - Qm.n Format of Fixed-Point Number
    - Floating-Point Numbers
      - IEEE-754 Scientific Notation

- **Computer Arithmetic**
  - Fixed-Point Arithmetic
    - Arithmetic, Logical
    - ALU, Shifters, Multiplier, Divider
  - Floating-Point Arithmetic
    - Arithmetic
- **Programming**
  - Compile, Assemble, Link, Load
  - Data Type (C Langualge)
  - Boundary Alignment

- **MIPS32 ISA**
  - MIPS32 Architecture
    - 32 GPR
    - Memory Allocation (Kernel/User Space)
    - Stack (Grows Down) & Heap (Grows up)
    - Static Data & Text Segment
  - R/I/J-type Instructions
    - Operands
      - Memory/Register/Immediate Operands
    - Addressing
      - Operands/Instruction Addressing
  - Assembler, Linker, Loader, Simulator
  - Assembly Syntax
    - Labels, Mnemonics, Operands, Comments
    - Directives, Pseudo Instructions, Macros

- **Programming**
  - Data Transfer
  - Arithmetic
  - Logical
  - Branch/Jump
  - FOR/WHILE
  - IF-ELSE
  - SWITCH-CASE
  - Array
  - Subroutine

3 Microprocessor Design

- **Single-Cycle MIPS32 Processor**
  - Instruction & Data Memory
  - Program Counting Register
  - Register File
  - ALU
  - Controller
  - 5-stage of Data Path
    - IF, ID, EX, MA, WB
- **Pipelined Processor**
  - Structural/Data/Control Hazards
- **Superscalar**
- **Exceptions & Interrupts**

4 Memory Management

- **Segmented Memory**
  - Real-Mode
  - Protected-Model
    - Segment Descriptor, Segment Selector
- **Paged Memory**
  - Logical Address, Linear Address
- **Cache**
  - Direct-mapped
  - Set-associative
  - Fully-associative
  - Cache Access Policies
- **Virtual Memory**
  - Virtual Address, Page Table, TLB

5 Bus

- **Bus Parameter**
- **Bus Structure**
  - Single
  - Dual
  - Multiple Bus
- **Handshaking**
- **Communication Mode**
  - Synchronization, Half Synchronization, Asynchronous
- **Arbitration**
  - Static
  - Dynamics
    - Centralized, Distributed

5 Bus

- **On-chip Bus**
  - AXI
- **Internal Bus**
  - SPI
  - IIC
- **System Bus**
  - PCI
- **Peripheral Bus**
  - SCSI, IDE, SATA, RS232, USB

6 Memory Interface

- **Typical Memory Chips**
  - SRAM
  - SSRAM
  - DDR2-SDRAM
  - FLASH
- **Design of Memory Interface**
  - Capacity Expansion
  - Address Mapping
  - Organization Structure
  - Various Data Type Access
- **Memory Controller**
  - AXI EMC
  - MIS

7 I/O Interface

- **Concept of I/O Interface**
- **I/O Port**
- **Connect to Bus**
- **Parallel I/O Interface**
  - Simple Interface
    - Switch Button Input Interface
    - Light-emitting Diode Display Interface
    - Keyboard Matrix Interface
    - 7-segment Display Interface
    - Analog-to-Digital Converter Interface
  - GPIO (General Purpose IO) Controller
  - EPC (External Peripheral Controller)

8 Interrupt

- **Concept**
  - IRQ, ISR, IV, IVT
  - Interrupt Response Flow
  - Interrupt Controller
- **Interrupt system of x86**
- **Interrupt system of MicroBlaze**
  - Interrupt Response Flow
- **AXI INTC**
- **GPIO Interrupt Interface**
- **Timer Interrupt Interface**
- **SPI Interrupt Interface**

9 DMA

- **Concept**
- **AXI CDMA**
  - Memory ↔ Memory
  - Memory ↔ I/O Device

10 UI

- **VGA Timing**
- **VGA Display Controller Design**

Knowledge & Skills

- **Number System and Arithmetic**
- **Verilog HDL**
- **MIPS32 Assembly**
- **Processor Design**
  - Data Path (Operators & ALU)
  - Controller (Instruction Decoding)
- **Interface Design**
  - Address, Data, Controll
  - Decoder, 3-State Buffer, Flip-Latch, Register
  - I/O Port
- **Reading Datasheet**
  - I/O Signals, Registers, Timings