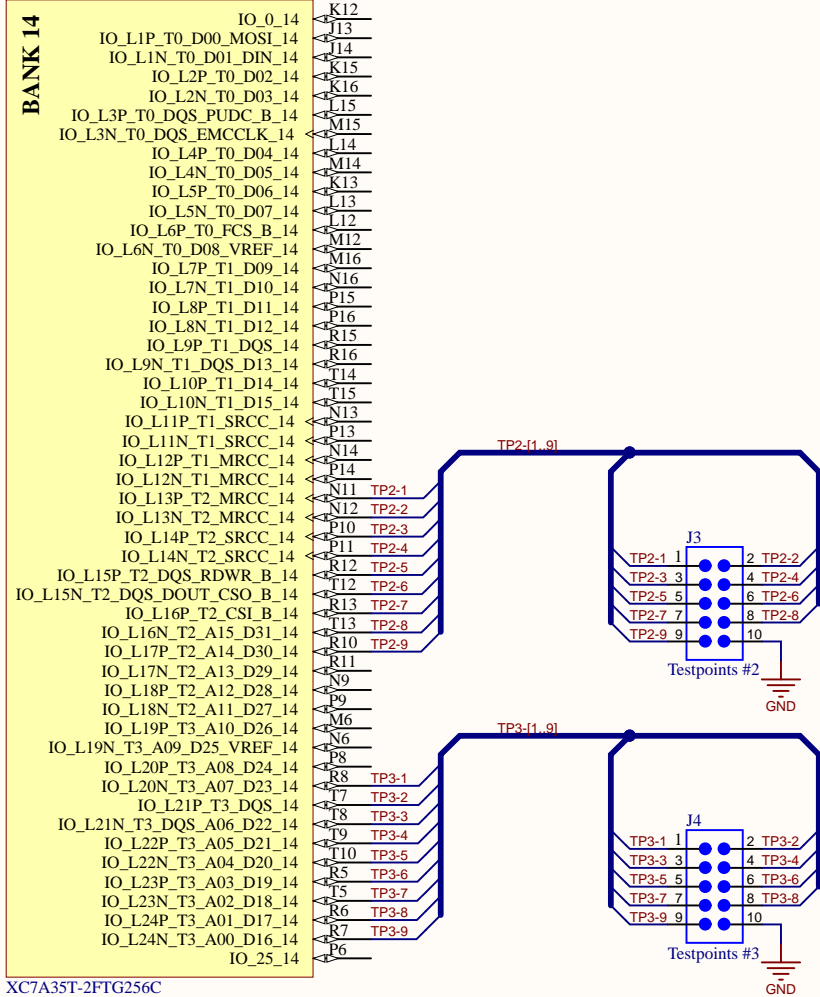


U1A

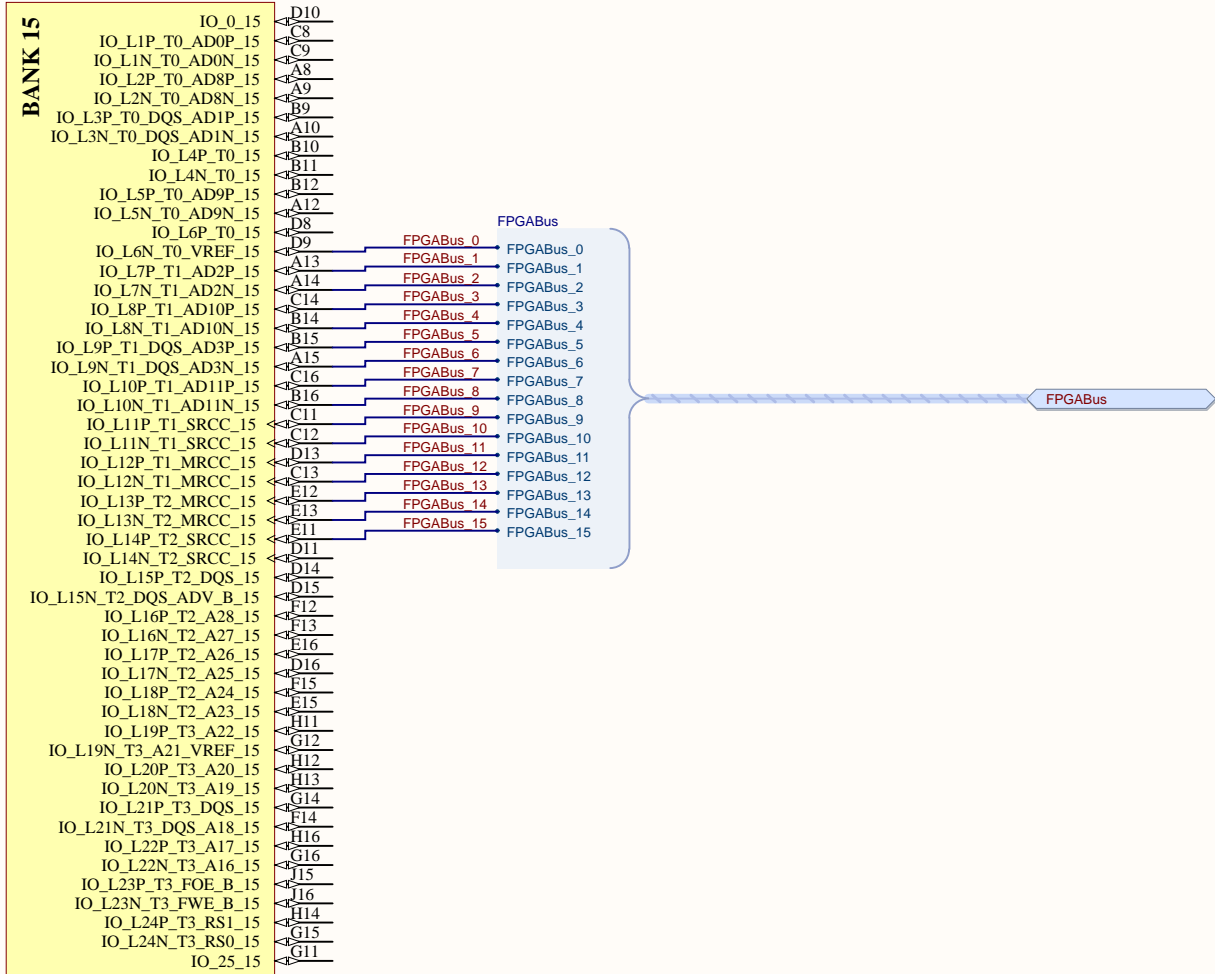


XC7A35T-2FTG256C

Board: sudo -ku	Version: 1.0
Sheetname: SheetName	Sheet * of *
Subject: TDT4295 Computer Project	Group: Energy
Schematic file: dmp16-pcb-v1-FPGA-Bank14.SchDoc	



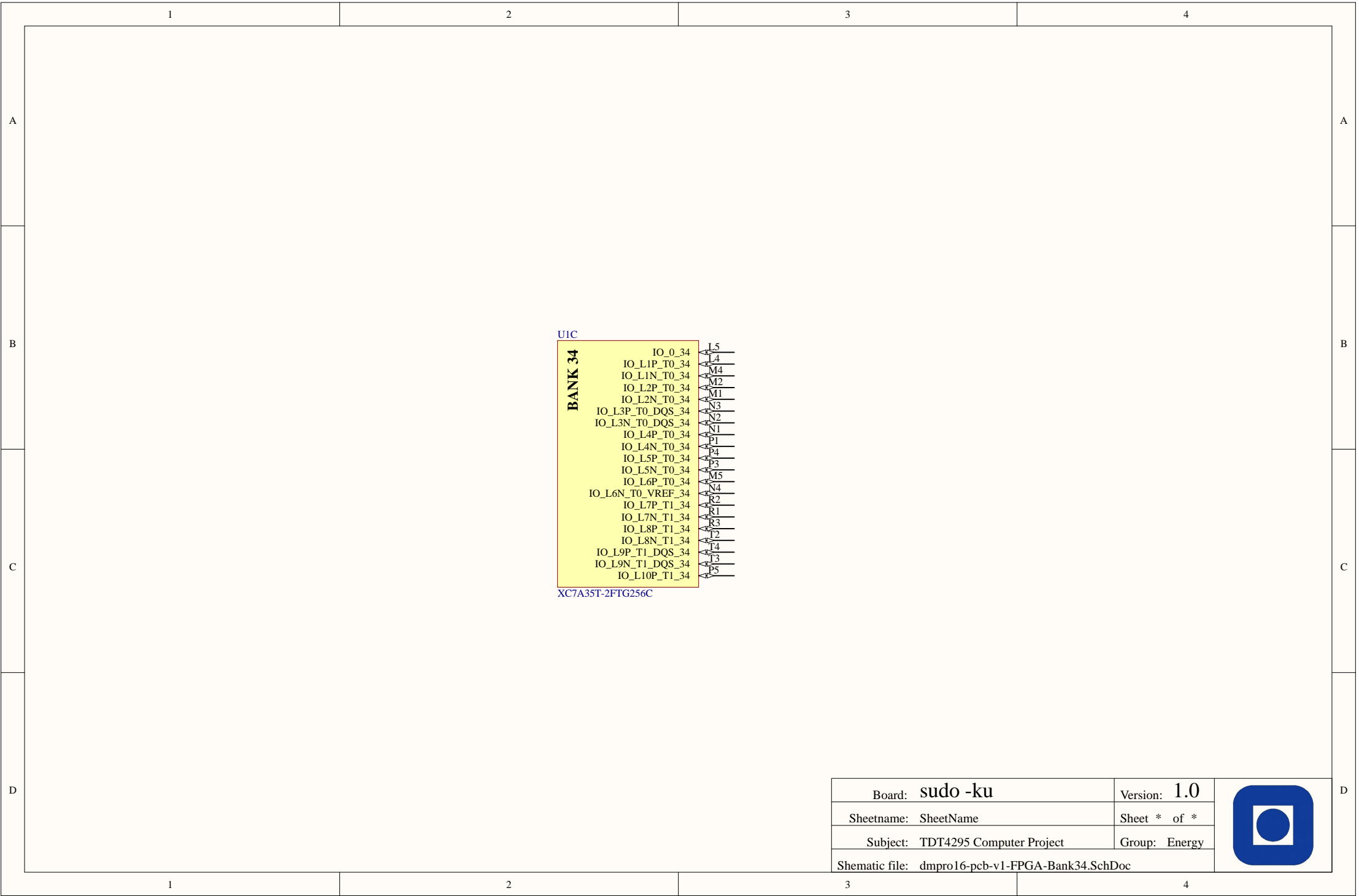
U1B



XC7A35T-2FTG256C

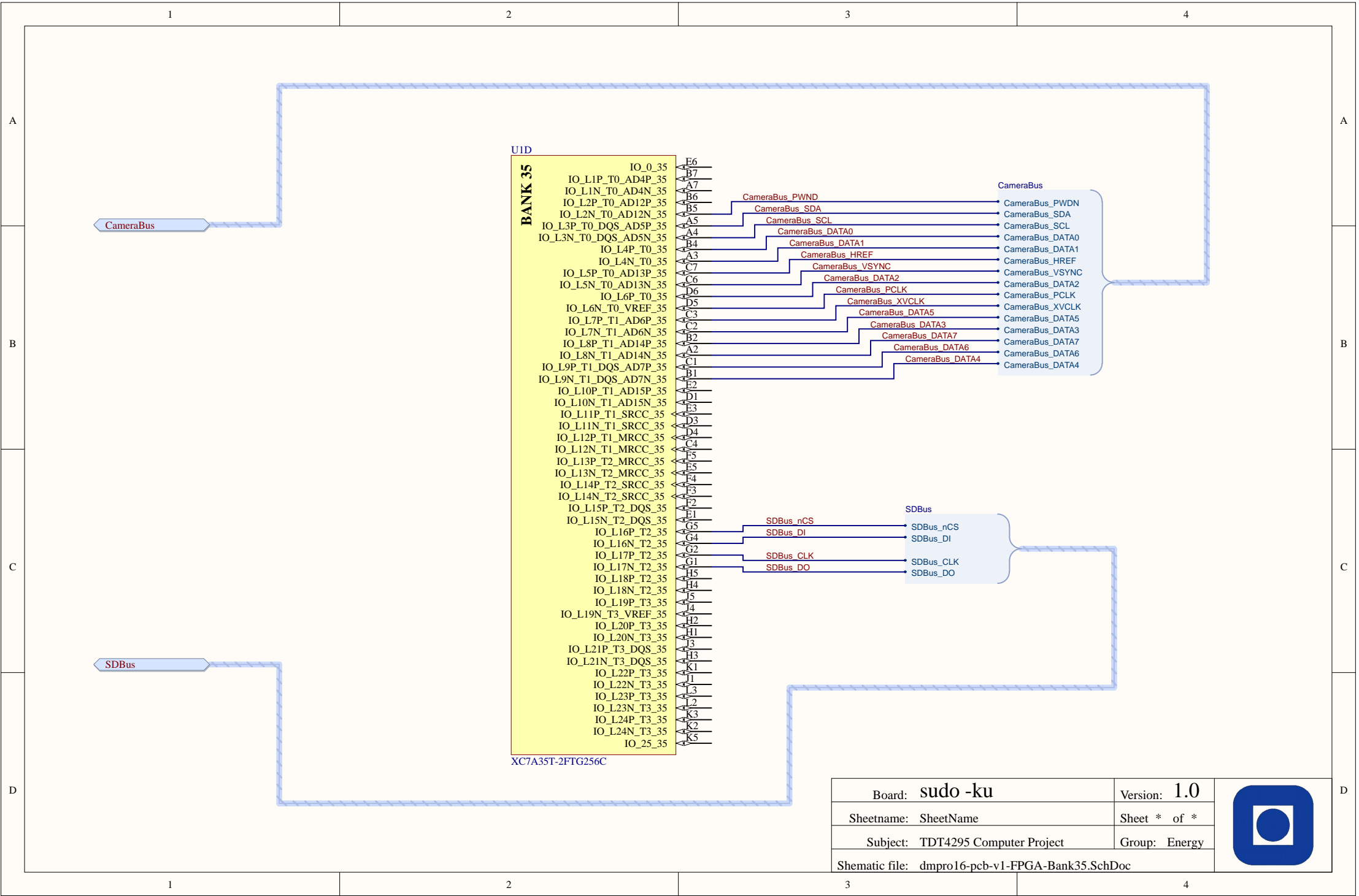
Board: sudo -ku	Version: 1.0
Sheetname: SheetName	Sheet * of *
Subject: TDT4295 Computer Project	Group: Energy
Schematic file: dmp16-pcb-v1-FPGA-Bank15.SchDoc	





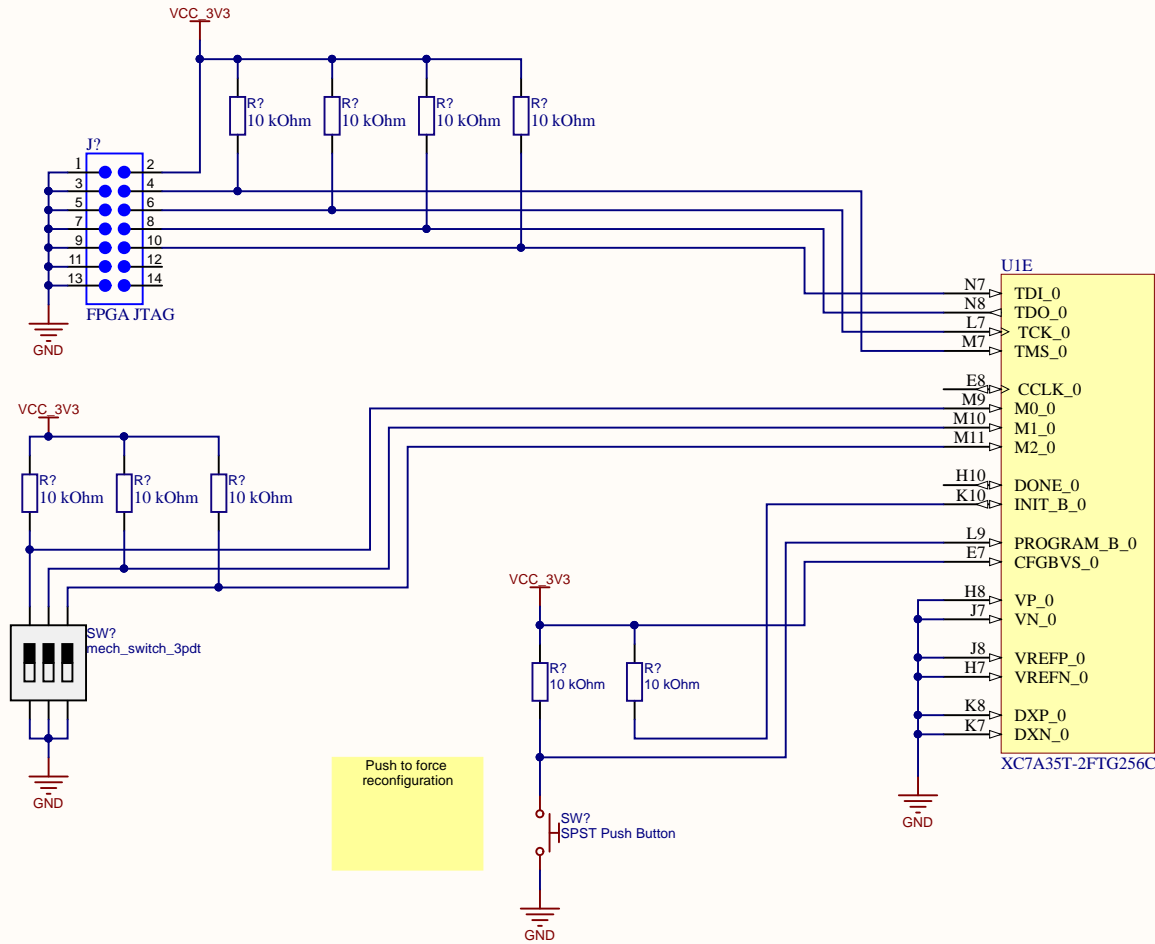
Board:	sudo -ku	Version:	1.0
Sheetname:	SheetName	Sheet * of *	
Subject:	TDT4295 Computer Project	Group:	Energy
Schematic file: dmp16-pcb-v1-FPGA-Bank34.SchDoc			





Note: this is a 2mm pitch jtag connector recommended by xilinx, might need to change later. Might even be better to have standard 2.54 mm pitch header to improve compatibility.

Default value = 0x111 = slave serial (internal pull ups in FPGA)
M[2:0]=
0x111 : Slave serial
0x101 : JTAG only
0x001 : Master SPI x1, x2, x4
0x000 : Master Serial



Done: High (open drain) when config done. indicator led with resistor to GND.

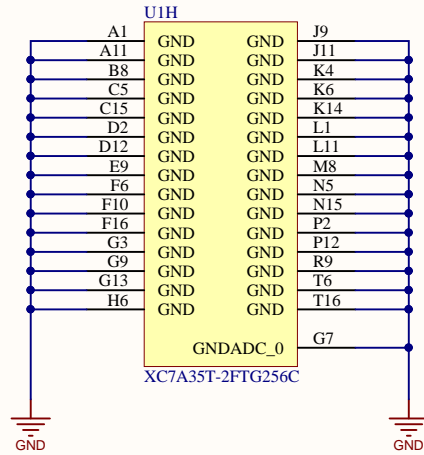
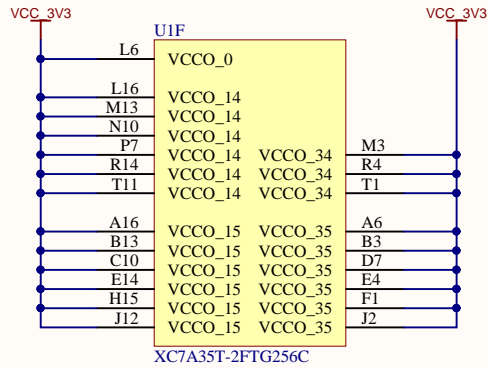
Program_B: Active low reset to config logic. 4.7kOhm pull up, push button to GND for manual config reset

Init_B: driven low during config reset, init or config error. Floating when init done, 4.7k pullup and (optionally indicator led. Not done on basys or arty, so dropped here as well).

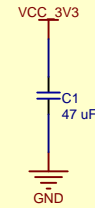
DX: Temperature-sensing diode inputs. Not used, VREFP should be shorted to ground, since no external reference is used.

Board: sudo -ku	Version: 1.0
Sheetname: SheetName	Sheet * of *
Subject: TDT4295 Computer Project	Group: Energy
Schematic file: dmpro16-pcb-v1-FPGA-Config.SchDoc	

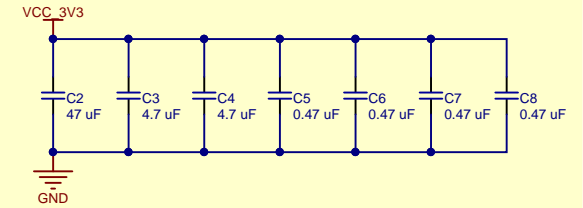




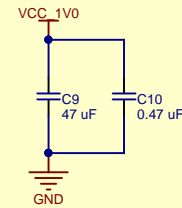
VCCO Bank 0 decoupling caps



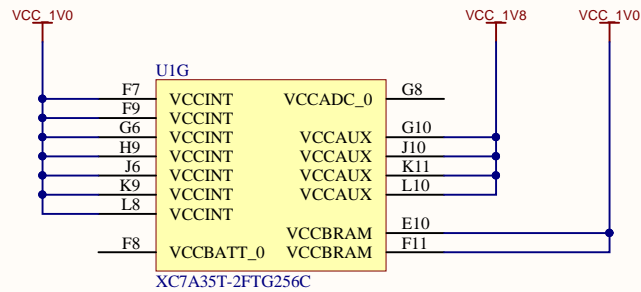
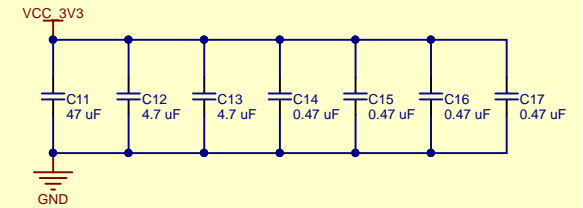
VCCO Bank 14 decoupling caps



VCCBRAM decoupling caps

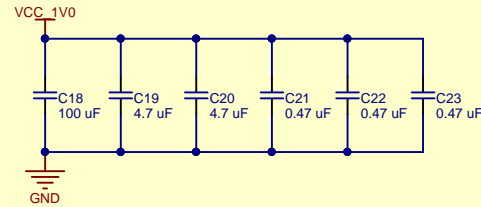


VCCO Bank 15 decoupling caps

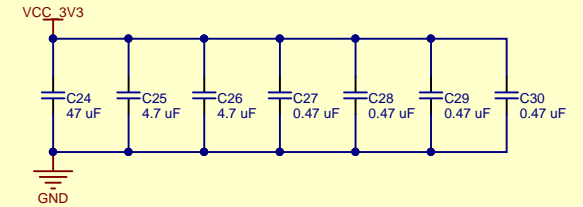


Do VCCADC and VCCBATT have to be connected to anything? If so, what can they be connected to?

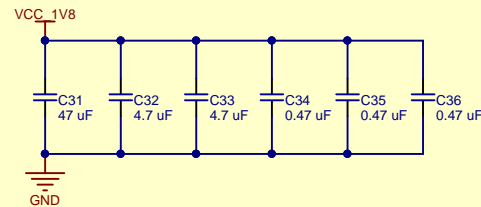
VCCINT decoupling caps



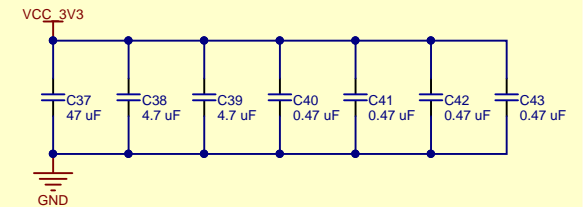
VCCO Bank 34 decoupling caps



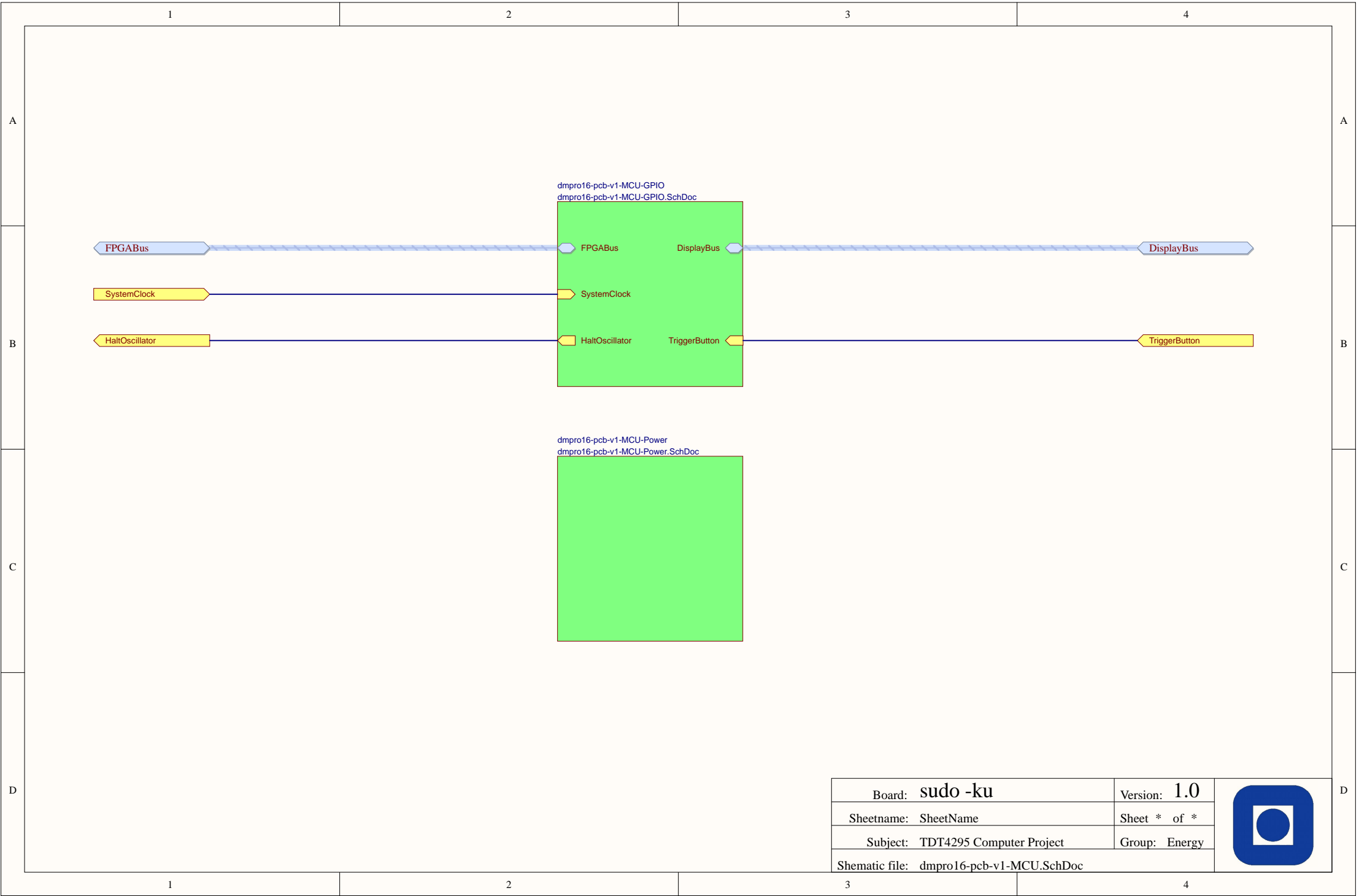
VCCAUX decoupling caps

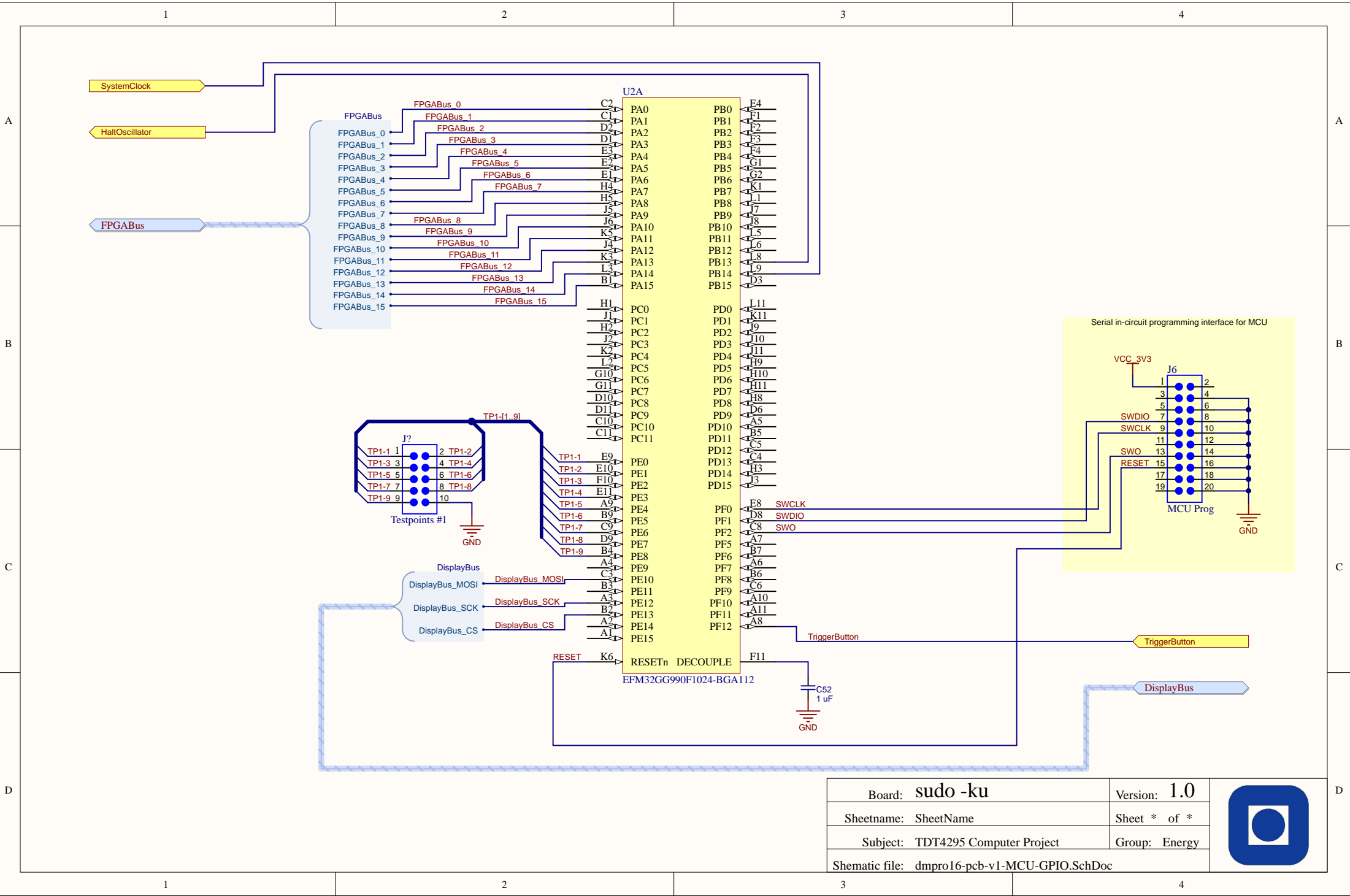


VCCO Bank 35 decoupling caps

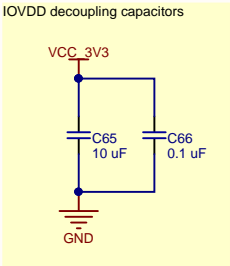
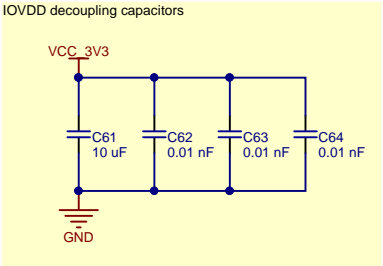
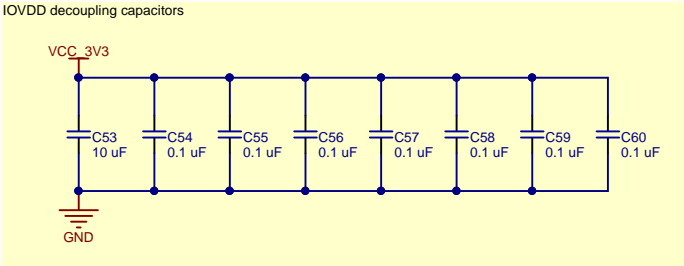
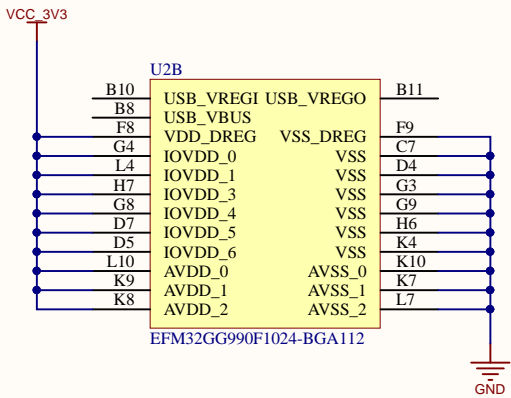



Board: sudo -ku	Version: 1.0	
Sheetname: SheetName	Sheet * of *	
Subject: TDT4295 Computer Project	Group: Energy	
Schematic file: dmpro16-pcb-v1-FPGA-Power.SchDoc		



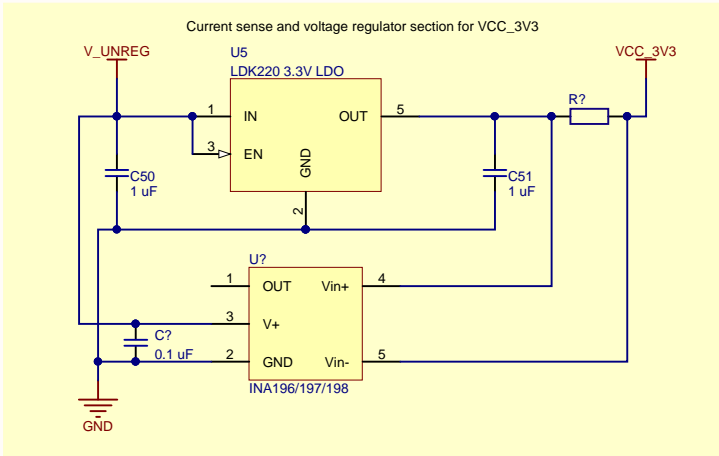
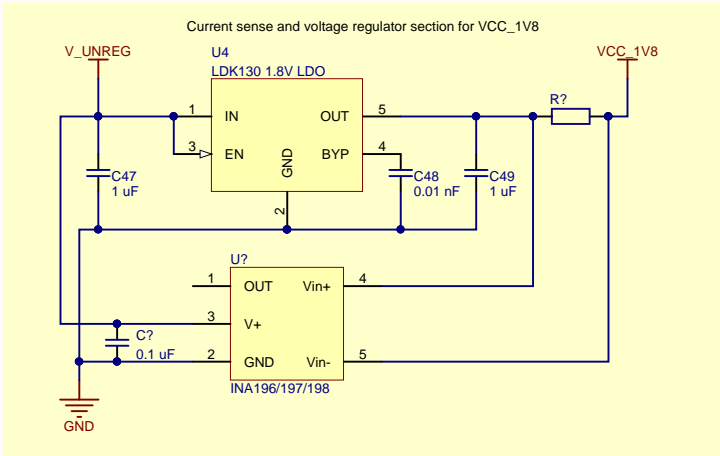
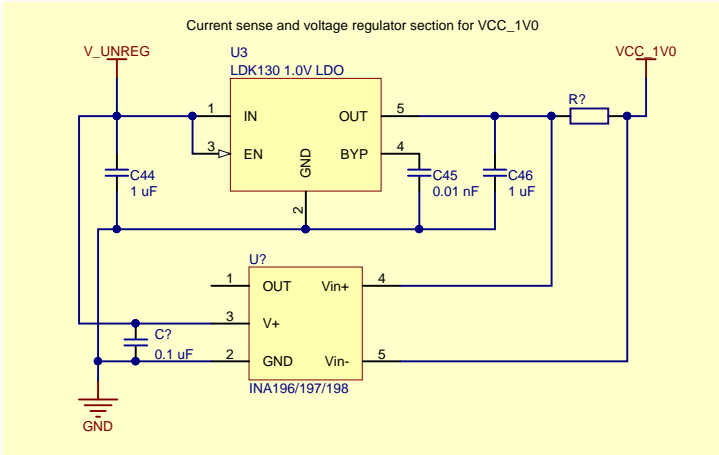
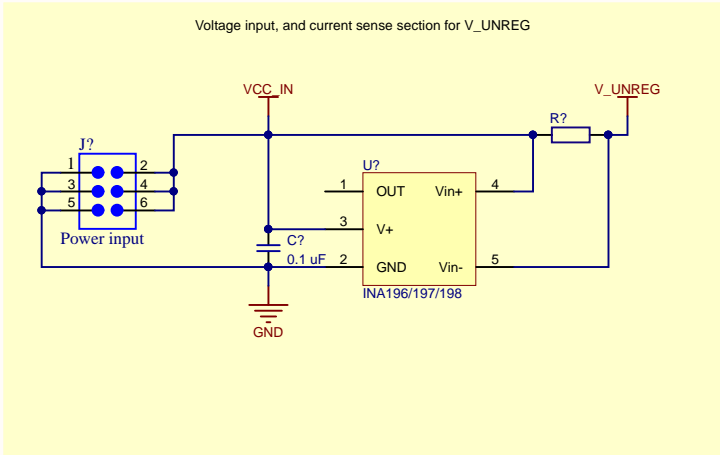


Board: sudo -ku	Version: 1.0	
Sheetname: SheetName	Sheet * of *	
Subject: TDT4295 Computer Project	Group: Energy	
Schematic file: dmp16-pcb-v1-MCU-GPIO.SchDoc		



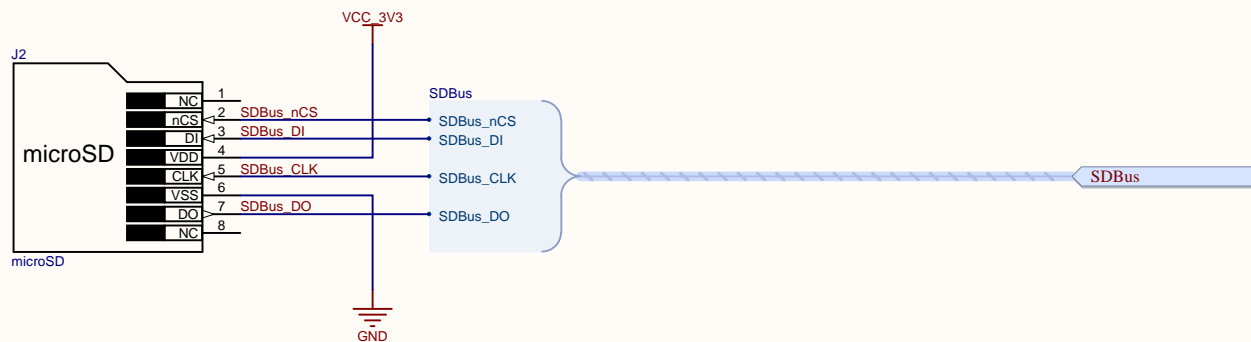
Board: sudo -ku	Version: 1.0	
Sheetname: SheetName	Sheet * of *	
Subject: TDT4295 Computer Project	Group: Energy	
Schematic file: dmpro16-pcb-v1-MCU-Power.SchDoc		


We assume 4 AAA cells provide battery power to the device. Ideally, one would use Li-ion batteries and switch mode power supplies

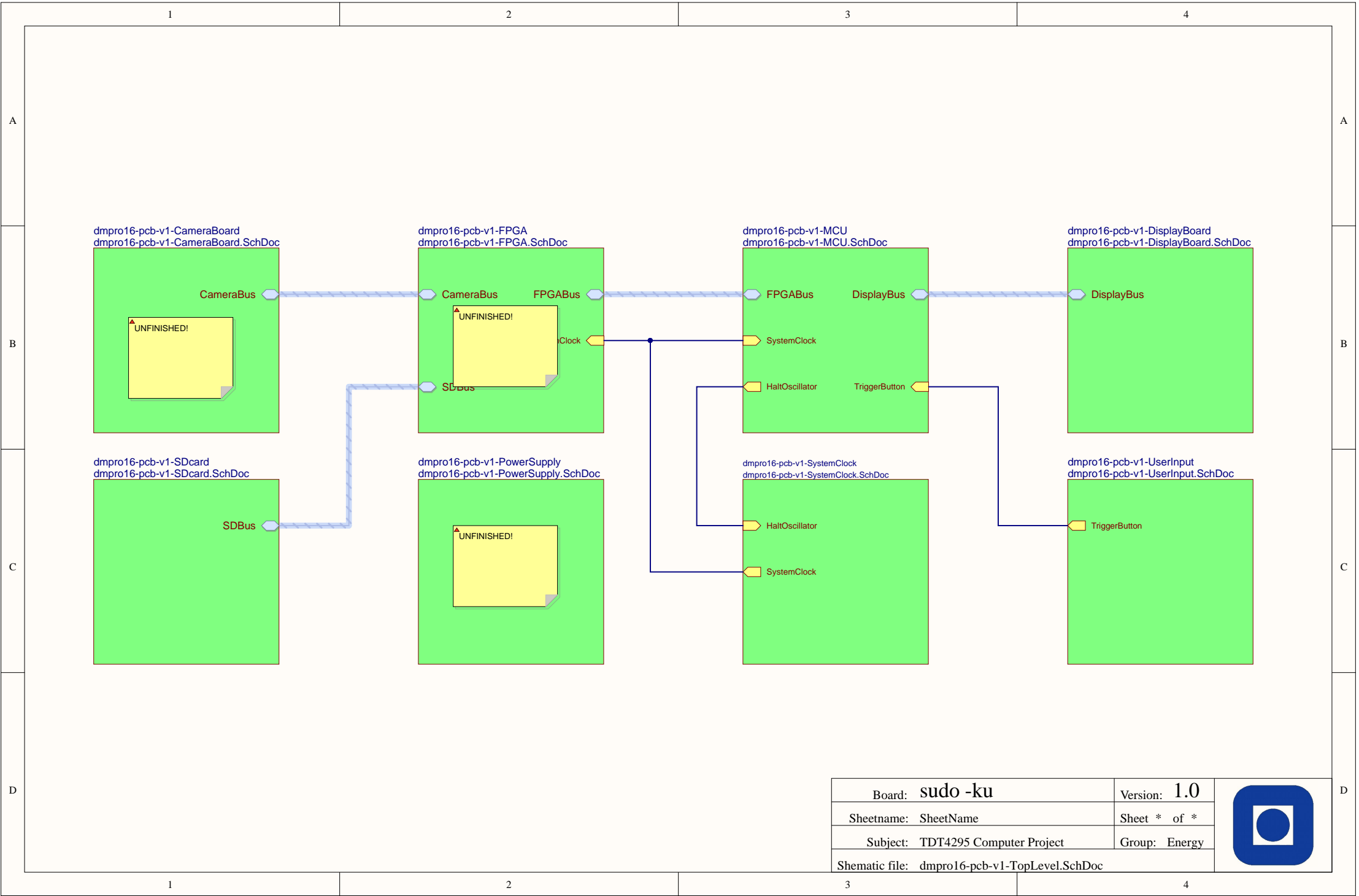


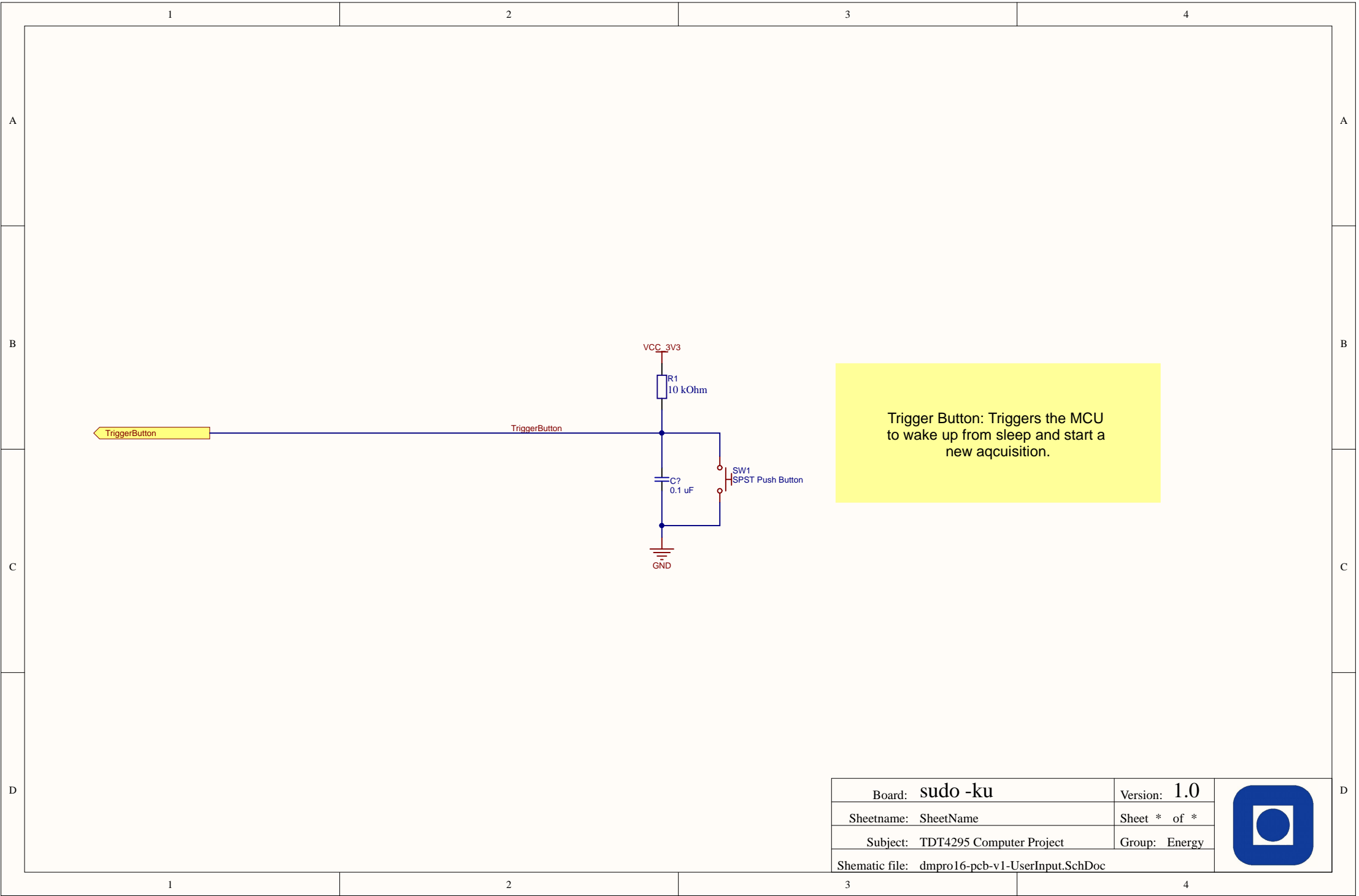
Board: sudo -ku	Version: 1.0
Sheetname: SheetName	Sheet * of *
Subject: TDT4295 Computer Project	Group: Energy
Schematic file: dmp16-pcb-v1-PowerSupply.SchDoc	






Board: sudo -ku	Version: 1.0	
Sheetname: SheetName	Sheet * of *	
Subject: TDT4295 Computer Project	Group: Energy	
Schematic file: dmp16-pcb-v1-SDcard.SchDoc		





1	2	3	4
A			A
B			B
C			C
D			D
1	2	3	4

Board: sudo -ku	Version: 1.0	
Sheetname: SheetName	Sheet * of *	
Subject: TDT4295 Computer Project	Group: Energy	
Schematic file: schematic_A4_template.SchDot		