Project
-Analogic Interface-

Systems with Integrated Circuits 2025

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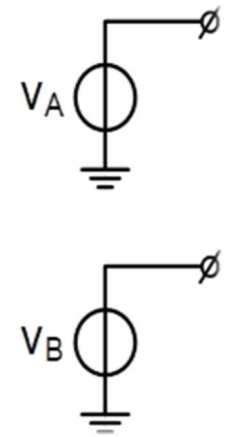
Year 3, Group e_2331

Content

1. Specifications

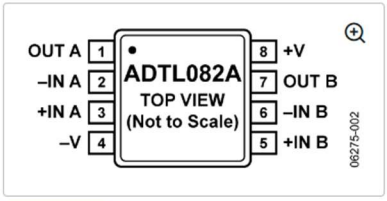
1.1 Etaj 1: V-V instrumentation amplifier with two operational amplifiers in a non-inverting configuration, input V.

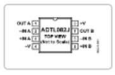
1.1.1 Signal source:differential voltage



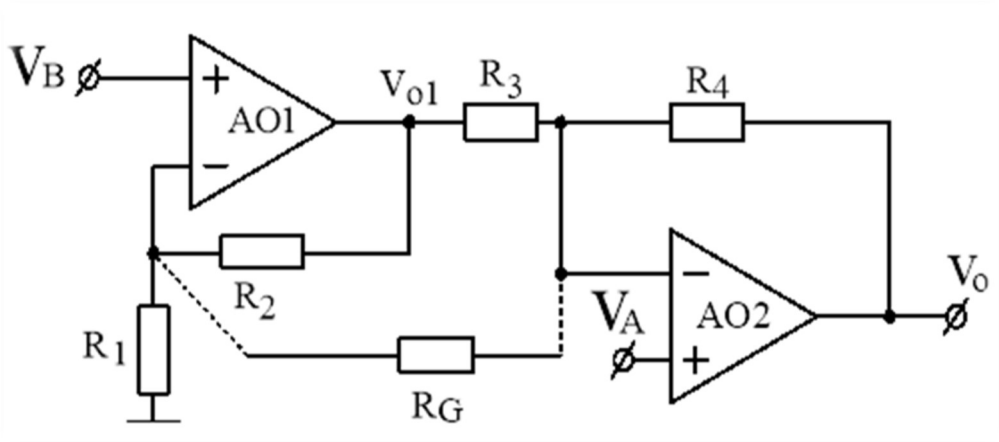
1.1.2 Operational Amplifier used

- TL082/TL084 compatible
- Low input bias current: 10 pA maximum
- Offset voltage
  5.5 mV maximum (ADTL082A/ADTL084A)
  9 mV maximum (ADTL082J/ADTL084J)
- ±15 V operation
- Low noise: 16 nV/√Hz
- Wide bandwidth: 5 MHz
- Slew rate: 20 V/µs
- CMRR: 80 dB minimum
- Total harmonic distortion: 0.001%
- Supply current: 1.2 mA typical
- Unity-gain stable





1.1.3 The circuit:

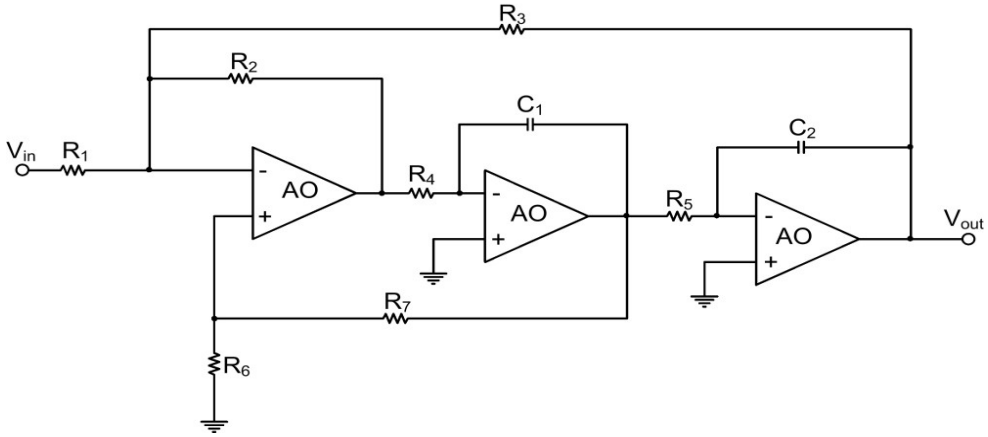


1.1.4 Characteristics

Etaj 1					
Tip Sursa semnal	amplitudine minima (pt castig maxim PGA)	amplitudine maxima (pt castig minim PGA)	unitate masura	Tip Etaj 1	|Castig| etaj 1 (liniar)
2	4.19E-02	8.35E-02	V (differential)	4	9

1.2 Etaj 2: A KHN Filter with 3 inverting OAs(Low Pass)

1.2.1 The circuit:

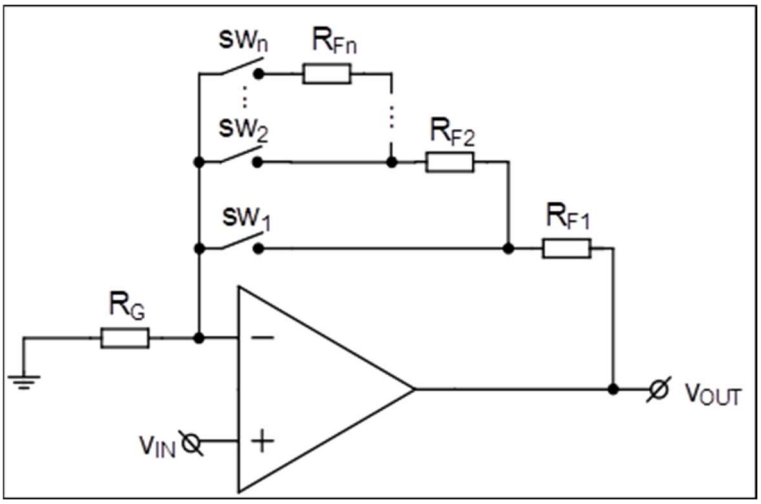


1.2.2 Characteristics of "Etaj 2"

Etaj 2				
tip Etaj 2	|H0| castig liniar in banda de trecere	Rintrare minim	Banda	Q
5	1.00E+00	1.00E+03	3000	0.707

1.3 Etaj 3: A PGA with RF in series and noninverting

1.3.1 The circuit

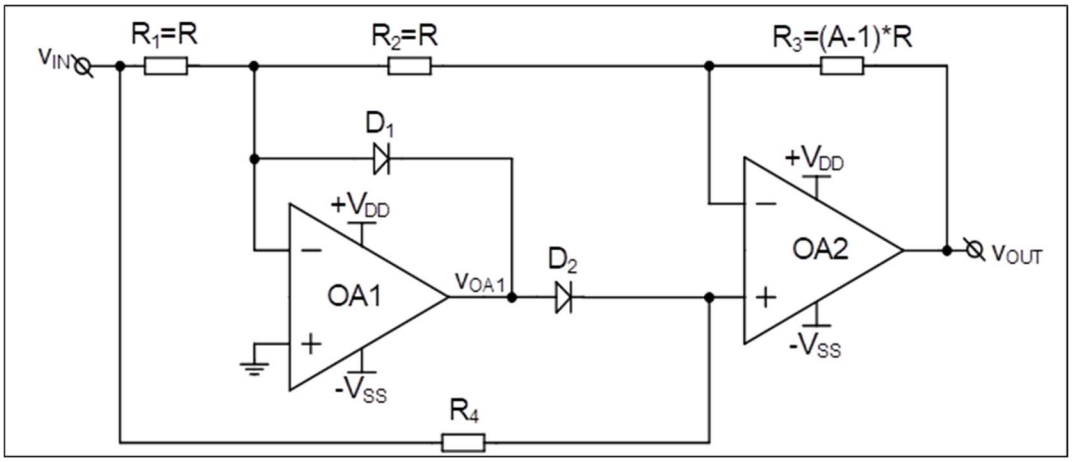


1.3.2 Characteristics

Etaj 3					
tip Etaj 3	castig minim [dB]	rezolutie (pas minim) [dB]	nr pasi	castig maxim [dB]	Rintrare minim
5	6	2	4	1.20E+01	

1.4 Etaj 4:Full wave rectifier

1.4.1.The circuit:



1.4.2 Characteristics:

Etaj 4	
tip Etaj 4	|Castig| etaj 4 (liniar)
3	2

2.Dimensioning

2.1 Etaj 1

For dimensioning this circuit I said that the RG is a part of the structure and I have used the formula of the gain:

$$A_d = \frac{v_O}{v_A - v_B} = 1 + \frac{R_4}{R_3}\left(1 + \frac{R_2 + R_3}{R_G}\right)$$

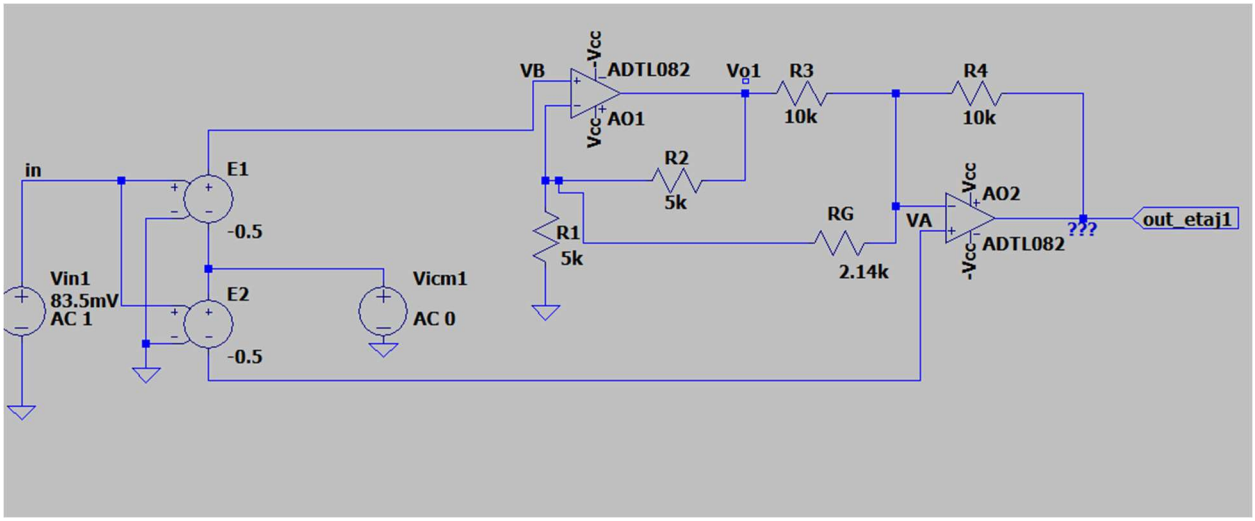
Knowing that my Ad is 9 in linear the formula will be:

$$8 = \frac{R4}{R3} * (1 + \frac{R2 + R3}{Rg})$$

I assume that R4 and R3 are equal and I give them the value 10k and for the R2 I say that is equal to R1 and I give them the value 5k

It result that Rg is 2.14k.

This is the dimensioned circuit in LtSPICE



2.2 Etaj 2

For dimensioning the resistors and the capacitors I have used the formulas from the course knowing that: H0=1(castigul liniar in banda de trecere),Rin=1k,f=3000Hz(banda),Q=0.707.

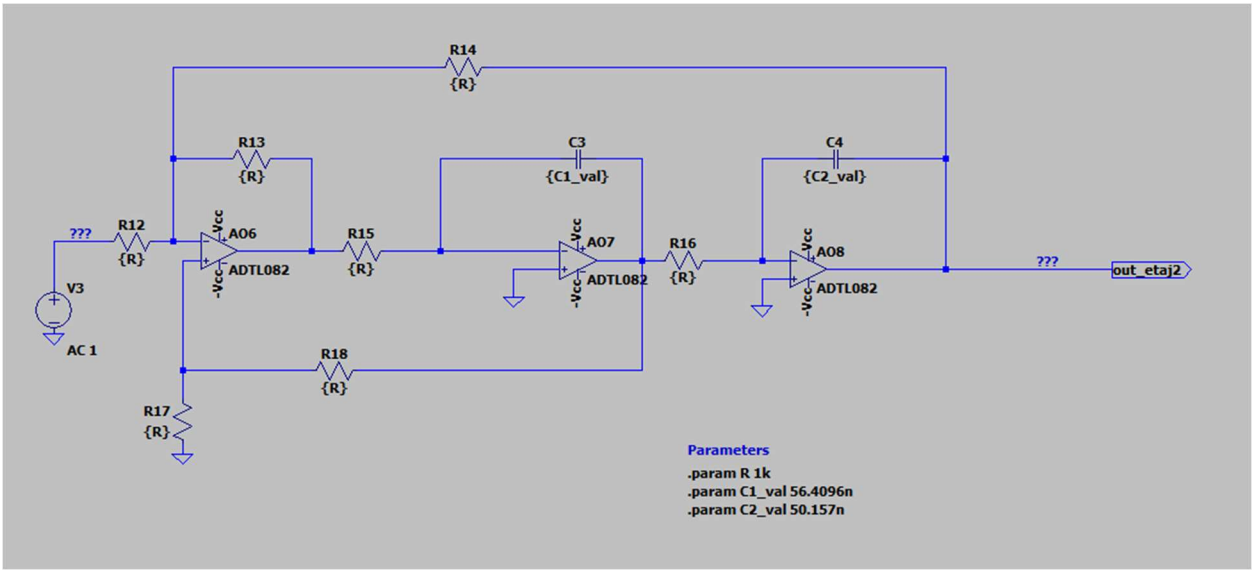
$$\omega = 2pi * f = 1.88e + 04[\frac{rad}{sec}]$$

f0 [Hz]	w0[rad/sec]	Q	H0[V/V]
3.00E+03	1.88E+04	7.07E-01	1.00E+00
	varianta 1		
	C1[F]	set C2[F]	set R[ohm]
	5.63E-08	5.00E-08	1.00E+03

$$C_1 = \frac{3Q}{2\omega_0 R}; C_2 = \frac{4C_1}{9Q^2} = \frac{2}{3Q\omega_0 R}$$

I obtained that C1=56.4nF and C2=50.1nF

The circuit for the KHN Filter



2.3 Etaj 3

For dimensioning the circuit I will utilize my specifications:
Castig maxim=12[dB];Castig minin=6[dB];nr pasi=4;rezolutie=2[dB]

|Av|={6,8,10,12}[dB]->{2,2.51,3.16,4 }

$$x_{liniar} = 10^{\frac{y[dB]}{20}}$$

y=6 => $x_{liniar} = 10^{\frac{6}{20}} = 2$

y=8 => $x_{liniar} = 10^{\frac{8}{20}} = 2.51$

y=10 => $x_{liniar} = 10^{\frac{10}{20}} = 3.16$

y=12 => $x_{liniar} = 10^{\frac{12}{20}} = 4$

The gain at noninverting is**:1+Rf/Rg.**Rin=Rg=>I choose for Rg to be 10k

Case 1:SW1-On,Sw2-off,Sw3-off,Sw4-off

$$R_f = R_1$$

$$|A_v| = 1 + \frac{R_1}{R_g} = 2 => R_1 = 1 * R_g => R_1 = R_g = 10k$$

Case 2:SW1-off,Sw2-on,Sw3-off,Sw4-off

$$R_f = R_1 + R_2$$

$$|A_v| = 1 + \frac{R_1 + R_2}{R_g} = 2.51 => R_1 + R_2 = 1.51 * R_g => R_2 = 5.1k$$

Case 3:SW1-off,Sw2-off,Sw3-on,Sw4-off

$$R_f = R_1 + R_2 + R_3$$

$$|A_v| = 1 + \frac{R_1 + R_2 + R_3}{R_g} = 3.16 => R_1 + R_2 + R_3 = 2.16 * R_g => R_3 = 6.5k$$

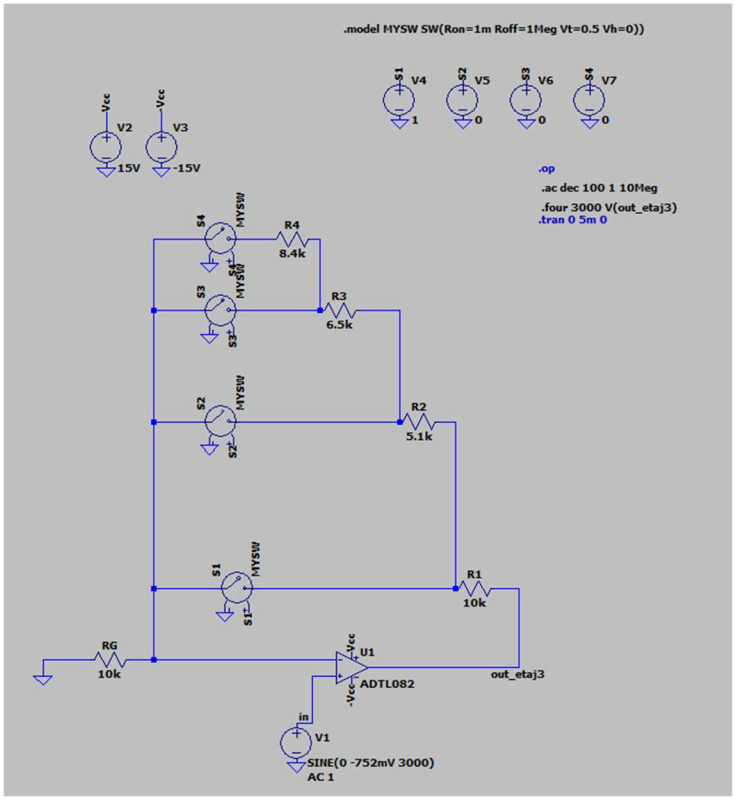
Case 4:SW1-off,Sw2-off,Sw3-off,Sw4-on

$$|A_v| = 1 + \frac{R_1 + R_2 + R_3 + R_4}{R_g} = 4 => R_1 + R_2 + R_3 + R_4 = 3 * R_g => R_4 = 8.4k$$

Rf_total=R1+R2+R3+R4=30k
Rtotal=Rg+Rf_total=40k

SW4	SW3	SW2	SW1	Rin=Rg	AV[dB]	AV[linear]	Obs	Banda
1	0	0	0	10k	12	4	castig.max=41.9mV	4.42Mhz
0	1	0	0	10k	10	3.16		3.51Mhz
0	0	1	0	10k	8	2.51		2.80Mhz
0	0	0	1	10k	6	2	castig.min=85.3mV	2.23Mhz

The PGA(Noninverting Rf series)

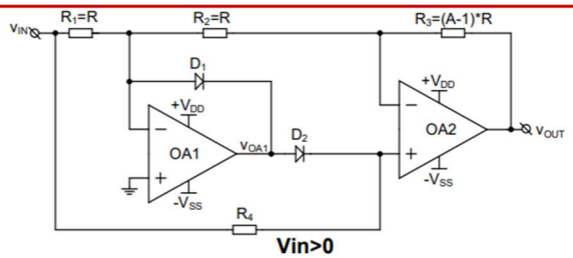


2.4 Etaj 4

Schematic

Advantage:
needs only two
matched resistors

Transfer function



Vin<0
Assume D_1, D_2 = OFF
V_1^+ =0; V_1^- <0 => V_{OA1} ↗V_{OH} => D_1 = OFF;
D_2 = ON
OA1 has a negative feedback loop as
$V_2^+ = V_2^-$ => $V_1^- = V_1^+$ =0 => i_{R1} = Vin/R_1

i_{R1} = Vin/R_1 closes through R2,R3 and V_1^- = 0

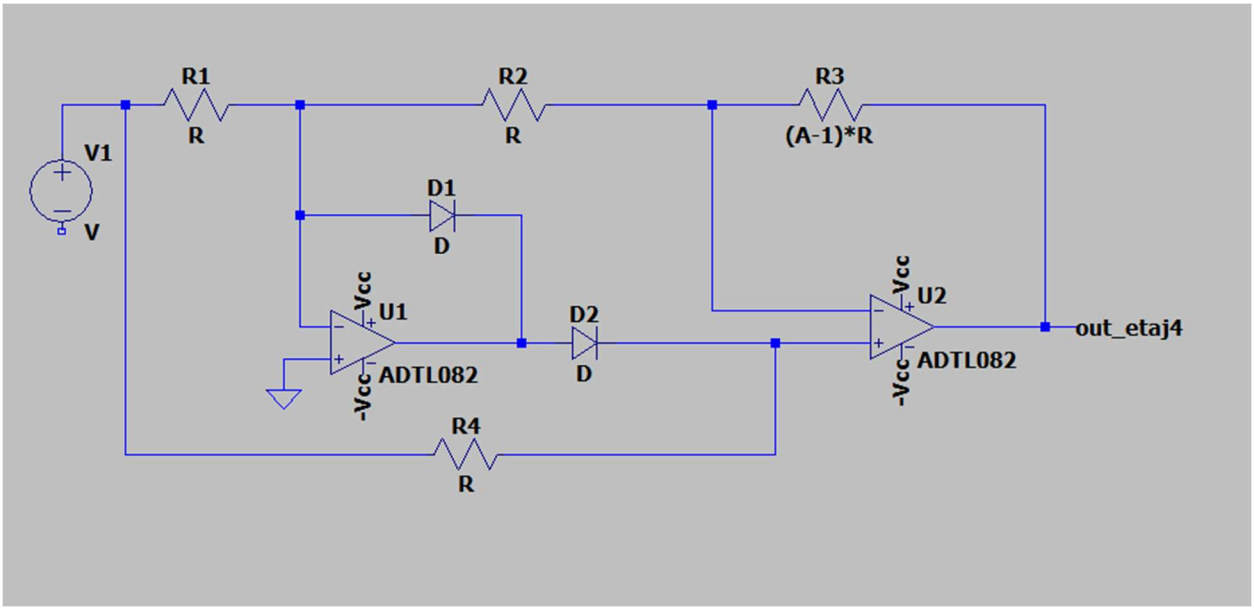
V_{Out} =0 – (R_2+R_3)V_{in} /R_1= -V_{in} (R_2+R_3)/R_1

Condition for operating as a FWR:
(R_2+R_3)/R_1 = 1+R_3/R_2 => R_1= R_2

Vin>0
Assume D_1, D_2 = OFF
V_1^+ =0; V_1^- >0 => V_{OA} ↘V_{OL} => D_1 = ON;
D_2 = OFF
OA1 has a negative feedback loop thru D_1
=> $V_1^- = V_1^+$ =0
i_{R1} = Vin/R_1 closes through D_1
OA2 implements an inverting amplifier
(or: $V_2^- = V_2^+$ = Vin => same current through
R_2 and R_3 = i_{R2} = Vin/R_2;
V_{Out} = V_{Out} +VinR$_3$/R_2)
V_{0ut} = V_{in} (1+R_3/R_2)

$$Vout = \begin{cases} A\,V_{In} & \text{if } V_{In} > 0 \\ -A\,V_{In} & \text{if } V_{In} < 0 \end{cases}$$

Full wave rectifier

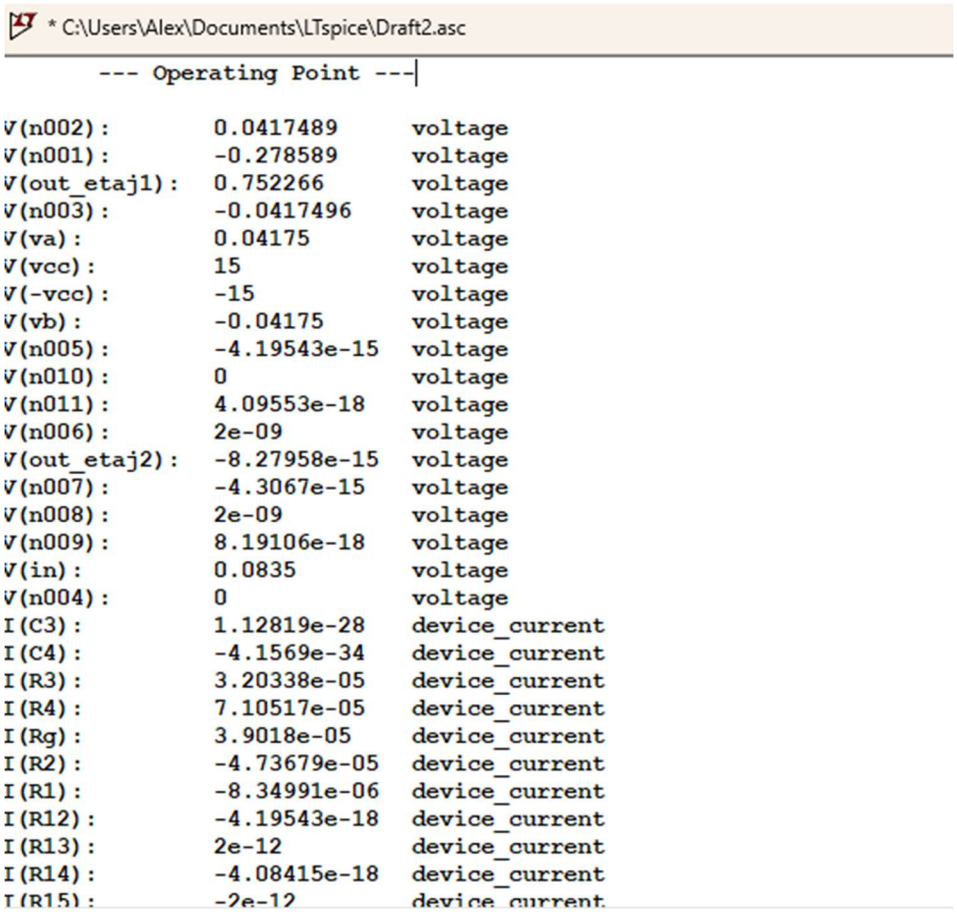


3.Characterization/Simulations

3.1 Characterization “etaj 1”(Instrumentation Amplifier)

3.1.1 DCOP

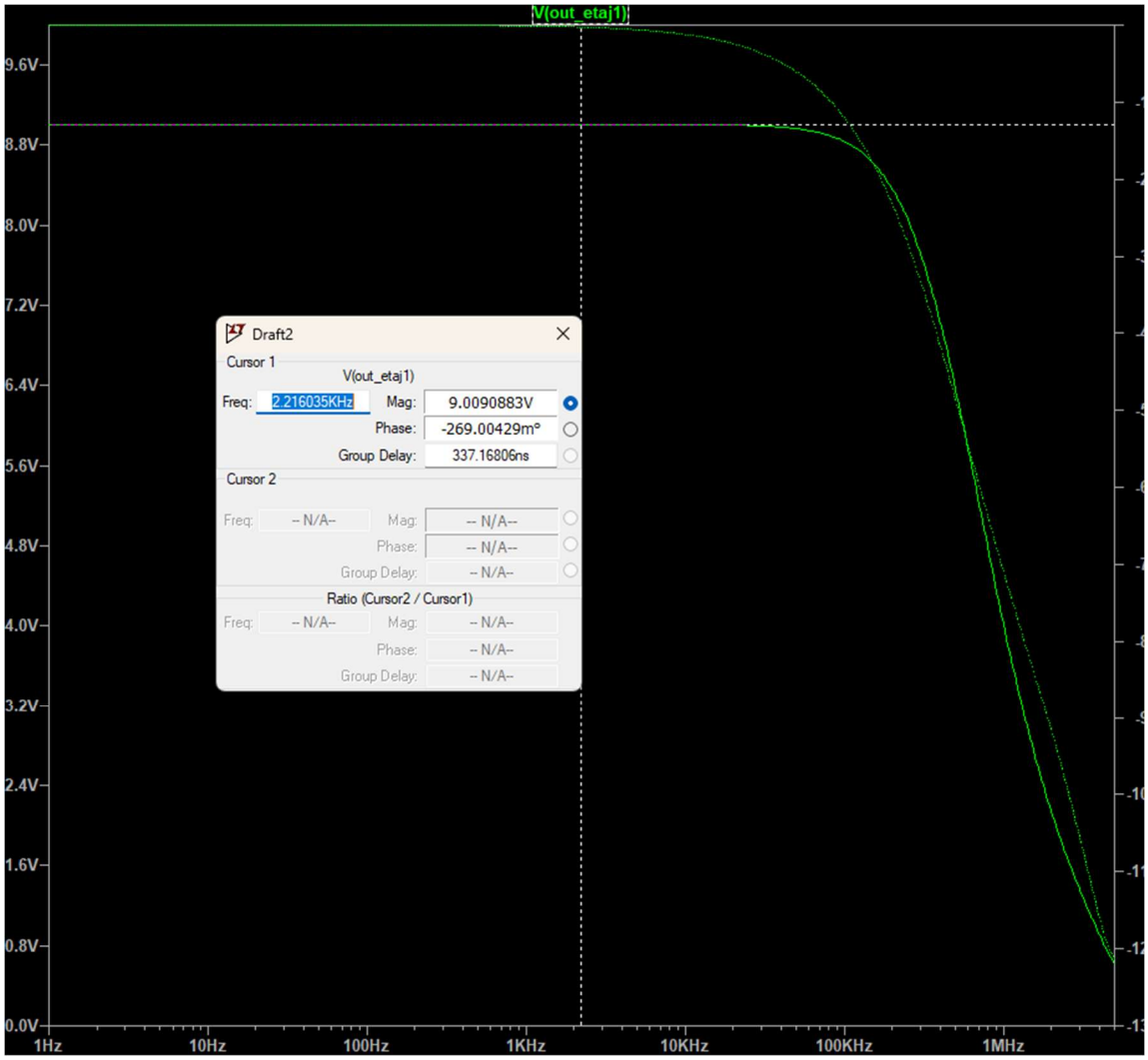
For the input I choose the maximum amplitude(83.5mV).The V(out_etaj1)is 752mV that means is amplified 9 times.



3.1.2 AC:castig la joasa frecventa

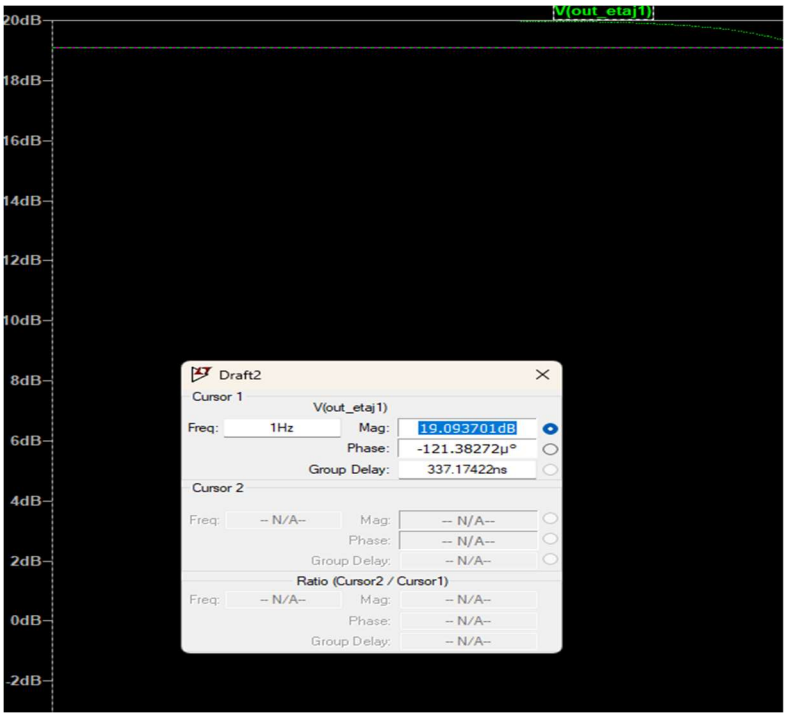
The simulation: .ac dec 100 .01 10Meg

To check if everything is working good,I switched in linear with the AC simulation and I verified if the measured gain is equal to the given one and it seems working.For the input I have used a SINE Signal with DC value:0,Amplitude:83.5mV and f=3000(the one from the table)



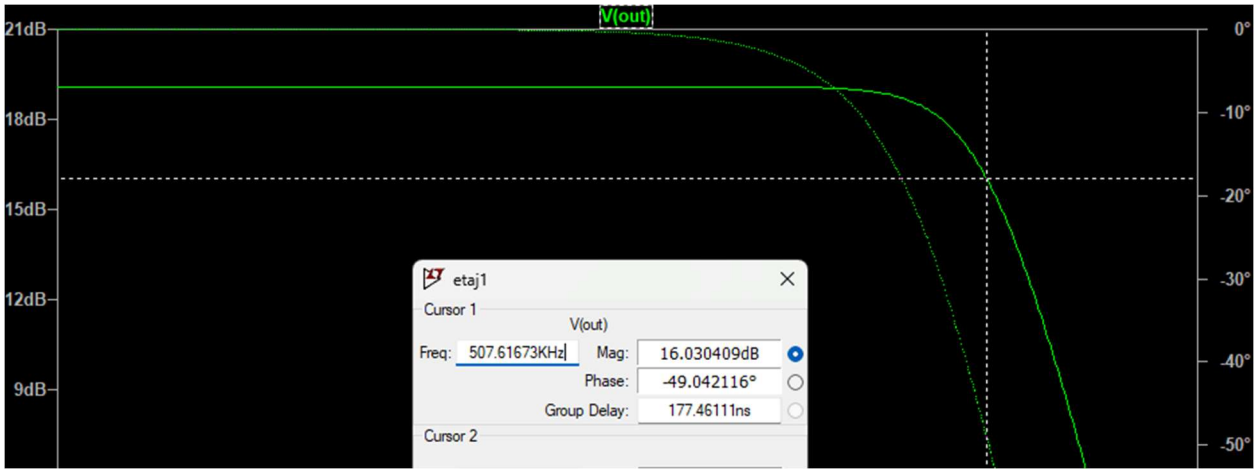
Then I moved into the Decibel simulations to measure the:

Low frequency gain is: 19.093701dB



3.1.3 AC:banda>banda filtru

To determine the bandwidth I have done the same AC simulation and I measured the band at -3dB



The bandwidth of the filter is 3Khz and the measured one is 507Khz which is bigger

3.1.4 AC:CMRR

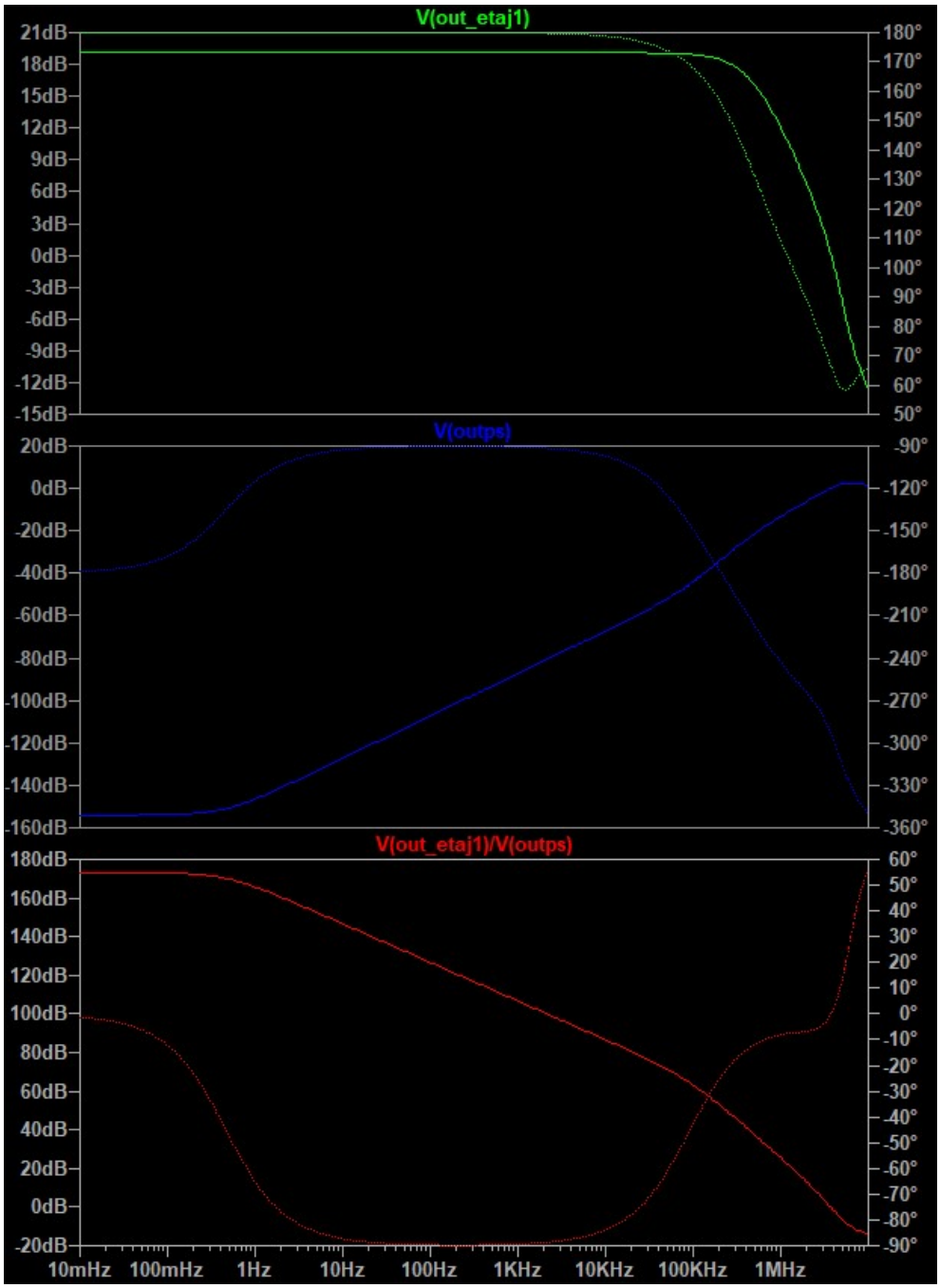
CMRR(Common mode rejection ratio) is the measure of a device's ability to reject the signal common to both the positive and negative device inputs.

To determine the CMRR I have used the circuit from the laboratory which is the same as mine but with a different circuit for CMRR and PSRR.At the input I put AC 0 and for Vicm AC 1

The ideal values needs to be 80dB minimum and here the measured one is 110dB

3.1.5 AC:PSRR

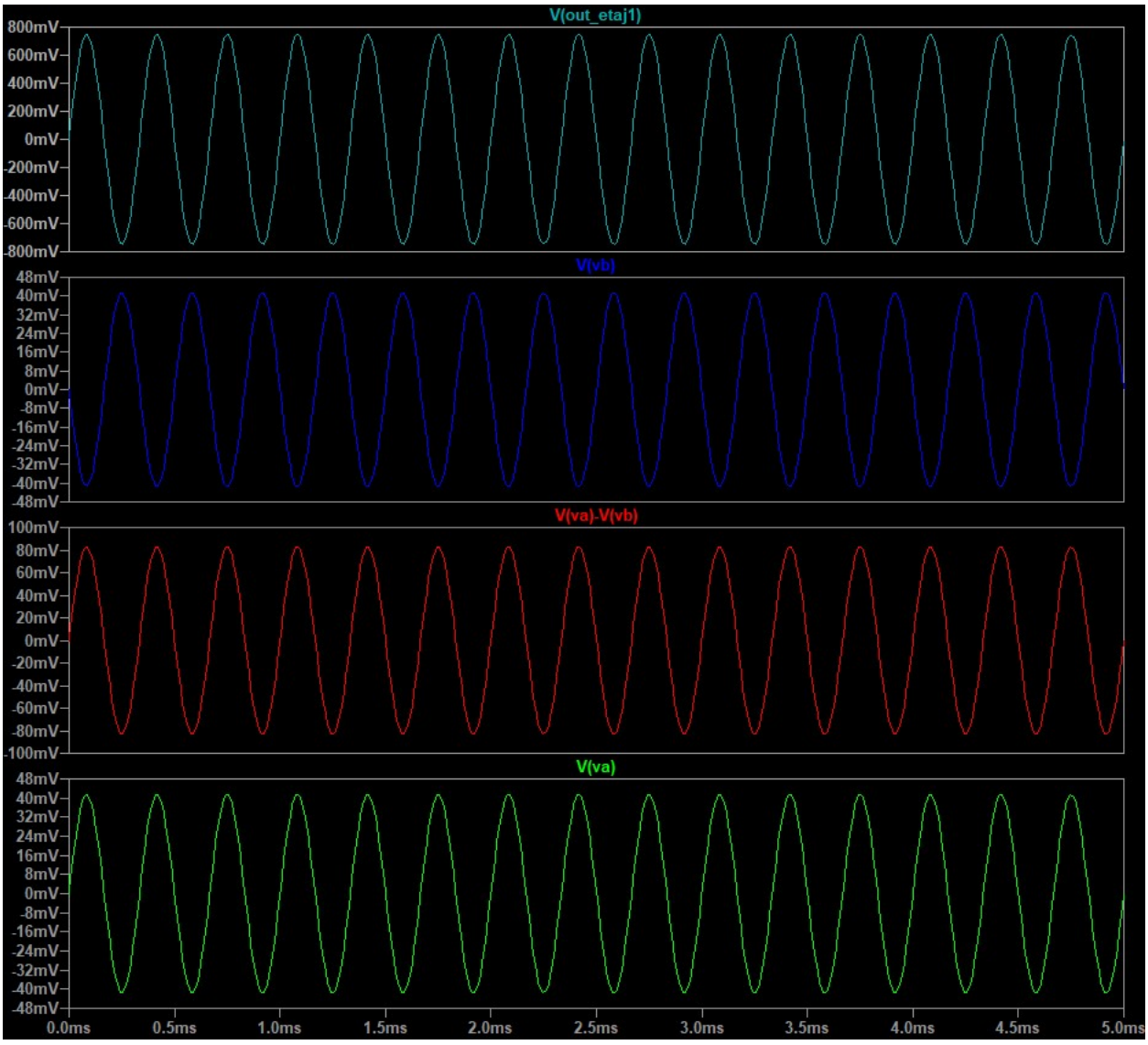
PSRR(Power supply rejection ratio)- a measure of a circuit's power supply's rejection expressed as a log ratio of output noise to input noise.Input AC 0 and Vicm 0 because I have another V+ that is Vpsr



the ideal values needs to be 80dB minimum and here the measured one is 100dB

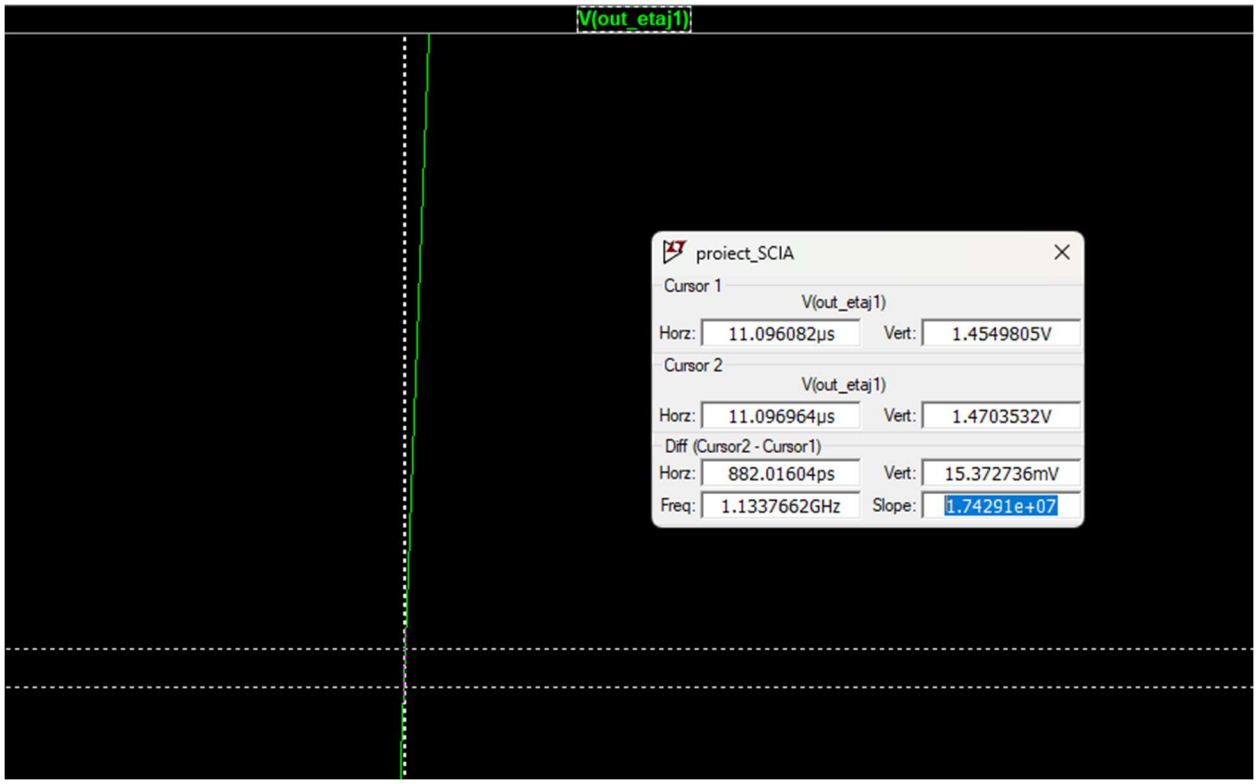
3.1.6 Transient:SR(slew rate)

The simulation used to verify if the circuit is working properly checking if Va-Vb=83.5mV and Vo=(Va-Vb)*9



The simulation for the Slew Rate:tran 20u

The Slew Rate is the maximum rate of change of an op amps output voltage
For measuring the Slew Rate we apply at the input a PULSE signal.



The measure Slew Rate is 17V/uS

3.1.7 Transient:Liniaritate>specs(THD<%1)

The simulation **The result**

```
.four 3k V(out_etaj1)
```

```
Total Harmonic Distortion:   0.304543%
```

3.2 Characterization "etaj 2"'(KHN Filter)

3.2.1 DCOP

The simulation OP. is the one that we need for this part and at the input we apply a DC input of 752mV

* C:\Users\Alex\Documents\LTspice\etaj2.asc

```
      --- Operating Point ---

V(vcc):         15              voltage
V(-vcc):        -15             voltage
V(n001):        6.73973e-07     voltage
V(n006):        0.752           voltage
V(n007):        6.73972e-07     voltage
V(n002):        1.99779e-09     voltage
V(out_etaj2):   -0.751998       voltage
V(n003):        -2.21457e-12    voltage
V(n004):        1.34994e-06     voltage
V(n005):        1.34794e-06     voltage
I(C1):          7.615e-26       device_current
I(C2):          -3.7718e-20     device_current
```

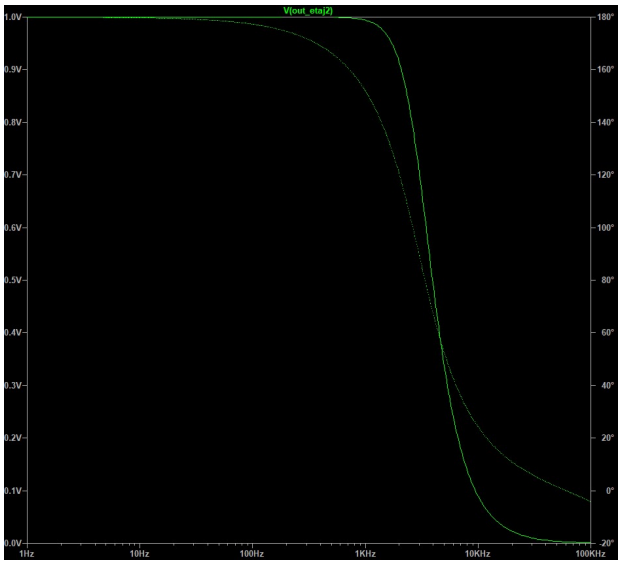
The output is -752mV as the calculated one

The formula for this one is: $\frac{Vout}{Vin} = \frac{H0}{1+\frac{2}{w}}$ and the result is -752mV

The output is negative due to the 3 inverting OpAmps.

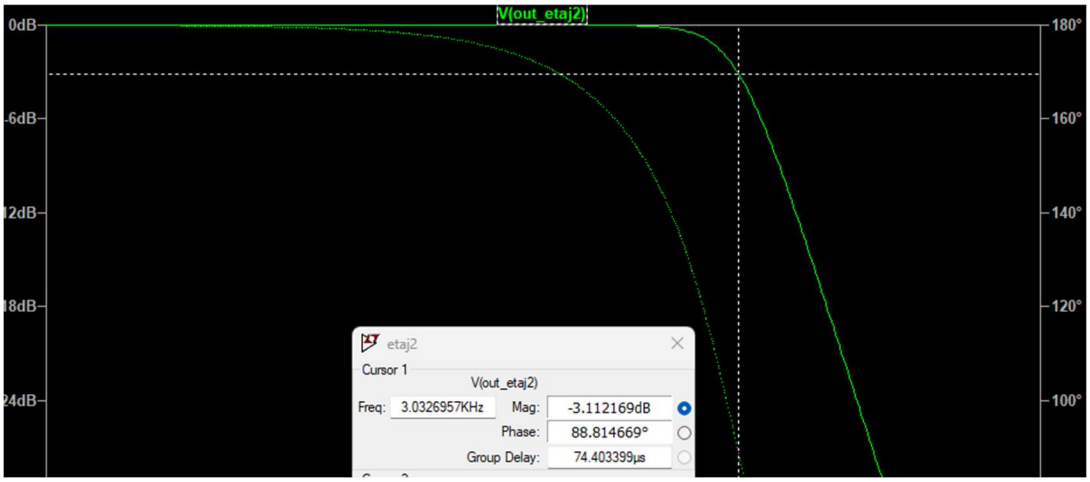
3.2.2 AC:Castig in banda de trecere=specs

The simulation here is:**ac dec 100 1 10k** and the H0 is 0dB.I moved in **linear** and I observed that I obtain 1 as in the specifications



3.2.3 AC:banda=specs

To measure the bandwidth for a low pass filter you have to measure it at -3dB

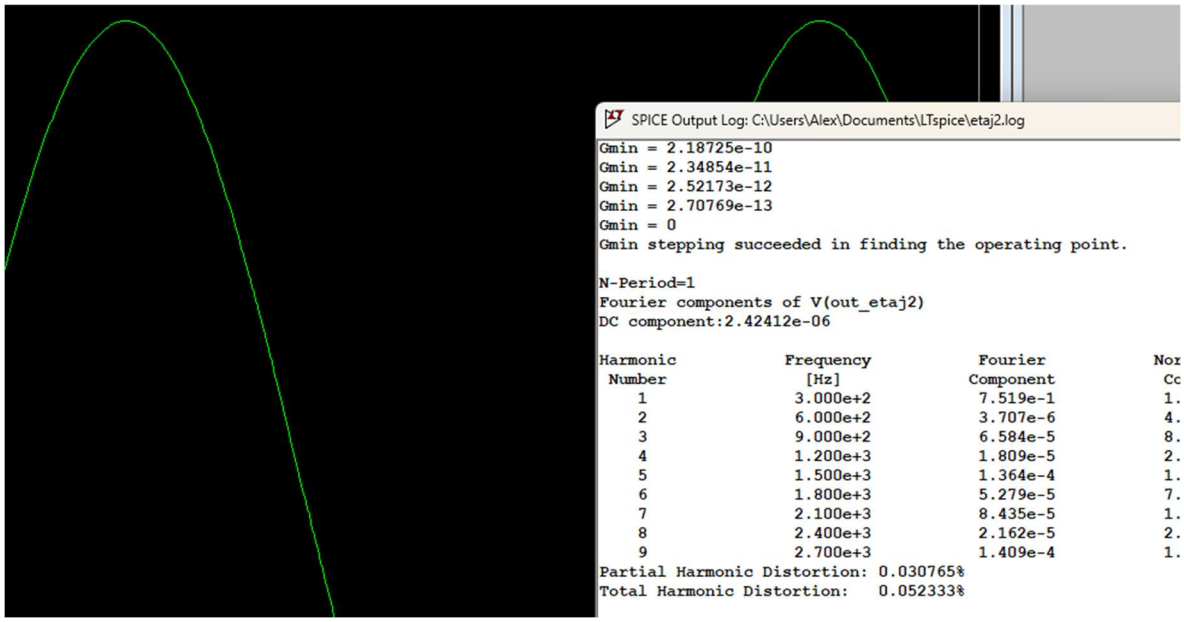


The bandwidth is 3.03kHz that is equal to the specs

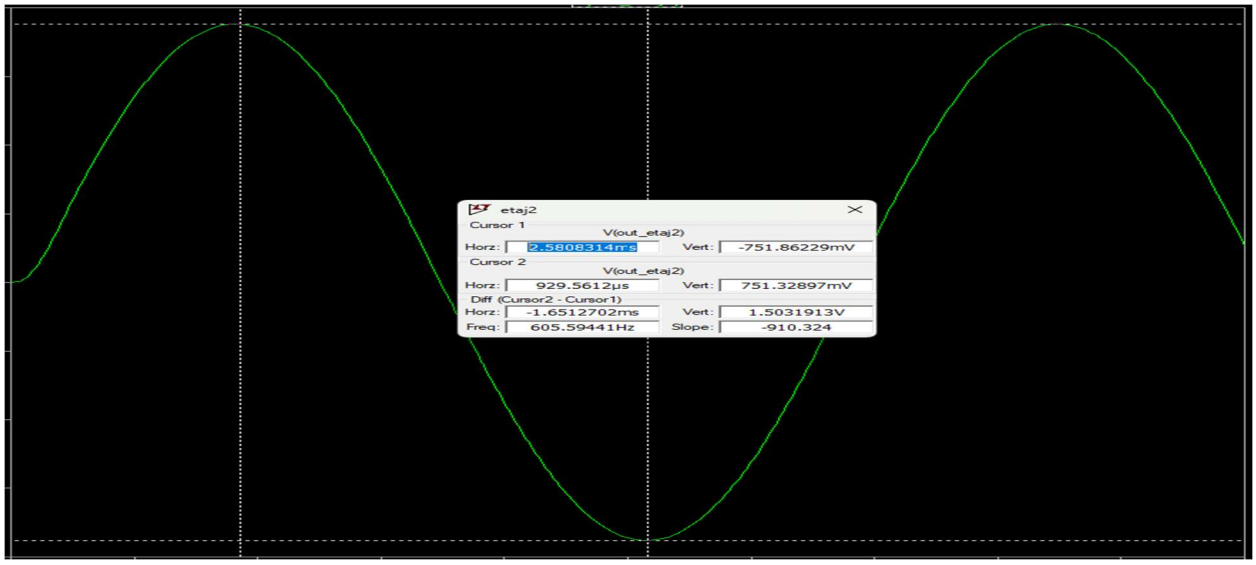
3.2.4 Transient:Liniaritate

For measuring the linearity it says in the General Specifications that I have to use "fara distorsiuni la fin_max/10 pt ampl_in*castig (THD<1%)" so I used the frequency 300Hz at the Sine input and my H0 is 1 and the THD should be less than 1%

The simulation is **.tran 5m 0 10u**



The THD is 0.0523%

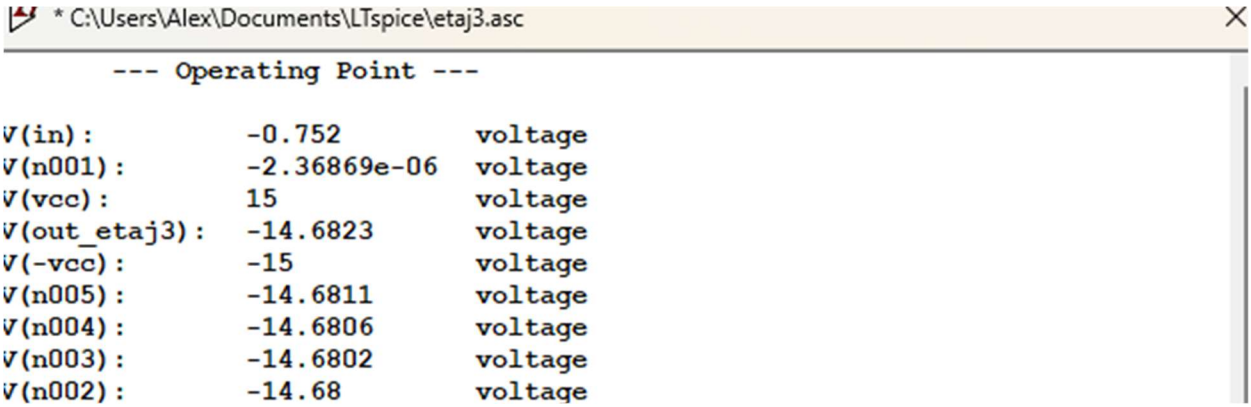


Amplitude peak to peak is -752mV

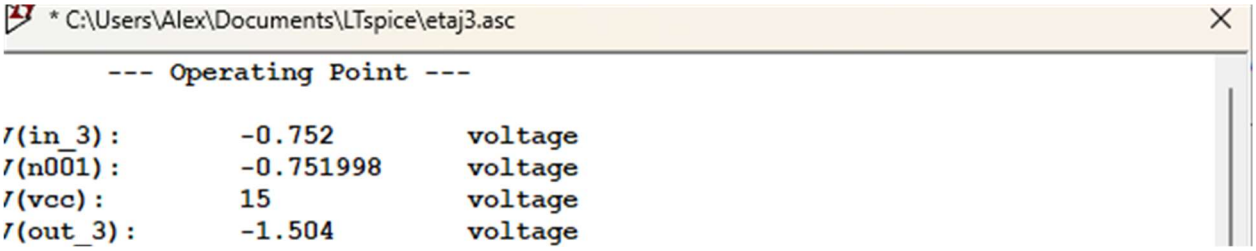
3.3 Characterization “etaj 3” (PGA noninverting)

3.3.1 DCOP

With the switches turned off ‘0’



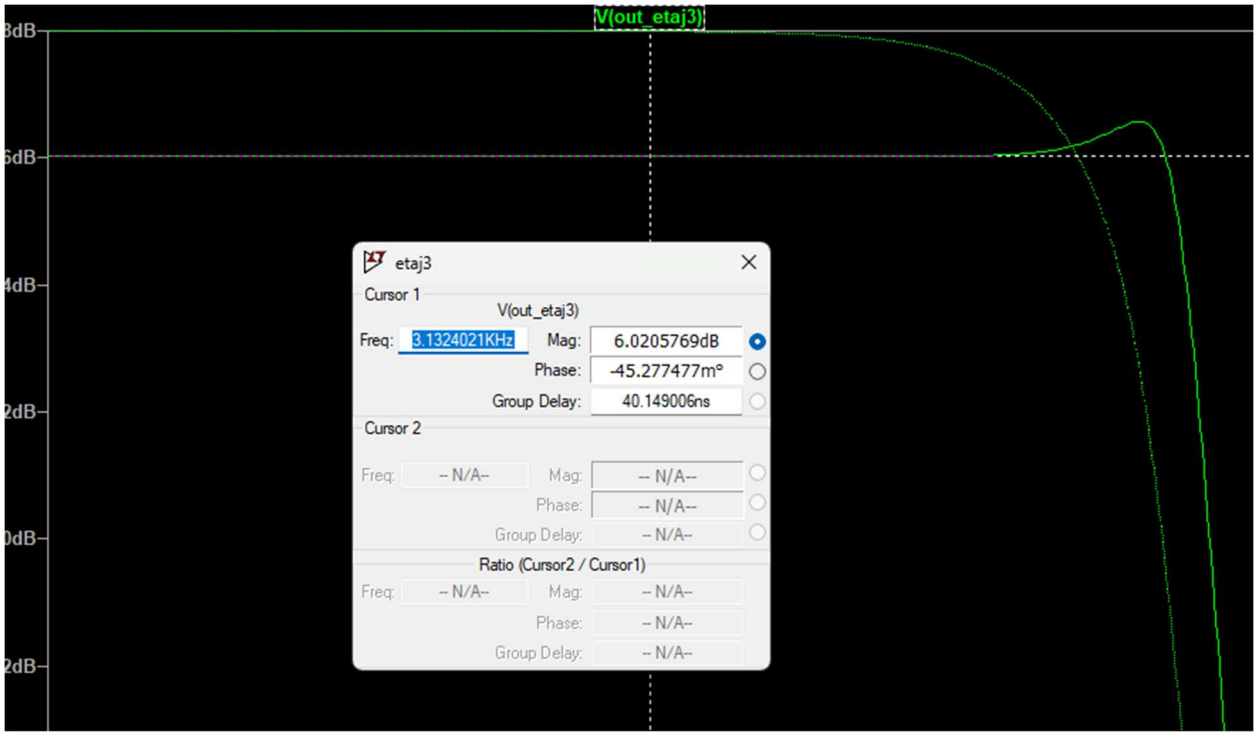
With switch 1 turned on and the maximum amplitude applied.



3.3.2 AC:toate treptele de castig

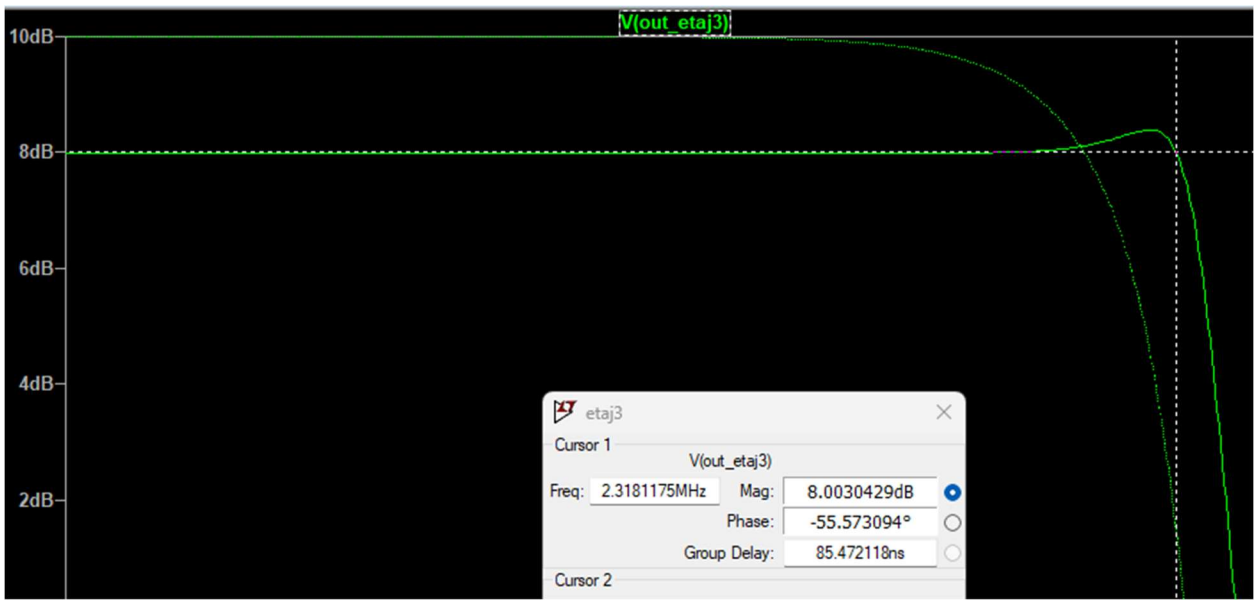
For the input I should have used the minim amplitude:41.9mV*9=377,1mV but I decide to use the maximum one that is 752mV and due to the filter I place it with negative value

Case 1:SW1-On,Sw2-off,Sw3-off,Sw4-off



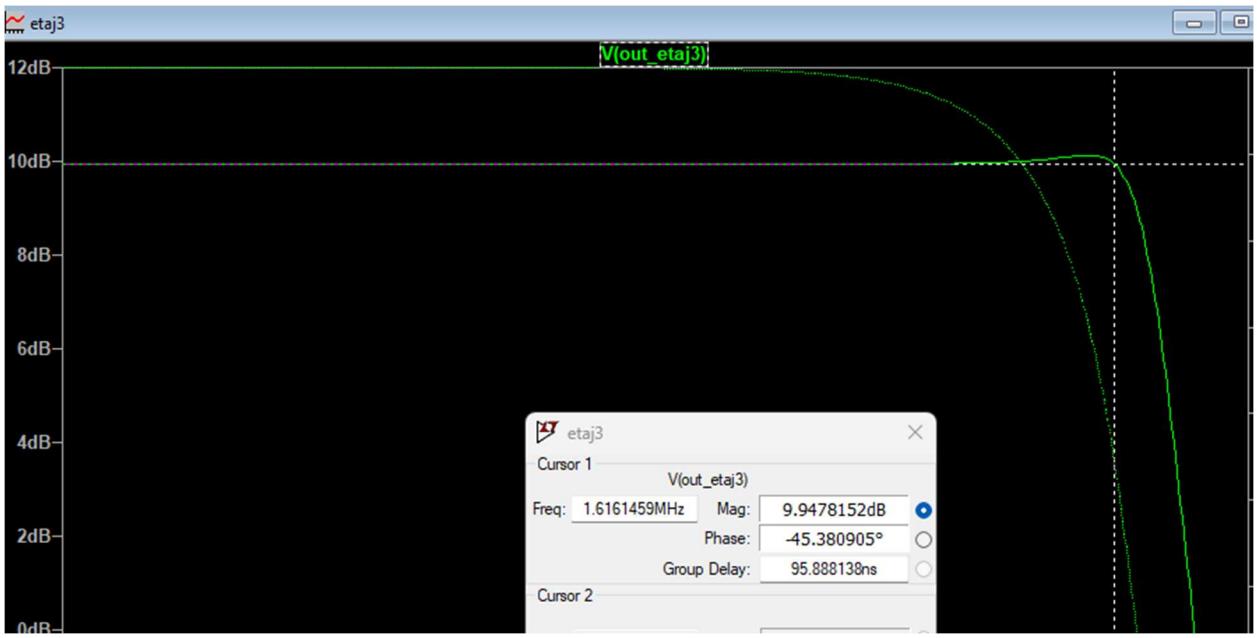
The measured gain is 6.02dB

Case 2:SW1-off,Sw2-on,Sw3-off,Sw4-off



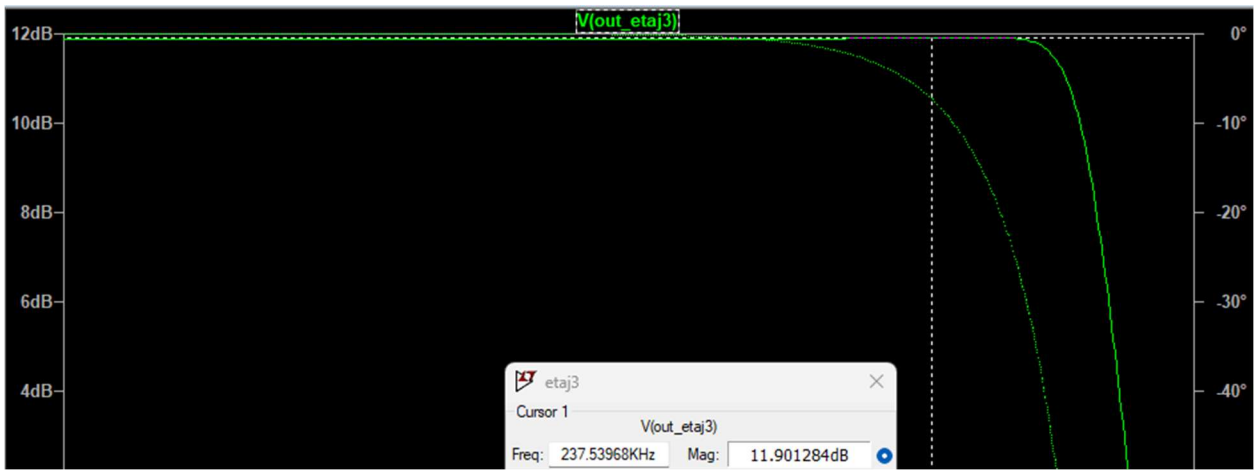
The measured gain is 8.00dB

Case 3:SW1-off,Sw2-off,Sw3-on,Sw4-off



The measured gain is 9.94dB

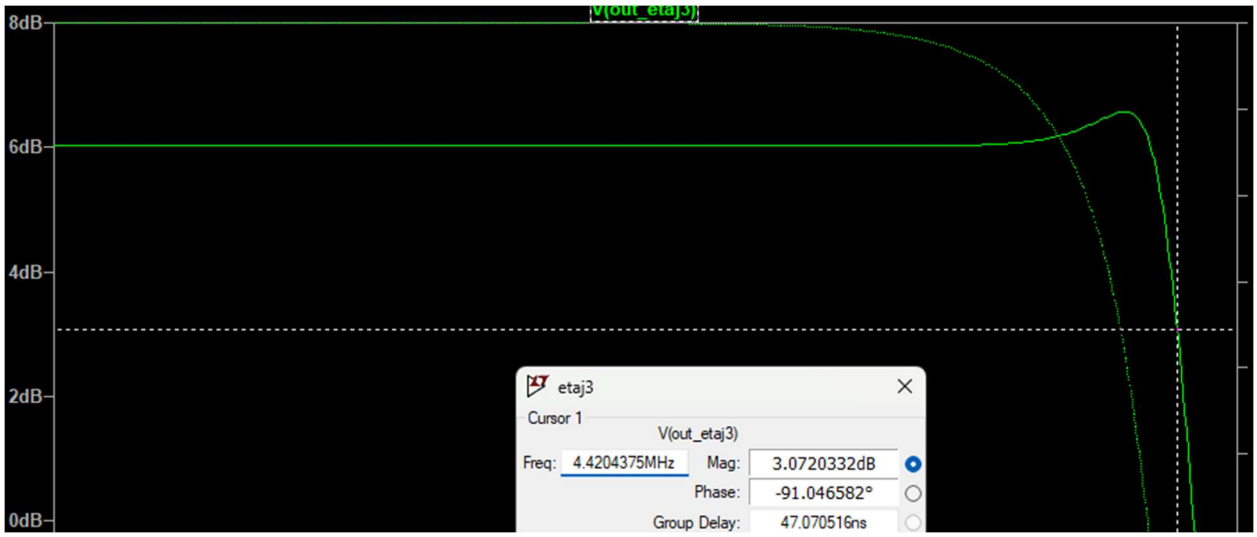
Case 4:SW1-off,Sw2-off,Sw3-off,Sw4-on



The measured gain is 11.90dB

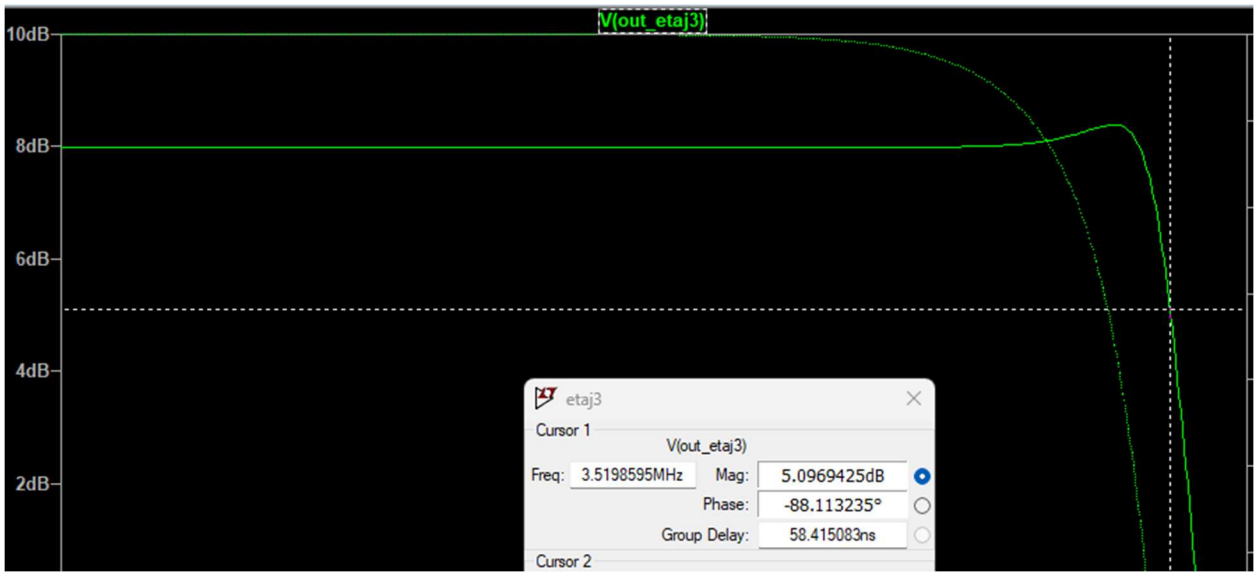
3.3.3 AC:Banda PGA

Case 1:SW1-On,Sw2-off,Sw3-off,Sw4-off



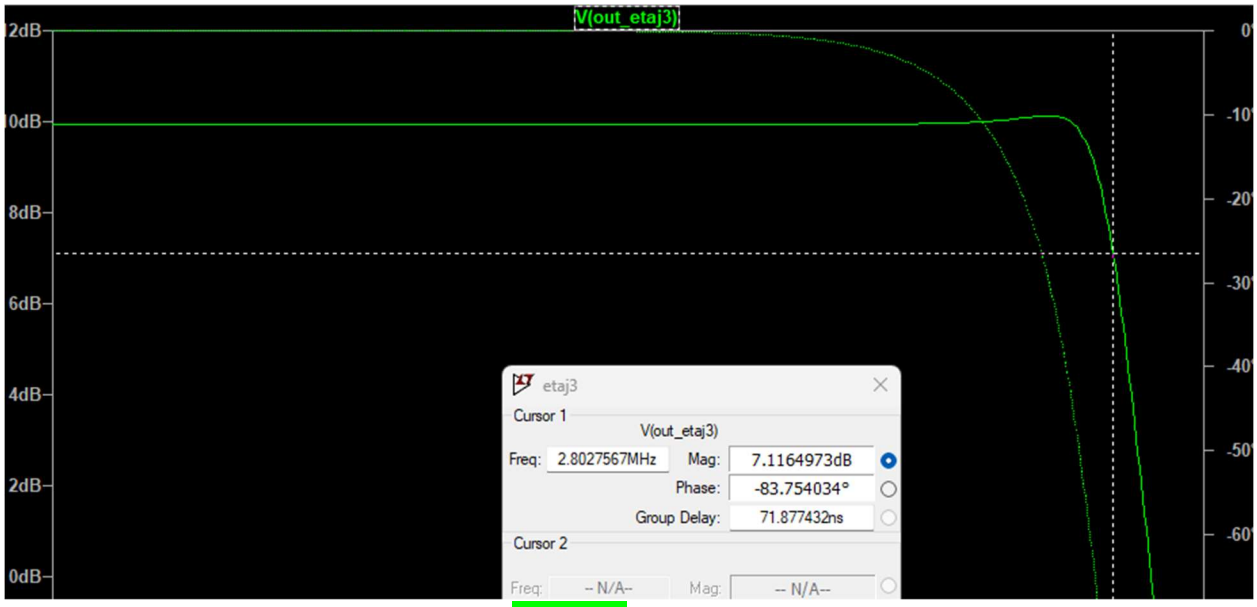
BW=4.42Mhz>'banda filtru'

Case 2:SW1-off,Sw2-on,Sw3-off,Sw4-off



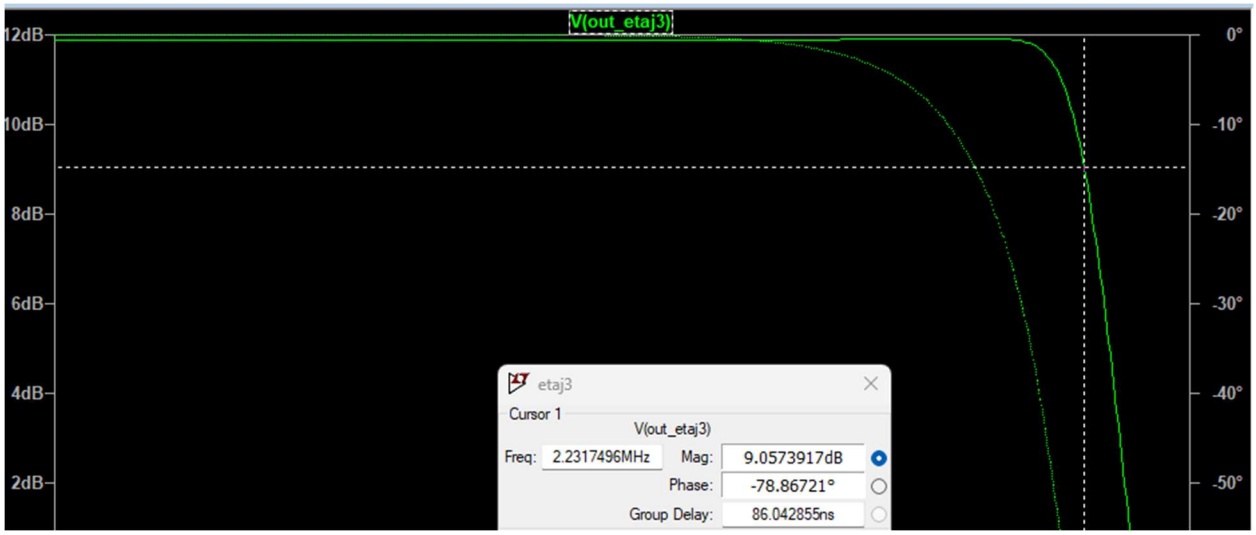
BW=3.51Mhz>'banda filtru'

Case 3:SW1-off,Sw2-off,Sw3-on,Sw4-off



BW=2.80Mhz>'banda filtru'

Case 4:SW1-off,Sw2-off,Sw3-off,Sw4-on



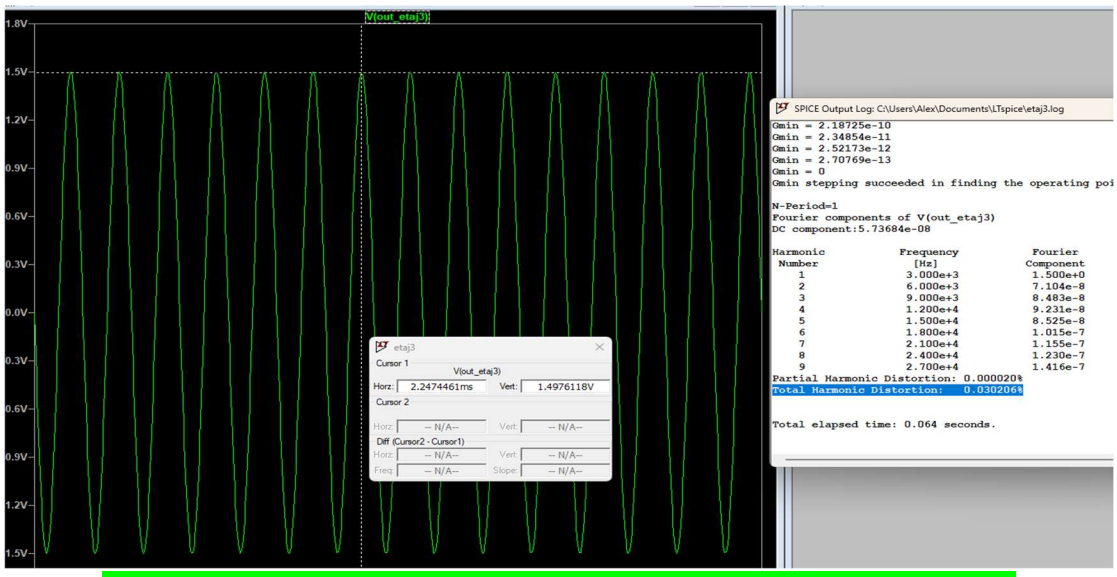
BW= 2.23Mhz>'banda filtru'

3.3.4 Transient:Liniaritate>Specs pt castig min/max(pentru THD<1%)

' fara distorsiuni la fin_max pt ampl_in_min*castig_max_PGA si ampli_in_max*castig_min PGA(THD<1%)'

The linearity for minimum gain(when Vin from ‘etaj 1’is 83.5mV)

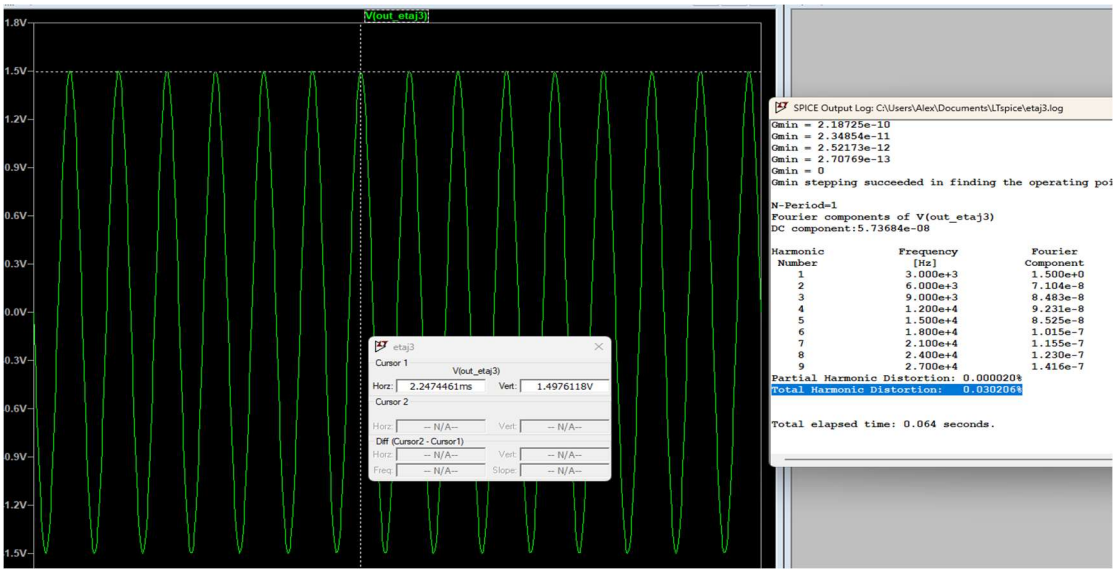
Ampl_in_max*castig_min: 83.5*2=167mV but with the amplification from etaj 1 the input is 752mV and with the castig_min that means:752*2=1.50



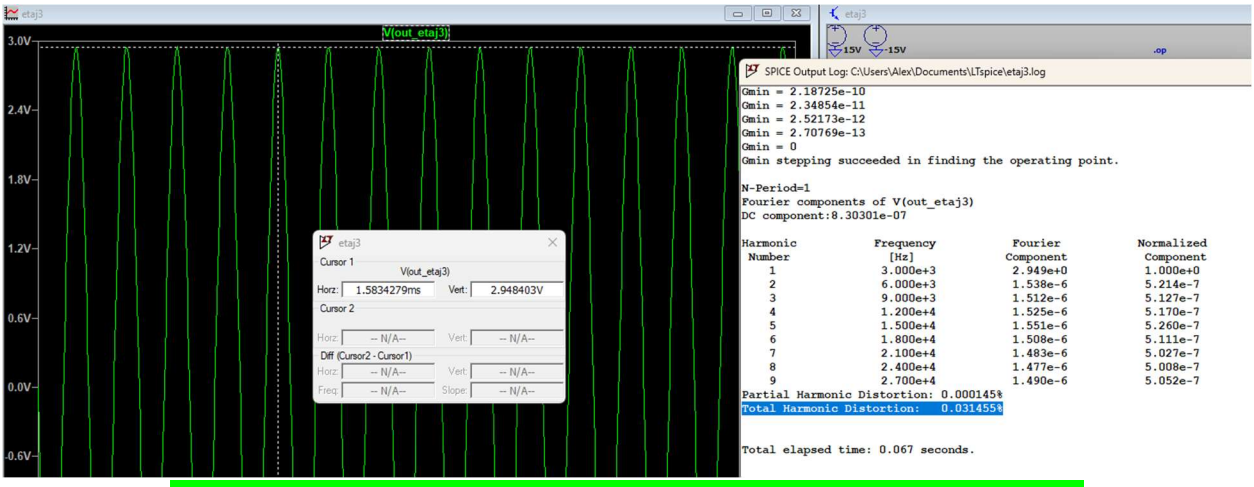
The THD is<1% and the amplitude for the circuit to be linear is |1.49|V

The linearity for maximum gain(when Vin is the output from the ‘etaj2’) but with the amplification from etaj 1 the input is 377mV and with the castig_min that means:

Ampl_in_min*castig_max: or 41.9*4=167.6



The simulation that I used for the output is that I placed the maximum amplitude and the maximum gain:752mV*4=3V but it s saturated

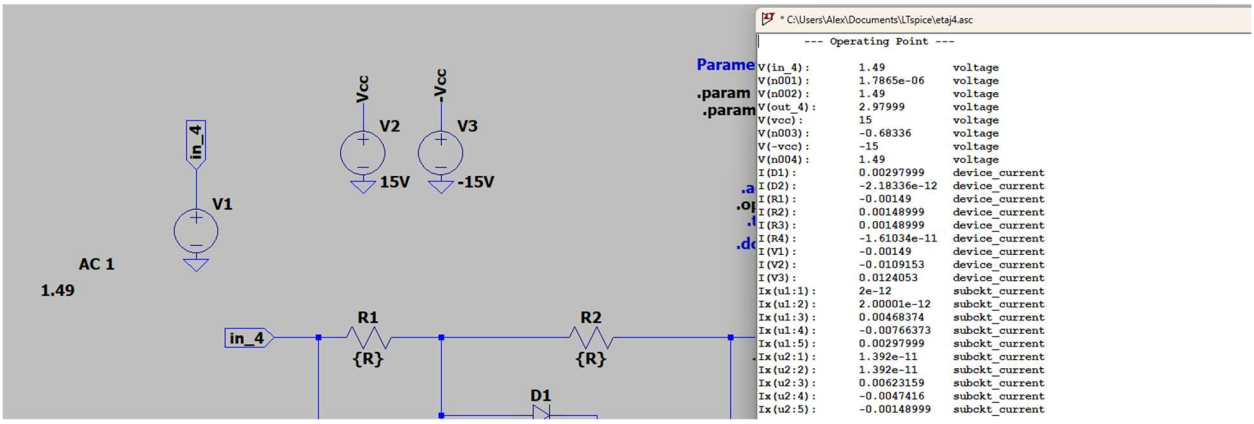


The THD is<1% and the amplitude for the circuit to be linear is |2.94|V

3.4 Characterization ‘etaj4’(Full wave rectifier)

3.4.1 DCOP

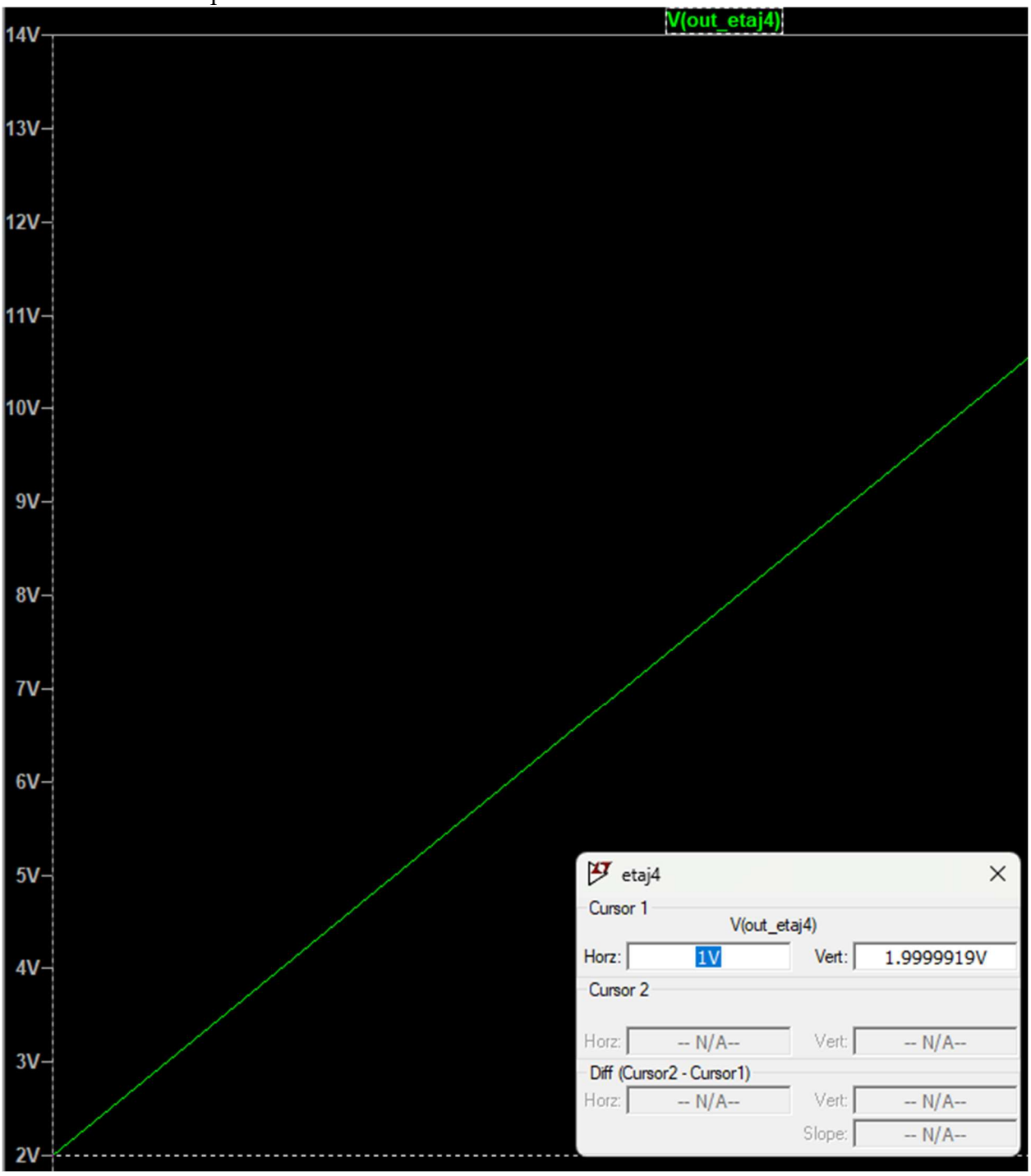
My voltage input is 1.49V



V(out_etaj4)=2.98V

3.4.2 DC Sweep+Transient:castig

I used the DC Sweep simulation with:.dc V1 1 10 1



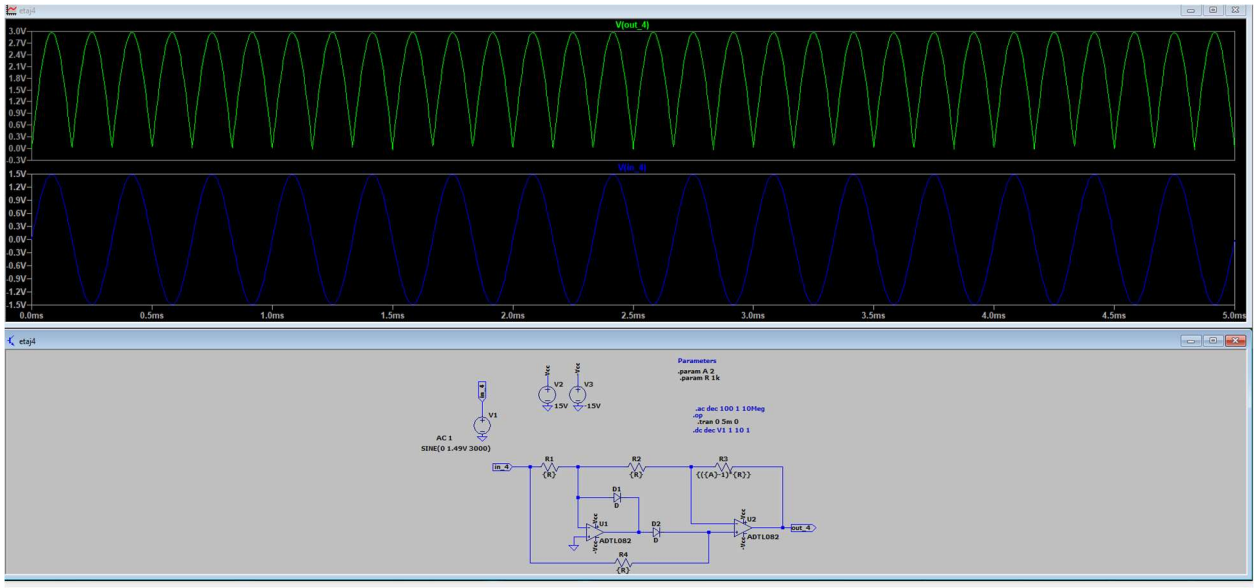
The gain is 1.9999

3.4.3 Transient:Implementare functie de circuit

Using the transient simulation and at the input I have used from the 'Etaj 3' the amplitude for the output when SW4 is on:2.94V.

Plotting the V(out_etaj4) I checked if the plot is like in the course

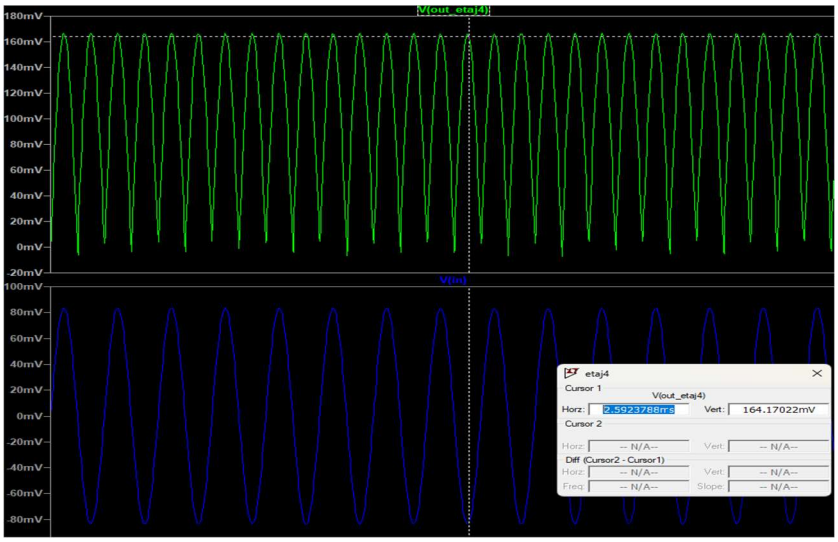
Vout=A*Vin when Vin>0 and Vout= -A*Vin when Vin<0

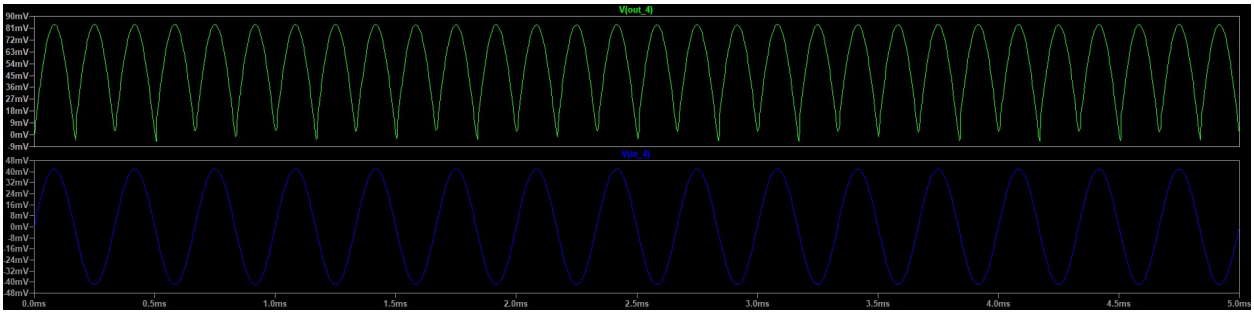


The maximum amplitude for the output is 2.98V (A*Vin)

3.4.4 Transient:domeniu de functionare>amplitudine intrare maxima

Case1: we can't verify the 'liniarity' because practically this circuit is a non linear one,but we can verify the functionality at maximum amplitude and minimum.

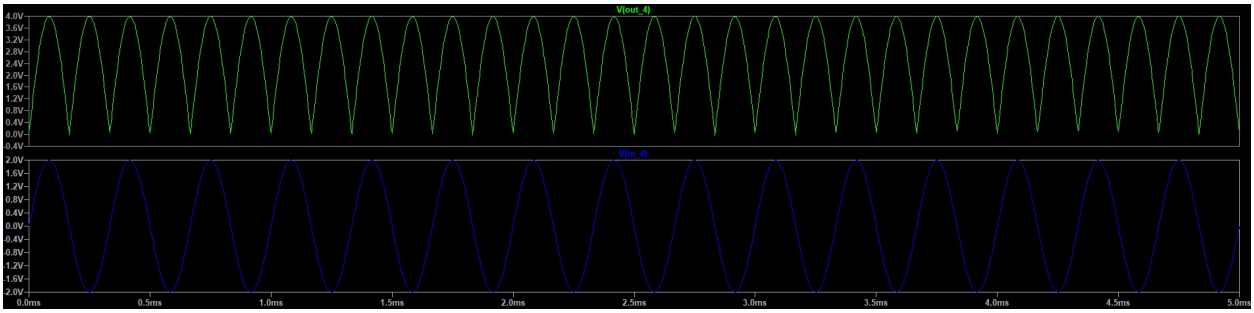




Case2:we can verify with this formula:

ampl_max*castig_etaj1*castig_etaj2*castig_etaj3_min=83.5mV*9*1*2=1.5V

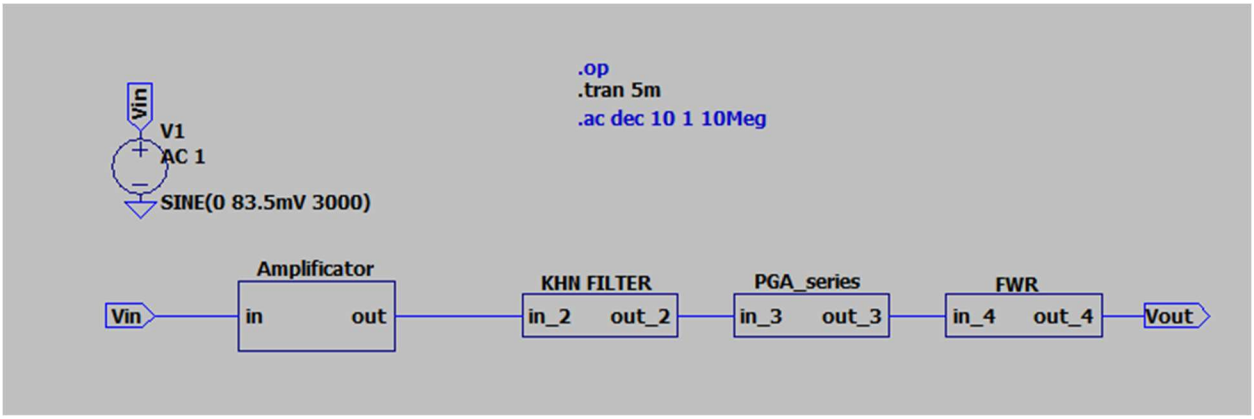
To fullfill the requirement we need a amplitude bigger than 1.5V so I am going to apply a SINE of V



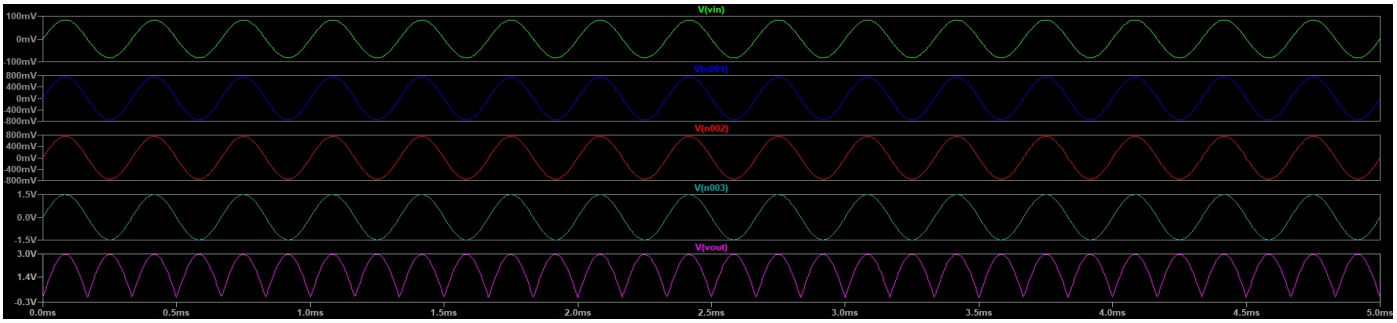
But the input signal looks a bit saturated at the top

4.Verification of the interface

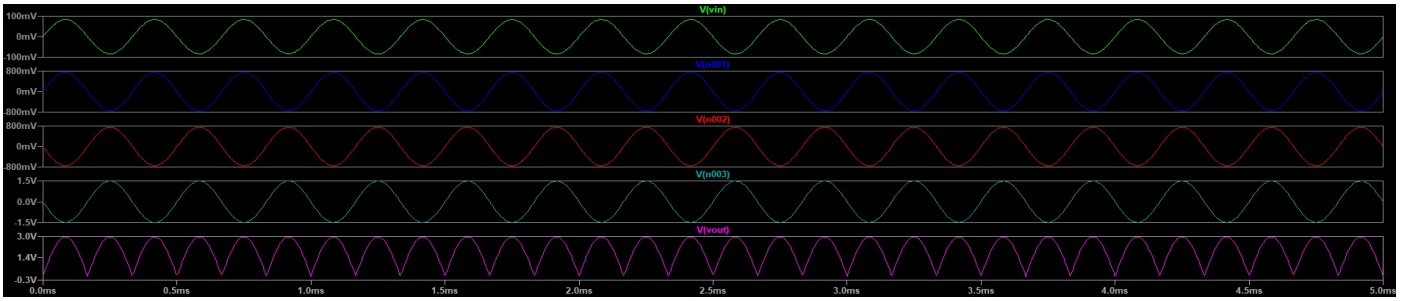
4.1 Block scheme



4.2 Transient simulation



Here it s when the input is negative from the PGA



5.Conclusions

This project was certainly challenging, requiring a great deal of time, effort, and persistence to navigate through the obstacles. However, it reinforced an important principle: if you are determined and take the time to thoroughly search for what you need, a solution is always within reach. Even when the process seemed overwhelming or the answers felt out of reach, careful research and consistent effort made it possible to overcome the difficulties. This experience highlighted the value of patience, resourcefulness, and a willingness to explore all available options to achieve it.