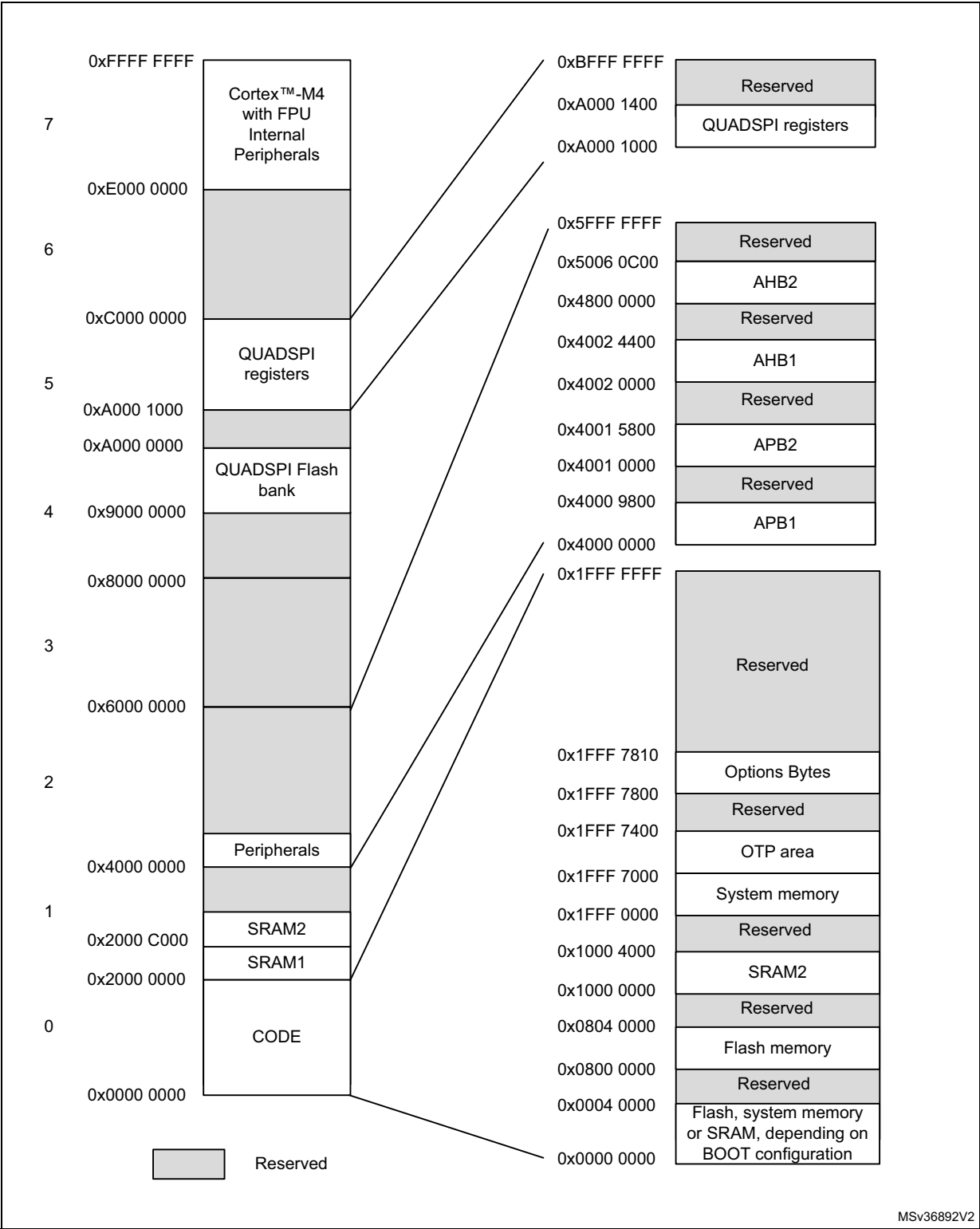


5 Memory mapping

Figure 6. STM32L432xx memory map



MSv36892V2

Table 17. STM32L432xx memory map and peripheral register boundary addresses⁽¹⁾

Bus	Boundary address	Size(bytes)	Peripheral
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5004 0400 - 0x5006 07FF	158 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	Reserved
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 0C00 - 0x4800 1BFF	4 KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
APB2	0x4001 5800 - 0x4001 FFFF	42 KB	Reserved
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4800 - 0x4000 53FF	3 KB	Reserved
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2000 - 0x4001 2BFF	3 KB	Reserved

Table 17. STM32L432xx memory map and peripheral register boundary addresses⁽¹⁾
(continued)

Bus	Boundary address	Size(bytes)	Peripheral
APB2	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800 - 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		Reserved
	0x4001 0000 - 0x4001 002F		SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	USB SRAM
	0x4000 6800 - 0x4000 6BFF	1 KB	USB FS
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00 - 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3400 - 0x4000 3BFF	2 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 1800 - 0x4000 27FF	4 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7

**Table 17. STM32L432xx memory map and peripheral register boundary addresses⁽¹⁾
(continued)**

Bus	Boundary address	Size(bytes)	Peripheral
APB1	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0400- 0x4000 0FFF	3 KB	Reserved
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.