Table 14. STM32L432xx pin definitions (continued)

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32					Alternate functions	Additional functions
13	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
14	PB0	I/O	FT_a	-	TIM1_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
15	PB1	I/O	FT_a	-	TIM1_CH3N, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
16	VSS	S	-	-	-	-
17	VDD	S	-	-	-	-
18	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
19	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
20	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, EVENTOUT	-
21	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, USB_DM, TIM1_BKIN2_COMP1, EVENTOUT	-
22	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, USB_DP, EVENTOUT	-
23	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, USB_NOE, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-

Table 14. STM32L432xx pin definitions (continued)

Pin Number	Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32					Alternate functions	Additional functions
24	PA14 (JTCK-SWCLK)	I/O	FT	(3)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SWPMI1_RX, SAI1_FS_B, EVENTOUT	-
25	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, TSC_G3_IO1, SWPMI1_SUSPEND, EVENTOUT	-
26	PB3 (JTDO-TRACE SWO)	I/O	FT_a	(3)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT	COMP2_INM
27	PB4 (NJTRST)	I/O	FT_fa	(3)	NJTRST, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, TSC_G2_IO1, SAI1_MCLK_B, EVENTOUT	COMP2_INP
28	PB5	I/O	FT	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
29	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP
30	PB7	I/O	FT_fa	-	LPTIM1_IN2, I2C1_SDA, USART1_RX, TSC_G2_IO4, EVENTOUT	COMP2_INM, PVD_IN
31	PH3/ BOOT0	I/O	FT	-	EVENTOUT	BOOT0
32	VSS	S	-	-	-	-
1	VDD	S	-	-	-	-

1. PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC14 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0394 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 15. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	-	-	-	SPI1_MISO	COMP1_OUT	USART3_CTS
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	COMP1_OUT	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

Table 15. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port B	PB0	-	TIM1_CH2N	-	-	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	-	-	-	-	-	USART3_RTS_ DE
	PB3	JTDO-TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	-	-	USART1_RX
Port C	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port H	PH3	-	-	-	-	-	-	-	-

1. Please refer to *Table 16* for AF8 to AF15.

Table 16. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	USB/QUADSPI	-	COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port A	PA0	-	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	-	-	-	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_ BK1_NCS	-	COMP2_OUT	-	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_ BK1_IO3	-	TIM1_BKIN_ COMP2	-	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_ BK1_IO2	-	COMP2_OUT	-	-	EVENTOUT
	PA8	-	-	-	-	SWPMI1_IO	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	USB_CRS_ SYNC	-	-	SAI1_SD_A	-	EVENTOUT
	PA11	-	CAN1_RX	USB_DM	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	USB_DP	-	-	-	-	EVENTOUT
	PA13	-	-	USB_NOE	-	SWPMI1_TX	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	-	-	SWPMI1_RX	SAI1_FS_B	-	EVENTOUT
	PA15	-	TSC_G3_IO1	-	-	SWPMI1_ SUSPEND	-	-	EVENTOUT

Table 16. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	USB/QUADSPI	-	COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_ BK1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS _DE	-	QUADSPI_ BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	-	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PB5	-	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	-	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	-	TSC_G2_IO4	-	-	-	-	-	EVENTOUT
Port C	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT
Port H	PH3	-	-	-	-	-	-	-	EVENTOUT

1. Please refer to *Table 15* for AF0 to AF7.