Arquitecturas Avanzadas de Computadores
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Microarchitecture Simulation Assignment

Introduction

In this assignment you will design and implement a set of experiments in order to show how performance and energy change when different microarchitectural parameters are used. Simulations will be performed with Gem5, an event driven simulator widely used in computer architecture research. Given that a large number of simulations are needed in order to explore the design space, you will be asked to write scripts to automate the process. Finally, a technical report should be written.

Goals

- To understand and quantify the effect of varying the main microarchitectural parameters of a processor.
- To gain experience with developing scripts for automating computer architecture simulations.
- To learn how microarchitecture research is typically performed.

Experiments

1. Perform a few manual simulations to get familiar with the tools and get a sense of how your workload responds to changes in the microarchitecture. For example, you can analyze the instruction-class profiling and determine if the configuration of Functional Units fit your workload. Cache misprediction rate might give you signs about the importance of exploring alternative configurations for it. Change the pipeline's width and analyze how the workload performance changes.
2. Define a design space exploration (DSE). For this, you must select a set of processor's parameters and their value ranges. For example, you could decide that the associativity of the L1 data cache must be explored with the values: 4, 8 and 16. Additionally, you might also consider that the default ROB is too small, and you want to simulate alternative sizes of 192 and 256 entries. You will end up with a list of parameters and the possible values for each parameter. The combination of all selected features and its values make up the DSE. Be reasonable with the number of parameters and values per parameter or you will end up with a DSE so huge that is impossible to explore in a lifetime.

3. Select a strategy to explore the DSE. You can either do a brute force exploration within reasonable ranges of parameter values or explore a wider space with smarter strategies such as Greedy or Evolutionary algorithms. It's ok to use brute force but using other heuristics will be rewarded in the grade.
4. Use *McPAT* to measure the power consumed by various processor configurations. Determine the best performance-energy trade-off using the Energy-Delay Product (EDP) metric.
   - Compute the energy consumed as the power multiplied by the CPI:

$$Energy = (Total\ leakage + Runtime\ Dynamic) * sytem.cpu.cpi$$

   - Compute the EDP as the energy multiplied by the CPI:

$$EDP = Energy * sytem.cpu.cpi$$

Write scripts to automate the simulations described above: for launching the simulations with varying parameters and for collecting and processing results. Use a git repository to develop the scripts.

Deliverables

A written report using the IEEE Conference Proceedings format that includes:

- Profiling results for all applications presented with barcharts.
- A brief description of the parameters modified in the simulations.
- The performance results obtained, presented in graphs (performance vs. resources) and analyzed.
- The energy-performance results obtained, presented in a graph with all simulation points placed on a 2D plot that shows performance vs. energy.
- Report the three processor configurations found to be the best in terms of performance, energy and EDP, respectively.
- A comparison between the simulation speeds obtained with the profiling, microarchitecture and power simulations.
- A link to the repo containing the scripts developed.
- A link to a cloud folder containing all simulation results

Deadline

Upload the report to the course website by the specified date. Be aware that validating the scripts and running the simulations will take several days. After that, you should count on a considerable amount of time for writing the report. Assignments submitted at a later date will have a proportional grade penalization.