# EE-316 Lab 7 CoverSheet

Name : _____
EID : _____
Section : _____
Problem: _____

Attachment Checklist:

- Lab7 CoverSheet
- Detailed Block Diagram (such as FIGURE 18-10)
- State Graph (including Done state, Done signal, Overflow signal)
- A printout of your VHDL code (including two **Process** statements, Asynchronous Reset)
- A printout of your waveform for three test cases ( Do not print Waveform Report )
- A printout of **HDL Synthesis Report** Only ( Do not print more than one page ! )

Signatures of the TA: