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# **EE 316 Lab 5.1 Cover Sheet**

## Name:  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

## EID:     \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

## Section:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

## Design Problem:\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Attachment checklist:

1. Coversheet for Lab 5.1

    2. Preparatory Questions & Answers

    3. State graph and table, K-maps, and equations (by hand)

    4. Printout of state table and verification window (*Print All* command in LogicAid)

    5-1. A state assignment (by hand)

    5-2. Printout of two different state assignments (5-1 and another) in LogicAid

    6. Transition table determined from the SimUaid simulation (by hand)

    7. Output sequences for Z under two different input sequences

    8. Printout of waveforms in landscape mode (scaled to 20ns/div)

    9. Printout of SimUAid circuit (with minimum no. of gates)

     (Before submission, you should save/remember all your Lab 5.1 work for Lab 6.2)

Signatures of the TA: