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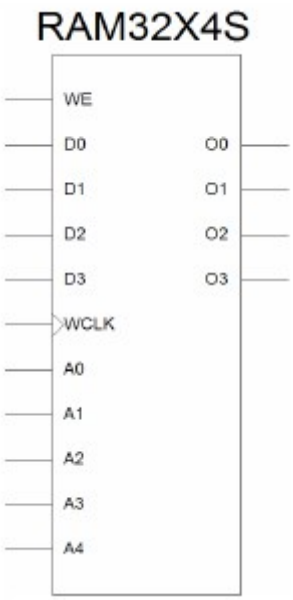
EEE 3342C
Experiment #7
27 July 2015

Objective

This experiment is intended to examine the use of RAM and ROM as a means of realizing combinatorial logic circuits using the Xilinx ISE simulation tool as well as on a BASYS 2 FPGA development board.

Diagrams

The following is a block diagram that shows a block diagram of the RAM that exemplifies what is being used in this experiment:



Equipment

The equipment used for this experiment included a computer with the Xilinx ISE design suite and Digilent ExPort installed as well as a Digilent BAYSYS 2 development board.

Procedure

Part 1

The first step in this experiment should be analyzing and understanding what our expected output should be based on any given set of inputs. This will give us a better understanding of how to build the schematic of the circuit. The below table is a comprehensive view of the logic possibilities in the circuit at any given moment, matched with their respective output. A third table is used to show the combination of the two functions and how they are implemented together.

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F1(w,x,y,z) = (w+x')(y+z')

w	x	y	z	w+x'	y+z'	F1
0	0	0	0	1	1	1
0	0	0	1	1	0	0
0	0	1	0	1	1	1
0	0	1	1	1	1	1
0	1	0	0	0	1	0
0	1	0	1	0	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	1	1
1	0	0	1	1	0	0
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	0	0
1	1	1	0	1	1	1
1	1	1	1	1	1	1

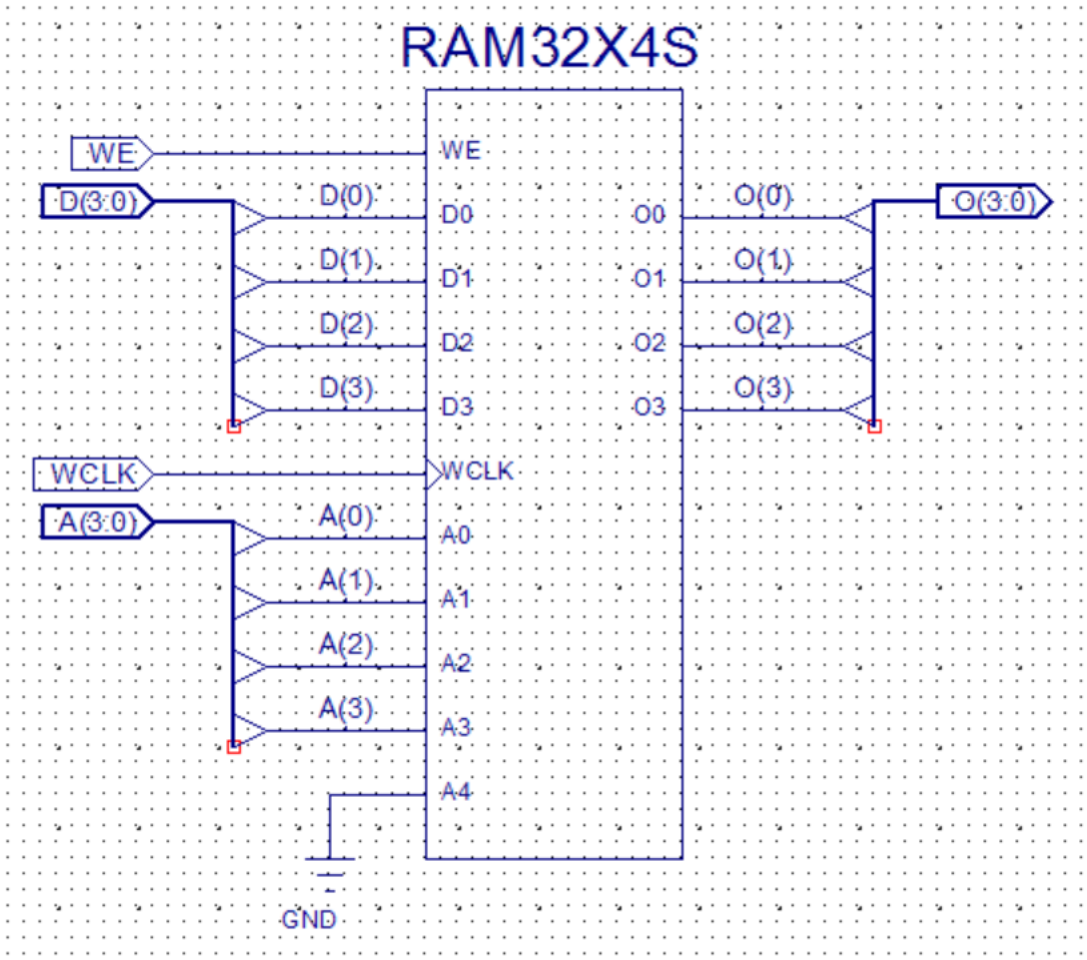
				x1	y1	x0	y0
Cout	S1	S0	F1	w	x	y	z
O3	O2	O1	O0	A3	A2	A1	A0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	1	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	1	1	1	1	1

F2(x1,x0,y1,y0) = 2 bit adder

x1	y1	x0	y0	Cout	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	1	1
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

These logic tables show the data should be at each address and.

Next, the following schematic was created:



After completion of the above schematic capture, the operator created constraints that mapped each input and output to specific pins of the CP132. The constraints were:

```
NET "WCLK" CLOCK_DEDICATED_ROUTE = FALSE;    //clock overide

NET "A[0]" LOC = "P11";     //sw0
NET "A[1]" LOC = "L3";      //sw1
NET "A[2]" LOC = "K3";      //sw2
NET "A[3]" LOC = "B4";      //sw3
NET "D[0]" LOC = "G3";      //sw4
NET "D[1]" LOC = "F3";      //sw5
NET "D[2]" LOC = "E2";      //sw6
NET "D[3]" LOC = "N3";      //sw7

NET "WE" LOC = "G12";       //btn0
NET "WCLK" LOC = "C11";     //btn1

NET "O[0]" LOC = "M5";         //led0
NET "O[1]" LOC = "M11";        //led1
NET "O[2]" LOC = "P7";         //led2
NET "O[3]" LOC = "P6";         //led3
```

Now, the operator was ready to implement the design a final time and create the .bit file used to program the BASYS 2 board. To transfer the file to the BASYS 2 board, Digilent Adept was used. Once in Adept, with the BASYS 2 board powered on, the operator selected the initialize chain button to establish communication between the computer and the BASYS 2 board. Next, the operator used the browse button next to the "FPGA" text to select the newly created *.bit file for programming the BASYS 2 board. Finally, the "program chain" button was used to push the program to the BASYS 2 board and the operator could test the program on the board for proper output.

Expected Results of Circuit

The expected results of this circuit can be seen in the logic table previously created. The ram should be able to store the values given at each address and output those given values when the address is called.

Design Specification Plan

The results of this experiment draw a sound conclusion that the objective has been met by the execution of the procedure. This is given by the fact that the test results match verbatim to that of the expected results based on the calculations performed beforehand. The methodology chosen for this experiment followed a calculation-first route such that the operator would know what to expect. Given that a successful attempt was made to design, simulate, and implement a function using RAM, which was the objective of this experiment, this experiment has met all of its requirements.

Test Plan

This experiment should be tested and verified by the following means. The tester should obtain a BASYS 2 development board with this program loaded on it. Once the tester has set up the board and powered it on, he should test for output based on the provided logic table.

Results

The outcome of this experiment accurately matched that of the calculations performed and presented in the expected results section of this report. This means that RAM was successfully designed and implemented, because when an address stored data, it later output the given data as it should.

Conclusion

In conclusion, this experiment as well as the report was a huge waste of time, similar to the rest. Nevertheless, we can see from it all that RAM has a useful place in logic design for the sake of things such as data and function storage. It would be great in the implementation of memoization such that a previously computed value can be called upon.

Questions

1. RAM provides the ability to change an implemented function without having to change circuitry.

2. Read/write memory is significantly more practical for something such as rapid prototyping or where stored data is not pertinent. However, ROM also has its own place and practicality depending on the needs of a product.

3. The advantage of having separate lines is the lack of complexity for an external device to know when the data it is receiving is valid or not. Shared lines, however,reduce complexity of the RAM and can also decrease package size.

4. See “Design Specification Plan” above. All products function as desired and intended. Therefore, all requirements of this lab have been completed

5. Test plan is above in section called “Test Plan”

6. A reduced component set, a precalculated set of outputs, and an easily reconfigurable system are the advantages of using RAM or ROM to implement combinatorial logic.

7. By using 8x 2-1 multiplexers, the address lines can be selected between the two separate RAM devices such that only one address is able to be selected at a time out of 64. This would be done such that the MSB directs toward the first or second device.