University of Central Florida

Department of Electrical Engineering and Computer Science,

EEE 3342C-0002: Digital Systems (Spring 2015)

Instructor:
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Graduate Teaching Assistants (GTA's)

Huang, Dan	[huangdan226@gmail.com]	Section 1(Grader)
Keshavarz Somayeh	[somayehkeshavarz@knights.ucf.edu]	Section 2(Grader)
Xiaolong Guo	[guoxiaolong@Knights.ucf.edu]	Lab instructor 11&12
Seyed Milad	Tayebi [tayebi@Knights.ucf.edu]	Lab instructor 13&14

Undergraduate Teaching Assistants
To Be Announced…

Meeting Time and Place:

EEE 3342C-0001	Mondays and Wednesday s	9:00am-10:15am	HEC Room 118
EEE 3342C-0002	Tuesdays and Thursdays	12:00pm -01:15pm	HEC Room 118

Labs Room, Meeting Time and TA:

0011 (lab) Monday	@ ENG 257 12:00-2:50pm	Xiaolong Guo
0012 (lab) Tuesday	@ ENG 257 9:00-11:50pm	Xiaolong Guo
0013 (lab) Wednesday	@ ENG 257 12:00-2:50pm	Seyed Milad tayebi
0014 (lab) Thursday	@ ENG 257 9:00-11:50pm	Seyed Milad tayebi

Office Hours:
Monday @ 10:30-12:30pm, Tuesday @ 1:30-3:30pm, Wednesday @ 10:30-12:30pm

Catalog Description:
EEE 3342C Digital Systems: PR: MAC 2311 (Calculus and Analytic Geometry I), MAC 2312 (Calculus and Analytic Geometry II), PHY 2048C (Physics for Engineers & Scientists I), PHY 2049C (Physics for Engineers & Scientists II) all with a C (2.0) or better grade Combinational and sequential logic circuits including registers, arithmetic units, memories, finite state machines, and design with programmable logic devices.

Textbook(s) and Reference(s):
Fundamentals of Logic Design, Sixth Edition by Charles H. Roth and Larry L. Kinney, Cengage Learning

Course Goals:

Upon successful completion of this course, students would

- Understand number systems and perform arithmetic operations on binary, octal and hexadecimal numbers.
- Implement Boolean algebra, Logic gates and K-map techniques.
- Use synthesis and analysis techniques in the design of combinational logic circuits.
- Analyze and design circuits using combinational logic.
- Analyze and design sequential circuits using all types of flip flops.
- Design finite state machines

Course topics:

- Number Systems and Conversion
- Boolean Algebra
- Applications of Boolean Algebra
- Karnaugh-Maps
- Multi-Level Gate Circuits
- Multiplexers, Decoders and Programmable Logic Devices
- Latches and Flip-Flops
- Register and Counters
- Sequential Circuits
- Analysis of Clocked Sequential Circuits
- State Graphs and Tables
- Circuits for Arithmetic Operations

Lab

This course has a lab component. In the lab, you will learn how to describe a logic design circuit in a Hardware Description Language (HDL). HDL is similar to programming but it is specifically for a logic circuit. We use the HDL language called Verilog to build circuits, test them by doing a waveform analysis on inputs and outputs of the circuit, you will then be able to download your circuit to a computer board that we have and test it.

Attendance Policy

- Attendance of all Labs is MANDATORY.
- Attendance of all lectures is expected and encouraged.
- If a student misses a lecture, he/she is responsible for its content.
- Missing three lectures results in a 3% reduction of a student's final grade.
- Missing two labs results in a student's final grade of "F".

Use of WebCourses

- The class uses WebCourses to provide you with the lecture notes and homework assignments.
- If you need to email the instructor or TAs about a grade, please use Webcourses mail. The university requires that we use the secure WebCourses mail to discuss grades.

Grading Policy:

Homework and quizzes	20%
Lab assignments and reports	20%
Exam1	20%
Exam2	20%
Final Exam	20%

Letter grades are based on the weighted average of the above components.

100-93%	A	87-83%	B+	77-73%	B-	67-64%	C	59-55%	D
92-88%	A-	82-78%	B	72-68%	C+	63-60%	C-	Below 54%	F

Some Important Milestones:

- First Lecture: Tuesday, January 13, 2015
- Exam 1: Thursday, February 19, 2015 (class time and location)
- Exam 2: Thursday, March 26, 2015 (class time and location)
- Last Lecture Held: Thursday April 23, 2015
- Final Exam: during university dictated final exam time Thursday, Thursday April 30, 2015, 10:00 AM – 12:50 PM, in the usual classroom.

Please note:

- All homework assignments are due **one week** from the day they are assigned.
- Homework will be assigned, collected, and **selectively graded**.
- Incomplete homework assignments can be submitted for partial credit.
- **No credit** will be given for late assignments.
- **No makeover** exams and/or homework assignments.
- Final Exam is Comprehensive.

Financial Aid New Policy

As of Fall 2014, all faculty members are required to document students' academic activity at the beginning of each course. In order to document that you began this course, please complete the following academic activity by the end of the first week of classes, or as soon as possible after adding the course, but no later than August 27. Failure to do so will result in a delay in the disbursement of your financial aid. See “Course Assignment” which is due by the end of the first week on webcourses.

Honor System Policy:

Consultation with fellow students is encouraged, especially on design issues. However, directly copying another student's work defeats the purpose of the assignments and is an honor code violation. All written assignments should be original work. Portions of written work that are taken word-for-word from other authors (students or researchers) will be assigned a failing grade and may result in a failing grade in the course.