```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/11/2017 05:22:09 PM
// Design Name:
// Module Name: Lab2AdderTop
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Lab2AdderTop(
    input C0,
    input A0,
    input A1,
    input A2,
    input B0,
    input B1,
    input B2,
    output S0,
    output S1,
    output S2,
    output S3
    );

    wire c1, c2;

    FullAdder adder0 (.AIn(A0), .BIn(B0), .CIn(C0), .SOut(S0), .COut(c1));
    FullAdder adder1 (.AIn(A1), .BIn(B1), .CIn(c1), .SOut(S1), .COut(c2));
    FullAdder adder2 (.AIn(A2), .BIn(B2), .CIn(c2), .SOut(S2), .COut(S3));

endmodule
```