```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/10/2017 12:59:22 PM
// Design Name:
// Module Name: FullAdder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module FullAdder(
    input AIn,
    input BIn,
    input CIn,
    output SOut,
    output COut
    );

    assign SOut = (AIn ^ BIn) ^ CIn;
    assign COut = AIn & BIn | CIn & (AIn ^ BIn);

endmodule
```