```
`timescale 1ns / 1ps

module Lab1(
    output L0,
    output L1,
    output L2,
    output L3,
    input BU,
    input BL,
    input BR,
    input S0,
    input S1,
    input S2
    );
    assign L0 = ~BU;
    assign L1 = BL & BR;
    assign L2 = S0 | S1;
    assign L3 = S0 ^ S1 ^ S2;
endmodule
```