```
`timescale 1ns / 1ps
//Justin Fortner
//ID#1481947
//jfortner
//Lab Sec 1C TU/TH 1:30-3:20
//10/12/17
//CE100


module Lab2Top(
    input sw0,
    input sw1,
    input sw2,
    input sw3,
    input sw4,
    input sw5,
    input sw6,
    output CA,
    output CB,
    output CC,
    output CD,
    output CE,
    output CF,
    output CG,
    output dp,
    output AN0,
    output AN1,
    output AN2,
    output AN3
    );

    wire n0, n1, n2, n3;

    Lab2AdderTop bigAdder (.C0(sw0), .A0(sw1), .A1(sw2), .A2(sw3), .B0(sw4),
.B1(sw5), .B2(sw6), .S0(n3), .S1(n2), .S2(n1), .S3(n0));
    SegConvert display (.N3(n3), .N2(n2), .N1(n1), .N0(n0), .A(CA), .B(CB), .C(CC),
.D(CD), .E(CE), .F(CF), .G(CG));

    assign dp = 1;
    assign AN0 = 0;
    assign AN1 = 1;
    assign AN2 = 1;
    assign AN3 = 1;

endmodule
```