Justin Kang

LinkedIn : linkedin.com/in/justin-kang-uoft
Email : js.kang@mail.utoronto.ca

Research Interests

I am a graduate student at The University of Toronto in the Edward S. Rogers Sr. Department of Electrical and Computer Engineering. Currently, I am conducting research in the field of Communication and Information Theory with applications to the Internet of Things, and the future of wireless technology. I will be completing my Master's degree 1 year ahead of schedule in August 2020.

Education

- **University of Toronto** — Toronto, ON
  Masters of Applied Science in Electrical and Computer Engineering; 4.0 — *Sept. 2019 – August 2020*
- **University of British Columbia** — Vancouver, BC
  Bachelors of Applied Science in Engineering Physics; 91.1% — *Sept. 2014 – May 2019*

Relevant Courses: (UBC) ELEC 402 *VLSI* A+, ELEC 431/432 *Communication Systems I and II* A+, PHYS 401 *Electromagnetic Theory* A+ (U of T) ECE 1501 *Error Control Codes* A+, ECE 1502 *Information Theory* A, ECE 1521 *Detection and Estimation Theory* A+, ECE 1504 *Statistical Learning* A+, ECE 1505 *Convex Optimization* A.

Programming Skills

- **Hardware**: SystemVerilog, Verilog, UVM, VHDL, SPCIE, Cadence (Layout and Schematic Tools), Synopsys VCS, ModelSim, Quartus
- **Software**: Python, MATLAB, C++, WireShark

Research Experience

- **University of Toronto** — Toronto, ON
  Research Assistant — *Sept. 2019 - Present*
  - **Wireless Systems**: Studying the fundamental limits of cooperative communications in massive access networks. These are networks with potentially millions of distributed nodes which must all be served simultaneously. Building the framework today for these networks of the future is crucial for the deployment of the next generation of technology, which will require exponentially more high throughput and low latency connections.
- **Intel Non-Volatile Memory Solutions Group** — Santa Clara, CA
  Research Assistant for Dr. Ravi H. Motwani's team — *May 2018 - August 2018*
  - **NAND ECC Decoders**: Novel augmentations to belief propagation algorithms for high-throughput, low code-rate LDPC decoders, enabling next generation of NAND memories at higher bit error rates.
  - **Low Complexity PON Decoders**: Research and prototyping of architectures for low cost and low power ONU devices. Proposed multiple parallel message passing algorithms with differing levels of message complexity to optimize decoder for logic area and throughput.
  - **Optane Failure Considerations**: Developing novel decoding algorithms to take advantage of knowledge of expected failure mechanisms derived from experimental analysis of Intel Optane memory.

Research Projects

- **Quantum Simulations for Phase Change Memories** Vancouver, BC
  Guided by Dr. Alireza Nojeh *January 2018 - May 2018*
  - **Geometric Optimization**: Structural relaxations simulations for the determination of optimal lattice parameters and ionic positions. Density Functional Theory self consistent field calculations using core electron pseudo-potentials. Different phases for each candidate material were investigated and found to have stable configurations.
  - **Band Structure Calculations**: Kohn-Sham band structures were calculated with all electron simulations, accounting for spin-orbital coupling. Band structures were analyzed to determine electronic properties of each phase. Based on electronic properties of the phase, the material's potential for use in phase change memories were evaluated.
- **Fitness Tracking with Machine Vision** Vancouver, BC
  Guided by Faculty at the Department of Physics at UBC *January 2018 - Present*
  - **Exercise Classification Neural Net**: A recurrent neural net was trained on over 30 hours of data with 11 different exercises, which was collected over several months. The resulting trained neural net was able to accurately predict which exercise was being performed with 97% accuracy.
  - **Repetition Counting**: Exercise repetition counting using principal component analysis on skeletal vectors for dimensional reduction. Filtering and spectrograms are used to isolate where an exercises is taking place, and peak counting algorithms are used to determine how many repetitions were performed.
  - **Awards**: In April 2018, this project was awarded both the *Bycast Award for Entrepreneurship* and the *UBC Design and Innovation Day Industry Award* for our accomplishments.

See https://justinkang221.github.io/ for papers containing the technical details of these and other projects

Industry Experience

- **Intel Non-Volatile Memory Solutions Group** Vancouver, BC
  Error Correction Engineering Intern *May 2017 - Dec 2017*
  - **Decoder Hardware Architecture**: Design and Optimization of BCH decoders. Timing analysis. Improving parallelism, making use of algebraic identities to reduce area and power, while improving throughput.
  - **ASIC Verification**: Verification of multiple IP blocks using the Universal Verification Methodology. Test bench design for hierarchical reuse.
- **Broadcom of Canada Limited** Vancouver, BC
  Software Verification Intern *Jan 2016 - April 2016*
  - **Software Verification**: Developed remotely executable scripts to run on build and testing severs in python and bash.
  - **Networking**: Managed all aspects of lab environment, including IP routing tables, SIP servers, gateway hardware, sever switches, and OLT for PON systems. Extensively used Wireshark to troubleshoot and identify bugs in packet delivery and routing.

Publications

- **Minimum Feedback for Collision-Free Random Access**
  2020 IEEE International Symposium on Information Theory (ISIT)
  - : Using mathematical tools, proving bounds for the fundamental requirements for a feedback-based random access architecture.

Patents

- **Intrinsic Information Bit-Flipping Decoder**
  Title: Techniques To Use Intrinsic Information For a Bit-Flipping Error Correction Control Decoder
  - **US 16/370178**: This patent describes a method of using intrinsic information additively in the decision process of a message-passing low complexity bit flipping decoder. The methods described present a significant advantage over traditional methods. It is particularly effective in hardware, as it only involves the addition of summation blocks to the standard algorithm. This technique is capable of producing results superior to a probabilistic intrinsic bit flipping decoder, but has a much lower hardware footprint.

Awards

Canadian Graduate Scholarship National Science and Engineering Research Council	2020
Graduate Fellowship Awarded by the University of Toronto	2019
Eric Roenitz Memorial Prize Greatest effort in Capstone Project	2019
Trek Excellence Scholarship Top 5% in each faculty (4 Awards)	2015-2019
Donald J. Evans Scholarship in Engineering Academic achievement (2 Awards)	2017-2018
Bycast Award For Entrepreneurship Project excellence	2017
UBC Design and Innovation Industry Award Project excellence	2017
Jimmar Memorial Scholarship Academic achievement	2016
Hector John MacLeod Scholarship Academic achievement	2015
Charles and Jane Banks Scholarship Academic achievement	2015
Charles Victor Ryder Scholarship Academic achievement	2015
Ron Bick Lee Memorial Scholarship Academic achievement	2015
Bronze Governor General's Award Academic achievement	2014
Chancellor Scholar Award Academic achievement	2014
BC Provincial Scholarship Top 20 exam scores out of 60,000 students	2014