Verilog lab

HDLBits

- https://hdlbits.01xz.net/wiki/Problem_sets

Wire & vector

1. Four wires
2. Vectors
3. Vectors in more detail
4. Vector part select

Logic gate

1. Inverter
2. AND gate
3. Declaring wires

Combinational logic

1. Simple circuit A
2. Thermostat

Module

1. Adder 1
2. Adder-subtractor

Sequential logic

1. Always blocks (clocked)
2. Four-bit binary counter

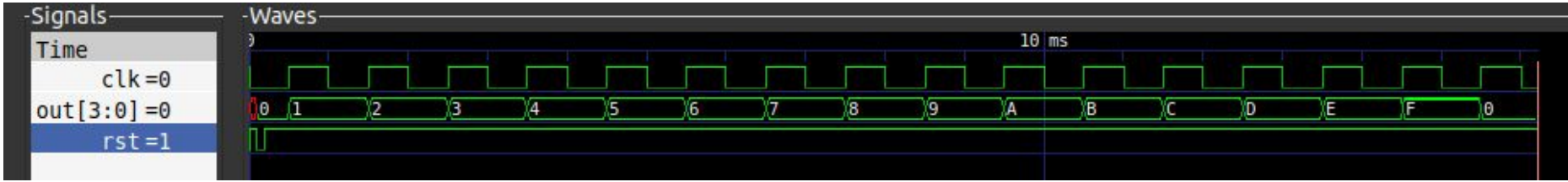
Testbench

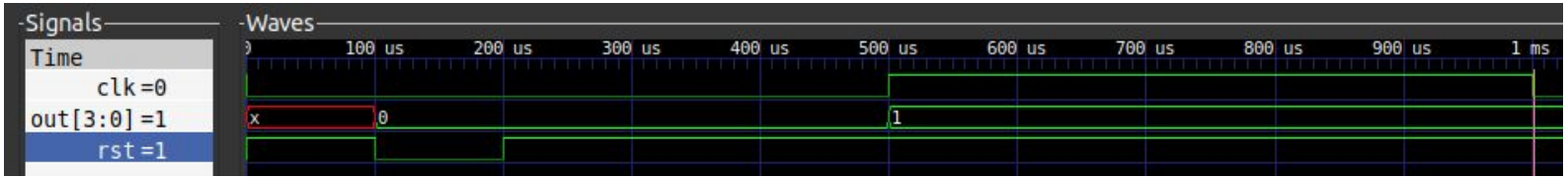
1. Clock
2. Testbench1

Accumulator

input: reset, clock

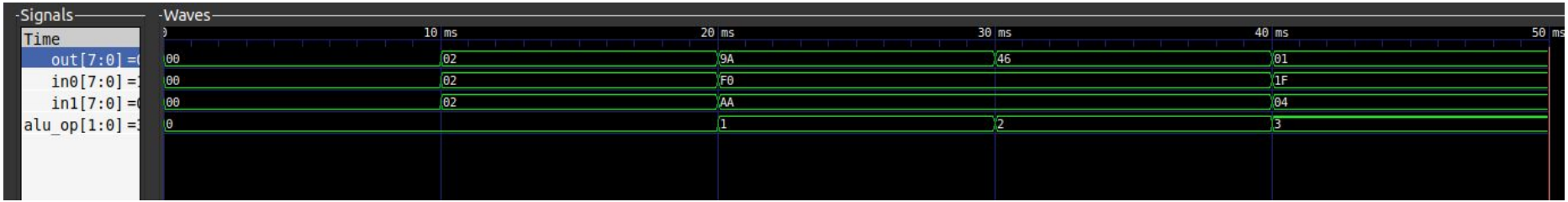
output: value of the accumulator





Baby ALU

- A simple 8 bit ALU
- Instruction
  - AND (ALUop 2'b00)
  - ADD (ALUop 2'b00)
  - SUB (ALUop 2'b00)
  - SRAI (ALUop 2'b00)



Baby ALU

- A simple 8 bit ALU
- Instruction
  - AND (ALUop 2’b00)
  - ADD (ALUop 2’b00)
  - SUB (ALUop 2’b00)
  - SRAI (ALUop 2’b00)