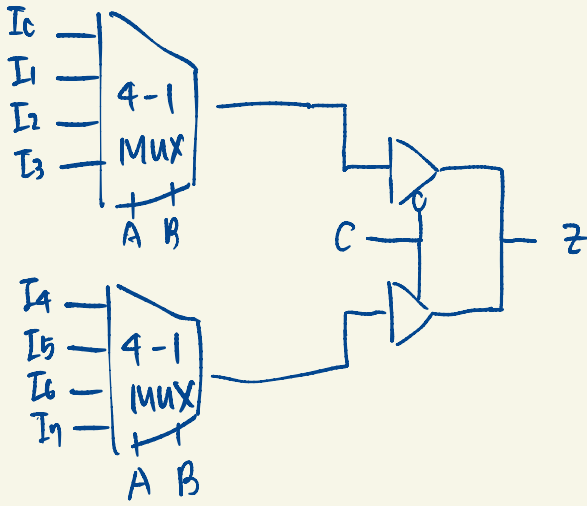
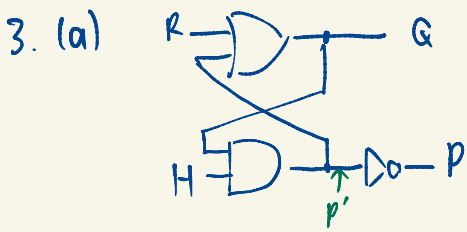


1.



2.

$A$	$B$	$Q$	$Q^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



$\therefore$  output of OR gate  $Q = R + p'$

$$\Rightarrow \underline{Q} = R + p' \stackrel{\substack{\uparrow \\ \therefore p = Q'}}{=} R + (Q)' = \underline{R + Q}$$

$$\Rightarrow R = 0 \dots \textcircled{1}$$

$\therefore$  output of AND gate  $p' = Q \cdot H$

$$\therefore Q = R + p' \Rightarrow p' = (R + p')H$$

$$\Rightarrow Q = (R + Q)H = \overset{0}{R}H + QH = QH$$

$$\therefore Q = QH \Rightarrow H = 1 \dots \textcircled{2}$$

$$\therefore \textcircled{1} \text{ \& } \textcircled{2} \Rightarrow R = 0, H = 1$$

(b).

R	H	Q	$Q^+$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	1
1	1	1	1

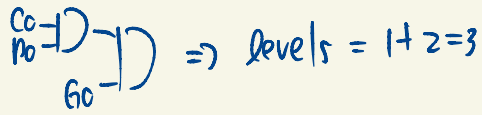
when  $R=1$  &  $H=0$ :  $\begin{cases} Q=1 \\ p'=0 \Rightarrow p=1 \end{cases}$   
 $\therefore p = Q' \Rightarrow$  not allowed.

Q \ RH	00	01	11	10
0	0	0	1	not allowed
1	0	1	1	not allowed

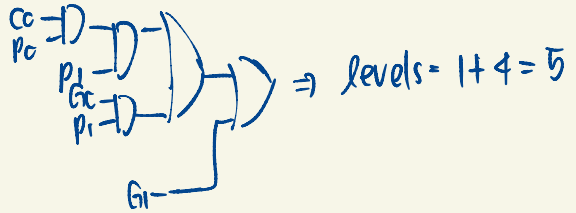
$$\Rightarrow Q^+ = RH + QH$$

7.

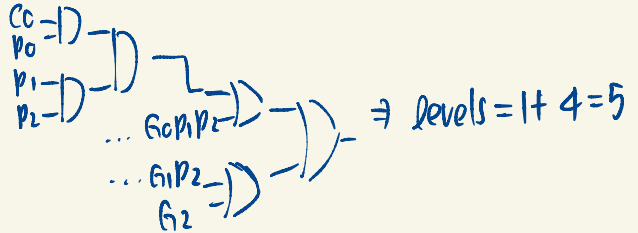
1 bit:  $\begin{matrix} A \\ B \end{matrix} \rightarrow \text{AND} - G +$   
 $\begin{matrix} A \\ B \end{matrix} \rightarrow \text{AND} - P$



2 bit:  $-11-+$





3 bit:  $-11-+$



$\Rightarrow \# \text{ of levels } F(n) = \underset{\substack{\uparrow \\ \text{for prod}}}{1} + \underset{\substack{\uparrow \\ \text{and xor gate}}}{2} \cdot (\lceil \log_2(n+1) \rceil)$

File Edit Search Time Markers View Help

 From: 0 sec To: 3276800 ns  Marker: 3100300 ps | Cursor: 2870600 ps

SST

- lab1\_main
  - adder
    - testcla
      - c\_op\_0p\_1
      - c\_op\_0p\_1p\_2
        - c\_1
        - c\_2
        - c\_3
        - fa\_0
        - fa\_1
        - fa\_2
        - g\_0
        - g\_0p\_1
        - g\_0p\_1p\_2
          - g\_1
          - g\_1p\_2
          - g\_2
          - p\_0

Signals

Time

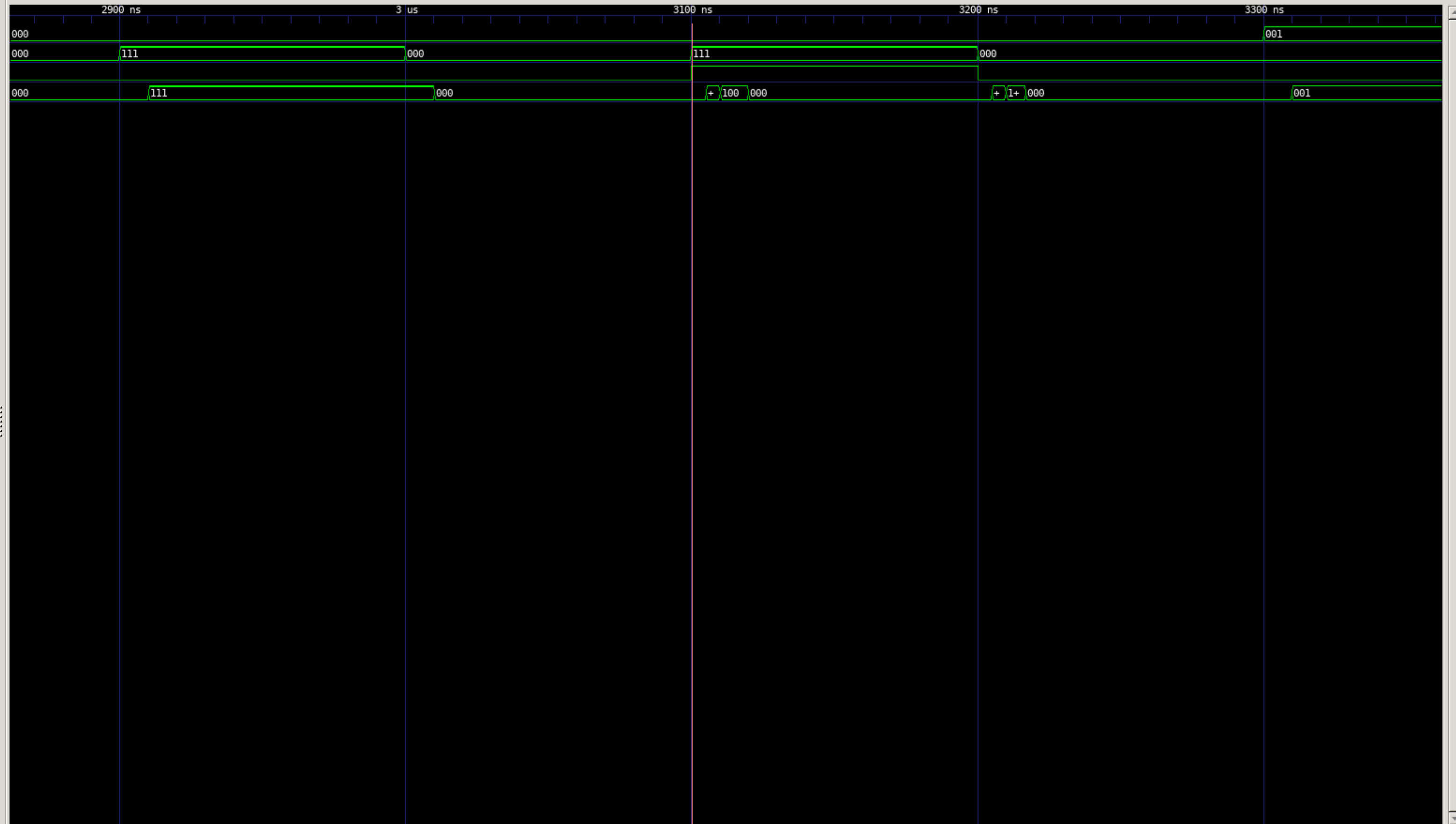
A[2:0] = 000

B[2:0] = 111

C0 = 1

S[2:0] = 000

Waves



Type Signals

wire A[2:0]

wire B[2:0]

wire C0

wire C1

wire C2

wire C3

wire S[2:0]

wire c0p0p1

wire c0p0p1p2

wire g0p1

wire g0p1p2

wire g1p2

wire g[2:0]

wire p[2:0]

wire pc0

wire temp0

wire temp1

wire temp2

Filter:

4.

(1).

```
module cla_g1(
    output C3,          // carry output
    output[2:0] S,      // sum
    input[2:0] A, B,    // operands
    input C0            // carry input
);

    // TODO:: Implement gate-level CLA
    wire [2:0] p, g;
    //0: first bit
    AND g_0(g[0], A[0], B[0]);
    OR p_0(p[0], A[0], B[0]);
    AND pc_0(pc0, p[0], C0);
    OR c_1(C1, g[0], pc0);
    FA fa_0(temp0, S[0], A[0], B[0], C0);

    //1: second bit
    AND g_1(g[1], A[1], B[1]);
    OR p_1(p[1], A[1], B[1]);
    AND4 c_0p_0p_1(c0p0p1, C0, p[0], p[1], 1'b1);
    AND g_0p_1(g0p1, g[0], p[1]);
    OR4 c_2(C2, g[1], g0p1, c0p0p1, 1'b0);
    FA fa_1(temp1, S[1], A[1], B[1], C1);

    //2: third bit
    AND g_2(g[2], A[2], B[2]);
    OR p_2(p[2], A[2], B[2]);
    AND4 c_0p_0p_1p_2(c0p0p1p2, C0, p[0], p[1], p[2]);
    AND4 g_0p_1p_2(g0p1p2, g[0], p[1], p[2], 1'b1);
    AND g_1p_2(g1p2, g[1], p[2]);
    OR4 c_3(C3, g[2], g1p2, g0p1p2, c0p0p1p2);
    FA fa_2(temp2, S[2], A[2], B[2], C2);

endmodule
```

(2).

```
module rca_gl(  
    output C3,          // carry output  
    output[2:0] S,      // sum  
    input[2:0] A, B,    // operands  
    input C0            // carry input  
);  
  
    // TODO:: Implement gate-level RCA  
    FA fa_0(C1, S[0], A[0], B[0], C0);  
    FA fa_1(C2, S[1], A[1], B[1], C1);  
    FA fa_2(C3, S[2], A[2], B[2], C2);  
endmodule
```

6. (a) Maximum propagation delay for rca\_gl (ripple carry adder)

```
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$ iverilog -o lab1_compiled.vvp lab1.v  
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$ vvp lab1_compiled.vvp  
VCD info: dumpfile lab1.vcd opened for output.  
The maximum delay is 23 ticks on transition 000+000+0 --> 000+111+1  
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$
```

(b) Maximum propagation delay for cla\_gl (carry lookahead adder)

```
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$ iverilog -o lab1_compiled.vvp lab1.v  
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$ vvp lab1_compiled.vvp  
VCD info: dumpfile lab1.vcd opened for output.  
The maximum delay is 20 ticks on transition 000+000+0 --> 000+011+1  
justin@DESKTOP-DSHM2G6:/mnt/c/Users/justi/OneDrive/Desktop/LAB-01$ _
```