

PCL-069  
phyCORE-i.MX 8M Mini

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Project: PCL-069		Department : F&E Author: T. Metz	
13.03.2020	PCB-No.: 1518.2	Revision : 001	Sheet 1 of 16

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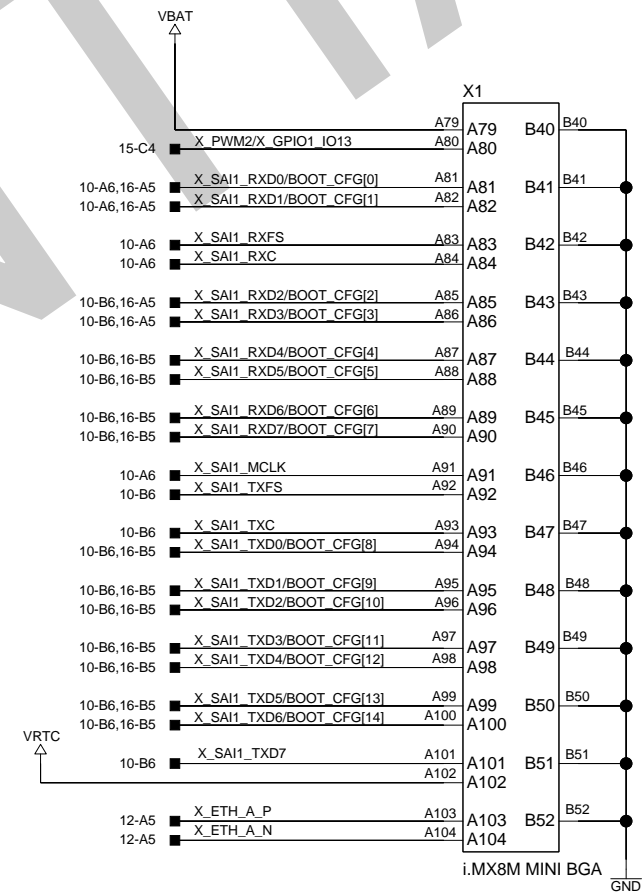
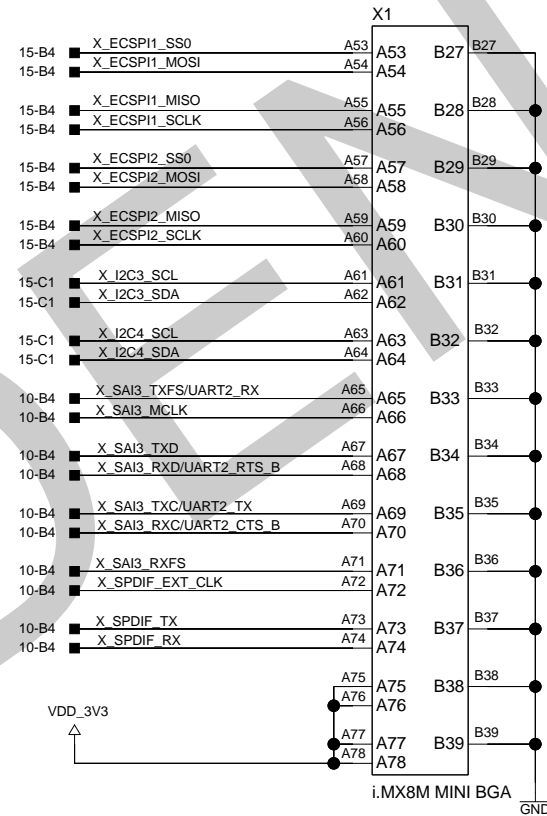
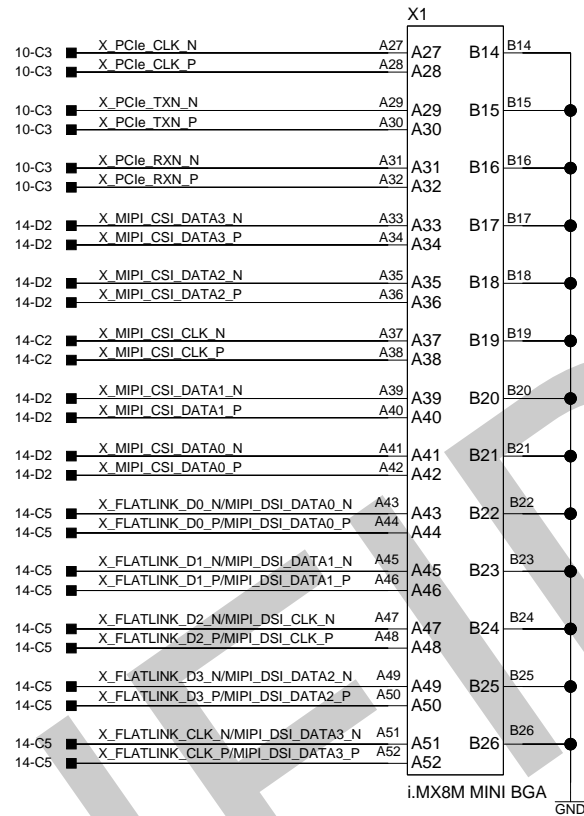
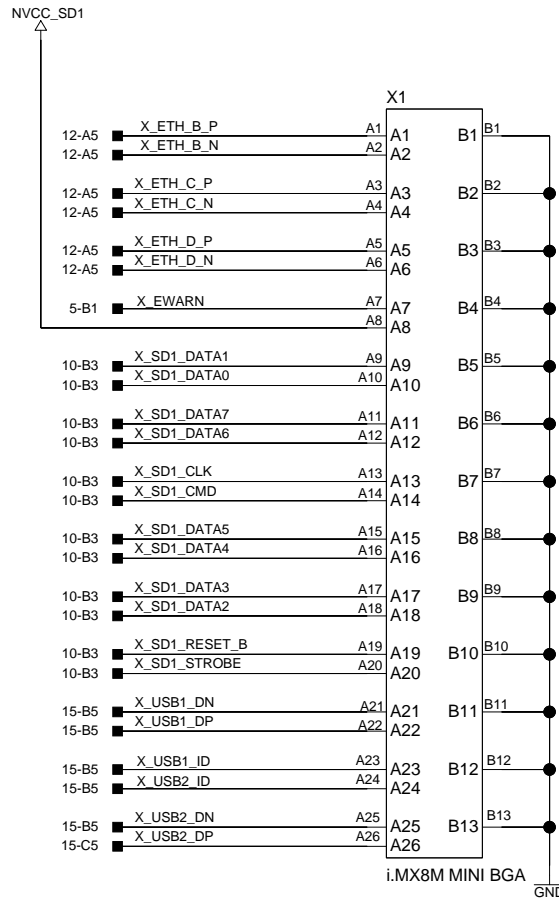
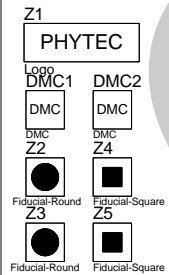
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		Author :	T. Metz
13.03.2020	PCB-No.: 1518.2	Revision :	001
		Sheet	2 of 16

1

2

3

4

5

6

A

A

B

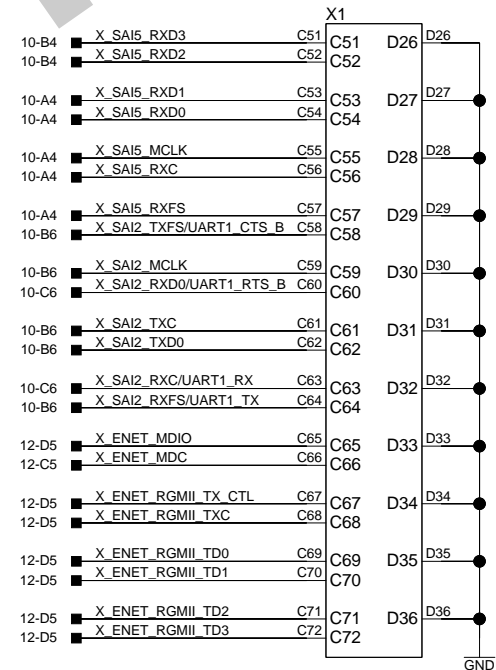
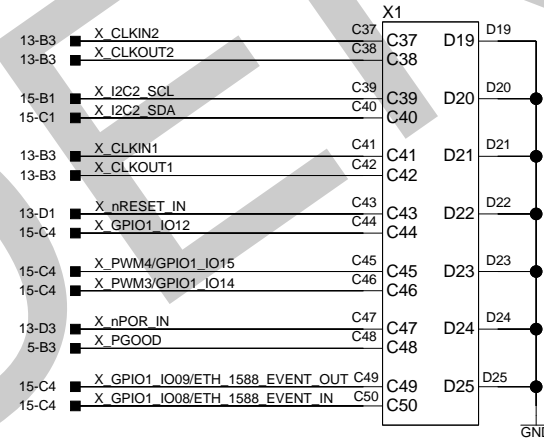
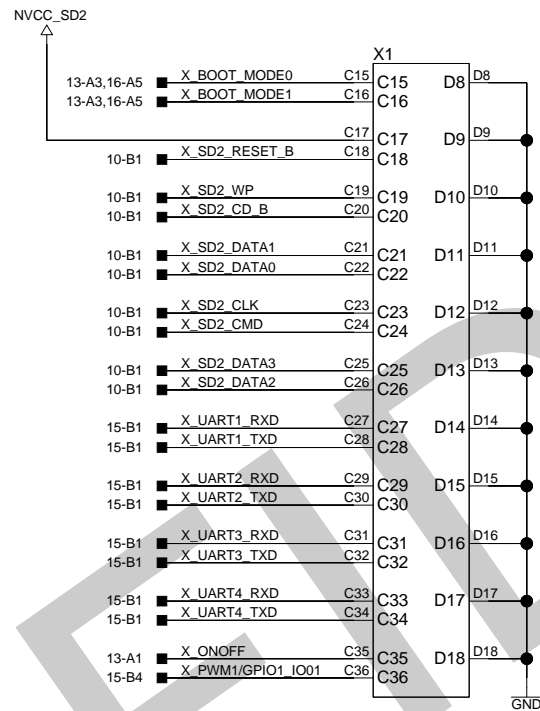
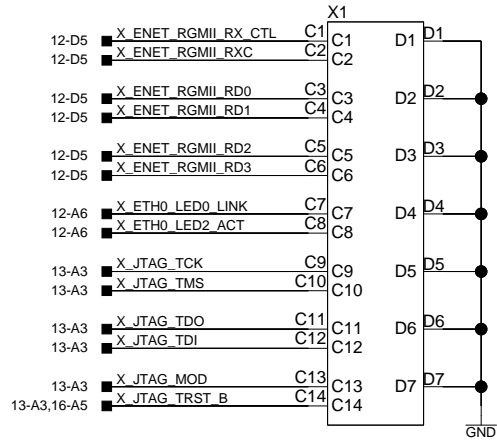
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13.03.2020

PCB-No.: 1518.2

Revision : 001

Sheet 3 of 16

A

B

C

D

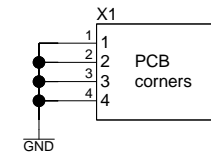
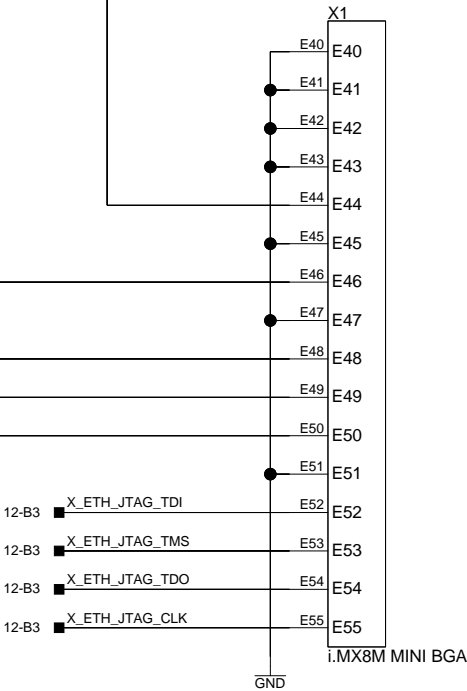
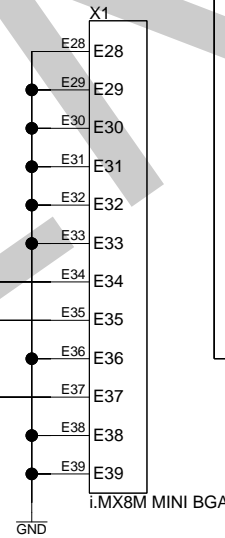
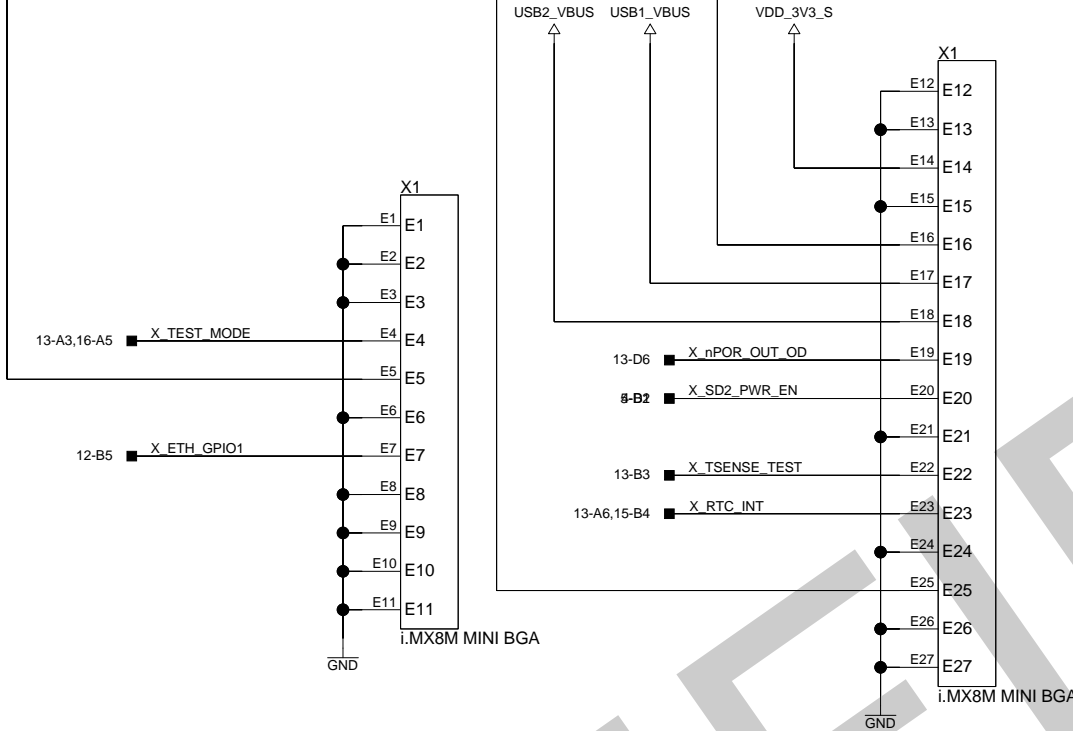
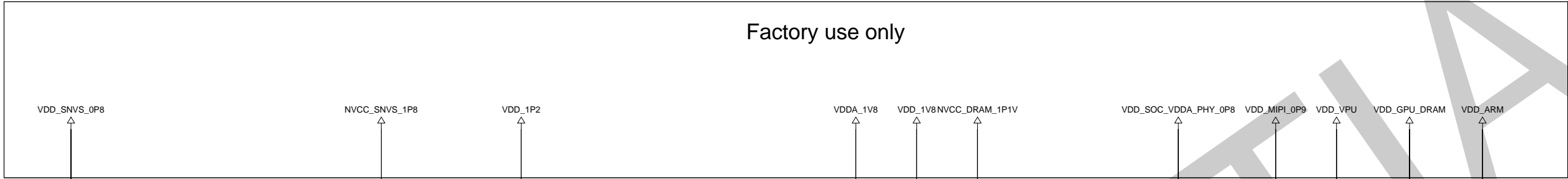
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Factory use only



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Author: T. Metz

13.03.2020

PCB-No.: 1518.2

Revision : 001

Sheet 4 of 16

A

B

C

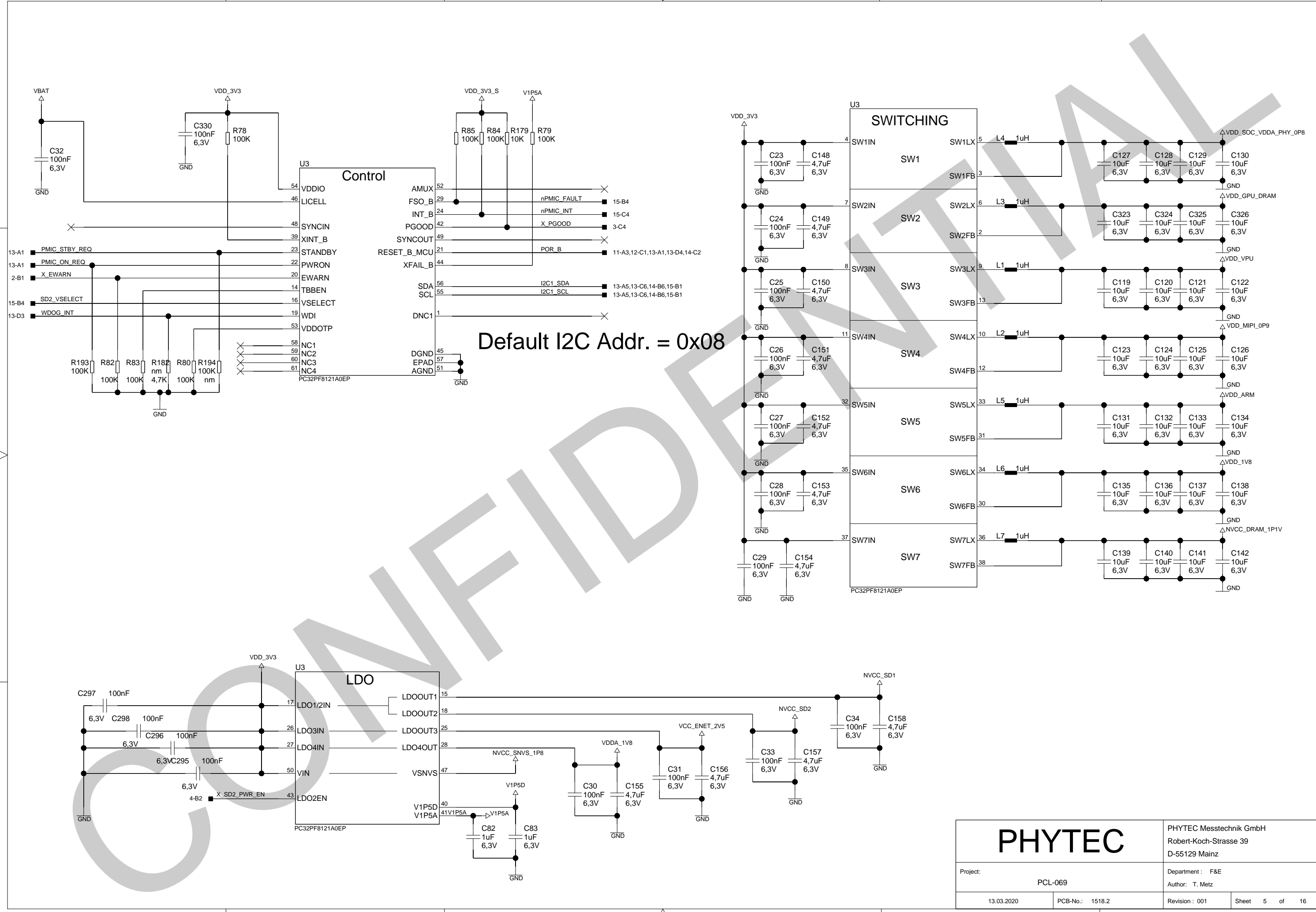
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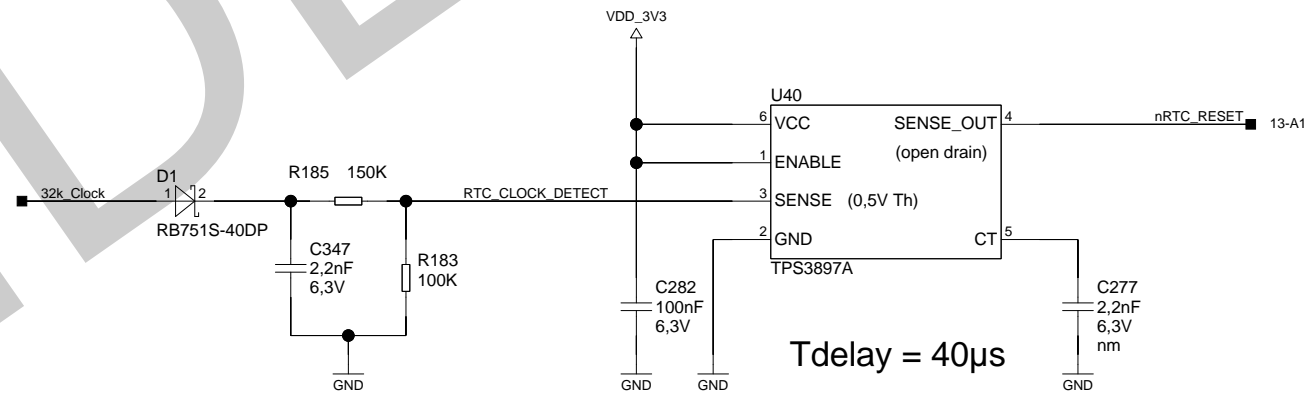
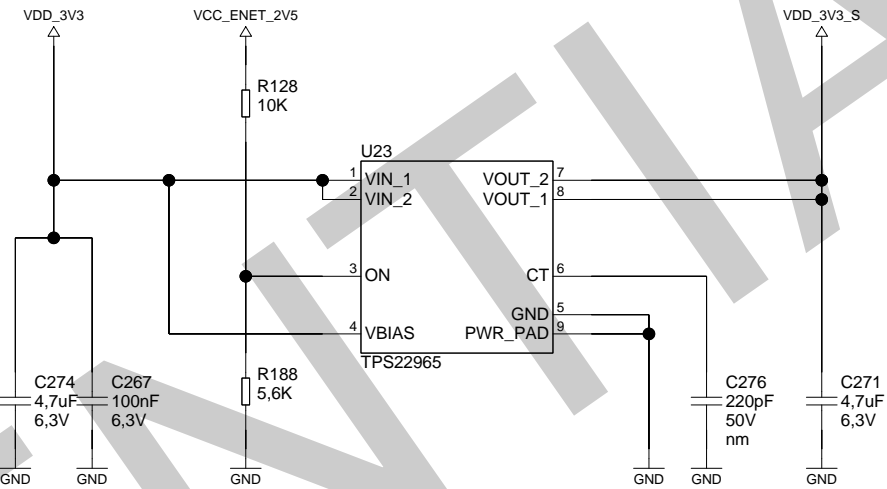
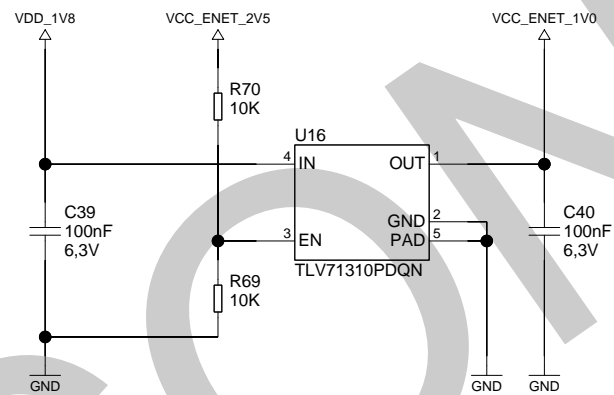
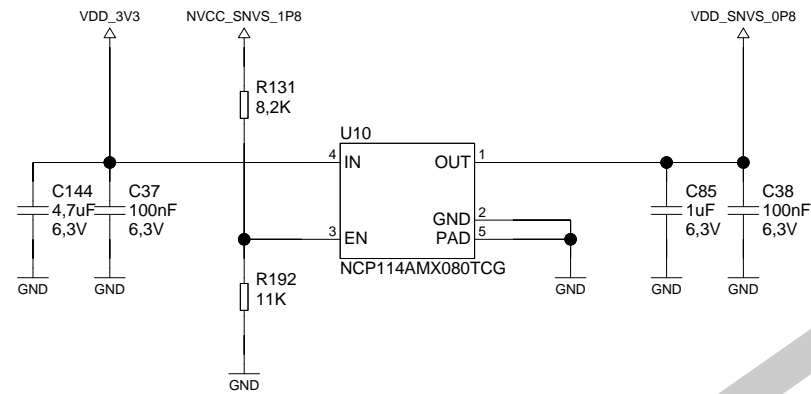
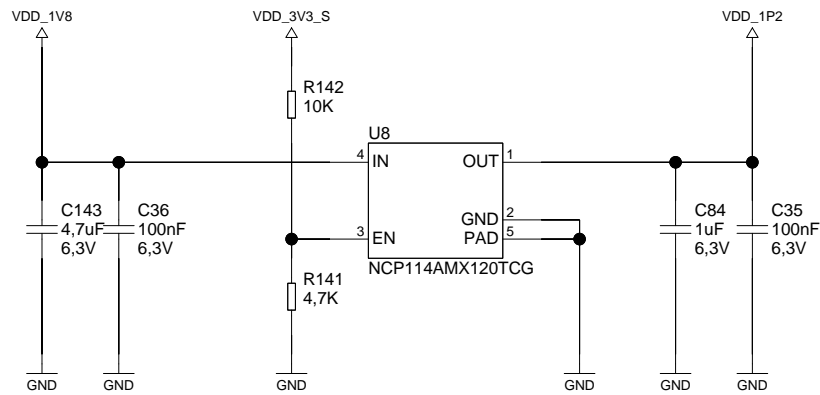
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Project:		Department : F&E	
PCL-069		Author : T. Metz	
13.03.2020	PCB-No.: 1518.2	Revision : 001	Sheet 5 of 16





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2

3

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A

B

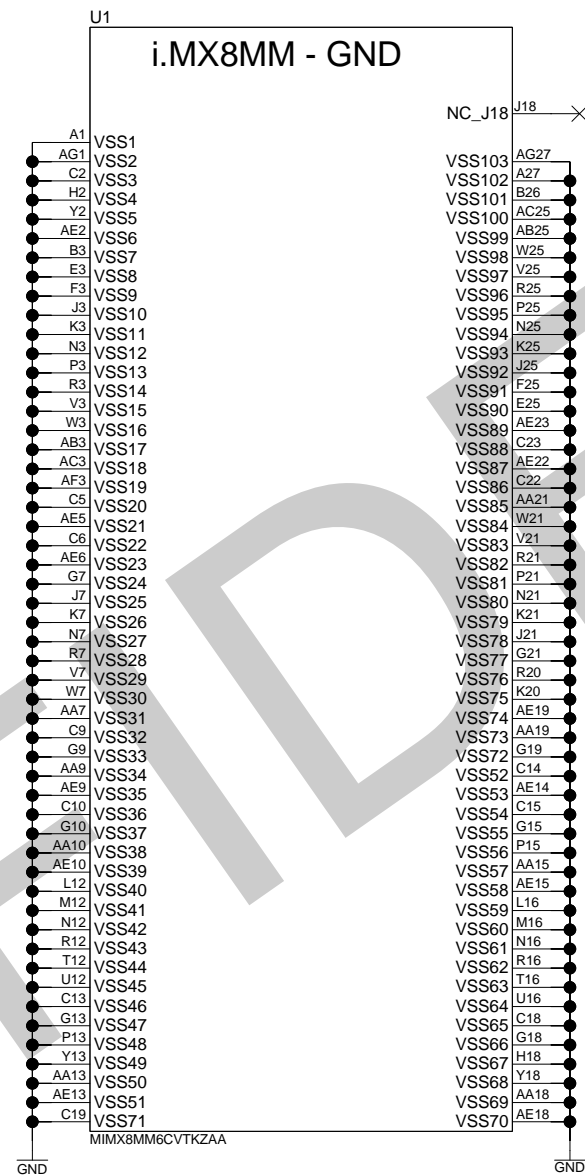
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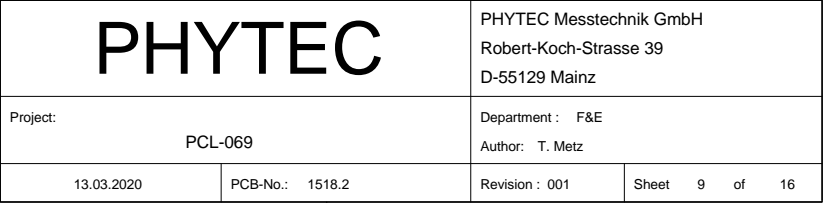
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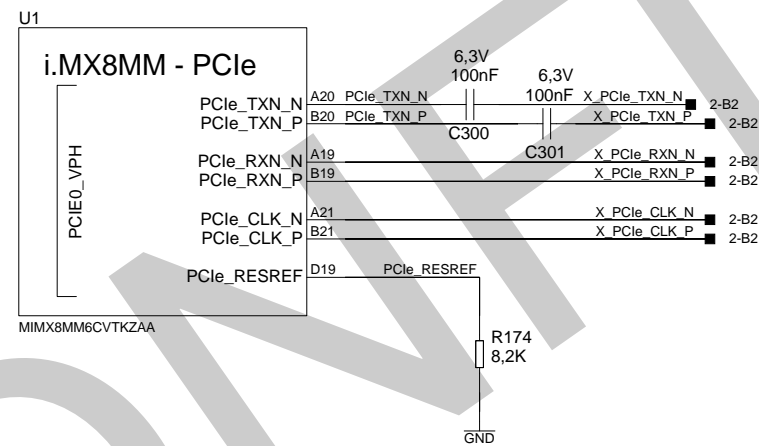
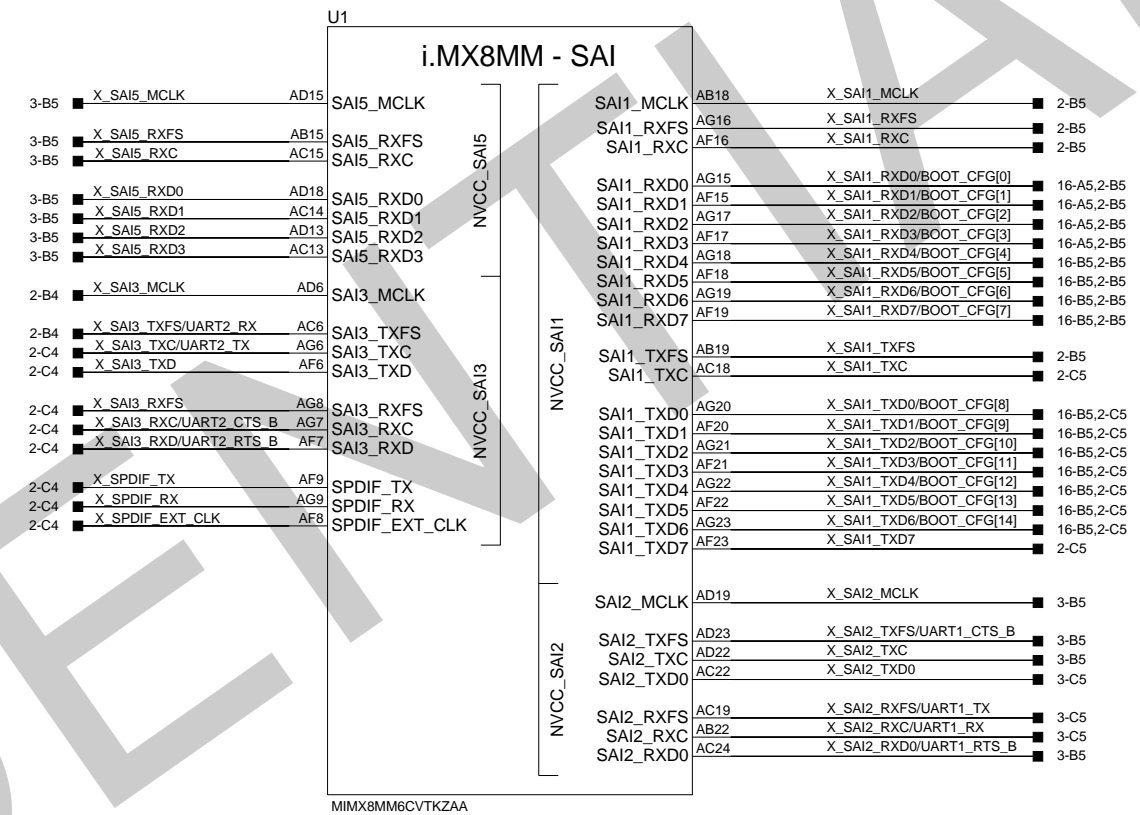
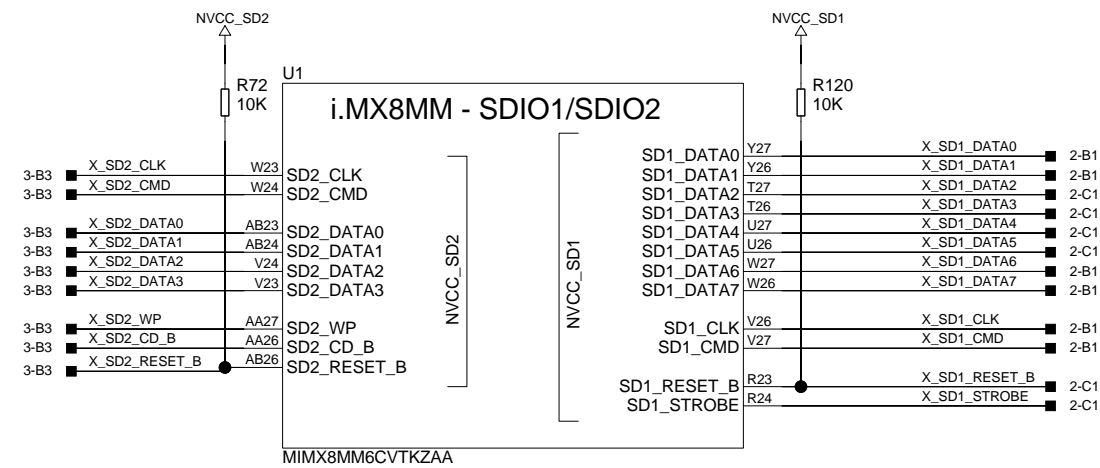
PCB-No.: 1518.2

Revision : 001

Sheet 8 of 16







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4

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A

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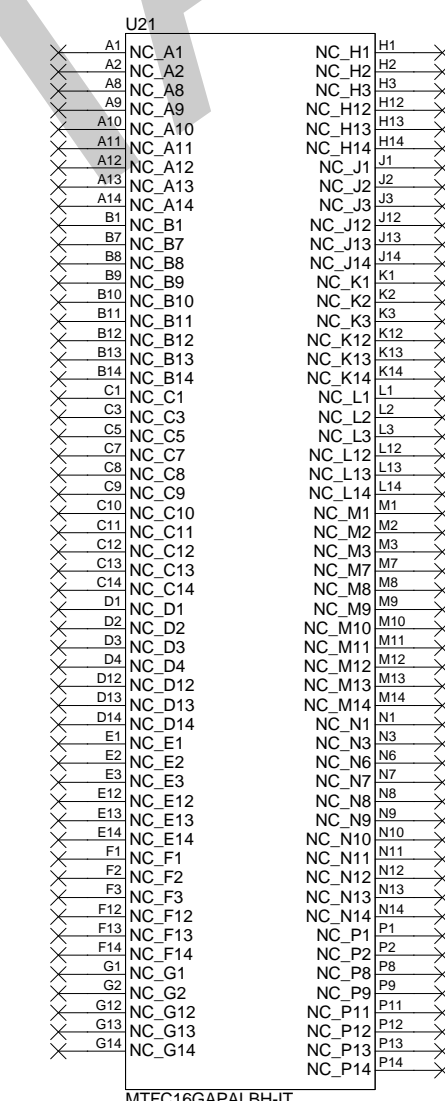
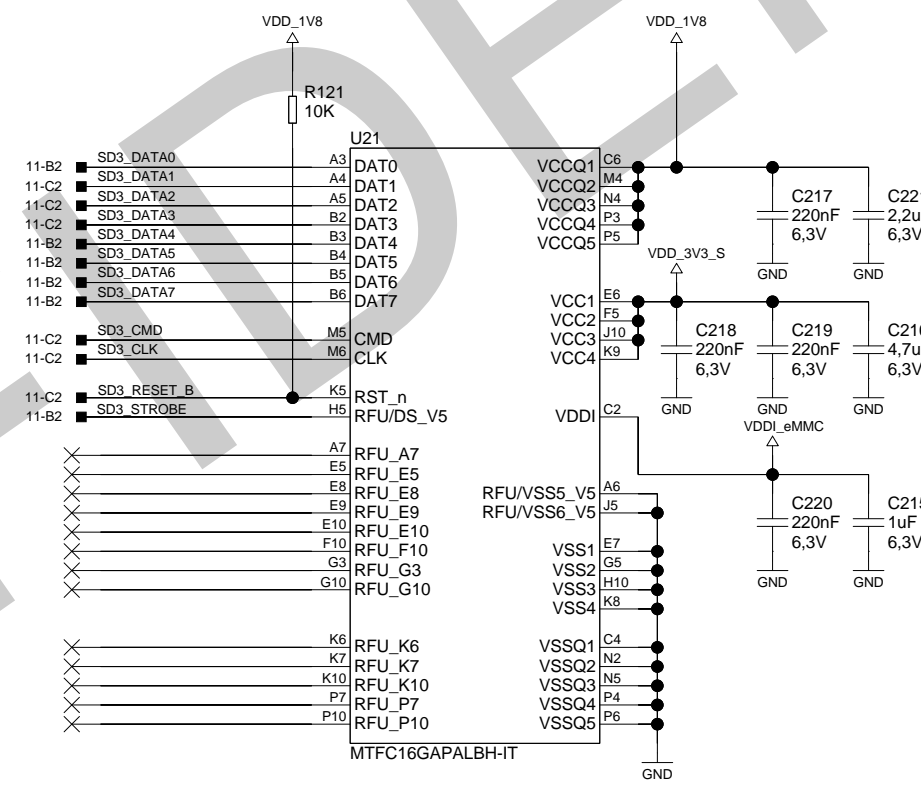
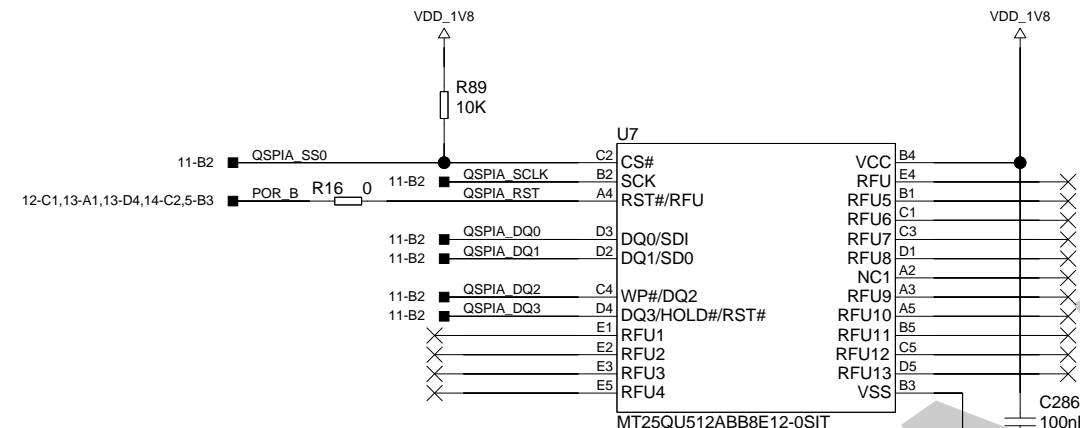
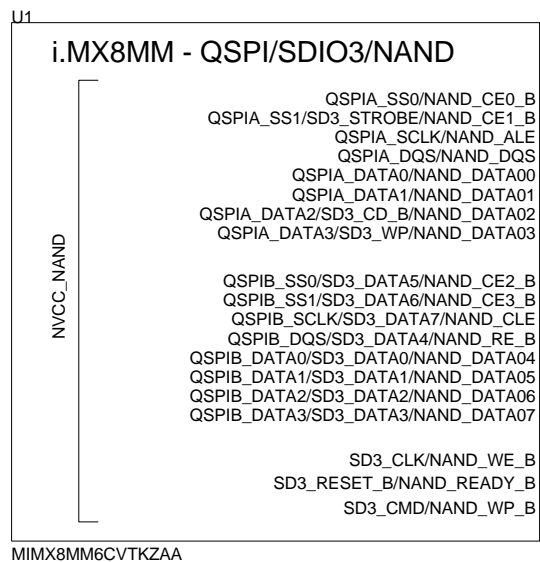
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Project:	PCL-069	Department : F&E	Author: T. Metz
13.03.2020	PCB-No.: 1518.2	Revision : 001	Sheet 11 of 16

A

B

C

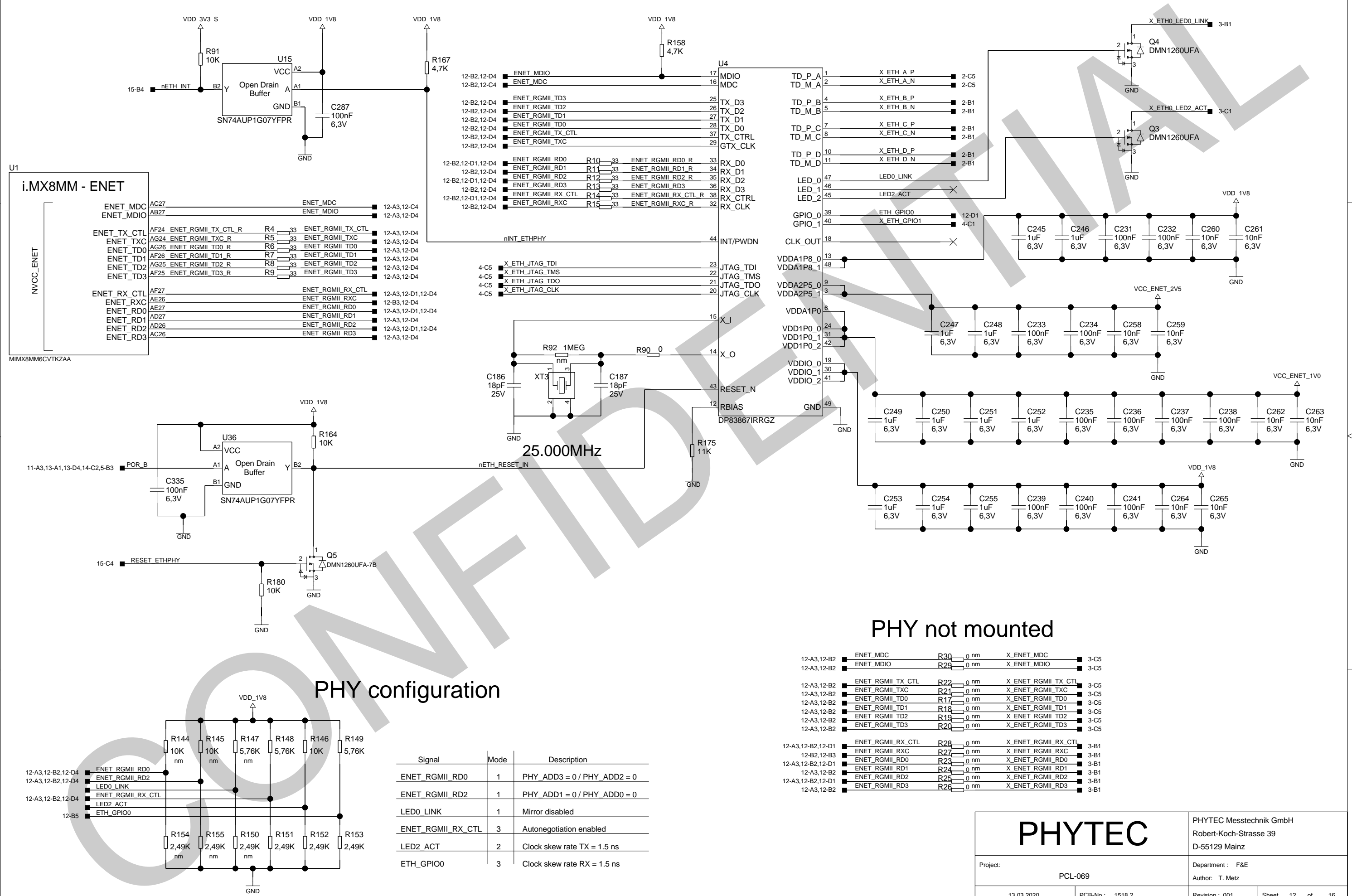
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Department : F&E  
Author: T. Metz  
Revision : 001  
Sheet 12 of 16

A

B

C

D

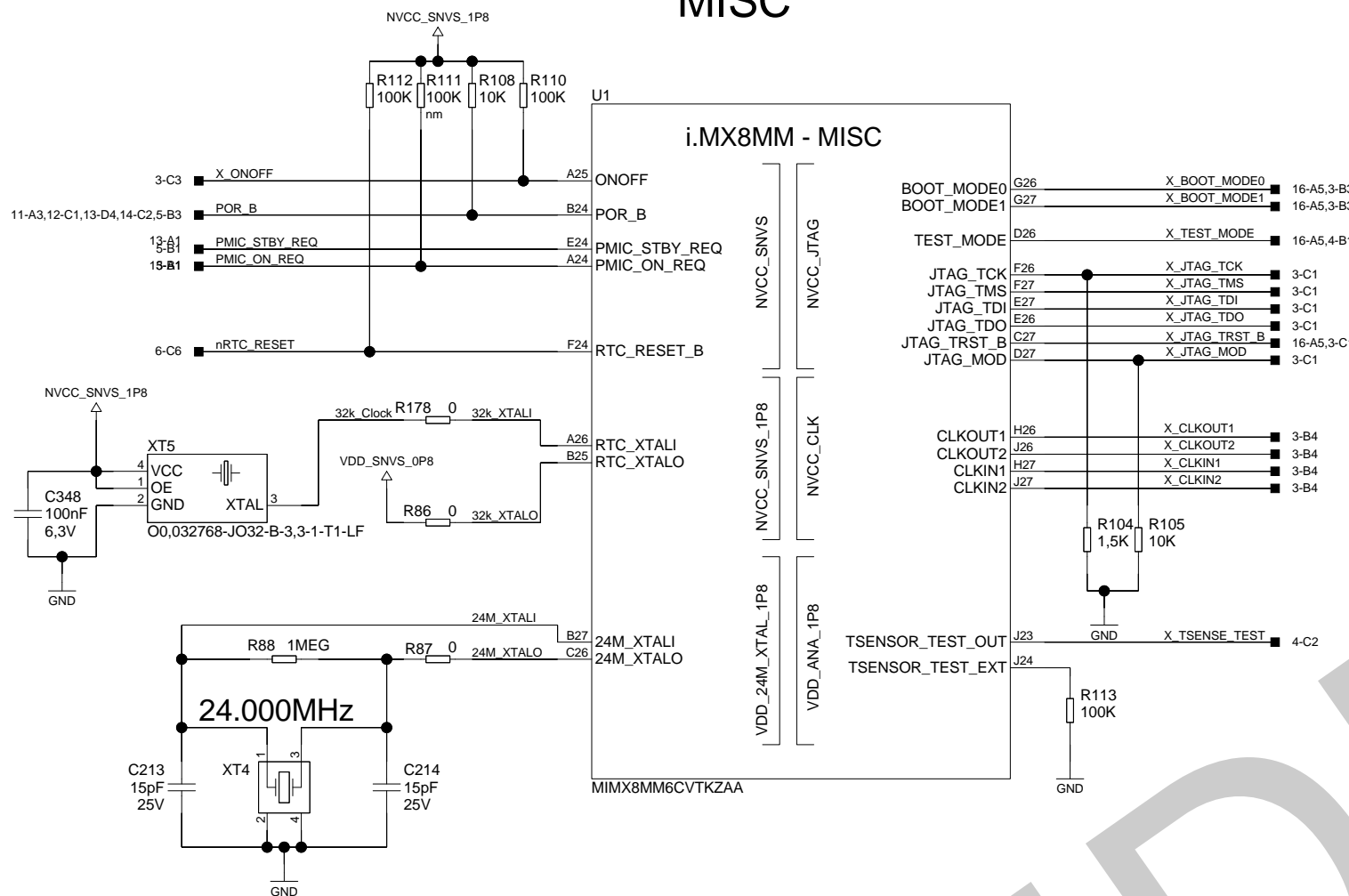
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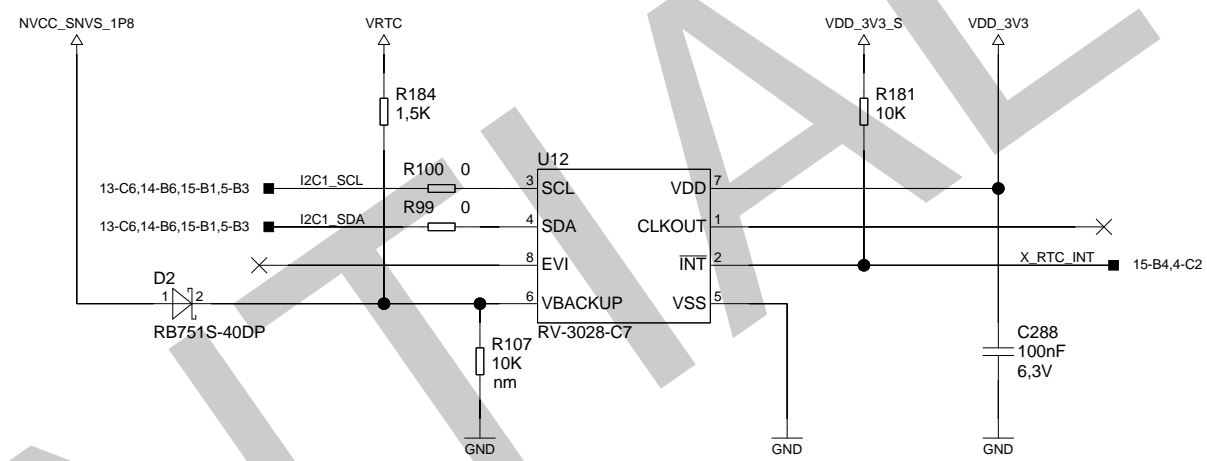
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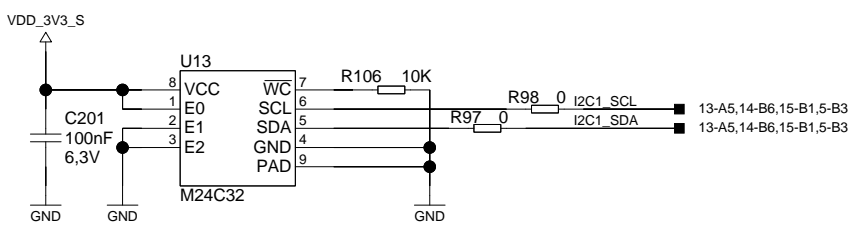


RTC  
I2C Addr. = 0x52

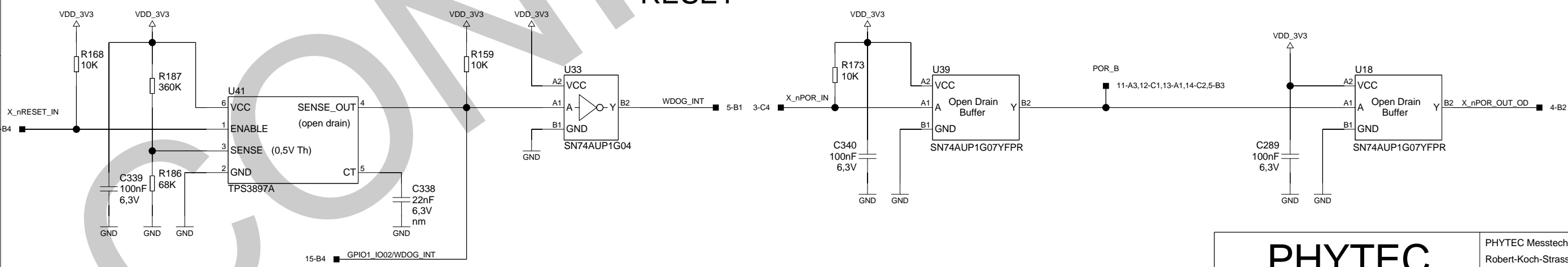


EEPROM

I2C Addr. = 0x51  
ID page I2C Addr. = 0x59 for factory use only



RESET



Acceptable lower limit VDD\_3V3: 3,14V  
Tdelay = 40 µs

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Project: PCL-069	Department : F&E Author : T. Metz
13.03.2020	PCB-No.: 1518.2
Revision : 001	Sheet 13 of 16

A

B

C

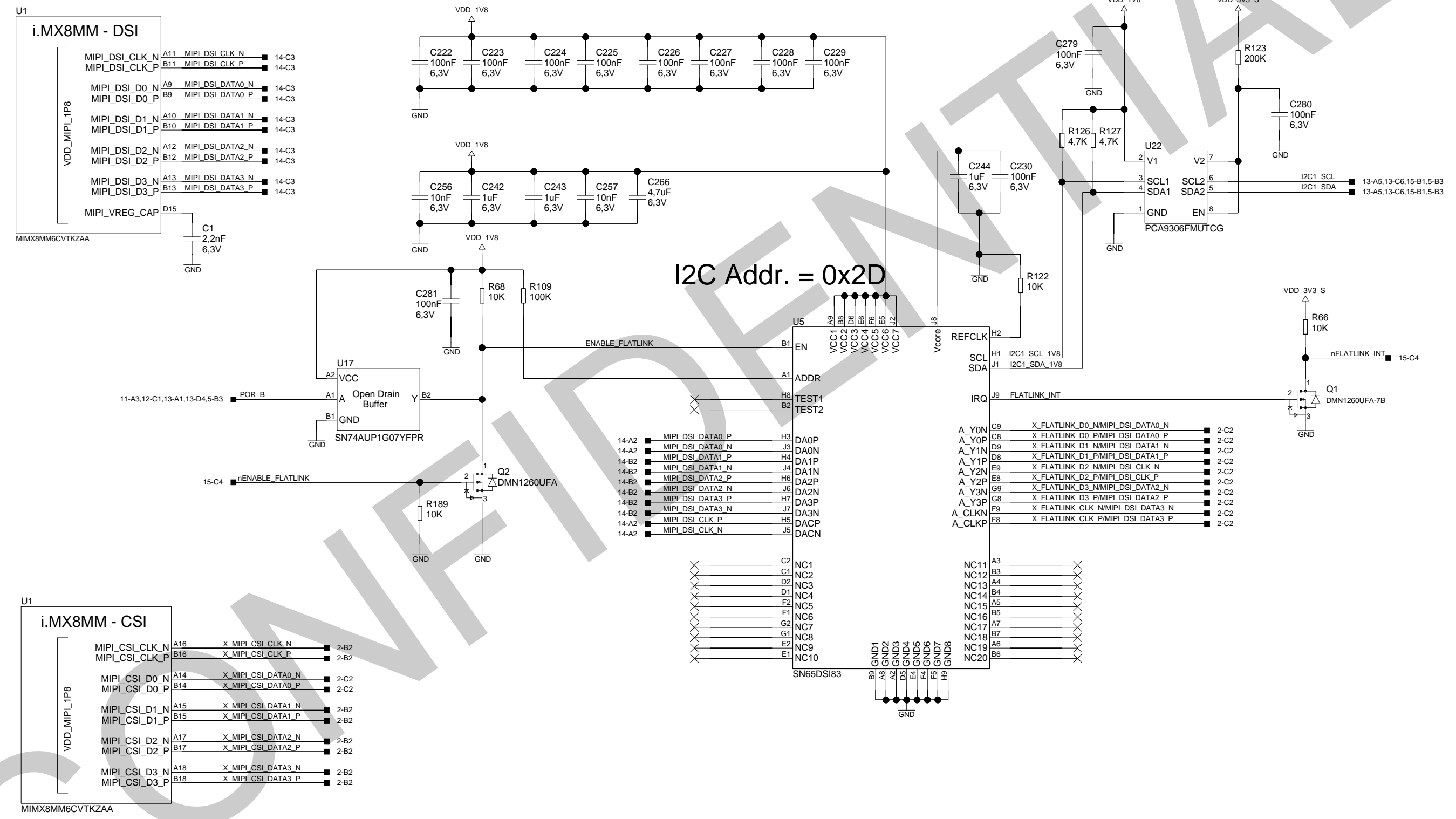
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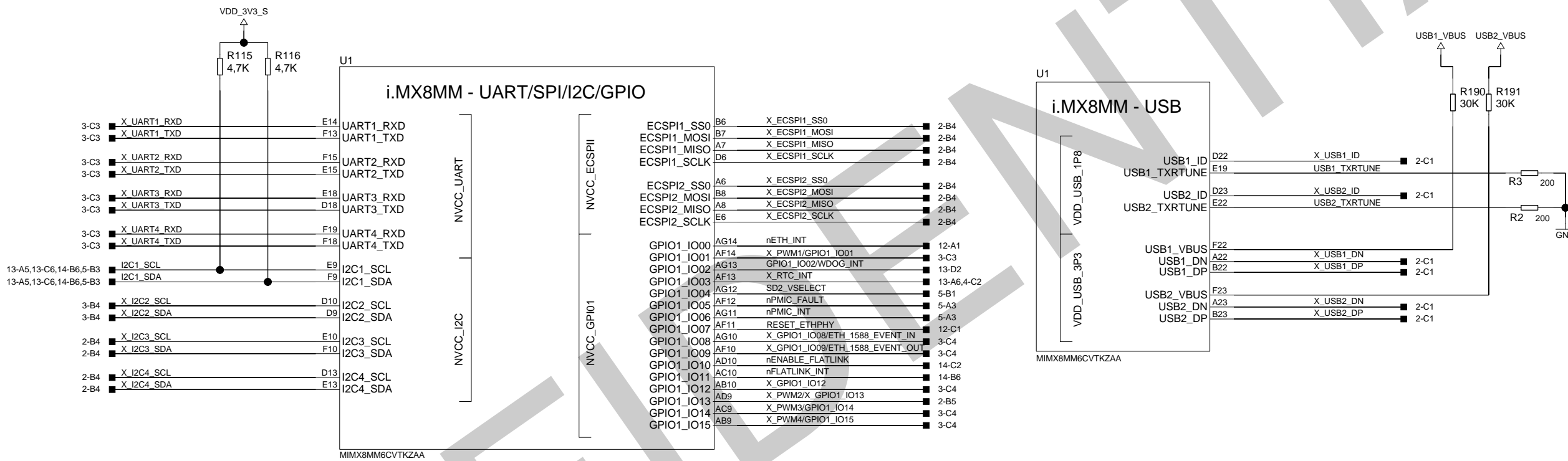
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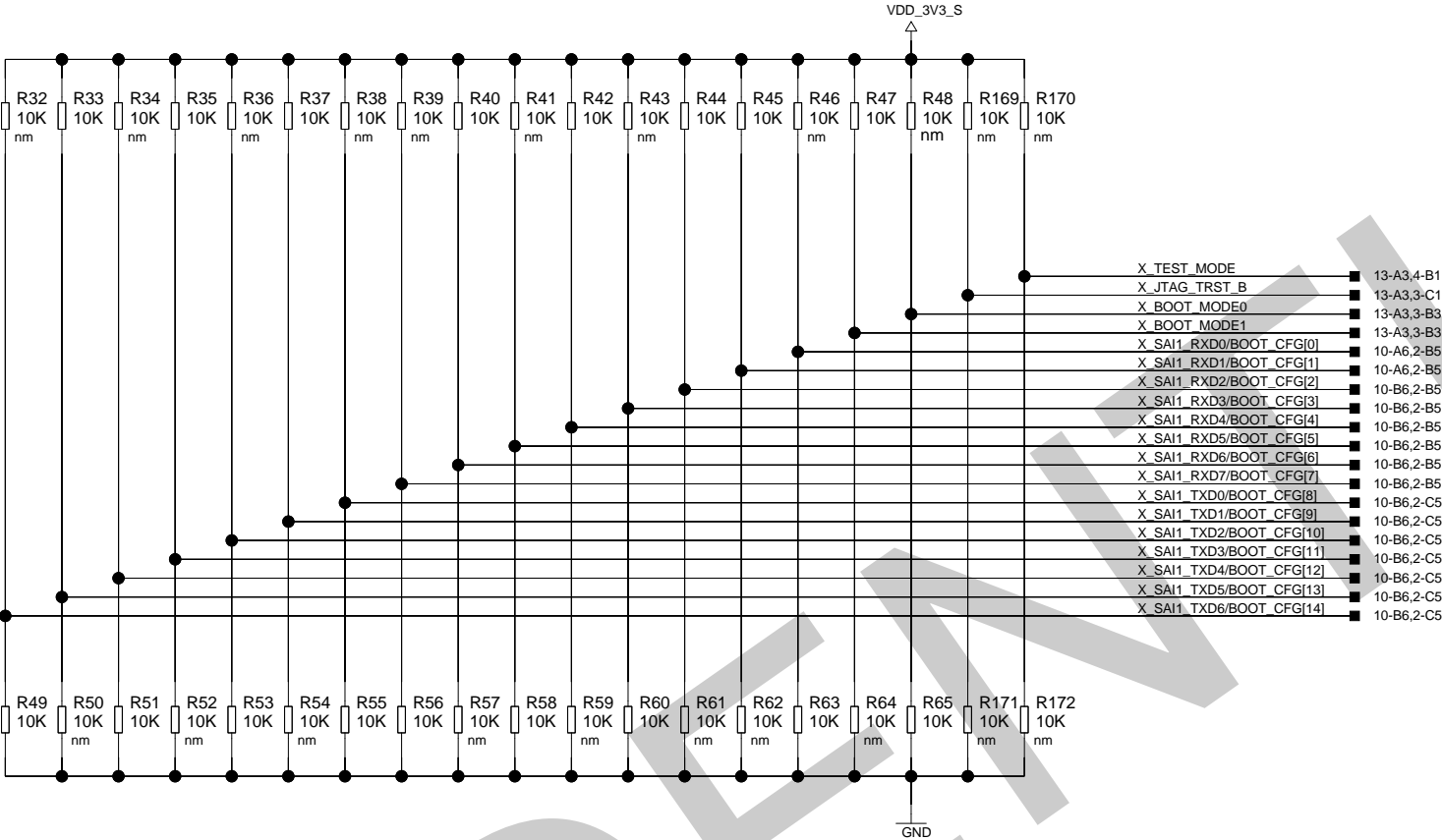
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Project:	PCL-069	Department :	F&E Author: T. Metz
13.03.2020	PCB-No.: 1518.2	Revision :	001
		Sheet	15 of 16

I2C1 addresses

Device	Address
PMIC	0x08
RTC	0x52
EEPROM	0x51
MIPI/FL Converter	0x2D



BOOT_MODE [1:0]	Boot type
00	Fuse boot
01	Serial downloader
10	Internal boot
11	Reserved

Default boot configuration for eMMC

CFG	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Level	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0

The table shows all available boot options for the SoM

Device	Addr	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]	
QSPI	0x470[15:0]	100			FLASH auto probe	FLASH TYPE: 000 - Device supports 3 Byte read by default 001 - Device supports 4 Byte read by default 010 - HyperFlash 1V8 011 - HyperFlash 3V3 100 - MXIC octal DDR			HOLD TIME: 00 - 50 us 01 - 1 ms 10 - 3 ms 11 - 10 ms		FLASH auto probe type		FlexSPI FLASH dummy cycle				
eMMC	0x470[15:0]	010			Port select: 10 - SD3		Power cycle enable: 0 - Disabled 1 - Enabled	SD loopback clock source SEL (SDR50 and SDR104 only): 0 - Through SD pad 1 - Direct	Fast boot: 0 - Regular 1 - Fast boot	Bus width: 000 - 1-Bit 001 - 4-Bit 010 - 8-Bit 101 - 4-Bit DDR (MMC 4.4) 110 - 8-Bit DDR (MMC 4.4) Remaining values are reserved			Speed: 00 - Normal 01 - High 10 - HS200 reserved 11 - Reserved		USDHC IO voltage selection: normal mode 0 - 3V3 1 - 1V8	USDHC IO voltage selection: Manufacturer mode 0 - 3V3 1 - 1V8	
SDIO	0x470[15:0]	001			Port select: 00 - SD1 01 - SD2		Power cycle enable: 0 - Disabled 1 - Enabled	SD loopback clock source SEL (SDR50 and SDR104 only): 0 - Through SD pad 1 - Direct	Fast boot: 0 - Regular 1 - Fast boot	Reserved		Bus width: 0 - 1-Bit 1 - 4-Bit	Speed: 000 - Normal / SDR12 001 - High / SDR25 010 - SDR50 011 - SDR104 101 - DDR50 reserved Remaining values are reserved			Reserved	

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Project: PCL-069		Department : F&E Author: T. Metz	
13.03.2020	PCB-No.: 1518.2	Revision : 001	Sheet 16 of 16