Assignment 3: A SIK Pipeline

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EE480 – Advanced Computer Architecture

I.   INTRODUCTION

The purpose of this assignment was to design and implement a pipelined implementation of SIK based on the previous assignment, a multi-cycle implementation of SIK.

II.   ENCODING THE INSTRUCTION SET

Compare to the multi-cycle implementation of the SIK, pipelined implemenation has 512 16 bit registers that consititude the stack of the machine. The first 256 of the registers are allocated for one thread and the second half is allocated for the second thread. The stack is indexed by 8-bt array of two elements, [7:0] sp [0:1]. Two separate program counters were used to keep track of which thread is executing which instruction, [15:0] pc [0:1].

III.   DESIGN AND ENCODING

The verilog code for project 5 from last semester was used as an reference for pipelining and the hyperthreading was attempted to implement. The idea of implementing hyperthreading is that to have a "switch" that identifies two threads. When switch = 0, the thread0 and switch = 1, thread1 would execute an instruction. However, only single thread implemantation was attempted to implement. The code has not been tested and there will be errors if it's compiled. The stage 3 of the project is implemented partially.

IV.   CONCLUSION

The program doesn't compile and some of the stages aren't implemented completely.