Assignment 3: A SIK Pipeline

Natsagdorj Baljinnyam, Justin Hill, Marco Reyes

EE480 – Advanced Computer Architecture

# Introduction

The purpose of this assignment was to design and implement a pipelined implementation of SIK based on the previous assignment, a multi-cycle implementation of SIK.

# encoding the instruction set

Compare to the multi-cycle implementation of the SIK, pipelined implemenation has 512 16 bit registers that consititude the stack of the machine. The first 256 of the registers are allocated for one thread and the second half is allocated for the second thread. The stack is indexed by 8-bt array of two elements, [7:0] sp [0:1]. Two separate program counters were used to keep track of which thread is executing which instruction, [15:0] pc [0:1].

1. DESIGN AND ENCODING

# Conclusion

# Rererence