Chrontel CH7025/CH7026 SDTV/VGA Encoder

Features

- TV encoder targets the handheld devices and other appropriate display devices used in consumer products.
- Supports multiple output formats, such as TV format (NTSC and PAL), analog RGB output for VGA. Sync signals can be provided in separate or composite manner (programmable composite sync generation).
- Three on-chip 10-bit high speed DACs providing flexible output capabilities, such as single, double or triple CVBS outputs, YPbPr output, RGB output and simultaneous CVBS and S-video outputs.
- 16Mbits SDRAM is used as frame buffer, supporting frame rate conversion.
- Flexible up and down scaling engine is embedded including de-flickering capability.
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB888, RGB666, RGB565 and etc), YCbCr (4:4:4 YCbCr, ITU656) and 2x or 3x multiplexed input. CPU interface is also supported.
- Supports for flexible input resolution up to 800x800 and 1024x650 (220x176, 320x240, 640x480, 720x480, 720x576, 800x480, 800x600, 480x800 and 600x800 etc.).
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each output is supported. (For RGB output, only brightness and contrast adjustment is supported).
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment are supported.
- 90/180/270 degree image rotation and vertical or horizontal flip functions are supported.
- Macrovision 7.1.L1 for SDTV is supported. (CH7025 only).
- TV/Monitor connection detection capability. DAC can be switched off based on detection result. (Driver support is required)
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported (2.3MHz –120MHz).
- Flexible input clock from crystal or oscillator is supported (2.3MHz – 64MHz).
- Only slave mode supported.
- Offered in 80-pin LQFP and 80-pin TFBGA package.
- Fully programmable through a serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.

General Description

The CH7025/CH7026 is a device targeting at handheld and similar systems which accepts a digital input signal, encodes and transmits data through three 10-bit DACs. This device is able to encode video signals and generate synchronization signals for NTSC and PAL standards. Analog RGB output and composite SYNC signal are also supported. The device accepts different data formats including RGB and YCbCr (e.g. RGB565, RGB666, RGB888, ITU656 like YCbCr, etc.). It has on-chip 16Mbit SDRAM frame buffer used for frame rate conversion as well as frame manipulations.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current update.

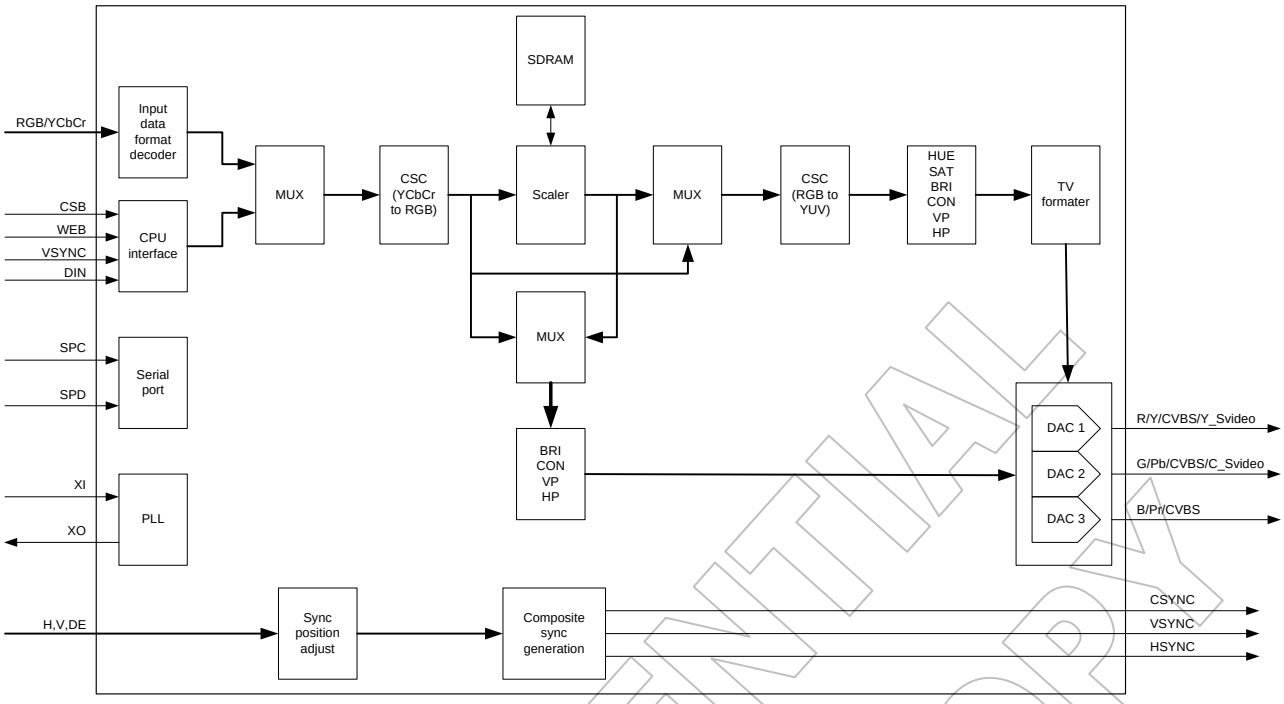

Figure 1: CH7025/CH7026 block diagram

Table of contents

1.0 Pin-out 5
1.1 Package Diagram 5
1.1.1 The 80-Pin BGA Package Diagram 5
1.1.2 The 80-Pin LQFP Package Diagram 6
1.2 Pin Description 7
2.0 Functional Description 11
2.1 Modes of operation 11
2.1.1 Graphics Controller to SDTV Encoder 11
2.1.2 ITU-R BT.601/656 TV Encoder 12
2.1.3 Analog RGB output 13
2.2 Input interface 13
2.2.1 Overview 13
2.2.2 Input Clock and Data Timing Diagram 13
2.2.3 Input data voltage 14
2.2.4 Input data format 14
2.3 Chip Output 19
2.3.1 TV output 19
2.3.2 VGA output 19
2.3.3 Video DAC output 20
2.3.4 DAC single/double termination 20
2.3.5 TV connection detect 20
2.3.6 Picture enhancement 20
2.3.7 Color Sub-carrier Generation 20
2.3.8 ITU-R BT.470 Compliance 21
2.3.9 SDRAM power down 21
3.0 Register control 22
3.1 Control Registers Index 22
3.2 Control Registers Map 25
3.3 Register Descriptions 27
4.0 Electrical specifications 54
4.1 Absolute maximum rating 54
4.2 Recommended operating conditions 54
4.3 Electrical characteristics 55
4.4 Digital inputs / outputs 55
4.5 AC specifications 56
5.0 Package Dimensions 57
6.0 Revision history 59

Figures and Tables

LIST OF FIGURES

Figure 1: CH7025/CH7026 block diagram 2
Figure 2: 80 pin BGA package 5
Figure 3: 80 pin LQFP package 6
Figure 4: Interlaced Sync Input/Output Timing 12
Figure 5: Clock, Data and Interface Timing 13
Figure 6: 12-bit Multiplexed Input Data Formats 19
Figure 7: 80 Pin BGA Package 57
Figure 8: 80 Pin LQFP Package 58

LIST OF TABLES

Table 1: Pin Description (BGA package) 7
Table 2: Pin Descriptions (LQFP package) 9
Table 3: Operation modes 11
Table 4: Typical input resolution 11
Table 5: ITU-R BT.601/656 TV Encoder Operating Modes 12
Table 6: Interlaced Sync Input/Output Timing 12
Table 7: Input data format 14
Table 8: Supported SDTV standards 19
Table 9: Composite sync type 20
Table 10: Video DAC Configurations for CH7025/CH7026 20
Table 11: Control Registers Index 22
Table 12: Serial Port Register Map (Page 1) 25
Table 13: SYNC output swapping sequence 29
Table 14: Multiple TV output configuration 30
Table 15: DAC output swapping sequence 30
Table 16: Input data format 31
Table 17: Output format 32
Table 18: Fame dropping selection 33
Table 19: SDTV reference burst amplitude adjustment BSTADJ[2:0] 43
Table 20: Video PLL1 feedback-divider 1 settings 48
Table 21: Video PLL1 pre-divider settings 49
Table 22: Post divider settings ratio of PLL2 49
Table 23: Video PLL1 feedback-divider 2 settings 49
Table 24: Post divider 1 settings of PLL3 50
Table 25: Post divider 3 settings of PLL3 50
Table 26: Video PLL1 Charge Pump trim settings 51
Table 27: Small step delay selection for latching clock in memory output buffer 51
Table 28: Delay selection for latching clock in memory buffer 51
Table 29: Delay selection for analog latching clock 51
Table 30: DAC gain settings 52
Table 31: Attached Display Mapping 53

1.0 Pin-out

1.1 Package Diagram

1.1.1 The 80-Pin BGA Package Diagram

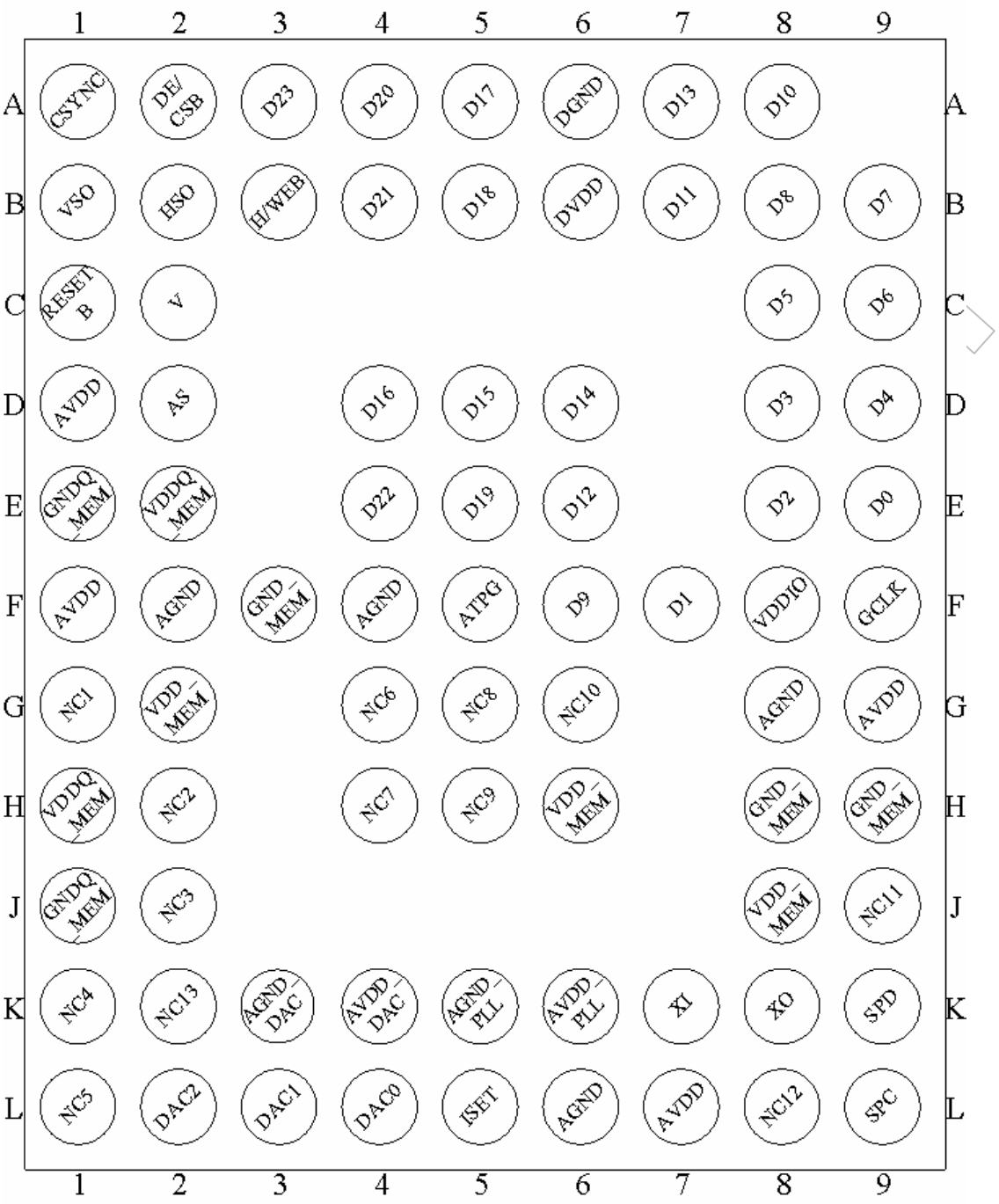

Figure 2: 80 pin BGA package

1.1.2 The 80-Pin LQFP Package Diagram

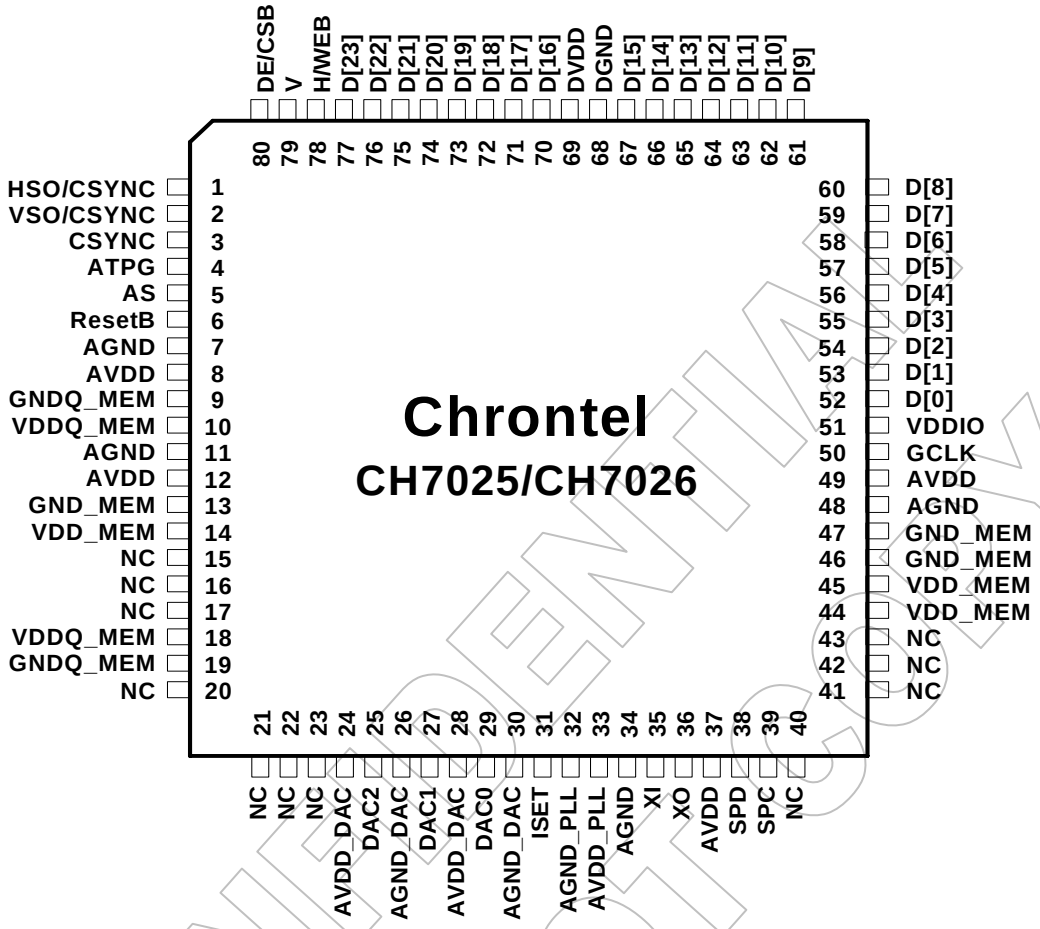

Figure 3: 80 pin LQFP package

1.2 Pin Description

Table 1: Pin Description (BGA package)

Pin #	Type	Symbol	Description
A3, E4, B4, A4, E5, B5, A5, D4, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8, F7, E9	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	I/O	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	I/O	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU interface The amplitude will be 0 to VDDIO.
D2	In	AS	Address select
F5	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
C1	In	ResetB	Reset * Input When this pin is low, the device is held in the hardware reset condition. When this pin is high, reset is controlled through the serial port.
K9	I/O	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
L9	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
L4	Out	DAC0	CVBS, S-video or Analog RGB output Full swing is up to 1.3v
L3	Out	DAC1	CVBS, S-video or Analog RGB output Full swing is up to 1.3v
L2	Out	DAC2	CVBS, S-video or Analog RGB output Full swing is up to 1.3v

Pin #	Type	Symbol	Description
L5	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
K7	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
K8	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
F9	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
B1	Out	VSO	Vertical sync signal output or composite sync output
B2	Out	HSO	Horizontal sync signal output or composite sync output
A1	Out	CSYNC	Composite sync output
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (1.8V or 2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground

Table 2: Pin Descriptions (LQFP package)

Pin #	Type	Symbol	Description
52 - 67 70 - 77	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
79	I/O	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
78	I/O	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
80	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
5	In	AS	Chip address select 0: 76h 1: 75h
4	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
6	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
38	I/O	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
39	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
29	Out	DAC0	CVBS, S-video or Analog RGB output Full swing is up to 1.3v
27	Out	DAC1	CVBS, S-video or Analog RGB output Full swing is up to 1.3v
25	Out	DAC2	CVBS, S-video or Analog RGB output Full swing is up to 1.3v
31	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
35	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.

Pin #	Type	Symbol	Description
36	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
50	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
2	Out	VSO/CSYNC	Vertical sync signal output or composite sync output, The amplitude of this pin is from 0 to AVDD
1	Out	HSO/CSYNC	Horizontal sync signal output or composite sync output, The amplitude of this pin is from 0 to AVDD
3	Out	CSYNC	Composite sync output, The amplitude of this pin is from 0 to AVDD
51	Power	VDDIO	IO supply voltage (1.2-3.3V)
69	Power	DVDD	Digital supply voltage (1.8V)
8,12,37,49	Power	AVDD	Analog supply voltage
33	Power	AVDD_PLL	PLL supply voltage
24,28	Power	AVDD_DAC	DAC power supply
10,18	Power	VDDQ_MEM	SDRAM output buffer supply voltage
14,44,45	Power	VDD_MEM	SDRAM device supply voltage
68	Power	DGND	Digital supply ground
7,11,34,48	Power	AGND	Analog supply ground
32	Power	AGND_PLL	PLL supply ground
26,30	Power	AGND_DAC	DAC supply ground
9,19	Power	GNDQ_MEM	SDRAM output buffer supply ground
13,46,47	Power	GND_MEM	SDRAM device supply ground

2.0 Functional Description

2.1 Modes of operation

The CH7025/CH7026 is capable of being operated as a TV encoder. **Table 3** describes the possible operating modes. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Basically, CH7025/CH7026 can take non-interlaced data from graphics controller and encode it to analog NTSC and PAL waveforms. It can also take in interlaced data from sources like MPEG decoder and perform simple SDTV encoding.

Table 3: Operation modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
Non-Interlaced	RGB / YCrCb[1]	Interlaced	CVBS, S-Video	SDTV encoder (NTSC / PAL) with non-interlaced input	2.1.1
Interlaced (480i, 576i)	RGB / YCrCb[1]	Interlaced	CVBS, S-Video	SDTV encoder (NTSC / PAL) with interlaced input	2.1.2

YCrCb signal has the following characteristics (assumed to be gamma corrected):

$$Y = 77/256 * R + 150/256 * G + 29/256 * B$$
$$Cr = 131/256 * R - 110/256 * G - 21/256 * B + 128$$
$$Cb = -44/256 * R - 87/256 * G + 131/256 * B + 128$$

Data is 8-bit or 10-bit width and follows ITU-R BT.656 format.
Data sequence is like : $Cb_0Y_0Cr_0Y_1, Cb_2Y_2Cr_2Y_3, ...$
Where $Cb_0Y_0Cr_0$ are co-sited samples, and Y_1 is the following Luma sample.

CH7025/CH7026 can also support analog RGB output through on DACs. Either horizontal and vertical sync or composite sync can be provided (DE signal can also be provided optionally). This kind of output format can be accepted by CRT or LCD monitors.

2.1.1 Graphics Controller to SDTV Encoder

CH7025/CH7026 is mainly designed as an SDTV encoder targeting handheld device market or some other applications that require TV out function such as displays in automobile. In this mode, the graphics controller of the handheld system or other system will send out non-interlaced data, sync and clock signals to CH7025/CH7026. CH7025/CH7026 can run in clock slave mode. In clock slave mode, no reference clock is output to the graphics controller. So the crystal becomes optional in the slave mode. However, if the clock from the graphics controller cannot meet the accuracy requirement of color sub-carrier generation, the crystal is still required, and it will be discussed in the later part of this document. Not only horizontal and vertical sync signals are normally sent to the device from the graphics controller, but also they can be embedded into the data stream in YCbCr input data formats. CH7025/CH7026 can also internally generate H and V sync then send them to graphics controller as reference. Input data can be unitary, 2X or 3X multiplexed , and the G_CLK clock signal can be 1X, 2X or 3X times the pixel rate. Input data will be scaled, scan converted and filtered, then encoded into the selected video standard and output from the video DACs. Various NTSC and PAL formats are supported. The device can output data in S-Video and CVBS format. The graphics resolutions supported are from 176x144 to 800x600. The typical resolutions are shown in **Table 4**. The device is capable of adding Macrovision encoding to the output signal (CH7025 only).

Table 4: Typical input resolution

Typical input resolution	176 x 144	176 x 220	220 x 176	240 x 320	320 x 240	240 x 240	480 x 640	640 x 480	480 x 480	720 x 480	720 x 576	800 x 480	800 x 576	856 x 480	800 x 600
Output TV format	NTSC_M, NTSC_J, NTSC_443 PAL_B/D/G/H/I, PAL_M, PAL_N, PAL_Nc, PAL_60														

2.1.2 ITU-R BT.601/656 TV Encoder

In interlaced data, sync and clock signals are input to the CH7025/CH7026 from a graphics controller or an MPEG decoder device. The YCbCr data format is most commonly used in these modes, but RGB data can be used as well. Not only horizontal and vertical sync signals are normally sent to the CH7025/CH7026 from the graphics device, but also they can be embedded into the data stream in YCbCr input data formats. In some cases, the chip itself can self generate H and V sync as reference for graphics controller. Data can be unitary, 2X or 3X multiplexed, and the GCLK clock signal can be 1X , 2X or 3X times the pixel rate. Input data bypasses the scaling, scan conversion and filtering blocks, is encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-Video and CVBS format. The graphics resolutions supported for ITU-R BT.601/656 TV output are shown in **Table 5**. The device is capable of adding Macrovision to the output signal (CH7025 only). The timing of the sync signals is shown in **Figure 4** below. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7025/CH7026 to identify the correct field.

Table 5: ITU-R BT.601/656 TV Encoder Operating Modes

Input Resolution	TV Output Standard
720x480i	NTSC
720x576i	PAL

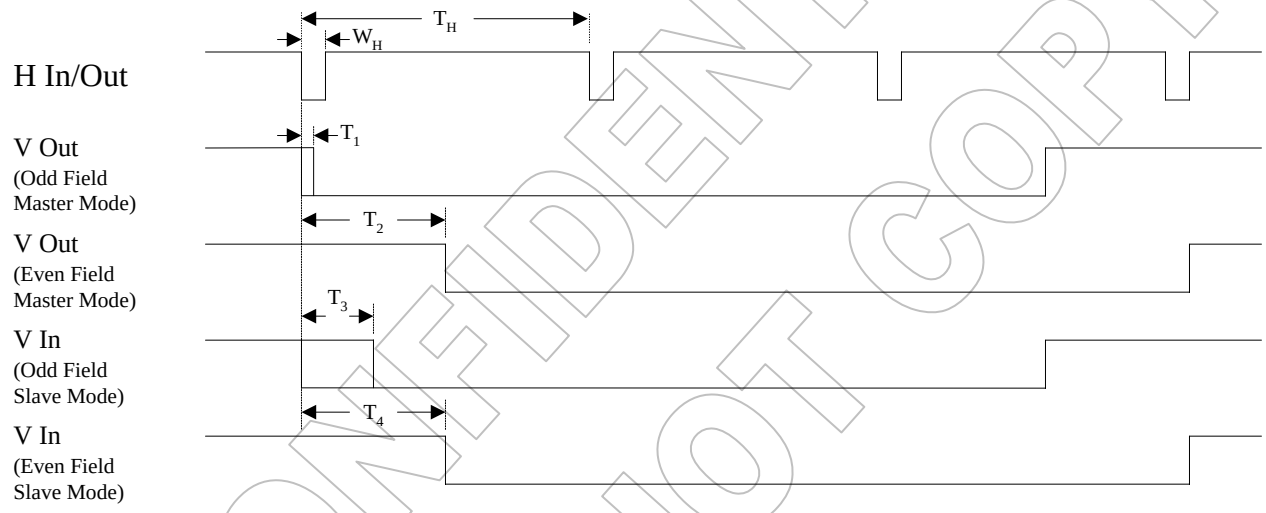

Figure 4: Interlaced Sync Input/Output Timing

Table 6: Interlaced Sync Input/Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_H	Total Line Period SDTV		63.5 / 64.0		 us
W_H	Hsync Width When output from CH7025/CH7026 When input to CH7025/CH7026	 1 1			 Pixel clocks Pixel clocks
T_1	Odd Field (Field 1) V SYNC out to H SYNC out alignment		0		us
T_2	Even Field (Field 2) V SYNC out delay from H SYNC out		$0.5*T_H$		us
T_3	Odd Field (Field 1) V SYNC in to H SYNC in alignment	0		$W_H - T_{PCK}$	us
T_4	Even Field (Field 2) V SYNC in delay from H SYNC in	W_H		$T_H - T_{PCK}$	us

2.1.3 Analog RGB output

CH7025/CH7026 can also be running under the analog RGB output mode. In this mode, the input data is the same as CH7025/CH7026 working as TV encoder and scaler could be bypassed. If the input resolution is not the same as what output requires, scaler can scale the input frame to expected size. On the contrary, if input frame size is what output requires, both scaler and SDRAM can be bypassed (in power down state). In addition, the sync signals can be provided in multiple formats such as separated vertical and horizontal sync, composite sync or both separated and composite sync. DE signal can also be provided optionally.

2.2 Input interface

2.2.1 Overview

Five distinct methods of transferring data to the CH7025/CH7026 are described. They are:

1. Unitary data, clock input at 1X the pixel rate
2. Multiplexed data, clock input at 1X of pixel rate
3. Multiplexed data, clock input at 2X of pixel rate
4. Multiplexed data, clock input at 3X of pixel rate
5. 16 or 24 bit CPU interface

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X or 3X pixel rate the data applied to the CH7025/CH7026 is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with one edge of the clock .The polarity of the pixel clock can be reversed under serial port control.

2.2.2 Input Clock and Data Timing Diagram

Figure 5 below shows the timing diagram for input data and clocks. The first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method.

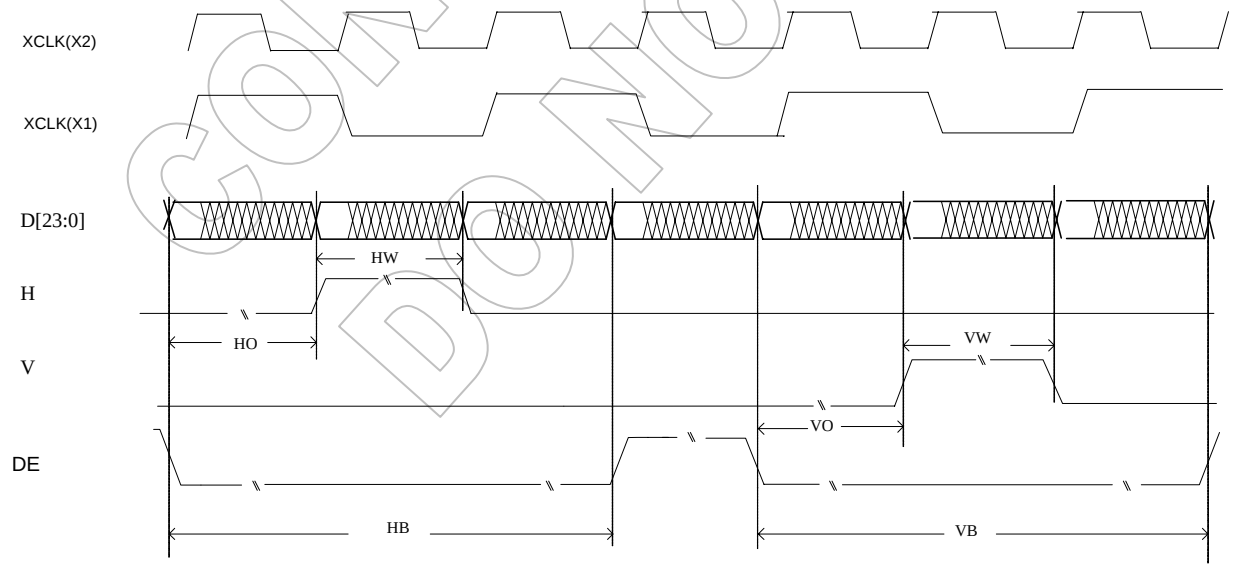

Figure 5: Clock, Data and Interface Timing

2.2.3 Input data voltage

The voltage level of input pins D[23:0], H, V, DE, SPC, SPD are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit **DIFFEN** is high, the input is pseudo differential mode that uses a reference voltage (VREF) to compare with input voltage and decide input logic value. The VREF value can be 80%, 70%, 60% and 50% of VDDIO value, referring to **VRTM[1:0]**. The pseudo differential mode can accept the wide range of the input voltage level from 1.2v to 3.3v, while the CMOS mode can accept 1.8v to 3.3v input voltage.

2.2.4 Input data format

The following table indicates the supported input data format by CH7025/CH7026.

Table 7: Input data format

MODE	HIGH	REVERSE	SWAP	IDF	D[23:16]	D[15:8]	D[7:0]
0	1'b0	1'b0	3'b000	4'b0000	R[7:0]	G[7:0]	B[7:0]
1				4'b0001	2'b00,R[5:0]	2'b00,G[5:0]	2'b00,B[5:0]
2				4'b0010	3'b000,R[4:0]	2'b00,G[5:0]	3'b000,B[4:0]
3				4'b0011	3'b000,R[4:0]	3'b000,G[4:0]	3'b000,B[4:0]
4				4'b0111	Y[7:0]	Cb[7:0]	Cr[7:0]
5				4'b1000	Y[7:0]	Cb[7:0]	Cr[7:0]
6				4'b1001	6'b000000,R[5:4]	R[3:0],G[5:2]	G[1:0],B[5:0]
7				4'b1010	8'b00000000	R[4:0],G[5:3]	G[2:0],B[4:0]
8				4'b1011	8'b00000000	1'b0,R[4:0],G[4:3]	G[2:0],B[4:0]
9			3'b001	4'b0000	R[7:0]	B[7:0]	G[7:0]
10				4'b0001	2'b00,R[5:0]	2'b00,B[5:0]	2'b00,G[5:0]
11				4'b0010	3'b000,R[4:0]	3'b000,B[4:0]	2'b00,G[5:0]
12				4'b0011	3'b000,R[4:0]	3'b000,B[4:0]	3'b000,G[4:0]
13				4'b0111	Y[7:0]	Cr[7:0]	Cb[7:0]
14				4'b1000	Y[7:0]	Cr[7:0]	Cb[7:0]
15				4'b1001	6'b000000,R[5:4]	R[3:0],B[5:2]	B[1:0],G[5:0]
16				4'b1010	8'b00000000	R[4:0],B[4:2]	B[1:0],G[5:0]
17				4'b1011	8'b00000000	1'b0,R[4:0],B[4:3]	B[2:0],G[4:0]
18			3'b010	4'b0000	G[7:0]	R[7:0]	B[7:0]
19				4'b0001	2'b00,G[5:0]	2'b00,R[5:0]	2'b00,B[5:0]
20				4'b0010	2'b00,G[5:0]	3'b000,R[4:0]	3'b000,B[4:0]
21				4'b0011	3'b000,G[4:0]	3'b000,R[4:0]	3'b000,B[4:0]
22				4'b0111	Cr[7:0]	Y[7:0]	Cb[7:0]
23				4'b1000	Cr[7:0]	Y[7:0]	Cb[7:0]
24				4'b1001	6'b000000,G[5:4]	G[3:0],R[5:2]	R[1:0],B[5:0]
25				4'b1010	8'b00000000	G[5:0],R[4:3]	R[2:0],B[4:0]
26				4'b1011	8'b00000000	1'b0,G[4:0],R[4:3]	R[2:0],B[4:0]
27			3'b011	4'b0000	G[7:0]	B[7:0]	R[7:0]
28				4'b0001	2'b00,G[5:0]	2'b00,B[5:0]	2'b00,R[5:0]
29				4'b0010	2'b00,G[5:0]	3'b000,B[4:0]	3'b000,R[4:0]
30				4'b0011	3'b000,G[4:0]	3'b000,B[4:0]	3'b000,R[4:0]

MODE	HIGH	REVERSE	SWAP	IDF	D[23:16]	D[15:8]	D[7:0]
31				4'b0111	Cb[7:0]	Cr[7:0]	Y[7:0]
32				4'b1000	Cb[7:0]	Cr[7:0]	Y[7:0]
33				4'b1001	6'b000000,G[5:4]	G[3:0],B[5:2]	B[1:0],R[5:0]
34				4'b1010	8'b00000000	G[5:0],B[4:3]	B[2:0],R[4:0]
35				4'b1011	8'b00000000	1'b0,G[4:0],B[4:3]	B[2:0],R[4:0]
36			3'b100	4'b0000	B[7:0]	R[7:0]	G[7:0]
37				4'b0001	2'b00,B[5:0]	2'b00,R[5:0]	2'b00,G[5:0]
38				4'b0010	3'b000,B[4:0]	3'b000,R[4:0]	2'b00,G[5:0]
39				4'b0011	3'b000,B[4:0]	3'b000,R[4:0]	3'b000,G[4:0]
40				4'b0111	Cr[7:0]	Y[7:0]	Cb[7:0]
41				4'b1000	Cr[7:0]	Y[7:0]	Cb[7:0]
42				4'b1001	6'b000000,B[5:4]	B[3:0],R[5:2]	R[1:0],G[5:0]
43				4'b1010	8'b00000000	B[4:0],R[4:2]	R[1:0],G[5:0]
44				4'b1011	8'b00000000	1'b0,B[4:0],R[4:3]	R[2:0],G[4:0]
45			3'b101	4'b0000	B[7:0]	G[7:0]	R[7:0]
46				4'b0001	2'b00,B[5:0]	2'b00,G[5:0]	2'b00,R[5:0]
47				4'b0010	3'b000,B[4:0]	2'b00,G[5:0]	3'b000,R[4:0]
48				4'b0011	3'b000,B[4:0]	3'b000,G[4:0]	3'b000,R[4:0]
49				4'b0111	Cr[7:0]	Cb[7:0]	Y[7:0]
50				4'b1000	Cr[7:0]	Cb[7:0]	Y[7:0]
51				4'b1001	6'b000000,B[5:4]	B[3:0],G[5:2]	G[1:0],R[5:0]
52				4'b1010	8'b00000000	B[4:0],G[5:3]	G[2:0],R[4:0]
53				4'b1011	8'b00000000	1'b0,B[4:0],G[4:3]	G[2:0],R[4:0]
54		1'b1	3'b000	4'b0000	R[0:7]	G[0:7]	B[0:7]
55				4'b0001	2'b00,R[0:5]	2'b00,G[0:5]	2'b00,B[0:5]
56				4'b0010	3'b000,R[0:4]	2'b00,G[0:5]	3'b000,B[0:4]
57				4'b0011	3'b000,R[0:4]	3'b000,G[0:4]	3'b000,B[0:4]
58				4'b0111	Y[0:7]	Cb[0:7]	Cr[0:7]
59				4'b1000	Y[0:7]	Cb[0:7]	Cr[0:7]
60				4'b1001	6'b000000,R[0:1]	R[2:5],G[0:3]	G[4:5],B[0:5]
61				4'b1010	8'b00000000	R[0:4],G[0:2]	G[3:5],B[0:4]
62				4'b1011	8'b00000000	1'b0,R[0:4],G[0:1]	G[2:4],B[0:4]
63			3'b001	4'b0000	R[0:7]	B[0:7]	G[0:7]
64				4'b0001	2'b00,R[0:5]	2'b00,B[0:5]	2'b00,G[0:5]
65				4'b0010	3'b00,R[0:4]	3'b00,B[0:4]	2'b000,G[0:5]
66				4'b0011	3'b000,R[0:4]	3'b000,B[0:4]	3'b000,G[0:4]
67				4'b0111	Y[0:7]	Cr[0:7]	Cb[0:7]
68				4'b1000	Y[0:7]	Cr[0:7]	Cb[0:7]
69				4'b1001	6'b000000,R[0:1]	R[2:5],B[0:3]	B[4:5],G[0:5]
70				4'b1010	8'b00000000	R[0:4],B[0:2]	B[3:4],G[0:5]
71				4'b1011	8'b00000000	1'b0,R[0:4],B[0:1]	B[2:4],G[0:4]
72			3'b010	4'b0000	G[0:7]	R[0:7]	B[0:7]

MODE	HIGH	REVERSE	SWAP	IDF	D[23:16]	D[15:8]	D[7:0]
73				4'b0001	2'b00,G[0:5]	2'b00,R[0:5]	2'b00,B[0:5]
74				4'b0010	2'b00,G[0:5]	3'b000,R[0:4]	3'b000,B[0:4]
75				4'b0011	3'b000,G[0:4]	3'b000,R[0:4]	3'b000,B[0:4]
76				4'b0111	Cb[0:7]	Y[0:7]	Cr[0:7]
77				4'b1000	Cb[0:7]	Y[0:7]	Cr[0:7]
78				4'b1001	6'b000000,G[0:1]	G[2:5],R[0:3]	R[4:5],B[0:5]
79				4'b1010	8'b00000000	G[0:5],R[0:1]	R[2:4],B[0:4]
80				4'b1011	8'b00000000	1'b0,G[0:4],R[0:1]	R[2:4],B[0:4]
81			3'b011	4'b0000	G[0:7]	B[0:7]	R[7:0]
82				4'b0001	2'b00,G[0:5]	2'b00,B[0:5]	2'b00,R[0:5]
83				4'b0010	2'b00,G[0:5]	3'b000,B[0:4]	3'b000,R[0:4]
84				4'b0011	3'b000,G[0:4]	3'b000,B[0:4]	3'b000,R[0:4]
85				4'b0111	Cb[0:7]	Cr[0:7]	Y[0:7]
86				4'b1000	Cb[0:7]	Cr[0:7]	Y[0:7]
87				4'b1001	6'b000000,G[0:1]	G[2:5],B[0:3]	B[4:5],R[0:5]
88				4'b1010	8'b00000000	G[0:5],B[0:1]	B[2:4],R[0:4]
89				4'b1011	8'b00000000	1'b0,G[0:4],B[0:1]	B[2:4],R[0:4]
90			3'b100	4'b0000	B[0:7]	R[0:7]	G[0:7]
91				4'b0001	2'b00,B[0:5]	2'b00,R[0:5]	2'b00,G[0:5]
92				4'b0010	3'b000,B[0:4]	3'b000,R[0:4]	2'b00,G[0:5]
93				4'b0011	3'b000,B[0:4]	3'b000,R[0:4]	3'b000,G[0:4]
94				4'b0111	Cr[0:7]	Y[0:7]	Cb[0:7]
95				4'b1000	Cr[0:7]	Y[0:7]	Cb[0:7]
96				4'b1001	6'b000000,B[0:1]	B[2:5],R[0:3]	R[4:5],G[0:5]
97				4'b1010	8'b00000000	B[0:4],R[0:2]	R[3:4],G[0:5]
98				4'b1011	8'b00000000	1'b0,B[0:4],R[0:1]	R[2:4],G[0:4]
99			3'b101	4'b0000	B[0:7]	G[0:7]	R[0:7]
100				4'b0001	2'b00,B[0:5]	2'b00,G[0:5]	2'b00,R[0:5]
101				4'b0010	3'b000,B[0:4]	2'b00,G[0:5]	3'b000,R[0:4]
102				4'b0011	3'b000,B[0:4]	3'b000,G[0:4]	3'b000,R[0:4]
103				4'b0111	Cr[0:7]	Cb[0:7]	Y[0:7]
104				4'b1000	Cr[0:7]	Cb[0:7]	Y[0:7]
105				4'b1001	6'b000000,B[0:1]	B[2:5],G[0:3]	G[4:5],R[0:5]
106				4'b1010	8'b00000000	B[0:4],G[0:2]	G[3:5],R[0:4]
108				4'b1011	8'b00000000	1'b0,B[0:4],G[0:1]	G[2:4],R[0:4]
109	1'b1	1'b0	3'b000	4'b0001	R[5:0],2'b00	G[5:0],2'b00	B[5:0],2'b00
110				4'b0010	R[4:0],3'b000	G[5:0],2'b00	B[4:0],3'b000
111				4'b0011	R[4:0],3'b000	G[4:0],3'b000	B[4:0],3'b000
112				4'b1001	R[5:0],G[5:4]	G[3:0],B[5:2]	B[1:0],6'b000000
113				4'b1010	R[4:0],G[5:3]	G[2:0],B[4:0]	8'b00000000
114				4'b1011	R[4:0],G[4:2]	G[1:0],B[4:0],1'b0	8'b00000000
115			3'b001	4'b0001	R[5:0],2'b00	B[5:0],2'b00	G[5:0],2'b00

MODE	HIGH	REVERSE	SWAP	IDF	D[23:16]	D[15:8]	D[7:0]
116				4'b0010	R[4:0],3'b000	B[4:0],3'b000	G[5:0],2'b00
117				4'b0011	R[4:0],3'b000	B[4:0],3'b000	G[4:0],3'b000
118				4'b1001	R[5:0],B[5:4]	B[3:0],G[5:2]	G[1:0],6'b000000
119				4'b1010	R[4:0],B[4:2]	B[1:0],G[5:0]	8'b00000000
120				4'b1011	R[4:0],B[4:2]	B[1:0],G[4:0],1'b0	8'b00000000
121			3'b010	4'b0001	G[5:0],2'b00	R[5:0],2'b00	B[5:0],2'b00
123				4'b0010	G[5:0],2'b00	R[4:0],3'b000	B[4:0],3'b000
124				4'b0011	G[4:0],3'b000	R[4:0],3'b000	B[4:0],3'b000
125				4'b1001	G[5:0],R[5:4]	R[3:0],B[5:2]	B[1:0],6'b000000
126				4'b1010	G[5:0],R[4:3]	R[2:0],B[4:0]	8'b00000000
127				4'b1011	G[4:0],R[4:2]	R[1:0],B[4:0],1'b0	8'b00000000
128			3'b011	4'b0001	G[5:0],2'b00	B[5:0],2'b00	R[5:0],2'b00
129				4'b0010	G[5:0],2'b00	B[4:0],3'b000	R[4:0],3'b000
130				4'b0011	G[4:0],3'b000	B[4:0],3'b000	R[4:0],3'b000
131				4'b1001	G[5:0],B[5:4]	B[3:0],R[5:2]	R[1:0],6'b000000
132				4'b1010	G[5:0],B[4:3]	B[2:0],R[4:0]	8'b00000000
133				4'b1011	G[4:0],B[4:2]	B[1:0],R[4:0],1'b0	8'b00000000
134			3'b100	4'b0001	B[5:0],2'b00	R[5:0],2'b00	G[5:0],2'b00
135				4'b0010	B[4:0],3'b000	R[4:0],3'b000	G[5:0],2'b00
136				4'b0011	B[4:0],3'b000	R[4:0],3'b000	G[4:0],3'b000
137				4'b1001	B[5:0],R[5:4]	R[3:0],G[5:2]	G[1:0],6'b000000
138				4'b1010	B[4:0],R[4:2]	R[1:0],G[5:0]	8'b00000000
139				4'b1011	B[4:0],R[4:2]	R[1:0],G[4:0],1'b0	8'b00000000
140			3'b101	4'b0001	B[5:0],2'b00	G[5:0],2'b00	R[5:0],2'b00
141				4'b0010	B[4:0],3'b000	G[5:0],2'b00	R[4:0],3'b000
142				4'b0011	B[4:0],3'b000	G[4:0],3'b000	R[4:0],3'b000
143				4'b1001	B[5:0],G[5:4]	G[3:0],R[5:2]	R[1:0],6'b000000
144				4'b1010	B[4:0],G[5:3]	G[2:0],R[4:0]	8'b00000000
145				4'b1011	B[4:0],G[4:2]	G[1:0],R[4:0],1'b0	8'b00000000
146		1'b1	3'b000	4'b0001	R[0:5],2'b00	G[0:5],2'b00	B[0:5],2'b00
147				4'b0010	R[0:4],3'b000	G[0:5],2'b00	B[0:4],3'b000
148				4'b0011	R[0:4],3'b000	G[0:4],3'b000	B[0:4],3'b000
149				4'b1001	R[0:5],G[0:1]	G[2:5],B[0:3]	B[4:5],6'b000000
150				4'b1010	R[0:4],G[0:2]	G[3:5],B[0:4]	8'b00000000
151				4'b1011	R[0:4],G[0:2]	G[3:4],B[0:4],1'b0	8'b00000000
152			3'b001	4'b0001	R[0:5],2'b00	B[0:5],2'b00	G[0:5],2'b00
153				4'b0010	R[0:4],3'b000	B[0:4],3'b000	G[0:5],2'b00
154				4'b0011	R[0:4],3'b000	B[0:4],3'b000	G[0:4],3'b000
155				4'b1001	R[0:5],B[0:1]	B[2:5],G[0:3]	G[4:5],6'b000000
156				4'b1010	R[0:4],B[0:2]	B[3:4],G[0:5]	8'b00000000
157				4'b1011	R[0:4],B[0:2]	B[3:4],G[0:4],1'b0	8'b00000000
158			3'b010	4'b0001	G[0:5],2'b00	R[0:5],2'b00	B[0:5],2'b00

MODE	HIGH	REVERSE	SWAP	IDF	D[23:16]	D[15:8]	D[7:0]
159				4'b0010	G[0:5],2'b00	R[0:4],3'b000	B[0:4],3'b000
160				4'b0011	G[0:4],3'b000	R[0:4],3'b000	B[0:4],3'b000
161				4'b1001	G[0:5],R[0:1]	R[2:5],B[0:3]	B[4:5],6'b000000
162				4'b1010	G[0:5],R[0:1]	R[2:4],B[0:4]	8'b00000000
163				4'b1011	G[0:4],R[0:2]	R[3:4],B[0:4],1'b0	8'b00000000
164			3'b011	4'b0001	G[0:5],2'b00	B[0:5],2'b00	R[0:5],2'b00
165				4'b0010	G[0:5],2'b00	B[0:4],3'b000	R[0:4],3'b000
166				4'b0011	G[0:4],3'b000	B[0:4],3'b000	R[0:4],3'b000
167				4'b1001	G[0:5],B[0:1]	B[2:5],R[0:3]	R[4:5],6'b000000
168				4'b1010	G[0:5],B[0:1]	B[2:4],R[0:4]	8'b00000000
169				4'b1011	G[0:4],B[0:2]	B[3:4],R[0:4],1'b0	8'b00000000
170			3'b100	4'b0001	B[0:5],2'b00	R[0:5],2'b00	G[0:5],2'b00
171				4'b0010	B[0:4],3'b000	R[0:4],3'b000	G[0:5],2'b00
172				4'b0011	B[0:4],3'b000	R[0:4],3'b000	G[0:4],3'b000
173				4'b1001	B[0:5],R[0:1]	R[2:5],G[0:3]	G[4:5],6'b000000
174				4'b1010	B[0:4],R[0:2]	R[3:4],G[0:5]	8'b00000000
175				4'b1011	B[0:4],R[0:2]	R[3:4],G[0:4],1'b0	8'b00000000
176			3'b101	4'b0001	B[0:5],2'b00	G[0:5],2'b00	R[0:5],2'b00
177				4'b0010	B[0:4],3'b000	G[0:5],2'b00	R[0:4],3'b000
178				4'b0011	B[0:4],3'b000	G[0:4],3'b000	R[0:4],3'b000
179				4'b1001	B[0:5],G[0:1]	G[2:5],R[0:3]	R[4:5],6'b000000
180				4'b1010	B[0:4],G[0:2]	G[3:5],R[0:4]	8'b00000000
181				4'b1011	B[0:4],G[0:2]	G[3:4],R[0:4],1'b0	8'b00000000
182	1'bx	1'bx	1'bx	4'b0100	R[7:3],G[7:5],R[2:0],G[1],G[4:2],B[7:3],G[0],B[2:0]		
183	1'bx	1'bx	1'bx	4'b0101	8'h00	Y[7:0]	C[7:0]
184	1'bx	1'bx	1'bx	4'b0110	4'h0,Y[9:0],C[9:0]		

IDF[3:0] describes the major input data format that CH7025/CH7026 accepts. They are: (**Table 16**)

IDF = 0: 888 RGB input
IDF = 1: 666 RGB input
IDF = 2: 565 RGB input
IDF = 3: 555 RGB input
IDF = 4: DVO input
IDF = 5: 8 bit YCbCr4:2:2 input
IDF = 6: 10 bit YCbCr4:2:2 input
IDF = 7: YCbCr4:4:4 input
IDF = 8: YCbCr4:4:4 input with embedded sync
IDF = 9: Consecutive aligned 666 RGB input
IDF = 10: Consecutive aligned 565 RGB input
IDF = 11: Consecutive aligned 555 RGB input

Table 7 above describe the 24-bit input data format under unitary mode. For multiplexed input, input data needs to be de-multiplexed to unitary input first then this table can be applied. The multiplexed input data format is shown in **Figure 8** below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel. (3X input has the similar feature)

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

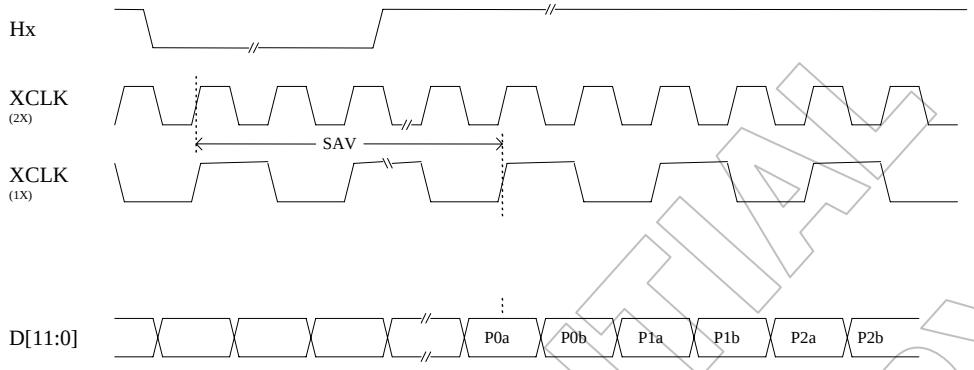

Figure 6: 12-bit Multiplexed Input Data Formats

In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connect error and correct it automatically, for example, if the input P14 and P15 are a group, but you take P13 and P14 as a group, the hardware can detect this error and correct it by run-in code.

2.3 Chip Output

2.3.1 TV output

The CH7025/CH7026 support the following output formats:

Table 8: Supported SDTV standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	60/1.001	858x525	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

CVBS, S-video, YPbPr and analog RGB output are supported, when output analog RGB, composite sync output is available.

2.3.2 VGA output

CH7025/CH7026 also supports analog RGB output through video DACs. Typically used resolution is 800x600, 856x480, 800x480 or 640x480. Vertical sync, horizontal sync and data enable signal are provided. Composite sync output is also supported. The type of composite sync can be programmed through the register map in Section 3.1.

Table 9: Composite sync type

CSSEL[2:0]	Composite sync type
0	Vsync XOR Hsync
1	Vsync OR Hsync
2	Vsync AND Hsync

2.3.3 Video DAC output

The DAC output is configured by the register bits **VFMT[2:0]**. **DACS[1:0]** bits are used to control the multiple output format i.e. dual or triple CVBS output, dual CVBS and S-Video output and etc. **DACSP[2:0]** bits are to swap the DAC output sequence such as CVBS, S-Video or S-Video, CVBS. Detailed information of these bits are described in register bits description section of this document. **Table 10** below lists the DAC output configurations of the CH7025/CH7026:

Table 10: Video DAC Configurations for CH7025/CH7026

DAC0	DAC1	DAC2
CVBS	Y	C
CVBS	CVBS	0
CVBS	CVBS	CVBS
Y(R)	Pb(G)	Pr(B)

2.3.4 DAC single/double termination

The DAC output of CH7025/CH7026 can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. See also the description of register bit **SEL_R**.

2.3.5 TV connection detect

CH7025/CH7026 can detect the TV connection by setting register SPPSNS. It can detect which DAC are connected, short to ground or not connected.

2.3.6 Picture enhancement

The CH7025/CH7026 has the capability of vertical and horizontal output picture position adjustment. It can automatically put the picture in the display center, and the vertical or horizontal position is also programmable through user input. And also it can provide brightness, contrast, hue, saturation adjustment and text enhancement functions. (For analog RGB output, only brightness and contrast adjustment is available).

CH7025/CH7026 also supports vertical or horizontal flip and rotation (0, 90, 180 and 270 degree) functions.

2.3.7 Color Sub-carrier Generation

CH7025/CH7026 has two ways to generate the color sub-carrier frequency. If the **GCLK** from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the **GCLK**. However, since even a ±0.01% sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7025/CH7026 has the ability to generate the sub-carrier frequency from the crystal when the **GCLK** from the graphics device cannot meet the requirement. In this case, the crystal has to be present. In other words, the only configuration where the off-chip crystal can be removed is when slave mode is used and the graphics controller provides **GCLK** with required characteristics.

In addition, CH7025/CH7026 has the capability to gen-lock the color sub-carrier with Vsync. Also, it has the ability to operate in a “stop dot crawl” mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.3.8 ITU-R BT.470 Compliance

The CH7025/CH7026 is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of **GCLK** from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the input resolution and the filter selection.

2.3.9 SDRAM power down

Generally, SDRAM can have two kinds of power down modes. One is power down mode, the other is deep power down mode. For power down mode, by dropping the CKE signal from high to low and holding CS signal high, then SDRAM goes into the power down mode. All data contents will be held in the bank. For deep power down mode, a command is required to issued. There is a bit called MEMPD in register map. It can be used to enable the deep power mode. During deep power mode, all the data in memory banks will be lost. **An very important thing required to be noted here is that not all the SDRAM parts support either power down or deep power down mode**. In these cases, even CH7025/CH7026 enters into power down, the leakage current is still large (> 100uA). This current is primarily derived from the SDRAM die. For detailed information about power down of SDRAM, please refer to SDRAM vendors' specifications.

3.0 Register control

The CH7025/CH7026 is controlled via a serial control port. The serial bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written into under all power down modes. The device should retain all register values during power down modes.

3.1 Control Registers Index

Table 11: Control Registers Index

Name	Description	Address	Page
A1[31:0]	Divider ratio for UCLK	4Dh – 50H	1
A2[7:0]	Divider ratio for MCLK	51h	1
ACIV	Sub-carrier generation method	41h	1
AFLTBP	Adaptive filter bypass	3Eh	1
AH_LB	Multiplexed input data alignment	0Bh	1
BC1[6:0]	A value of AX+B adjustment on R channel	3Bh	1
BC2[7:0]	B value of AX+B adjustment on R channel	3Ch	1
BPSEL	TV bypass clock selection	55h	1
BRI[7:0]	Brightness control value	31h	1
BSTADJ[2:0]	Burst amplitude adjustment	40h	1
CBS_SV[1:0]	Dual, triple or single TV output configuring bits	0Ah	1
CBW	Chroma filter bandwidth selection	3Dh	1
CFBP	Chroma filter bypass enable	3Fh	1
CKINV	Clock inversion bit for latch clock	75h	1
CPUEN	CPU interface enable	0Bh	1
CSBINV	Inversion bit for CSB signal of CPU interface	0Eh	1
CSSEL[2:0]	Composite sync type selector	08h	1
CTA[6:0]	Contrast control value	30h	1
DACAT0[1:0]	DAC connection status for DAC0	7Fh	1
DACAT1[1:0]	DAC connection status for DAC1	7Fh	1
DACAT2[1:0]	DAC connection status for DAC2	7Fh	1
DACS[1:0]	Multiple TV output configuration	0Ah	1
DACG[1:0]	DAC gain adjustment	77h	1
DBP	Dither function bypass	3Eh	1
DACKINV	DAC clock inversion bits	75h	1
DACPD[2:0]	DAC power down bits	04h	1
DACSP[2:0]	DAC output sequence swap bits	0Ah	1
DEPO_I	Input DE signal polarity	07h	1
DEPO_O	Output DE signal polarity	07h	1
DES	Using encoded sync	09h	1
DID[7:0]	Device ID	00h	1
DIFFEN[1:0]	Differential input mode enable	76h	1
DISPON	Clock signal selection for DAC detection	7Dh	1
DNSMPEN	4:3 down sample enable	0Eh	1
DOTB	Dot crawl enable	40h	1
DPCKN4	Divider value	53h	1
DPSEL[1:0]	Pixel and latching clock selection	55h	1
DPD	Digital power down	04h	1
DVALID	SDRAM ready signal	7Eh	1
FIELD_SW	Switch odd/even field for TV scaling	32h	1
FLDS	Field sync selector (odd or even)	09h	1
FLDSEN	Enabling field sync selection	09h	1
FMDRP[1:0]	Frame drop enable	0Eh	1
FPD	Full power down	04h	1
FSCSPP[18:0]	Sub-carrier frequency adjustment value	46h – 48h	1

Name	Description	Address	Page
GC1[6:0]	A value of AX+B on G channel	39h	1
GC2[7:0]	B value of AX+B on G channel	3Ah	1
GCKOFF	Indicator whether input GCLK is on or off	06h	1
GKD[1:0]	Graphics clock delay selection	73h	1
GKDEN	Graphics clock delay enable	72h	1
GSEL	Graphics clock selection	55h	1
HAI[10:0]	Input total active pixels per line	0Fh, 10h	1
HAO[10:0]	Output total active pixels per line	1Bh, 1Ch	1
HEND[10:0]	Horizontal end position for image zoom feature	27h, 29h	1
HFLIP	Horizontal flip	2Dh	1
HFLN_EN	Enable half line difference for TV scaling	32h	1
HIGH	Non-multiplexed input data alignment	0Ch	1
HO[10:0]	Input horizontal sync offset value	12h, 13h	1
HOO[10:0]	Output horizontal sync offset value	1Eh, 1Fh	1
HP[11:0]	Horizontal position adjustment value	35h – 36h	1
HPO_I	Input HS polarity	07h	1
HPO_O	Output HS polarity	07h	1
HREPT	Enable repeat mode for horizontal scaling	0Fh	1
HST[10:0]	Horizontal start position for image zoom feature	27h, 28h	1
HTI[10:0]	Input total pixels per line	0Fh, 11h	1
HTO[10:0]	Output total pixels per line	1Bh, 1Dh	1
HUE[6:0]	HUE adjustment value	2Eh	1
HVAUTO	Using self countered timing values	0Fh	1
HW[10:0]	Input horizontal sync width	12h, 14h	1
HWO[10:0]	Output horizontal sync width	1Eh, 20h	1
IDF[3:0]	Input data format	0Ch	1
IMGZOOM	Image zoom feature enable	27h	1
INTEN	Drop vertical sync every one fame	07h	1
INTLACE	Interlaced input indicator	0Bh	1
LNSEL[1:0]	The number of line used for vertical scaling selection	09h	1
MASKEN	Masking data during horizontal or vertical position adjustment	2Dh	1
MEMIDLE	Reset SDRAM to IDLE state	06h	1
MEMINIT	Reset SDRAM to initialization state	06h	1
MEMPD	Memory deep power enable	05h	1
MLKINV	Memory buffer latching clock inversion	75h	1
MONOB	Mono output enable	3Dh	1
MULTI[1:0]	Multiplexed input type selection	0Bh	1
PBPREN	YPBPR output enable	0Dh	1
PDIO	IO buffer power down bit	05h	1
PDMIO	Memory IO buffer power down bit	05h	1
PDPLL[1:0]	PLL power down bits	04h	1
PLL1CP[1:0]	PLL1 charge pump trimming	70h	1
PLL1N1[2:0]	PLL1 pre-divider ratio control	52h	1
PLL1N2[2:0]	PLL1 feedback divider 2 control	52h	1
PLL1N3[2:0]	PLL1 feedback divider 3 control	53h	1
PLL2N5[2:0]	PLL2 post-divider ratio control	53h	1
PLL3N6[1:0]	PLL3 pre-divider ratio control	54h	1
PLL3N7	PLL3 to DPCK divider 7 ratio control	54h	1
PLL3N8[1:0]	PLL3 to DPCK divider 8 ratio control	54h	1
POS3X[1:0]	3x input data position select	0Bh	1
RC1[6:0]	A value of AX+B on R channel	37h	1
RC2[7:0]	B value of AX+B on R channel	38h	1
RGBEN	Enable RGB output of SDTV	32h	1
RGBNC	Bypass RGB in backend for SDTV RGB output	08h	1

Name	Description	Address	Page
RESETDB	Device reset	02h	1
REVERSE	Input data is LSB first	0Bh	1
RFLOPEN	Rotation control	06h	1
ROTATE[1:0]	Rotation selection	2Dh	1
SAT[6:0]	Saturation control value	2Fh	1
SCREQ[26:0]	Value for calculate sub-carrier frequency from crystal	42h – 45h	1
SDPD	SDRAM power bit	04h	1
SDSEL[2:0]	SDRAM settings selection	49h	1
SEL_R	Single or double termination selection	77h	1
SPPSNS	DAC detection enable	7Dh	1
STOP	Stop signal	06h	1
SWAP[2:0]	Swapping bit for RGB sequence	0Ch	1
SWP_PAPB	P0a or P0b first selector	0Eh	1
SWP_YC	Swap YC for BT656 input	0Eh	1
SWRDIM	Enable immediately switch bank for SDRAM reading	06h	1
SYNCS[3:0]	Swap the output sync	08h	1
SYO	Enabling sync output	09h	1
TCAC[1:0]	Setting for SDRAM	4Ah	1
TDD[2:0]	Setting for SDRAM	4Ch	1
TDPL[1:0]	Setting for SDRAM	4Ch	1
TE[2:0]	Text enhancement	32h	1
TEBP	Text enhance bypass	3Eh	1
TMRD[1:0]	Setting for SDRAM	4Ch	1
TRAS[3:0]	Setting for SDRAM	4Bh	1
TRC[3:0]	Setting for SDRAM	4Bh	1
TRCD[2:0]	Setting for SDRAM	4Ah	1
TRP[2:0]	Setting for SDRAM	4Ah	1
UKINV	UCLK inversion	75h	1
UVBP[1:0]	Filter pass enable on C channel	3Fh	1
V18_25B	1.8 or 2.5v memory buffer voltage indicator	76h	1
VAI[10:0]	Input total active lines per frame	15h, 16h	1
VAO[10:0]	Output total active lines per frame	21h, 22h	1
VEND[10:0]	Vertical end position for image zoom feature	2Ah, 2Bh	1
VFFSPP[2:0]	Vertical scaling filter selection	3Dh	1
VFLIP	Vertical flip	2Dh	1
VFMT[3:0]	Output video format	0Dh	1
VID[7:0]	Revision ID	01h	1
VO[10:0]	Input vertical sync offset	18h, 19h	1
VOO[10:0]	Output vertical sync offset	24h, 25h	1
VP[11:0]	Vertical position adjustment value	33h –34h	1
VPO_I	Input VS polarity	07h	1
VPO_O	Output VS polarity	07h	1
VRTM[1:0]	IO differential mode vref trimming	76h	1
VSINV	Inversion for VSYNC signal of CPU interface	0Eh	1
VST[10:0]	Vertical start position for image zoom feature	2Ah, 2Bh	1
VTI[10:0]	Input total lines per frame	15h, 17h	1
VTO[10:0]	Output total lines per frame	21h, 23h	1
VW[10:0]	Input vertical sync width	18h, 19h	1
VWO[10:0]	Output vertical sync width	24h, 26h	1
WEBINV	Inversion for WEB signal of CPU interface	0Eh	1
WRFAST	Frame write fast indicator	0Dh	1
XCH	Multiplexed and non-multiplex clock selector	55h	1
XSEL	Using external crystal as reference to generate sub-carrier	41h	1
XTAL[3:0]	Crystal frequency selection	41h	1

Name	Description	Address	Page
YC2RGB	YCbCr to RGB output enable	0Dh	1
YCFRT[3:0]	The weight of bypassed Luma component of CVBS Luma output	42h	1
YCV[2:0]	CVBS Luma filter select	3Eh	1
YFBP[4:0]	Filter bypass on Y channel	3Fh	1
YSFRT[3:0]	The weight of bypassed Luma component of S-video Luma output	46h	1
YSV[2:0]	S-Video Luma filter select	40h	1
YUVBPEN	YUV bypass enable	0Dh	1

3.2 Control Registers Map

Table 12: Serial Port Register Map (Page 1)

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
01h	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
02h						RSA	RESETIB	RESETDB
03h								PG
04h	PDPLL[1]	PDPLL[0]	DACPD[2]	DACPD[1]	DACPD[0]	SDPD	DPD	FPD
05h						MEMPD	PDMIO	PDIO
06h	GCKOFF			RFLOPEN	SWRDIM	MEMIDLE	MEMINIT	STOP
07h		INTEN	DEPO_O	HPO_O	VPO_O	DEPO_I	HPO_I	VPO_I
08h	RGBNC	CSSEL[2]	CSSEL[1]	CSSEL[0]	SYNCS[3]	SYNCS[2]	SYNCS[1]	SYNCS[0]
09h	LNSEL[1]	LNSEL[0]			SYO	DES	FLDS	FLDSEN
0Ah		CBS_SV[1]	CBS_SV[0]	DACS[1]	DACS[0]	DACSP[2]	DACSP[1]	DACSP[0]
0Bh	INTLACE	CPUEN	POS3X[1]	POS3X[0]	MULTI[1]	MULTI[0]	AH_LB	REVERSE
0Ch	HIGH	SWAP[2]	SWAP[1]	SWAP[0]	IDF[3]	IDF[2]	IDF[1]	IDF[0]
0Dh	WRFAST	PBPREN	YC2RGB	YUVBPEN	VFMT[3]	VFMT[2]	VFMT[1]	VFMT[0]
0Eh	CSBINV	VSINV	WEBINV	SWP_YC	SWP_PAPB	DNSMPEN	FMDRP[1]	FMDRP[0]
0Fh	HVAUTO	HREPT	HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
10h	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
11h	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
12h			HW[10]	HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
13h	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
14h	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
15h			VTI[10]	VTI[9]	VTI[8]	VAI[10]	VAI[9]	VAI[8]
16h	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
17h	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
18h			VW[10]	VW[9]	VW[8]	VO[10]	VO[9]	VO[8]
19h	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
1Ah	VW[7]	VW[6]	VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
1Bh			HTO[10]	HTO[9]	HTO[8]	HAO[10]	HAO[9]	HAO[8]
1Ch	HAO[7]	HAO[6]	HAO[5]	HAO[4]	HAO[3]	HAO[2]	HAO[1]	HAO[0]
1Dh	HTO[7]	HTO[6]	HTO[5]	HTO[4]	HTO[3]	HTO[2]	HTO[1]	HTO[0]
1Eh			HWO[10]	HWO[9]	HWO[8]	HOO[10]	HOO[9]	HOO[8]
1Fh	HOO[7]	HOO[6]	HOO[5]	HOO[4]	HOO[3]	HOO[2]	HOO[1]	HOO[0]
20h	HWO[7]	HWO[6]	HWO[5]	HWO[4]	HWO[3]	HWO[2]	HWO[1]	HWO[0]
21h			VTO[10]	VTO[9]	VTO[8]	VAO[10]	VAO[9]	VAO[8]
22h	VAO[7]	VAO[6]	VAO[5]	VAO[4]	VAO[3]	VAO[2]	VAO[1]	VAO[0]
23h	VTO[7]	VTO[6]	VTO[5]	VTO[4]	VTO[3]	VTO[2]	VTO[1]	VTO[0]
24h			VWO[10]	VWO[9]	VWO[8]	VOO[10]	VOO[9]	VOO[8]
25h	VOO[7]	VOO[6]	VOO[5]	VOO[4]	VOO[3]	VOO[2]	VOO[1]	VOO[0]
26h	VWO[7]	VWO[6]	VWO[5]	VWO[4]	VWO[3]	VWO[2]	VWO[1]	VWO[0]
27h	IMGZOOM		HEND[10]	HEND[9]	HEND[8]	HST[10]	HST[9]	HST[8]
28h	HST[7]	HST[6]	HST[5]	HST[4]	HST[3]	HST[2]	HST[1]	HST[0]
29h	HEND[7]	HEND[6]	HEND[5]	HEND[4]	HEND[3]	HEND[2]	HEND[1]	HEND[0]
2Ah			VEND[10]	VEND[9]	VEND[8]	VST[10]	VST[9]	VST[8]
2Bh	VST[7]	VST[6]	VST[5]	VST[4]	VST[3]	VST[2]	VST[1]	VST[0]
2Ch	VEND[7]	VEND[6]	VEND[5]	VEND[4]	VEND[3]	VEND[2]	VEND[1]	VEND[0]
2Dh				MASKEN	VFLIP	HFLIP	ROTATE[1]	ROTATE[0]
2Eh		HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Fh		SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
30h		CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
31h	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
32h	RGBEN	HFLN_EN	FIELD_SW			TE[2]	TE[1]	TE[0]
33h					VP[11]	VP[10]	VP[9]	VP[8]
34h	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]	VP[1]	VP[0]
35h					HP[11]	HP[10]	HP[9]	HP[8]
36h	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]	HP[1]	HP[0]
37h		RC1[6]	RC1[5]	RC1[4]	RC1[3]	RC1[2]	RC1[1]	RC1[0]
38h	RC2[7]	RC2[6]	RC2[5]	RC2[4]	RC2[3]	RC2[2]	RC2[1]	RC2[0]
39h		GC1[6]	GC1[5]	GC1[4]	GC1[3]	GC1[2]	GC1[1]	GC1[0]
3Ah	GC2[7]	GC2[6]	GC2[5]	GC2[4]	GC2[3]	GC2[2]	GC2[1]	GC2[0]
3Bh		BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
3Ch	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
3Dh	MONOB		CBW			VFFSPP[2]	VFFSPP[1]	VFFSPP[0]
3Eh	DBP	TEBP		AFLTBP		YCV[2]	YCV[1]	YCV[0]
3Fh	CFBP	UVBP[1]	UVBP[0]	YFBP[4]	YFBP[3]	YFBP[2]	YFBP[1]	YFBP[0]
40h	YSV[2]	YSV[1]	YSV[0]		DOTB	BSTADJ[2]	BSTADJ[1]	BSTADJ[0]
41h	XSEL	XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]	ACIV		
42h	YCFRT[3]	YCFRT[2]	YCFRT[1]	YCFRT[0]		SCREQ[26]	SCREQ[25]	SCREQ[24]
43h	SCREQ[23]	SCREQ[22]	SCREQ[21]	SCREQ[20]	SCREQ[19]	SCREQ[18]	SCREQ[17]	SCREQ[16]
44h	SCREQ[15]	SCREQ[14]	SCREQ[13]	SCREQ[12]	SCREQ[11]	SCREQ[10]	SCREQ[9]	SCREQ[8]
45h	SCREQ[7]	SCREQ[6]	SCREQ[5]	SCREQ[4]	SCREQ[3]	SCREQ[2]	SCREQ[1]	SCREQ[0]
46h	YSFRT[3]	YSFRT[2]	YSFRT[1]	YSFRT[0]		FSCSPP[18]	FSCSPP[17]	FSCSPP[16]
47h	FSCSPP[15]	FSCSPP[14]	FSCSPP[13]	FSCSPP[12]	FSCSPP[11]	FSCSPP[10]	FSCSPP[9]	FSCSPP[8]
48h	FSCSPP[7]	FSCSPP[6]	FSCSPP[5]	FSCSPP[4]	FSCSPP[3]	FSCSPP[2]	FSCSPP[1]	FSCSPP[0]
49h	SDSEL[3]	SDSEL[2]	SDSEL[1]	SDSEL[0]				
4Ah	TRP[2]	TRP[1]	TRP[0]	TRCD[2]	TRCD[1]	TRCD[0]	TCAC[1]	TCAC[0]
4Bh	TRAS[3]	TRAS[2]	TRAS[1]	TRAS[0]	TRC[3]	TRC[2]	TRC[1]	TRC[0]
4Ch		TDD[2]	TDD[1]	TDD[0]	TMRD[1]	TMRD[0]	TDPL[1]	TDPL[0]
4Dh	A1[31]	A1[30]	A1[29]	A1[28]	A1[27]	A1[26]	A1[25]	A1[24]
4Eh	A1[23]	A1[22]	A1[21]	A1[20]	A1[19]	A1[18]	A1[17]	A1[16]
4Fh	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
50h	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
51h	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]
52h			PLL1N2[2]	PLL1N2[1]	PLL1N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
53h		DPCKN4	PLL2N5[2]	PLL2N5[1]	PLL2N5[0]	PLL1N3[2]	PLL1N3[1]	PLL1N3[0]
54h				PLL3N8[1]	PLL3N8[0]	PLL3N7	PLL3N6[1]	PLL3N6[0]
55h				XCH	BPSEL	DPSEL[1]	DPSEL[0]	GSEL
72h								GKDEN
73h			MLKD[1]	MLKD[0]			GKD[1]	GKD[0]
75h	MLKINV		DACKINV		UKINV			CKINV
76h				V18_25B	VRTM[1]	VRTM[0]	DIFFEN[1]	DIFFEN[0]
77h		SEL_R		DACG[1]	DACG[0]			
7Dh							DISPON	SPPSNS
7Eh					DVALID			
7Fh			DACAT2[1]	DACAT2[0]	DACAT1[1]	DACAT1[0]	DACAT0[1]	DACAT0[0]

3.3 Register Descriptions

Below are the descriptions for registers of the 1st page, which is accessible to the customer.

Device ID Register — Address: 00h

BIT:	7	6	5	4	3	2	1	0
SYMBOL	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAUL	0	1	0	1	0	1	0	1

DID[7:0] (bits 7-0) is the device ID. It is read-only and the value is 55h for Macrovision part CH7025. 54h for non-Macrovision part CH7026.

Revision ID Register — Address: 01h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

VID[7:0] (bits 7-0) is the revision ID.

Reset Register — Address: 02h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESETIB	RESETDB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

RSA (bit 2) resets the burst generation circuit. When RSA is '1', the circuit is reset. When RSA is '0' the circuit is enabled.

RESETIB (bit 1) resets all control registers. When RESETIB is '0' the control registers are reset to the default values. When RESETIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

RESETDB (bit 0) resets the datapath. When RESETDB is '0' the datapath is reset. When RESETDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

Page selection Register — Address: 03h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PG
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

PG (bit 0) is for page selection. This register is physically the same for both page 1 and page 2.

0: 1st page
1: 2nd page

Power state Register 1 Address: 04h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	PDPLL[1]	PDPLL[0]	DACPD[2]	DACPD[1]	DACPD[0]	SDPD	DPD	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

PDPLL[1] (bit 7) is power down control for PLL1 and PLL2. When high, PLL1 and PLL2 are powered down.

PDPLL[0] (bit 6) is power down control for PLL3. When high, PLL3 is powered down.

DACPD[2] (bit 5) is power down control for DAC1. When high, DAC3 is powered down.

DACPD[1] (bit 4) is power down control for DAC1. When high, DAC2 is powered down.

DACPD[0] (bit 3) is power down control for DAC0. When high, DAC1 is powered down.

SDPD (bit 2) is power down control for SDRAM and its control logic. When high, SDRAM and its control logic is powered down.

DPD (bit 1) is power down control for digital path. When DPD is “1”, digital path is powered down.

FPD (bit 0) controls the power on/off state. When FPD is “0”, the CH7025/CH7026 is in power-up state. When FPD is “1”, the CH7025/CH7026 is in power-down state. At power-down state, the CH7025/CH7026 accepts SPP access.

Power state Register 2 Address: 05h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reversed	Reversed	Reversed	Reversed	Reversed	MEMPD	PDMIO	PDIO
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

MEMPD (bit 2) is the memory power down enable bit. Once it’s high. SDRAM will enter into deep power down mode.

PDMIO (bit 1) is power down control for SDRAM I/O buffers. When high, SDRAM I/O buffers are powered down.

PDIO (bit 0) is power down control for I/O buffers. When high, I/O buffers are powered down.

SDRAM and Scaler enable Register Address: 06h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GCKOFF	Reversed	Reversed	RFLOPEN	SWRDIM	MEMIDLE	MEMINIT	STOP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	0	0	1	1

GCKOFF(bit 7) is to indicate whether input GCLK is off.

RFLOPEN(bit 4) is to enable rotation and flip to be implemented between writing frame buffer and reading frame buffer in back and forth mode. When input frame line is bigger than 720, then should disable the bit.

SWRDIM(bit3) is to enable immediately switch bank for SDRAM reading. When input frame line is bigger than 720, then should enable the bit.

MEMIDLE (bit 2) is to set SDRAM in IDLE state.

MEMINIT (bit 1) is to set SDRAM in initialization state. Once it goes low, initialization sequence is beginning.

STOP (bit 0) is to stop the scaler and SDRAM control operation. When it's high, these logics are stopped. This bit is required for programming the chip.

Sync configuration Register Address: 07h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reversed	INTEN	DEPO_O	HPO_O	VPO_O	DEPO_I	HPO_I	VPO_I
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	1	1	1

INTEN (bit 6) is to control if filtering out a sync every one video frame. If it is "1", sync signals will be generated every two frame. Otherwise, sync signals will be generated every frame.

DEPO_O (bit 5) is to indicate the polarity for output DE signal. When it is "1", the polarity of DE is high. Otherwise, the polarity is low.

HPO_O (bit 4) is to indicate the polarity for output H signal. When it is "1", the polarity of H is high. Otherwise, the polarity is low.

VPO_O (bit 3) is to indicate the polarity for output V signal. When it is "1", the polarity of V is high. Otherwise, the polarity is low.

DEPO_I (bit 2) is to indicate the polarity for input DE signal. When it is "1", the polarity of DE is high. Otherwise, the polarity is low.

HPO_I (bit 1) is to indicate the polarity for input H signal. When it is "1", the polarity of H is high. Otherwise, the polarity is low.

VPO_I (bit 0) is to indicate the polarity for input V signal. When it is "1", the polarity of V is high. Otherwise, the polarity is low.

SYNC output configuration Register Address: 08h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RGBNC	CSSEL[2]	CSSEL[1]	CSSEL[0]	SYNCS[3]	SYNCS[2]	SYNCS[1]	SYNCS[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

RGBNC(bit 7) is to bypass RGB in backend for SDTV RGB output.

CSSEL[2:0] (bit 6 – 4) is to select the composite sync type. Please refer to **Table 9**.

SYNCS[3] (bit 3) is to select the composite sync output or DE output. If it is "1", DE signal is selected. Otherwise composite sync is output.

SYNCS[2:0] (bit 2 – 0) is to swap the SYNC output sequence.

Table 13: SYNC output swapping sequence

SYNCS[2:0]	VS_O/CS	HS_O/CS	DE_O/CS
0	VSYNC	HSYNC	DE/CSYNC
1	VSYNC	DE/CSYNC	HSYNC
2	HSYNC	VSYNC	DE/CSYNC
3	HSYNC	DE/CSYNC	VSYNC

4	DE/CSYNC	VSYNC	HSYNC
5	DE/CSYNC	HSYNC	VSYNC

SYNC selection Register Address: 09h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LNSEL[1]	LNSEL[0]	Reserved	Reserved	SYO	DES	FLDS	FLDSEN
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

LNSEL[1:0] (bit 7 – 6) is to select the number of lines used for vertical scaling. Default is 0: 4 lines; 1: 3 lines; 2 or 3: 2 lines.

SYO (bit 3) is to enable generating internal sync to VGA controller. When it is "1", enable this feature.

DES (bit 2) is embedded sync selection signal. If the sync information is embedded into input data, this bit will be high.

FLDS (bit 1) is the even or odd field sync selection signal. When it is "0", the even field sync will be selected. Otherwise, the odd field sync is selected. This feature is available only when input is interlaced.

FLDSEN (bit 0) is used to enable the field sync selection feature described above. When it is "1", above feature is enabled.

DAC output configuration Register Address: 0Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	CBS_SV[1]	CBS_SV[0]	DACS[1]	DACS[0]	DACSP[2]	DACSP[1]	DACSP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CBS_SV[1:0] (bit 6 – 5) is to configure the single or multiple TV output feature. When is "00", triple output is enabled: When it is "01", single output is enabled; Otherwise, dual output is enabled.

DACS[1:0] (bit 4 – 3) is to configure the multiple TV output feature.

Table 14: Multiple TV output configuration

DACS[1:0]	Output
0	CVBS and S-Video output
1	Dual CVBS output
2	Triple CVBS output

DACSP[2:0] (bit 2 – 0) is to swap the DAC output sequence.

Table 15: DAC output swapping sequence

DACSP[2:0]	DAC0	DAC1	DAC2
0	R or Y	G or PB	B or PR
1	R or Y	B or PR	G or PB
2	G or PB	R or Y	B or PR
3	G or PB	B or PR	R or Y
4	B or PR	R or Y	G or PB
5	B or PR	G or PB	R or Y

Input data format Register 1 Address: 0Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	INTLACE	CPUEN	POS3X[1]	POS3X[0]	MULTI[1]	MULTI[0]	AH_LB	REVERSE
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

INTLACE (bit 7) is to indicate if the input is interlaced. Active high.

CPUEN (bit 6) is the enable signal for data transmitted through CPU interface. Once it's high, this feature is enabled.

POS3X[1:0] (bit 5 – 4) is to configure where the 3x input data is located in 24 bit data input pins. If it is "0", the lower 8 bits will be used; If it is "1", the middle 8 bits will be used; If it is "2", using the upper 8 bits.

MULTI[1:0] (bit 3 – 2) is to select the 1x, 2x or 3x input. When it is "0", input data is 1x: When it is "1", input data is 2x; When it is "2", input data is 3x.

AH_LB (bit 1) is to choose if multiplexed input data is aligned to higher or lower bits among D[23:0]. If it is "1", align to higher bits; If it is "0", align to lower bits.

REVERSIE (bit 0) is to choose if input data is MSB first or LSB first. If it is "1", input data is LSB first. Otherwise, input is MSB first.

Input data format Register 2 Address: 0Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HIGH	SWAP[2]	SWAP[1]	SWAP[0]	IDF[3]	IDF[2]	IDF[1]	IDF[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HIGH (bit 7) is to choose if the non multiplexed data is aligned to higher or lower bits among D[23:0]. When it is "1", data is aligned to higher bits. Otherwise, align to lower bits.

SWAP[2:0] (bit 6 – 4) is to swap the data input sequence. For details, please refer to **Table 7**.

IDF[3:0] (bit 3 – 0) is to configure the input data format. For details, please refer to **Table7**.

Table 16: Input data format

IDF[3:0]	Input data format (non-multiplexed)
0	RGB 888
1	RGB 666
2	RGB 565
3	RGB 555
4	RGB DVO
5	8-bit YCbCr 4:2:2
6	10-bit YCbCr 4:2:2
7	YCbCr 4:4:4
8	YCbCr 4:4:4 with embedded sync
9	Consecutive aligned 666 RGB input
10	Consecutive aligned 565 RGB input
11	Consecutive aligned 555 RGB input

Output video format Register Address: 0Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	WRFAST	PBPREN	YC2RGB	YUVBPEN	VFMT[3]	VFMT[2]	VFMT[1]	VFMT[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

WRFAST (bit 7) is to indicate the input frame rate is higher than output frame rate. Active high.

PBPREN (bit 6) is to enable the YPBPR output.

YC2RGB (bit 5) is to indicate YCbCr input mode. When it is "1", input data is YCbCr.

YUVBPEN (bit 4) is to indicate the TV bypass mode when input is YCbCr. Active high.

VFMT[3:0] is to select output format.

Table 17: Output format

VFMT[3:0]	Output format
0	NTSC_M
1	NTSC_J
2	NTSC_443
3	PAL_B/D/G/H/I
4	PAL_M
5	PAL_N
6	PAL_Nc
7	PAL_60
8	VGA out
9	VGA out (bypass scaler)
10	Sub-carrier output
11	DAC test output

MISC control Register Address: 0Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CSBINV	VSINV	WEBINV	SWP_YC	SWP_PAPB	DNSMPEN	FMDRP[1]	FMDRP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	0	0	0

CSBINV (bit 7) is to invert the CSB signal of CPU interface, active low.

VSINV (bit 6) is to invert the VSYNC signal of CPU interface, active low.

WEBINV (bit 5) is to invert the WEB signal of CPU interface, active low.

SWP_YC (bit 4) is to swap the YC signal under BT656 input.

SWP_PAPB (bit 3) is to select in 2x multiplexed input mode P0a is first or P0b is first.

DNSMPEN (bit 2) is to enable the 4:3 down sampling feature. Active high.

FMDRP[1:0] (bit 1 – 0) is the select the frame dropping rate.

Table 18: Fame dropping selection

DMDRP[1:0]	Dropping rate
0	Don't drop
1	2:1 drop
2	3:1 drop
3	4:1 drop

Input timing Register 1 Address: 0Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HVAUTO	HREPT	HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	1

HVAUTO (bit 7) is to select the self countered timing values. Active high.

HREPT(bit 6) is to enable repeat method for horizontal scaling.

HTI[10:8] (bits 5-3) combine with HTI[7:0] to define HTI[10:0], the Input Horizontal Total Pixels.

HAI[10:8] (bits 2-0) combine with HAI[7:0] to define HAI[10:0], the Input Horizontal Active Pixels.

Input timing Register 2 Address: 10h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HAI[7:0] (bits 7-0) combine with HAI[10:8] to define HAI[10:0], the Input Horizontal Active Pixels.

Input timing Register 3 Address: 11h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	1	1	0	1

HTI[7:0] (bits 7-0) combine with HTI[10:8] to define HTI[10:0], the Input Horizontal Total Pixels.

Input timing Register 4 Address: 12h

BIT:	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	HW[10]	HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAUL	0	0	0	0	0	0	0	0

HW[10:8] (bits 5-3) combine with HW[7:0] to define HW[10:0], the Input Horizontal Sync Width.

HO[10:8] (bits 2-0) combine with HO[7:0] to define HO[10:0], the Input Horizontal Sync Offset.

Input timing Register 5 Address: 13h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HO[7:0] (bits 7-0) combine with HO[10:8] to define HO[10:0], the Input Horizontal Sync Offset.

Input timing Register 6 Address: 14h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

HW[7:0] (bits 7-0) combine with HW[10:8] to define HW[10:0], the Input Horizontal Sync Width

Input timing Register 7 Address: 15h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VTI[10]	VTI[9]	VTI[8]	VAI[10]	VAI[9]	VAI[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

VTI[10:8] (bits 5-3) combine with VTI[7:0] to define VTI[10:0], the Input Vertical Total Pixels.

VAI[10:8] (bits 2-0) combine with VAI[7:0] to define VAI[10:0], the Input Vertical Active Pixels.

Input timing Register 8 Address: 16h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	0	0

VAI[7:0] (bits 7-0) combine with VAI[10:8] to define VAI[10:0], the Input Vertical Active Pixels.

Input timing Register 9 Address: 17h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	1	1	1	1

VTI[7:0] (bits 7-0) combine with VTI[10:8] to define VTI[10:0], the Input Vertical Total Pixels.

Input timing Register 10 Address: 18h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VW[10]	VW[9]	VW[8]	VO[10]	VO[9]	VO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VW[10:8] (bits 5-3) combine with VW[7:0] to define VW[10:0], the Input Vertical Sync Width.

VO[10:8] (bits 2-0) combine with VO[7:0] to define VO[10:0], the Input Vertical Sync Offset.

Input timing Register 11 Address: 19h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	0

VO[7:0] (bits 7-0) combine with VO[10:8] to define VO[10:0], the Input Vertical Sync Offset.

Input timing Register 12 Address: 1Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VW[7]	VW[6]	VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

VW[7:0] (bits 7-0) combine with VW[10:8] to define VW[10:0], the Input Horizontal Sync Width

Output timing Register 1 Address: 1Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	HTO[10]	HTO[9]	HTO[8]	HAO[10]	HAO[9]	HAO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	0	1	0	1

HTO[10:8] (bits 5-3) combine with HTO[7:0] to define HTO[10:0], the Output Horizontal Total Pixels.

HAO[10:8] (bits 2-0) combine with HAO[7:0] to define HAO[10:0], the Output Horizontal Active Pixels.

Output timing Register 2 Address: 1Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HAO[7]	HAO[6]	HAO[5]	HAO[4]	HAO[3]	HAO[2]	HAO[1]	HAO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	0	1	1	0

HAO[7:0] (bits 7-0) combine with HAO[10:8] to define HAO[10:0], the Output Horizontal Active Pixels.

Output timing Register 3 Address: 1Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HTO[7]	HTO[6]	HTO[5]	HTO[4]	HTO[3]	HTO[2]	HTO[1]	HTO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	0	1	0	0

HTO[7:0] (bits 7-0) combine with HTO[10:8] to define HTO[10:0], the Output Horizontal Total Pixels.

Output timing Register 4 Address: 1Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	HWO[10]	HWO[9]	HWO[8]	HOO[10]	HOO[9]	HOO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HWO[10:8] (bits 5-3) combine with HWO[7:0] to define HWO[10:0], the Output Horizontal Sync Width.

HOO[10:8] (bits 2-0) combine with HOO[7:0] to define HOO[10:0], the Output Horizontal Sync Offset.

Output timing Register 5 Address: 1Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HOO[7]	HOO[6]	HOO[5]	HOO[4]	HOO[3]	HOO[2]	HOO[1]	HOO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HOO[7:0] (bits 7-0) combine with HOO[10:8] to define HOO[10:0], the Output Horizontal Sync Offset.

Output timing Register 6 Address: 20h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HWO[7]	HWO[6]	HWO[5]	HWO[4]	HWO[3]	HWO[2]	HWO[1]	HWO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

HWO[7:0] (bits 7-0) combine with HWO[10:8] to define HWO[10:0], the Output Horizontal Sync Width

Output timing Register 7 Address: 21h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VTO[10]	VTO[9]	VTO[8]	VAO[10]	VAO[9]	VAO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	0	1

VTO[10:8] (bits 5-3) combine with VTO[7:0] to define VTO[10:0], the Output Vertical Total Pixels.

VAO[10:8] (bits 2-0) combine with VAO[7:0] to define VAO[10:0], the Output Vertical Active Pixels.

Output timing Register 8 Address: 22h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VAO[7]	VAO[6]	VAO[5]	VAO[4]	VAO[3]	VAO[2]	VAO[1]	VAO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	0	0	0

VAO[7:0] (bits 7-0) combine with VAO[10:8] to define VAO[10:0], the Output Vertical Active Pixels.

Output timing Register 9 Address: 23h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VTO[7]	VTO[6]	VTO[5]	VTO[4]	VTO[3]	VTO[2]	VTO[1]	VTO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	1	0	1

VTO[7:0] (bits 7-0) combine with VTO[10:8] to define VTO[10:0], the Output Vertical Total Pixels.

Output timing Register 10 Address: 24h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VWO[10]	VWO[9]	VWO[8]	VOO[10]	VOO[9]	VOO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VWO[10:8] (bits 5-3) combine with VWO[7:0] to define VWO[10:0], the Output Vertical Sync Width.

VOO[10:8] (bits 2-0) combine with VOO[7:0] to define VOO[10:0], the Output Vertical Sync Offset.

Output timing Register 11 Address: 25h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VOO[7]	VOO[6]	VOO[5]	VOO[4]	VOO[3]	VOO[2]	VOO[1]	VOO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	0

VOO[7:0] (bits 7-0) combine with VOO[10:8] to define VOO[10:0], the Output Vertical Sync Offset.

Output timing Register 12 Address: 26h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VWO[7]	VWO[6]	VWO[5]	VWO[4]	VWO[3]	VWO[2]	VWO[1]	VWO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

VWO[7:0] (bits 7-0) combine with VWO[10:8] to define VWO[10:0], the Output Horizontal Sync Width

Image zooming Register 1 Address: 27h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IMGZOOM	Reserved	HEND[10]	HEND[9]	HEND[8]	HST[10]	HST[9]	HST[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

IMGZOOM (bit 7) is to enable the image zoom feature. Active high.

HEND[10:8] (bit 5 – 3) combine with HEND[7:0] to define HEND[10:0], the Horizontal End position.

HST[10:8] (bit 2 – 0) combine with HST[7:0] to define HST[10:0], the Horizontal Start position.

Image zooming Register 2 Address: 28h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HST[7]	HST[6]	HST[5]	HST[4]	HST[3]	HST[2]	HST[1]	HST[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

HST[7:0] (bit 7 – 0) combine with HST[10:8] to define HST[10:0], the Horizontal Start position.

Image zooming Register 3 Address: 29h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HEND[7]	HEND[6]	HEND[5]	HEND[4]	HEND[3]	HEND[2]	HEND[1]	HEND[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

HEND[7:0] (bit 7 – 0) combine with HEND[10:8] to define HEND[10:0], the Horizontal End position.

Image zooming Register 4 Address: 2Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VEND[10]	VEND[9]	VEND[8]	VST[10]	VST[9]	VST[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

VEND[10:8] (bit 5 – 3) combine with VEND[7:0] to define VEND[10:0], the Vertical End position.

VST[10:8] (bit 2 – 0) combine with VST[7:0] to define VST[10:0], the Vertical Start position.

Image zooming Register 5 Address: 2Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VST[7]	VST[6]	VST[5]	VST[4]	VST[3]	VST[2]	VST[1]	VST[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

VST[7:0] (bit 7 – 0) combine with VST[10:8] to define VST[10:0], the Vertical Start position.

Image zooming Register 6 Address: 2Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VEND[7]	VEND[6]	VEND[5]	VEND[4]	VEND[3]	VEND[2]	VEND[1]	VEND[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	0	0	0

VEND[7:0] (bit 7 – 0) combine with VEND[10:8] to define VEND[10:0], the Vertical End position.

Image rotation and flip Register Address: 2Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	MASKEN	VFLIP	HFLIP	ROTATE[1]	ROTATE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

MASKEN (bit 4) is to mask the display when doing horizontal or vertical position adjustment.

VFLIP (bit 3) is the vertical flip bit.

HFLIP (bit 2) is the horizontal flip bit.

ROTATE[1:0] (bit 1 – 0) is the image rotation bit. When it is “00”, no rotation; When it is “01”, 90 degree rotation; When it is “10”, 180 degree rotation; When it is “11”, 270 degree rotation.

Hue adjustment Register Address 2Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HUE[6:0] (bits 6-0) define the TV Hue control HUE[6:0]. The adjusted angle in the color space is (HUE[6:0]-64)/2 degrees, positive angle is toward magenta color, negative angle is toward green color.

Saturation adjustment Register Address: 2Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

SAT[6:0] (bits 6-0) define the TV Color Saturation control SAT[6:0]. The Color Saturation is multiplied by SAT[6:0]/64.

Contrast adjustment Register — Address 30h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

CTA[6:0] (bits 6-0) define the TV contrast control CTA[6:0]. The Luma is multiplied by CTA[6:0]/64.

Brightness adjustment Register — Address 31h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

BRI[7:0] (bits 7-0) define the TV brightness control BRI[7:0]. The Brightness will be adjusted by (BRI[7:0]-128).

Text enhancement Register — Address 32h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RGBEN	HFLN_EN	FIELD_SW	Reserved	Reversed	TE[2]	TE[1]	TE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	0	1	0	0

RGBEN(bit 7) is to enable RGB output of TV format

HFLN_EN(bit 6) is to enable half line difference for TV scaling.

FIELD_SW(bit 5) is to switch odd/even field for TV scaling.

TE[2:0] (bits 2-0) define TV Sharpness control (Text Enhancement) TE[2:0]. TE[2:0]=100 means no enhancement. Larger setting than 100 boosts the high frequency band of the picture. Smaller setting than 100 smoothes the image.

Vertical position adjustment Register 1 — Address 33h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	VP[11]	VP[10]	VP[9]	VP[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

VP[11:8] (bits 3-0) combine with VP[7:0] to define the TV horizontal position adjustment VP[11:0].

Vertical position adjustment Register 2 — Address 34h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]	VP[1]	VP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VP[7:0] (bits 7-0) combine with VP[11:8] to define the TV vertical position adjustment VP[11:0]. The number of lines that is adjusted is determined by VP[11:0]-2048. If the value is positive, the picture is moved upward; if the value is negative, the picture is moved downward.

Horizontal position adjustment Register 1 — Address 35h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	HP[11]	HP[10]	HP[9]	HP[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

HP[11:8] (bits 3-0) combine with HP[7:0] to define the TV horizontal position adjustment HP[11:0].

Horizontal position adjustment Register 2 — Address: 36h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]	HP[1]	HP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HP[7:0] (bits 7-0) combine with HP[11:8] to define TV horizontal position adjustment HP[11:0]. The number of pixels that is adjusted is determined by HP[11:0]-2048. If the value is positive, the picture is moved to the right; if the value is negative, the picture is moved to the left.

AX + B adjustment Register 1 — Address: 37h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	RC1[6]	RC1[5]	RC1[4]	RC1[3]	RC1[2]	RC1[1]	RC1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

RC1[6:0] (bit 6 – 0) is the A value of AX/64+B on R channel.

AX + B adjustment Register 2 — Address: 38h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RC2[7]	RC2[6]	RC2[5]	RC2[4]	RC2[3]	RC2[2]	RC2[1]	RC2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

RC2[7:0] (bit 7 – 0) is the B value of AX/64+B on R channel. 2's complement.

AX + B adjustment Register 3 — Address: 39h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	GC1[6]	GC1[5]	GC1[4]	GC1[3]	GC1[2]	GC1[1]	GC1[6]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

GC1[6:0] (bit 6 – 0) is the A value of AX/64+B on G channel.

AX + B adjustment Register 4 — Address: 3Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GC2[7]	GC2[6]	GC2[5]	GC2[4]	GC2[3]	GC2[2]	GC2[1]	GC2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

GC2[7:0] (bit 7 – 0) is the B value of AX/64+B on G channel.

AX + B adjustment Register 5 — Address: 3Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

BC1[6:0] (bit 6 – 0) is the A value of AX/64+B on B channel.

AX + B adjustment Register 6 — Address: 3Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

BC2[7:0] (bit 7 – 0) is the B value of AX/64+B on B channel.

Filter setting Register 1 — Address: 3Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	MONOB	Reserved	CBW	Reserved	Reserved	VFFSPP[2]	VFFSPP[1]	VFFSPP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	1	0	0

MONOB (bit 7) is the display mono image. Active low.

CBW (bit 5) increases TV Chroma bandwidth, when CBW='1'; otherwise decrease the Chroma bandwidth.

VFFSPP[2:0] (bits 2-0) define the TV Adaptive Flicker Filter Control VFFSPP[2:0]. Allowed values are 0 to 6 (7 is reserved). Larger setting has stronger De-flicker effect. When VFFSPP is 7, VFC1 and VFC2 are used.

Filter setting Register 2 — Address: 3Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DBP	TEBP	Reserved	AFLTBP	Reserved	YCV[2]	YCV[1]	YCV[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	1	0	0

DBP (bit 7) is the dither function enable.

TEBP (bit 6) is the text enhancement function on VGA output.

AFLTBP (bit 4) is used to bypass the adaptive filter on RGB channel.

YCV[2:0] (bit 2 - 0) define the Composite Luma channel bandwidth control YCV[2:0]. YCV[2:0] can be set to 0, 1, 2, 3, 4, 5. Smaller YCV value results in higher Luma channel bandwidth.

Filter bypass register Address: 3Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CFBP	UVBP[1]	UVBP[0]	YFBP[4]	YFBP[3]	YFBP[2]	YFBP[1]	YFBP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CFBP (bit 7) bypasses TV Chroma filter, when CFBP='1'; otherwise enable the filter.

UVBP[1:0] (bits 6-5) is to bypass one or two UV component filter at bkend, when the corresponding bit is '1';otherwise pass the UV component filter.

YBP[4:0] (bits 4-0) is to bypass one or more Y component filter at bkend, when the corresponding bit is '1';otherwise pass the Y component filter.

Burst setting Register Address: 40h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	YSV[2]	YSV[1]	YSV[0]	Reserved	DOTB	BSTADJ[2]	BSTADJ[1]	BSTADJ[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

YSV[2:0] (bit 7 - 5) define the S-video Luma channel bandwidth control YSV[2:0]. YSV[2:0] can be set to 0, 1, 2, 3, 4, 5. Smaller YSV value results in higher Luma channel bandwidth.

DOTB (bit 3) enables TV Dot Crawl reduction when set to '1'. '0' disables Dot Crawl reduction.

BSTADJ[2:0] (bit 2 – 0) is the set the amplitude of burst.

Table 19: SDTV reference burst amplitude adjustment BSTADJ[2:0]

BSTADJ[2:0]	Function
PAL, PAL-Nc,	
111	-28mV
110	-14mV
000	Nominal
001	+14mV
010	+28mV
011	+42mV
100	+56mV
101	+70mV
NTSC-M,NTSC443	
111	-4 IRE
110	-2 IRE
000	Nominal
001	+2 IRE
010	+4 IRE
011	+6 IRE
100	+8 IRE
101	+10 IRE
PAL-M/N	
111	-28mV

110	-14mV
000	Nominal
001	+14mV
010	+28mV
011	+42mV
100	+56mV
101	+70mV
NTSC-J	
111	-4 IRE
110	-2 IRE
000	Nominal
001	+2 IRE
010	+4 IRE
011	+6 IRE
100	+8 IRE
01	+10 IRE

Sub-carrier generation method Register Address: 41h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XSEL	XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]	ACIV	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	0	0	1	0

XSEL (bit 7): whether the crystal frequency is predefined or not. When the crystal frequency is predefined, some registers, such as SCFREQ, will be calculated inside the chip to save programming effort.

1: using predefined values;
0: using other values.

XTAL[3:0] (bits 6 - 3): predefined crystal frequencies.

0: 3.6864MHz
1: 3.579545MHz
2: 4MHz
3: 12MHz
4: 13MHz
5: 13.5MHz
6: 14.318MHz
7: 14.7456MHz
8: 16MHz
9: 18.432MHz
10: 20MHz
11: 26MHz
12: 27MHz
13: 32MHz
14: 40MHz
15: 49MHz

ACIV(bit 2) controls whether the FSCI value is used to set the sub-carrier frequency, or the automatically calculated (CIV) value. When the ACIV value is '1', the number calculated and present at the SCFREQ registers will automatically be used as the increment value for sub-carrier generation. Whenever this bit is set to '1', the CFRB bit should be set to '0'.

Sub-carrier frequency setting Register 1 Address: 42h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	YCFRT[3]	YCFRT[2]	YCFRT[1]	YCFRT[0]	Reserved	SCREQ[26]	SCREQ[25]	SCREQ[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

YCFRT[3:0](bit 7-4) is to define the weight of bypassed Luma component of CVBS Luma output.

SCFREQ[26:24] (bit 2 – 0) combine with SCFREQ[23:16], SCFREQ[15:8], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 2 Address: 43h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[23]	SCREQ[22]	SCREQ[21]	SCREQ[20]	SCREQ[19]	SCREQ[18]	SCREQ[17]	SCREQ[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[23:16] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[15:8], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 3 Address: 44h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[15]	SCREQ[14]	SCREQ[13]	SCREQ[12]	SCREQ[11]	SCREQ[10]	SCREQ[9]	SCREQ[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[15:8] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 4 Address: 45h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[7]	SCREQ[6]	SCREQ[5]	SCREQ[4]	SCREQ[3]	SCREQ[2]	SCREQ[1]	SCREQ[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[7:0] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[15:8] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

SCFREQ = (Fsc / Fs) * (2 ^ 26)
Fsc, desired sub-carrier frequency, There are five values of sub-carrier frequency:

Sub-carrier frequency setting Register 5 Address: 46h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	YSFRT[3]	YSFRT[2]	YSFRT[1]	YSFRT[0]	Reserved	FSCSPP[18]	FSCSPP[17]	FSCSPP[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	0	0	0	0

YSFRT[3:0](bit 7-4) is to define the weight of bypassed Luma component of S-video Luma output.

FSCSPP[18:16] (bit 2 – 0) combines with FSCSPP[15:8] and FSCSPP[7:0] to adjust the SDTV sub-carrier frequency. The minimum adjustment step is 1.609 Hz. Total adjustment range is: -421.875 ~ 421.873 KHz.

Sub-carrier frequency setting Register 6 Address: 47h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FSCSPP[15]	FSCSPP[14]	FSCSPP[13]	FSCSPP[12]	FSCSPP[11]	FSCSPP[10]	FSCSPP[9]	FSCSPP[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

FSCSPP[15:8] (bit 7 – 0) combines with FSCSPP[18:16] and FSCSPP[7:0] to adjust the SDTV sub-carrier frequency.

Sub-carrier frequency setting Register 7 Address: 48h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FSCSPP[7]	FSCSPP[6]	FSCSPP[5]	FSCSPP[4]	FSCSPP[3]	FSCSPP[2]	FSCSPP[1]	FSCSPP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

FSCSPP[7:0] (bit 7 – 0) combines with FSCSPP[18:16] and FSCSPP[15:8] to adjust the SDTV sub-carrier frequency.

SDRAM setting Register 1 Address: 49h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SDSEL[3]	SDSEL[2]	SDSEL[1]	SDSEL[0]	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

SDSEL[3:0] (bit 7 – 4) is to select SDRAM settings.

SDRAM setting Register 2 Address: 4Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TRP[2]	TRP[1]	TRP[0]	TRCD[2]	TRCD[1]	TRCD[0]	TCAC[1]	TCAC[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	1	1	1	1

TRP[2:0] (bit 7 – 5) is the T_{RP} parameter of SDRAM.

TRCD[2:0] (bit 4 – 2) is the T_{RCD} parameter of SDRAM.

TCAC[1:0] (bit 1 – 0) is the T_{CAC} parameter of SDRAM.

SDRAM setting Register 3 Address: 4Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TRAS[3]	TRAS[2]	TRAS[1]	TRAS[0]	TRC[3]	TRC[2]	TRC[1]	TRC[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	1	0	1	0

TRAS[3:0] (bit 7 – 4) is the T_{RAS} parameter of SDRAM.

TRC[3:0] (bit 3 – 0) is the T_{RC} parameter of SDRAM.

SDRAM setting Register 4 Address: 4Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	TDD[2]	TDD[1]	TDD[0]	TMRD[1]	TMRD[0]	TDPL[1]	TDPL[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	1	0	1	0

TDD[2:0] (bit 6 – 4) is the T_{DD} parameter of SDRAM.

TMRD[1:0] (bit 3 – 2) is the T_{MRD} parameter of SDRAM.

TDPL[1:0] (bit 1 – 0) is the T_{DPL} parameter of SDRAM.

Digital divider settings Register 1 Address: 4Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[31]	A1[30]	A1[29]	A1[28]	A1[27]	A1[26]	A1[25]	A1[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	0	0	0

A1[31:24](bits7-0) combine with A1[23:16], A1[15:8] and A1[7:0] to define the clock divider for UCLK. A1[31:0] is calculated by the following equation:

$$A1 = (CLK_{out} * PLL1N1 * PLL2N5 * 2^{20})/CLK_{in}$$

The value of PLL1N1 and PLL2N2 will be described in register 52h. CLK_{in} is generally supposed to be input pixel clock (**GCLK**). A special condition is that if **GCLK** frequency is pretty low (< 1.5MHz) and a crystal or oscillator is presented on **XI/XO** pins of chip, CLK_{in} is equal to the frequency of crystal or oscillator. CLK_{out} is the clock used to drive output (TV or VGA).

Digital divider settings Register 2 Address: 4Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[23]	A1[22]	A1[21]	A1[20]	A1[19]	A1[18]	A1[17]	A1[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 3 Address: 4Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 4 Address: 50h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 5 Address: 51h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

A2[7:0](bit 7 - 0) is to define the clock divider for MCLK. The value of A2 is calculated by following equation:

$$A2 = (CLK_{in} * 2^{12})/(PLL1N1 * PLL3N6 * CLK_{out})$$

CLK_{in} is the same as what described in calculating A1 value in register 4Dh. CLK_{out} is supposed to the speed of SDRAM clock. **PLL3N6** will be described in register 54h. Based on above equation, the final results may not be an integer. So only the integer part of result will be used. If the remaining part or float part of above result is not zero, the integer part needs to be added by 1.

Analog divider setting Register 1 Address: 52h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	PLL1N2[2]	PLL1N2[1]	PLL1N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	1

PLL1N2[2:0] (bit 5 - 3): control the video PLL1 feedback-divider 1 value based on the following table. Other values are not allowed. For single edge rate (SDR) input mode, the value of PLL1N2 is equal to PLL1N1. For dual edge rate (DDR) input mode, PLL1N2 is equal to twice of PLL1N1.

PLL1N2 = PLL1N1 (SDR mode)
PLL1N2 = 2*PLL1N1 (DDR mode)

Table 20: Video PLL1 feedback-divider 1 settings

PLL1N2[2:0]	000	001	010	011	100	101
Post-divider	1	2	4	8	16	32

PLL1N1[2:0] (bit 2 – 0) control the pre-divider of PLL1. It makes sure that the frequency range input the PFD of PLL1 is from 2.3 to 4.6MHz. It must hold the following relationship:

$$2.3\ MHz \le (CLK_{in}/PLL1N1) \le 4.6\ MHz$$

CLKin here is the same as what described in calculating A1 value in register 4Dh. The ratio settings are based on following table:

Table 21: Video PLL1 pre-divider settings

PLL1N1[2:0]	000	001	010	011	100	101
Pre-divider	1	2	4	8	16	32

Analog divider setting Register 2 Address: 53h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DPCKN4	PLL2N5[2]	PLL2N5[1]	PLL2N5[0]	PLL1N3[2]	PLL1N3[1]	PLL1N3[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	1	0	0

DPCKN4 (bit 6) control the divider ratio for multiplexed input. When it is "1", ratio is 1/3; Otherwise ratio is 1/2. For 2x input mode, DPCKN4 is 0; For 3x input mode, DPCKN4 is 1.

PLL2N5[2:0] (bit 5 – 4)control the divider after the output from PLL2's VCO. The value is calculated from:

$$2.3\ MHz \le (CLK_{out} * PLL2N5)/64 \le 4.6MHz$$

CLKout is the same as what described in register 4Dh.

The value is based on the following table:

Table 22: Post divider settings ratio of PLL2

PLL2N5[2:0]	000	001	010	011	100	101
Post-divider	1	2	4	8	16	32

PLL1N3[2:0] (bit 2 - 0): control the video PLL1 feedback-divider 2 value based on the following table. Other values are not allowed. The calculation of PLL1N2 value must follow the equation:

$$PLL1N3 = 32/PLL1N2$$

Table 23: Video PLL1 feedback-divider 2 settings

PLL1N3[2:0]	000	001	010	011	100	101
Post-divider	1	2	4	8	16	32

Analog divider setting Register 3 Address: 54h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	PLL3N8[1]	PLL3N8[0]	PLL3N7	PLL3N6[1]	PLL3N6[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

PLL3N8[1:0] (bit 4 – 3) is the post divider 1 ratio after PLL3. The settings are based on following table:

Table 24: Post divider 1 settings of PLL3

PLL3N8[1:0]	00	01	10	11
Post-divider	1	2	4	8

PLL3N7 (bit 2) is the post divider 2 ratio after PLL3. When it is "1", ratio is 1/3;Otherwise 1/1.

The value of PLL3N7 and PLL3N8 can be determined flexibly. This is to derive a clock signal which is larger than the clock frequency (WEB) of CPU interface. The relationship is:

(CLKout*PLL3N6)/(PLL3N7*PLL3N8) > WEB

CLK_{out} is the SDRAM driving clock.

PLL3N6[1:0] (bit 1 – 0) is the post divider 3 ratio after PLL3. The value of PLL3N6 can be calculated by:

$$2.3\ MHz \le (CLK_{out} * PLL3N6)/64 \le 4.6MHz$$

CLK_{out} here is the SDRAM driving clock.

The settings are based on following table:

Table 25: Post divider 3 settings of PLL3

PLL3N6[1:0]	00	01	10	11
Post-divider	1	2	4	8

Clock selection Register Address: 55h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	XCH	BPSEL	DPSEL[1]	DPSEL[0]	GSEL
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	1	0	0

XCH (bit 4) is to select the pixel clock to driver digital logic. When under 2x or 3x multiplexed input mode, XCH is 1. Otherwise 0.

BPSEL (bit 3) is to select the TV bypass clock for BT656. For BT656 input mode, this bit is "1"; For other TV bypass mode, it is "0". Under 2x/3x input and TV bypass mode, BPSEL is 1. Otherwise 0.

DPSEL (bit 2 – 1) is to select the clock for analog latching. When it is "0x", select input pixel clock after PLL; When it is "10", select input G_CLK directly; When it is "11", select memory clock. When using CPU interface, DPSEL can not be 10B; When input G_CLK is lower than 2MHz, DPSEL must be 10B.

GSEL (bit 0) is to select the clock source for generating UCLK. When it is "1", select crystal; Otherwise select input G_CLK. When input G_CLK is lower than 2MHz and a crystal or oscillator (> 2.3MHz) is presented on XI/XO pins, GSEL needs to be 1, otherwise 0.

PLL charge pumping trimming Register Address: 70h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	R	Reserved	Reserved	Reserved	Reserved	Reserved	PLL1CP[1]	PLL1CP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	1	0	1

PLL1CP[1:0] (bits 1 – 0) control the video PLL1 charge pump current per the following table. Default value is 01.

Table 26: Video PLL1 Charge Pump trim settings

PLL3CP[1:0]	00	01	10	11
Current (Ua)	3	5.9	8.7	11.6

Clock delay enable Register Address: 72h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GKDEN
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

MLKD1[1:0] (bit 7 – 6) are small step delay (0.15ns each step) control bits for memory latching clock in memory output buffer.

Table 27: Small step delay selection for latching clock in memory output buffer

MLKD1 [1:0]	Delay (ns)
00	0.278
01	0.438
10	0.596
11	0.741

GKDEN (bit 0) is the delay enable for analog latching clock.

Clock delay configure Register 1 Address: 73h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	MLKD[1]	MLKD[0]	Reserved	Reserved	GKD[1]	GKD[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

MLKD[1:0] (bit 5 – 4) is to select the delay for latching clock in memory IO buffer.

Table 28: Delay selection for latching clock in memory buffer

MLKD [1:0]	Delay (ns)
00	0.405
01	0.904
10	1.402
11	1.892

GKD[1:0] (bit 1 – 0) is to select the delay for analog latching clock.

Table 29: Delay selection for analog latching clock

GKD [1:0]	Delay (ns)
00	2.25
01	2.90
10	3.50
11	4.08

Clock inversion Register — Address: 75h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	MLKINV	Reserved	DACKINV	Reserved	UKINV	Reserved	Reserved	CKINV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	0	0	0	0

MLKINV (bit 7) is to invert the latching clock in memory IO buffer.

DACKINV (bit 5) is to invert the DACCLK before DAC.

UKINV (bit 3) is to invert the UCLK.

CKINV (bit 0) is to invert the PCLK and PCLKX.

IO input setting Register — Address: 76h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	V18_25B	VRTM[1]	VRTM[0]	DIFFEN[1]	DIFFEN[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	1	0	0

V18_25B (bit 4) is to select the memory IO buffer voltage is 1.8v or 2.5v. When it is “0”, memory supply is 2.5v; Otherwise, 1.8v.

VRTM[1:0] (bit 1 – 0) control the trimming settings of the voltage reference generator

VRTM1	VRTM0	VREF
0	0	about 50% of VDDIO
0	1	about 60% of VDDIO
1	0	about 70% of VDDIO
1	1	about 80% of VDDIO

DIFFEN [1:0] (bit 1 – 0) enable the differential input mode of data and GCLK buffer. DIFFEN [1] is used to set data buffer, the other is for GCLK buffer

DAC trimming Register — Address: 77h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SEL_R	Reserved	DACG[1]	DACG[0]	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	1	1

SEL_R (bit 6) is to select the single or double termination.

DACG[1:0] (bits 4-3) control the DAC gain for different TV modes per the following table.

Table 30: DAC gain settings

DACG[1:0]	Output formats
00	NTSC-M, NTSC 443,PAL-M, PAL-N
01	PAL-B/D/G/H/K/I/Nc
11	NTSC-J
10	Reserved

Band-gap trimming Register — Address: 78h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	1	0

SDRAM test and DAC sense Register — Address: 7Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DISPON	SPPSNS
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DISPON (bit 1) is to select the clock source for DAC, if it is '1', select dcore backend clock, otherwise, select crystal clock.

SPPSNS (bit 0) is the DAC sense signal for connection detect.

SDRAM status Register — Address: 7Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	DVALID	Reserved	Reserved	Reserved
TYPE:	R	R	R	R	R	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DVALID (bit 3) is the read only bit. If it is "1", it will indicate that SDRAM has been initialized.

Attach display Register — Address: 7Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	DACAT2[1]	DACAT2[0]	DACAT1[1]	DACAT1[0]	DACAT0[1]	DACAT0[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

DACAT2[1:0] (bits 5-4) return attach information for DAC3 channel according to the table below.
DACAT1[1:0] (bits 3-2) return attach information for DAC2 channel according to the table below.
DACAT0[1:0] (bits 1-0) return attach information for DAC1 channel according to the table below.

Table 31: Attached Display Mapping

DACAT0[1:0]	Attached Display
00	No Attached Display
01	Connected
11	Short to ground
10	Reserved

4.0 Electrical specifications

4.1 Absolute maximum rating

Symbol	Description	Min	Typ	Max	Units
	All 1.8V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		2.5 5.0	V
	Input voltage of all digital pins (see note[3])	GND – 0.5		VDDIO+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-40		85	°C
T_{STOR}	Storage temperature	-40		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering			TBA	°C

Note:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce permanent damage.
3. The digital input voltage will follow the I/O supply voltage (VDDIO), the I/O supply voltage range is from 1.2V to 3.3V.

4.2 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	2.5	3.3	3.5	V
AVDD_DAC	DAC Power Supply Voltage	2.5	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.14		3.5	V
RL1	Output load to DAC Current Reference		1.2k		Ω
RL2	Output load to DAC Outputs		37.5		Ω
VDDQ_MEM	Memory data interface supply	2.375	2.5	2.625	V
		1.71(1)	1.8(1)	1.89(1)	
VDD_MEM	Memory core supply	2.375	2.5	2.625	V
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	2.5	3.3	3.5	V
	Ambient operating temperature	0		70	°C

Notes:
For SDRAM with 1.8V voltage supply

4.3 Electrical characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		38		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		30		mA
I_{VDD33} (1)	Total VDD33 supply current (3.3V supplies) (see note)		30		mA
I_{VDDQ}	Memory data interface supply current		0.1		mA
I_{VDD_MEM}	Memory core supply current		20		mA
I_{PD}	Total Power Down Current		<20		uA

Notes:
1. Applies for one DAC and single 75Ohm termination. The current of every DAC is less than 25mA for single termination and less than 50mA for double termination.
2. Some memories do not support deep power down mode.

4.4 Digital inputs / outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data I/O (1) High Voltage		VDDIO/2 +0.25		VDDIO + 0.5	V
V_{DATAIL}	Data I/O Low Voltage		GND-0.5		VDDIO/2-0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (2)		VDD33 – 0.5		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage (2)		GND-0.5		0.6	V
V_{SYNCOH}	Miscellaneous Output High Voltage (3)		VDD33 x 0.8			V
V_{SYNCOL}	Miscellaneous Output Low Voltage (3)				0.3	V
I_{MISCPU}	Miscellaneous Input Pull Up Current (2)	V_{IN} = 0	0.5		5.0	uA
I_{MISCPD}	Miscellaneous Input Pull Down Current (2)	V_{IN} = VDD33	0.1		1.1	uA

Notes:
1. Applies to D[23:0], GCLK, H, V and DE. VDDIO is the I/O supply, ranging from 1.2V to 3.3V.
2. Applies to AS, RESETB and ATPG.
3. Applies to HSO, VSO, CSYNC.

4.5 AC specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency		2.3		64	MHz
f_{GCLK}	Input (GCLK) frequency		1.5		120	MHz
DC_{GCLK}	Input (GCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{GJIT}	GCLK clock jitter tolerance			10		ns
t_S	Setup Time: D[23:0], H, V and DE to GCLK	GCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to GCLK	D[23:0], H, V, DE = Vref to GCLK	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

5.0 Package Dimensions

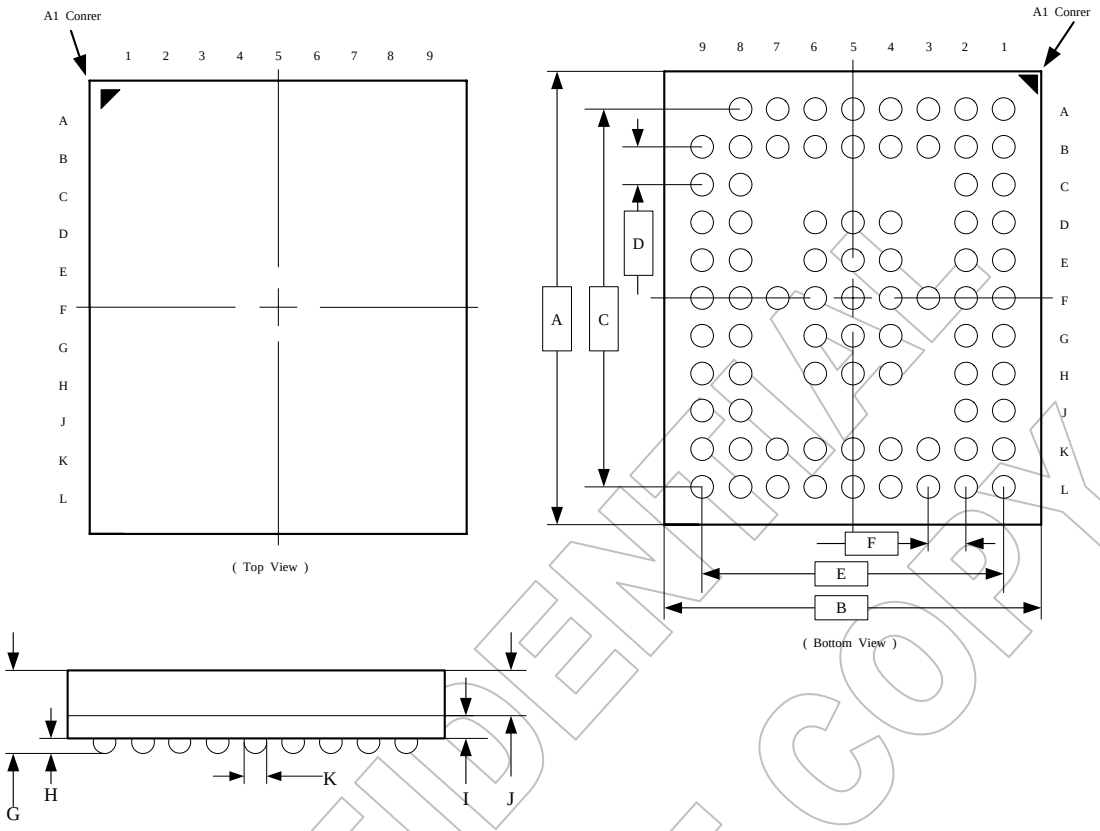

Figure 7: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

1. All dimensions conform to JEDEC standard MO-216.

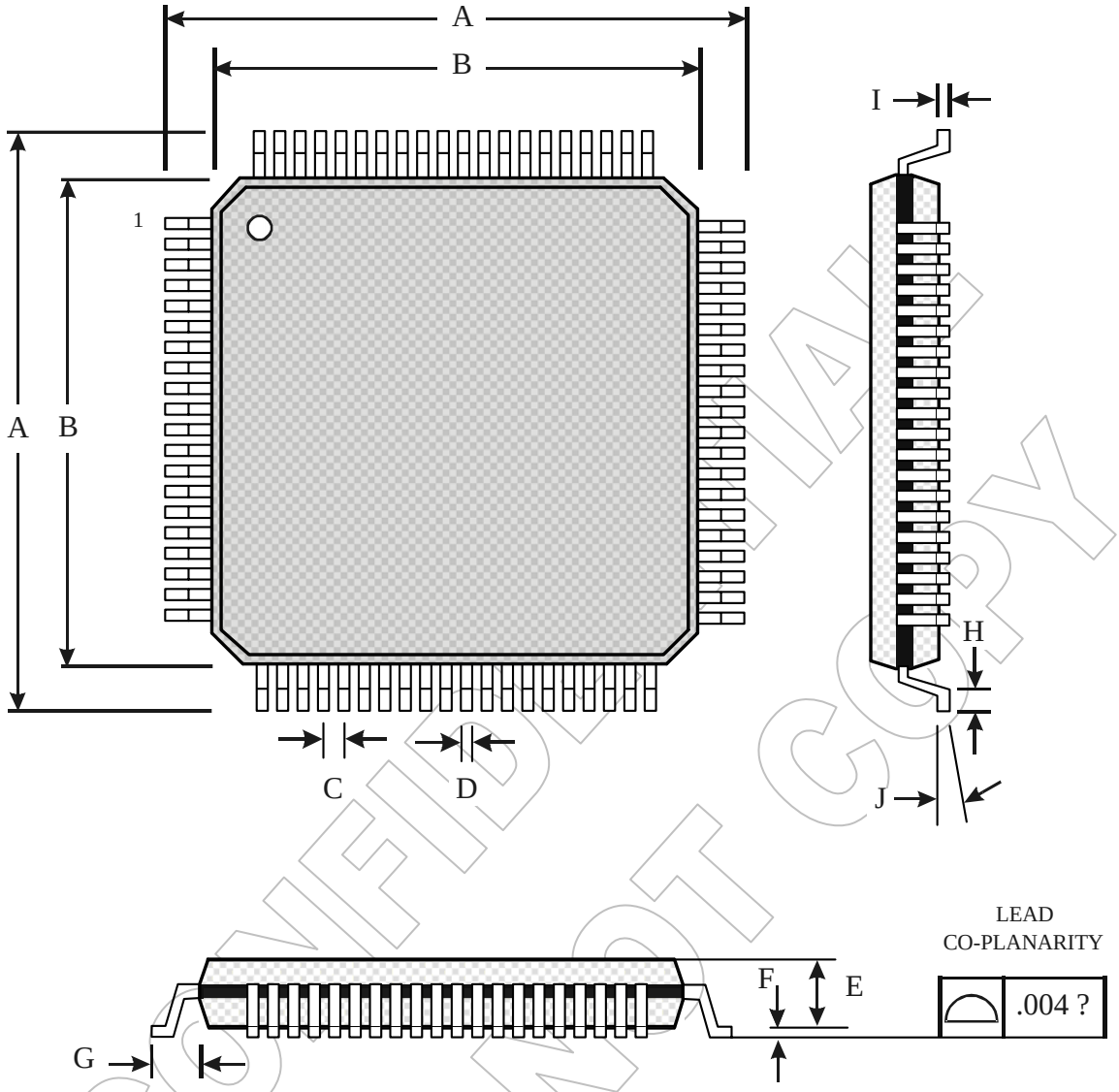

Figure 8: 80 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
80 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	11.90	9.90	0.40	0.13	1.35	0.05	1.00	0.45	0.09	0°
	MAX	12.10	10.10		0.23	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

6.0 Revision history

Rev. #	Date	Section	Description
0.1	12/19/2006	All	Initial preliminary release.
0.2	03/09/2007	Pin-out, package	Modified BGA pin-out, add the package dimensions.
0.2	03/09/2007	SDRAM power down	Add 2.4 SDRAM power down section
0.2	03/09/2007	Electrical spec, Register description	Adding index, table and figure list; modify electrical spec. Modified the range of VDDIO, VDD_MEM and VDDQ_MEM, modified some Register description
0.3	03/12/2007	Register Description	Add detailed Register Map and Description
0.4	06/06/2007	Register Map and Register Description	Modified some Register Map and Register description.
0.6	08/14/2007	Input date format, Register description	Add some input data format, add function test section, Add several register and their description. Modified the description of IDF5/6 and IDF9/10/11, Modified the formula of A1 and PLL3N6 calculation, Modified the description of DPSEL[1:0] register.
0.61	09/05/2007	All	Add CH7026 description. Update 4.1 Operating Temperature Add Ambient operating temperature to 4.2 Add Ordering Information.
0.62	09/14/2007	Title Pin-out, Register description, Electrical specifications	Change Title to CH7025/CH7026 SDTV/VGA Encoder. Add LQFP80 package type, Modified YC2RGB description, Change operate temperature to –40~85,
0.63	09/27/2007	Features & Description Figure 1 and Figure 3 4.3 Ordering Information	Update Features and General Description on Page1. Update Figure 1 and Figure 3. Update I_{VDDQ} and I_{VDD_MEM}. Add Part number for LQFP.

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ORDERING INFORMATION

Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7025A-GF	80TFBGA, Lead-free	Macrovision™	Commercial : 0 to 70°C
CH7025A-GFI	80TFBGA, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7025A-TF	80LQFP, Lead-free	Macrovision™	Commercial : 0 to 70°C
CH7025A-TFI	80LQFP, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7026A-GF	80TFBGA, Lead-free	None	Commercial : 0 to 70°C
CH7026A-GFI	80TFBGA, Lead-free	None	Industrial : -40 to 85°C
CH7026A-TF	80LQFP, Lead-free	None	Commercial : 0 to 70°C
CH7026A-TFI	80LQFP, Lead-free	None	Industrial : -40 to 85°C

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