K9XXG08UXM

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Document Title

1G x 8 Bit / 2G x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Feb. 1st 2005	Advance
0.1	1. Cycle time is changed from 35ns to 30ns 2. Technical note is changed.	Apr. 1st 2005	Advance
0.2	1. AC Para. tRHW deleted 2. the power recovery time of minmum is changed from 10μs to 100μs(p38)	Sept. 1. 2005	Advance
0.3	1. Leaded part is eliminated. 2. tR 50us -> 60us (p. 3,12,31) 3. tRHW, tCSD parameter is defined. 4. Technical note is added.(p.16)	Mar. 20th. 2006	Advance
0.4	1. Endurance is changed (10K->5K)	Apr. 20th 2006	Advance
0.5	1. Max. tPROG is changed (2ms->3ms)	Apr. 25th 2006	Advance
0.6	1. Address scramble is added (p.33) 2. Program/Erase Characteristics Note 3 is added(p.11)	June 30th 2006	Preliminary

1G x 8 Bit / 2G x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9G8G08U0M-P	2.7V ~ 3.6V	X8	TSOP1
K9G8G08U0M-I			52ULGA
K9LAG08U1M-I			

FEATURES

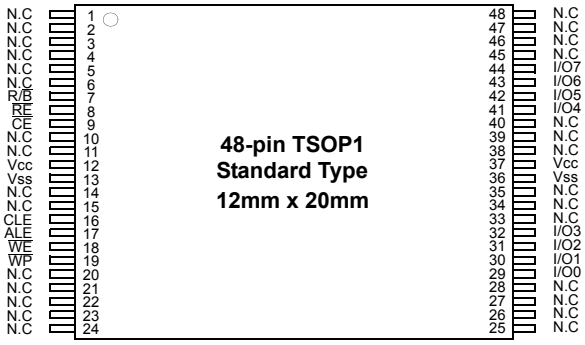
- Voltage Supply : 2.7 V ~ 3.6 V
- Organization
  - Memory Cell Array : (1G + 32M)bit x 8bit
  - Data Register : (2K + 64)bit x8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (256K + 8K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 60μs(Max.)
  - Serial Access : 30ns(Min.)
- Memory Cell : 2bit / Memory Cell
- Fast Write Cycle Time
  - Program time : 800μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 5K Program/Erase Cycles(with 4bit/512byte ECC)
  - Data Retention : 10 Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
  - K9G8G08U0M-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9G8G08U0M-ICB0/IIB0
    52 - Pin ULGA (12 x 17 / 1.00 mm pitch)
  - K9LAG08U1M-ICB0/IIB0
    52 - Pin ULGA (12 x 17 / 1.00 mm pitch)

GENERAL DESCRIPTION

Offered in 1Gx8bit, the K9G8G08U0M is a 8G-bit NAND Flash Memory with spare 256M-bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 800μs on the 2,112-byte page and an erase operation can be performed in typical 1.5ms on a (256K+8K)byte block. Data in the data register can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9G8G08U0M′s extended reliability of 5K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9G8G08U0M is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)

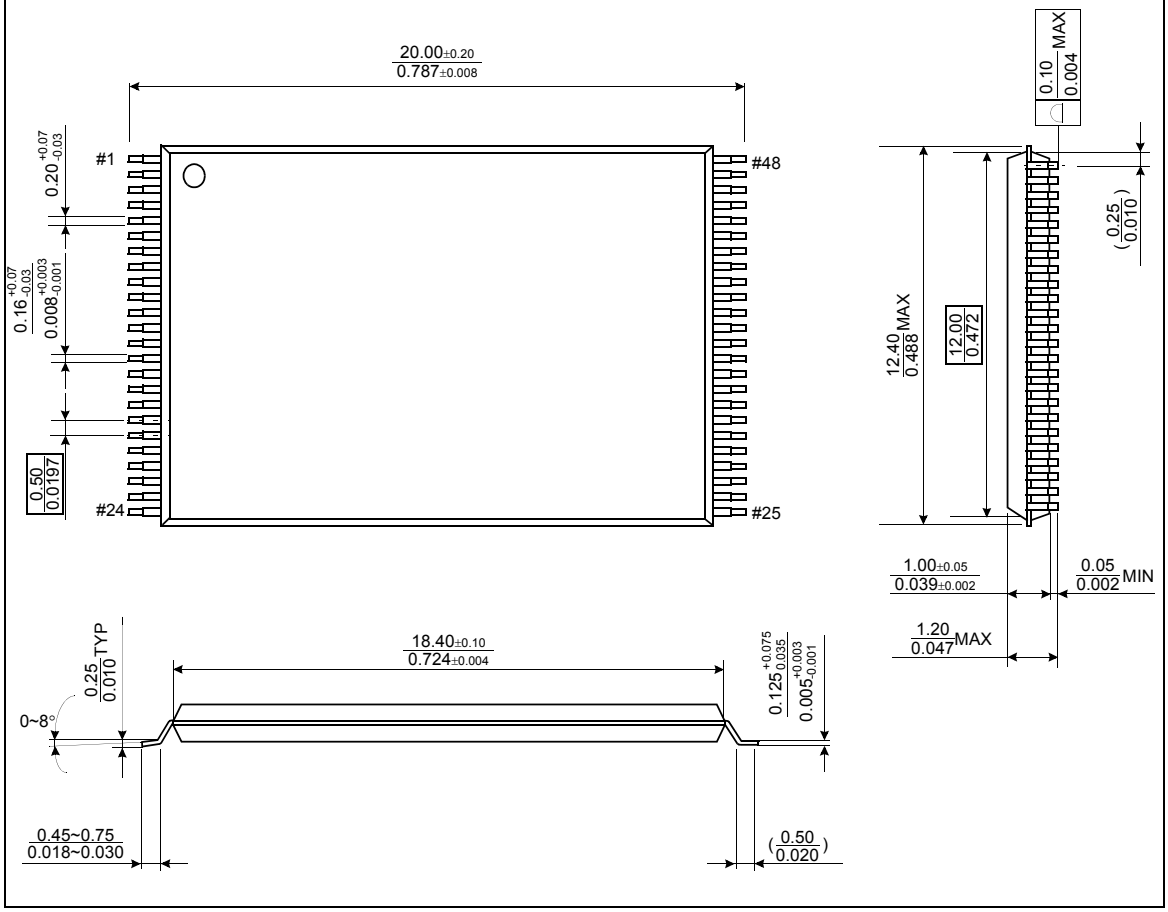
K9G8G08U0M-PCB0/PIB0



PACKAGE DIMENSIONS

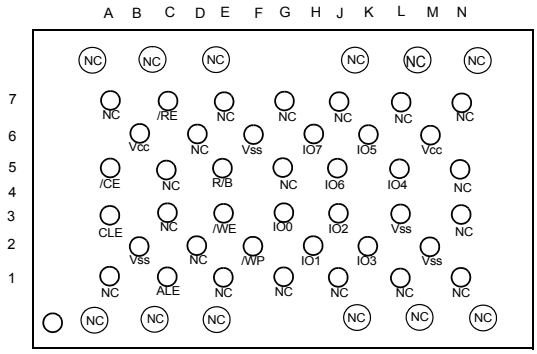
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



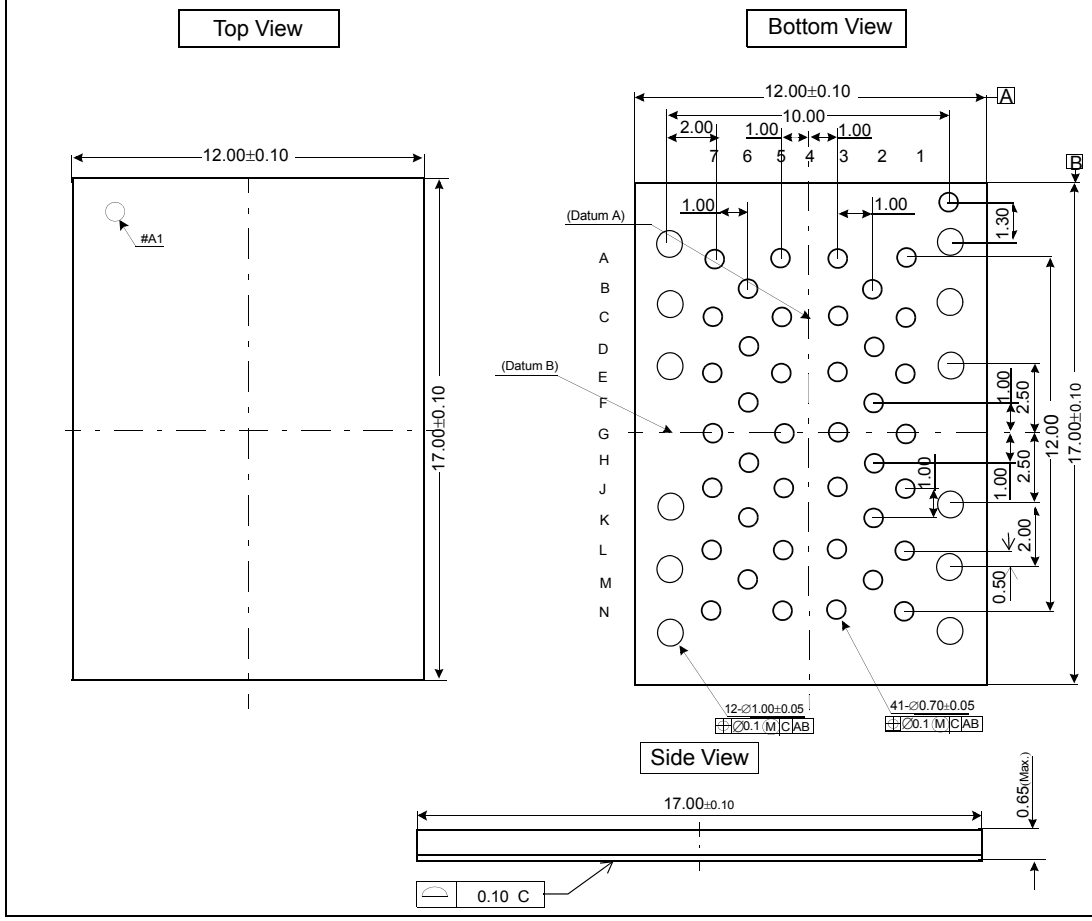
PIN CONFIGURATION (ULGA)

K9G8G08U0M-ICB0/IIB0

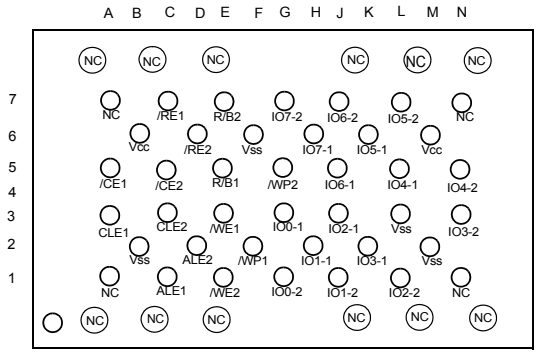


PACKAGE DIMENSIONS

52-ULGA (measured in millimeters)

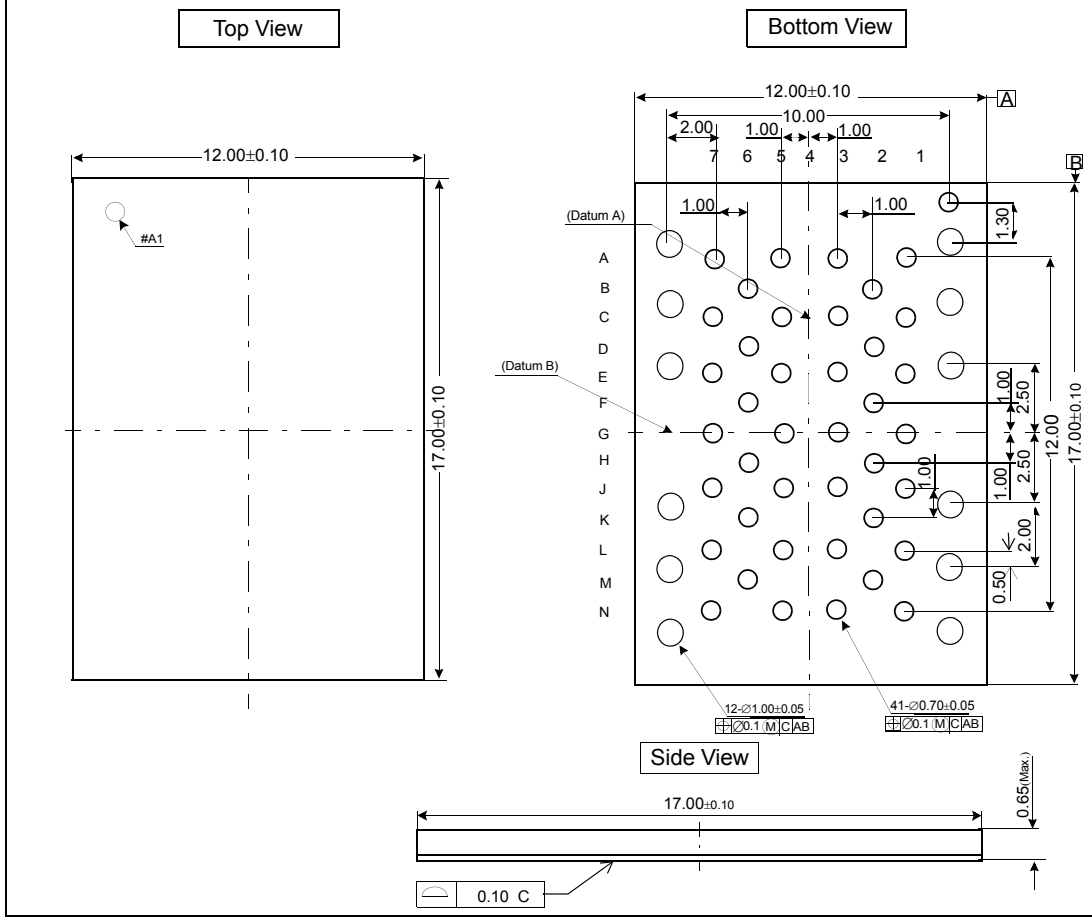


K9LAG08U1M-ICB0/IIB0



PACKAGE DIMENSIONS

52-ULGA (measured in millimeters)



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

Figure 1-1. K9G8G08U0M Functional Block Diagram

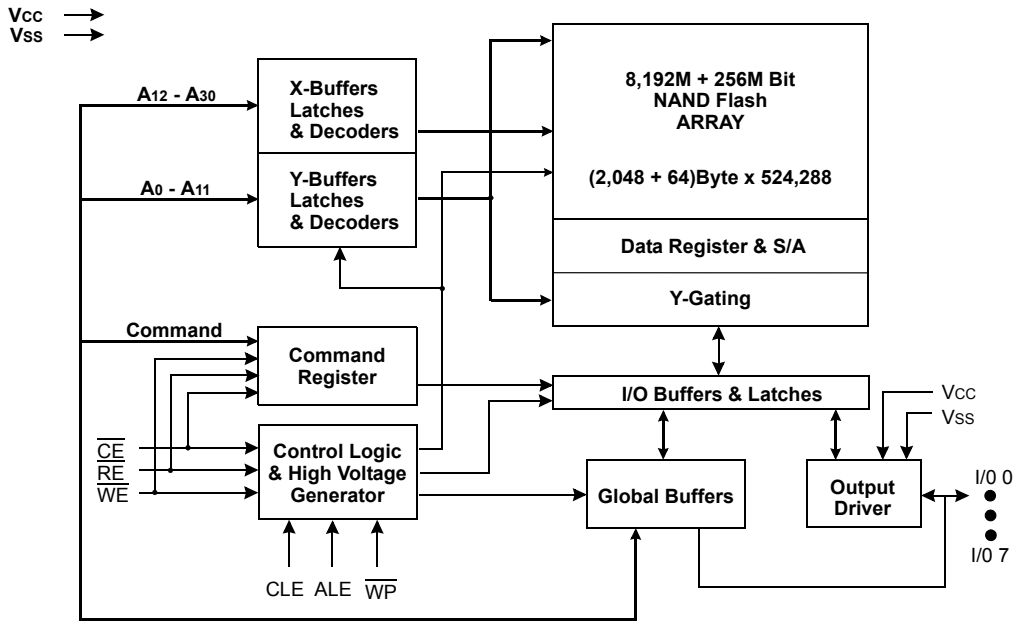
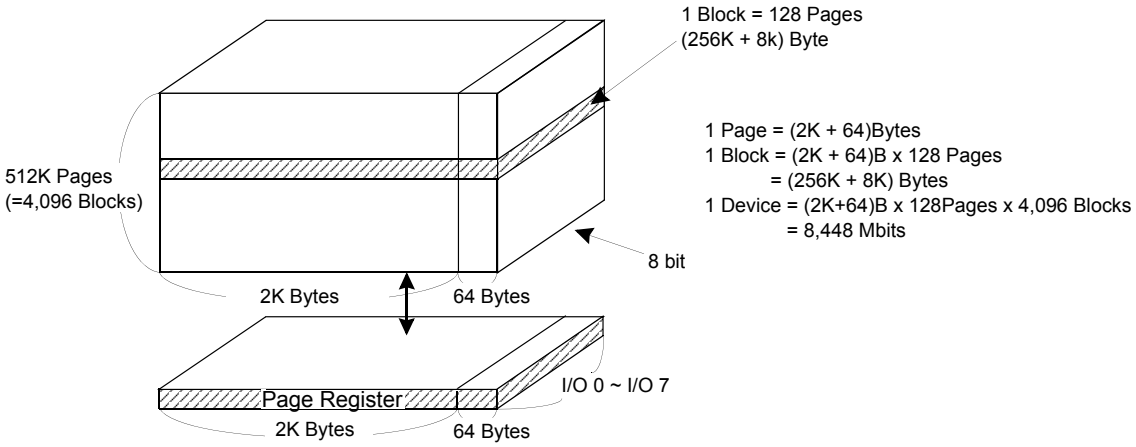


Figure 2-1. K9G8G08U0M Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	**Column Address**
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	**Row Address**
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	**Row Address**
5th Cycle	A28	A29	A30	*L	*L	*L	*L	*L	**Row Address**

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than required.

Product Introduction

The K9G8G08U0M is a 8,448Mbit(8,858,370,048 bit) memory organized as 524,288 rows(pages) by 2,112x8 columns. Spare 64 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. A cell has 2-bit data. Total 1,081,344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4,096 separately erasable 256K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9G8G08U0M.

The K9G8G08U0M has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 1G-byte physical space requires 30 addresses, thereby requiring five cycles for addressing : 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9G8G08U0M.

Table 1. Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Two-Plane Page Program (2)	80h----11h	81h----10h	
Block Erase	60h	D0h	
Two-Plane Block Erase	60h----60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Status	70h		O

NOTE : 1. Random Data Input/Output can be executed in a page.
2. Any command between 11h and 81h is prohibited except 70h and FFh.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		V_{IN}	-0.6 to + 4.6	
		$V_{I/O}$	-0.6 to Vcc+0.3 (<4.6V)	
Temperature Under Bias	K9XXG08UXM-XCB0	T_{BIAS}	-10 to +125	°C
	K9XXG08UXM-XIB0		-40 to +125	
Storage Temperature	K9XXG08UXM-XCB0	T_{STG}	-65 to +150	°C
	K9XXG08UXM-XIB0			
Short Circuit Current		Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9XXG08UXM-XCB0 :T_A=0 to 70°C, K9XXG08UXM-XIB0:T_A=-40 to 85°C)

Parameter	Symbol	K9XXG08UXM			Unit
		Min	Typ.	Max	
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	tRC=30ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	
	Erase	I_{CC3}	-	-	15	30	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Input High Voltage		V_{IH}(1)	-	0.8 x Vcc	-	Vcc+0.3	V
Input Low Voltage, All inputs		V_{IL}(1)	-	-0.3	-	0.2 x Vcc	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE :
1. VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25°C. Not 100% tested.
3. The typical value of the K9LAG08U1M's I_{SB2} is 20µA and the maximum value is 100µA.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
K9G8G08U0M	N_{VB}	3,996	-	4,096	Blocks
K9LAG08U1M	N_{VB}	7,992		8,192	Blocks

NOTE :
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3. The number of valid block is on the basis of single plane operations, and this may be decreased with two plane operations.

* : Each K9G8G08U0M chip in the K9LAG08U1M has Maximun 100 invalid blocks.

AC TEST CONDITION

(K9XXG08UXM-XCB0 :TA=0 to 70°C, K9XXG08UXM-XIB0:TA=-40 to 85°C)

Parameter	K9XXG08UXM
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(5clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(5clock)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎎	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.8	3	ms
Dummy Busy Time for Multi Plane Program	t_{DBSY}		0.5	1	μs
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	t_{BERS}	-	1.5	10	ms

NOTE
1. Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2. Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25°C temperature.
3. Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B(Table 2).
   Page Group A: Page 0, 1, 2, 3, 6, 7, 10, 11, ... , 110, 111, 114, 115, 118, 119, 122, 123
   Page Group B: Page 4, 5, 8, 9, 12, 13, 16, 17, ... , 116, 117, 120, 121, 124, 125, 126, 127

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}(1)	15	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
$\overline{CE}$ Setup Time	t_{CS}(1)	20	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	15	-	ns
ALE Setup Time	t_{ALS}(1)	15	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}(1)	15	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	30	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	-	ns
Address to Data Loading Time	t_{ADL}(2)	70(2)		ns

NOTES : 1. The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low.
2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	60	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	15	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	30	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	20	ns
$\overline{CE}$ Access Time	t_{CEA}	-	25	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	10	-	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	-	ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	ns
$\overline{CE}$ High to Output Hold	t_{COH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	10	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the last page of every initial invalid block has non-FFh data at the column address of 2,048.The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

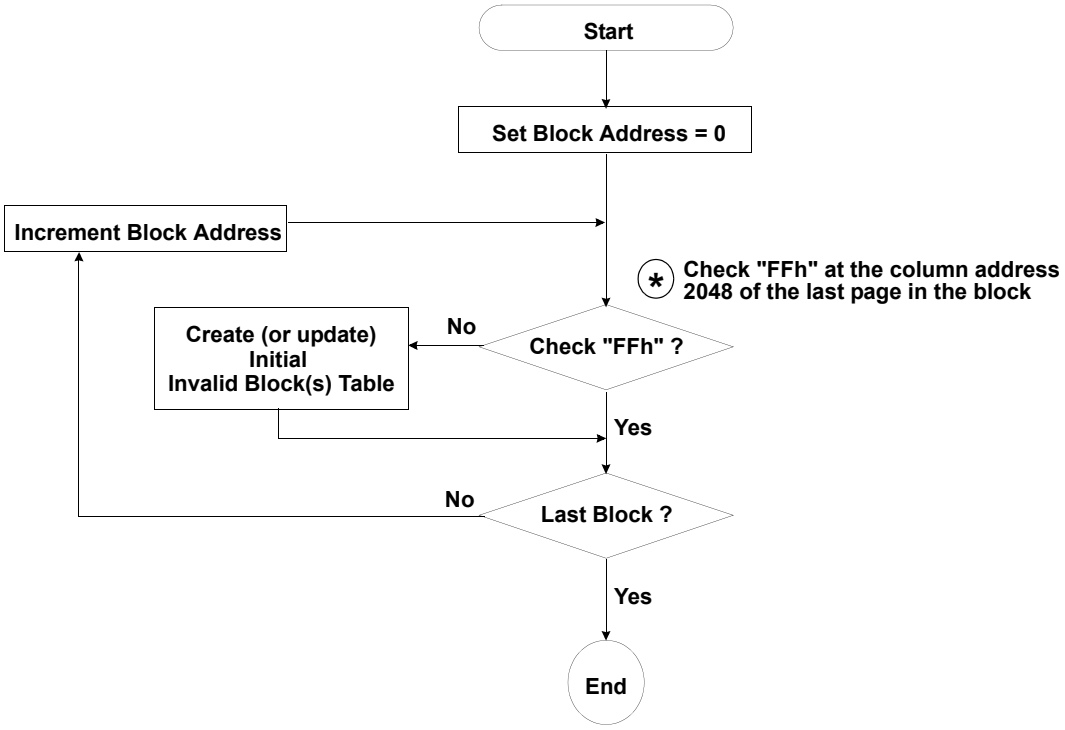


Figure 3. Flow chart to create initial invalid block table.

NAND Flash Technical Notes *(Continued)*

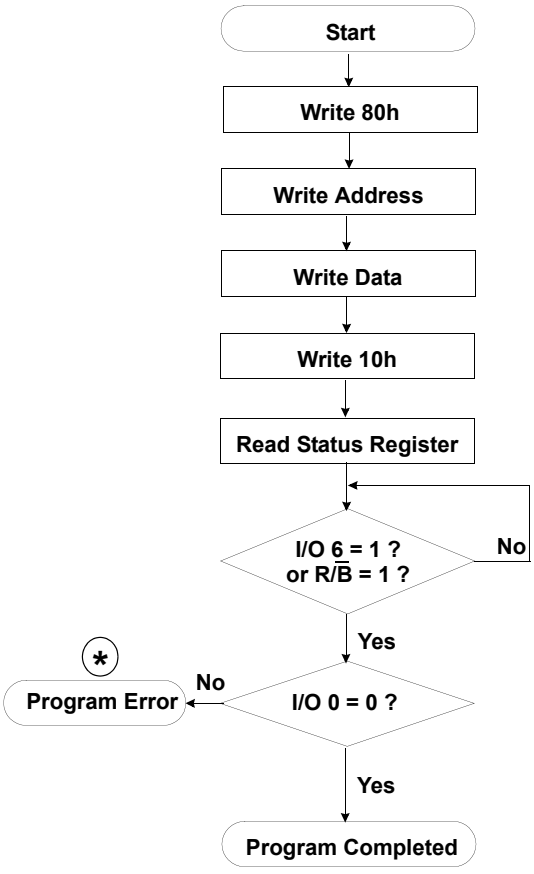
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to Four Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> RS Code etc.
Example) 4bit correction / 512-byte

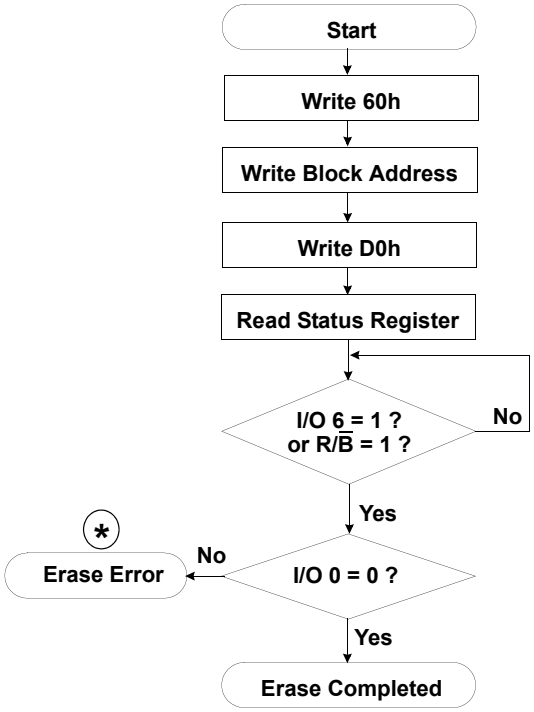
Program Flow Chart



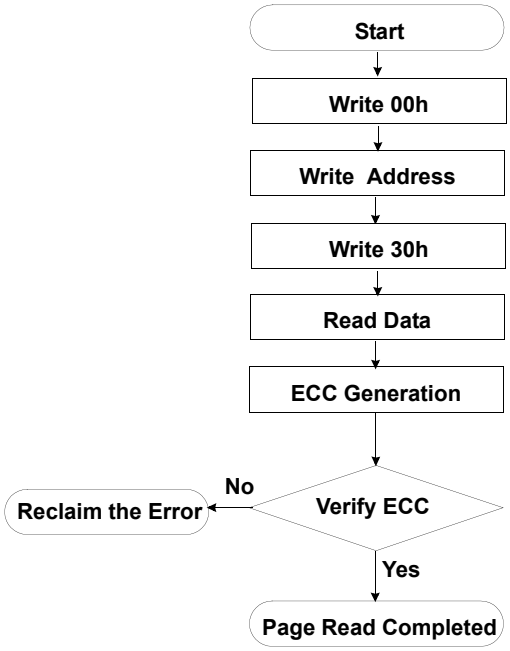
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

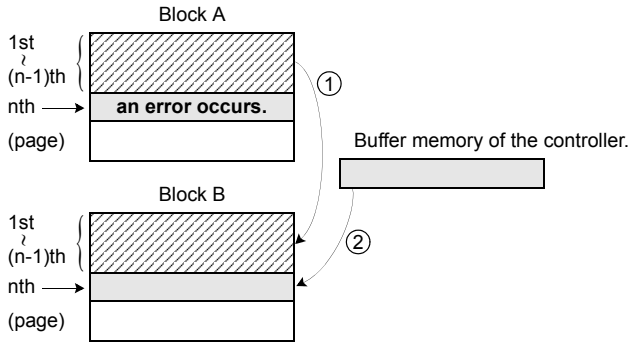


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement

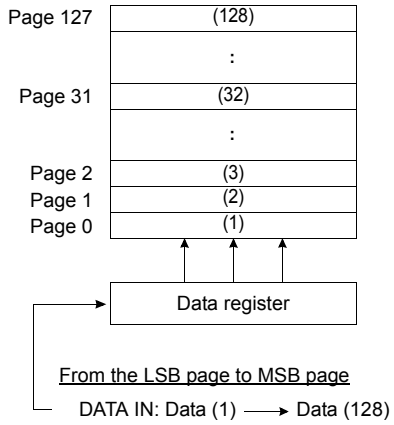


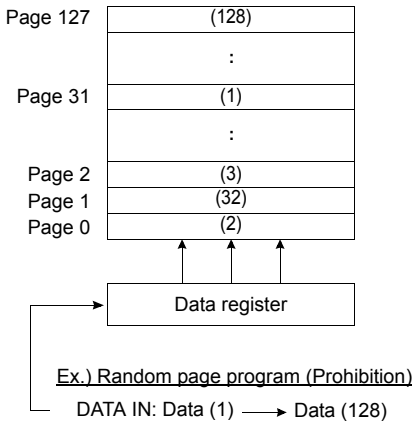
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

NAND Flash Technical Notes *(Continued)*

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.





System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.

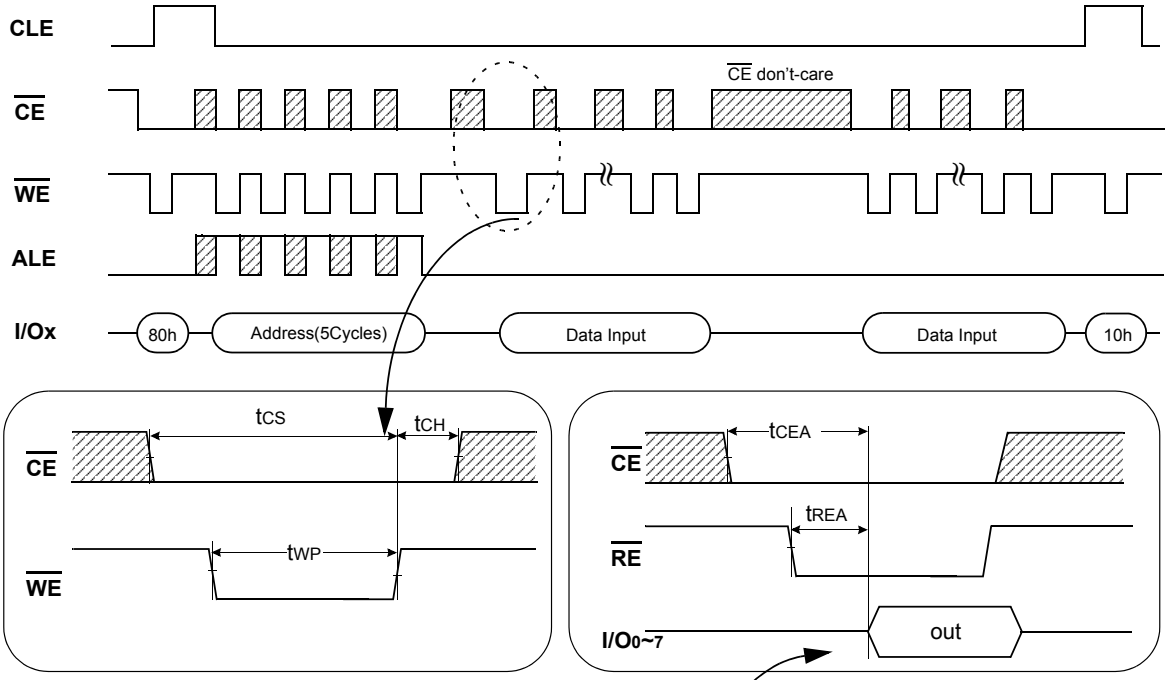
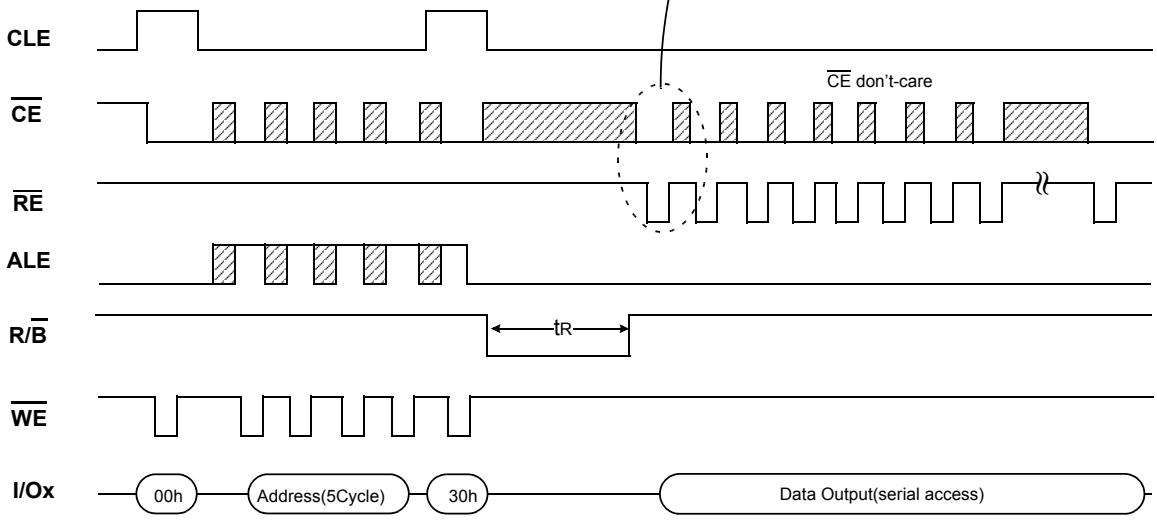


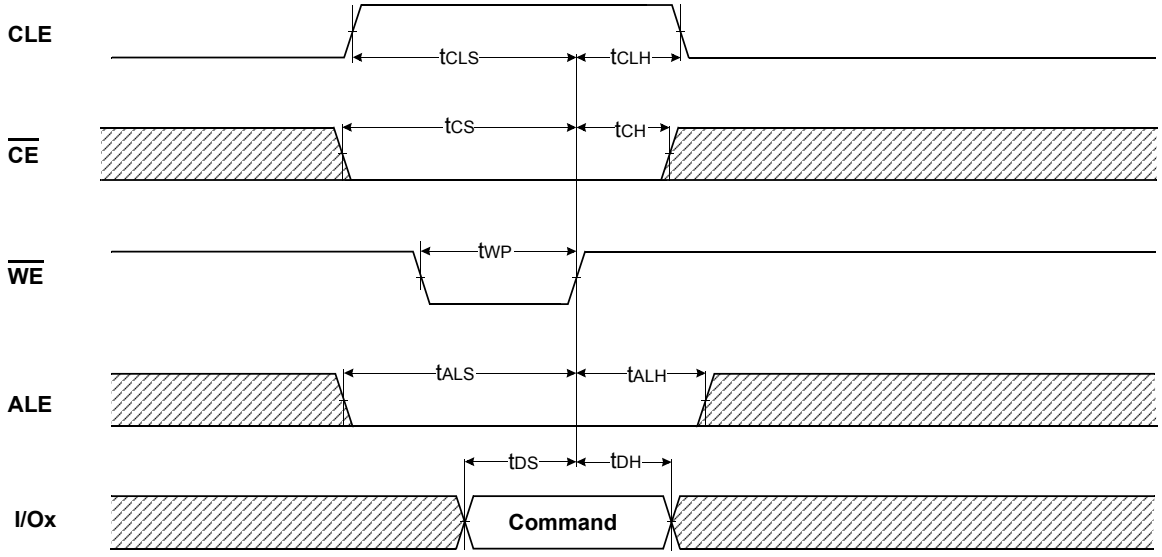
Figure 5. Read Operation with $\overline{CE}$ don't-care.



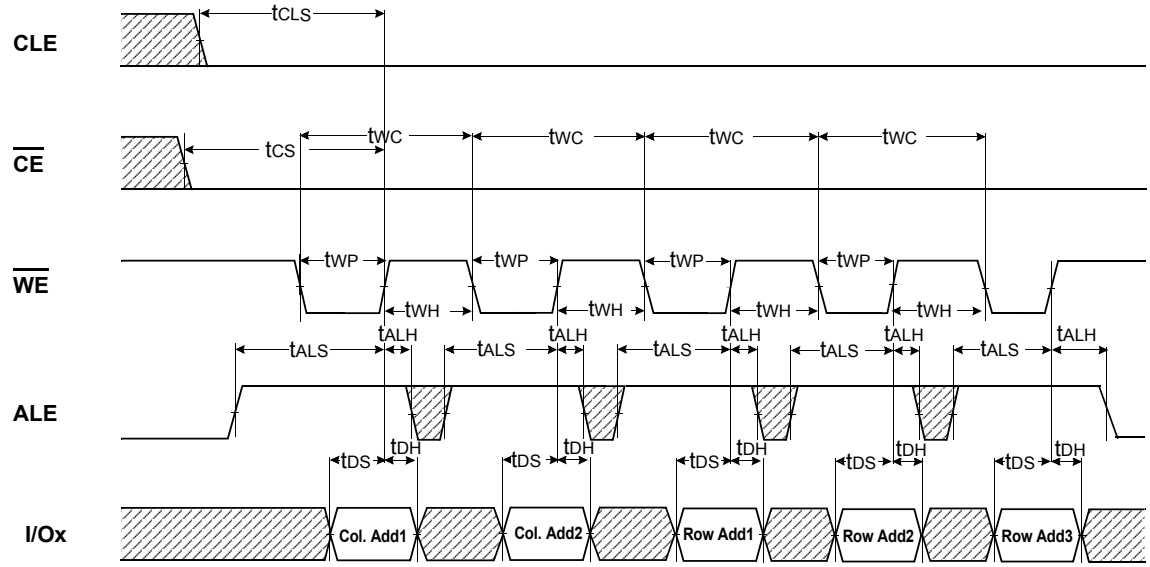
NOTE

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9G8G08U0M	I/O 0 ~ I/O 7	~2,112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A30

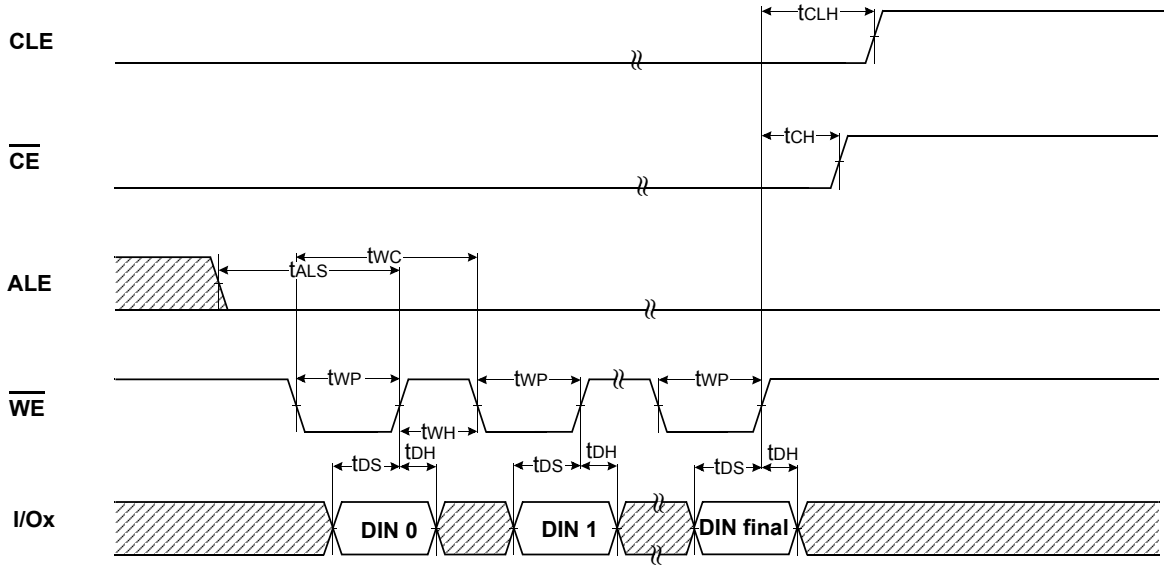
Command Latch Cycle



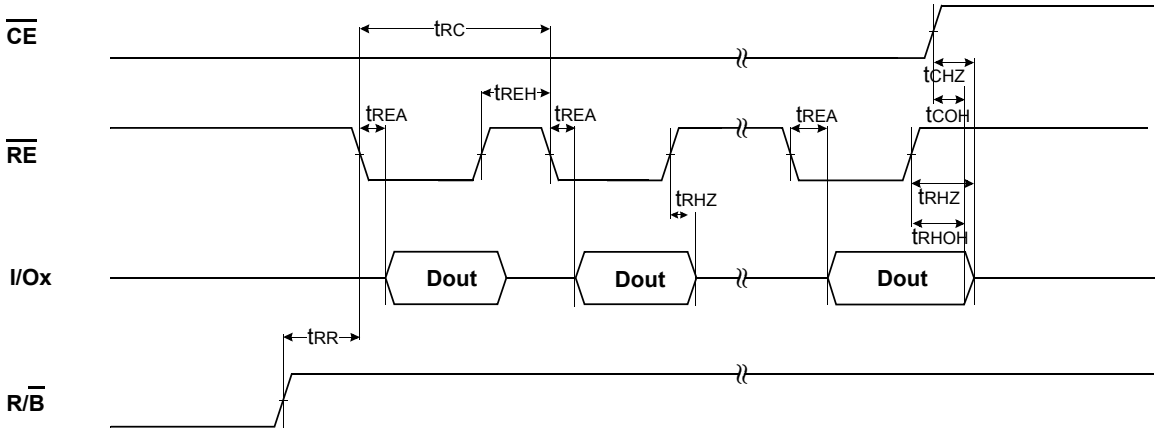
Address Latch Cycle



Input Data Latch Cycle

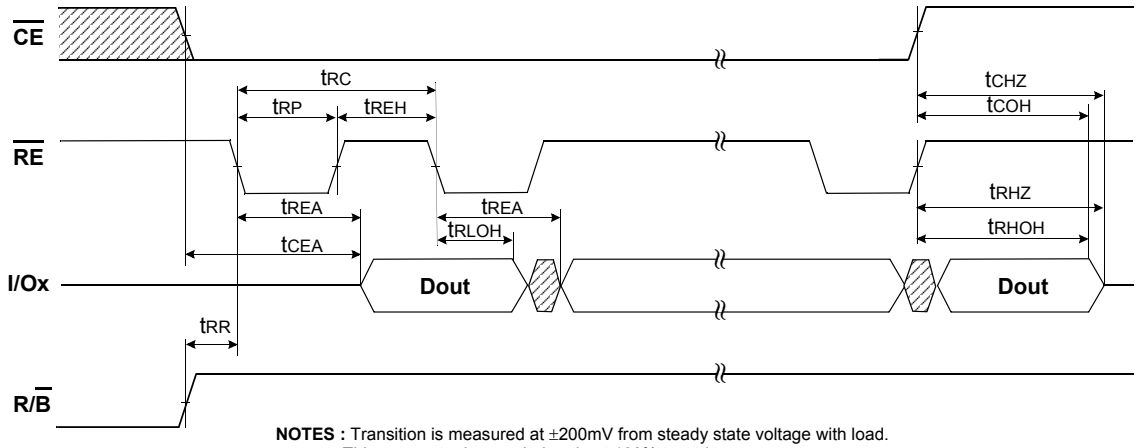


* Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)



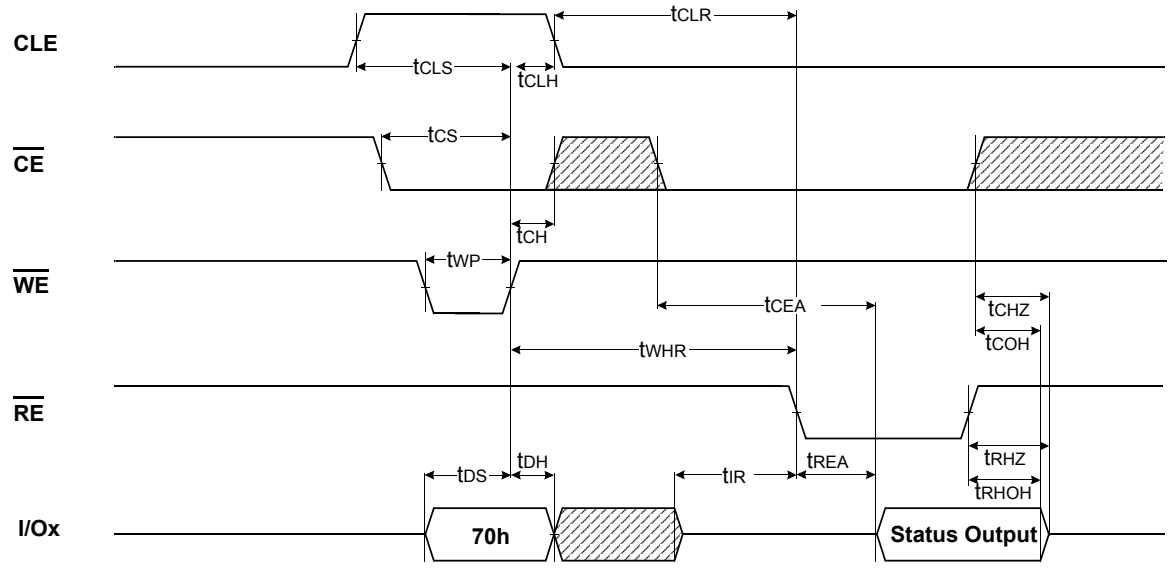
NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 20MHz.
tRHOH starts to be valid when frequency is lower than 20MHz.

Serial Access Cycle after Read(EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)

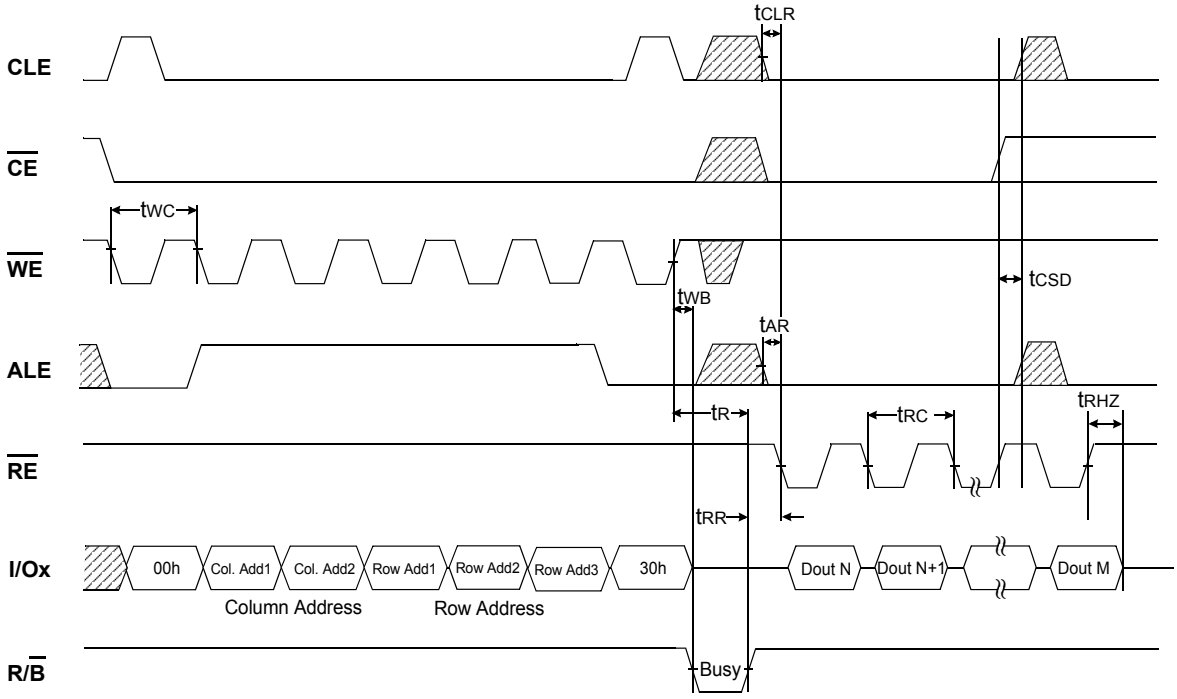


NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 20MHz.
tRHOH starts to be valid when frequency is lower than 20MHz.

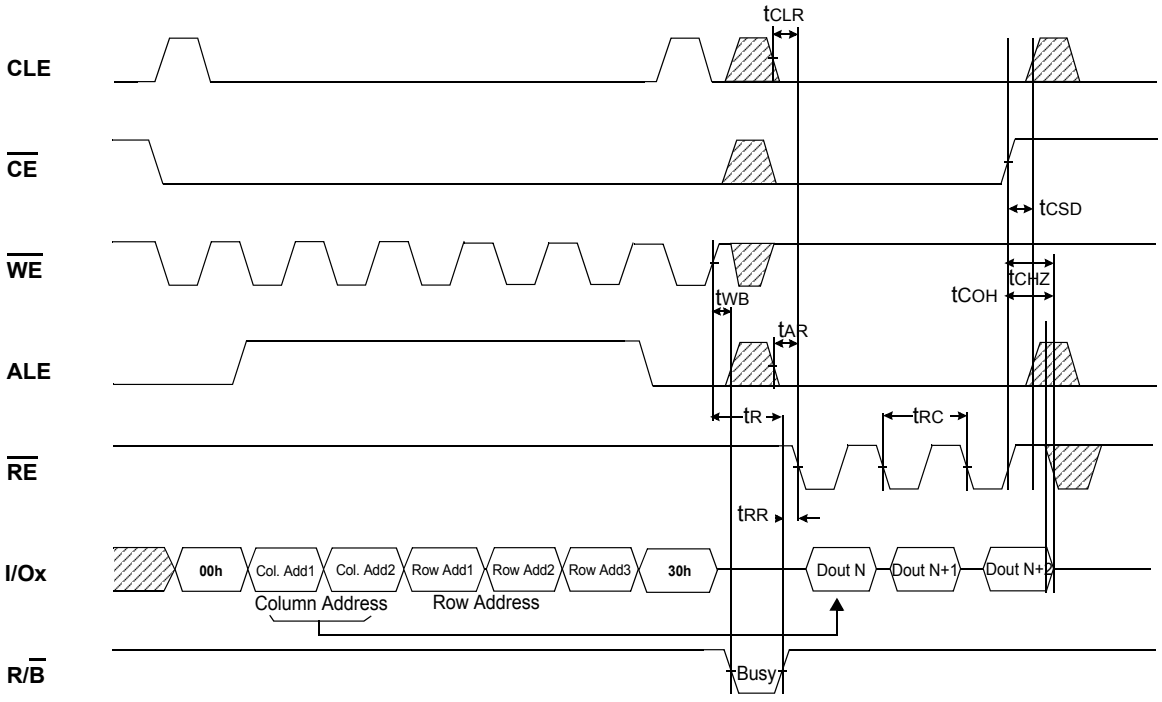
Status Read Cycle



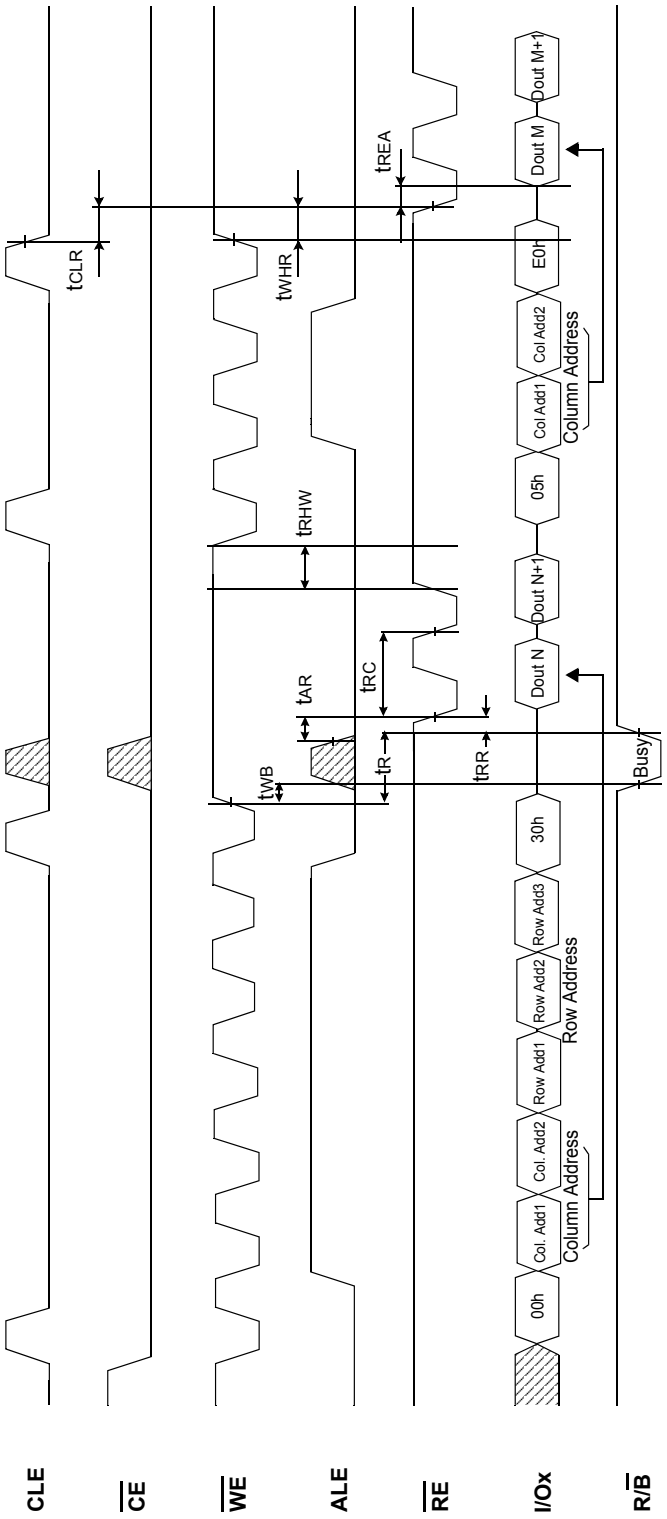
Read Operation



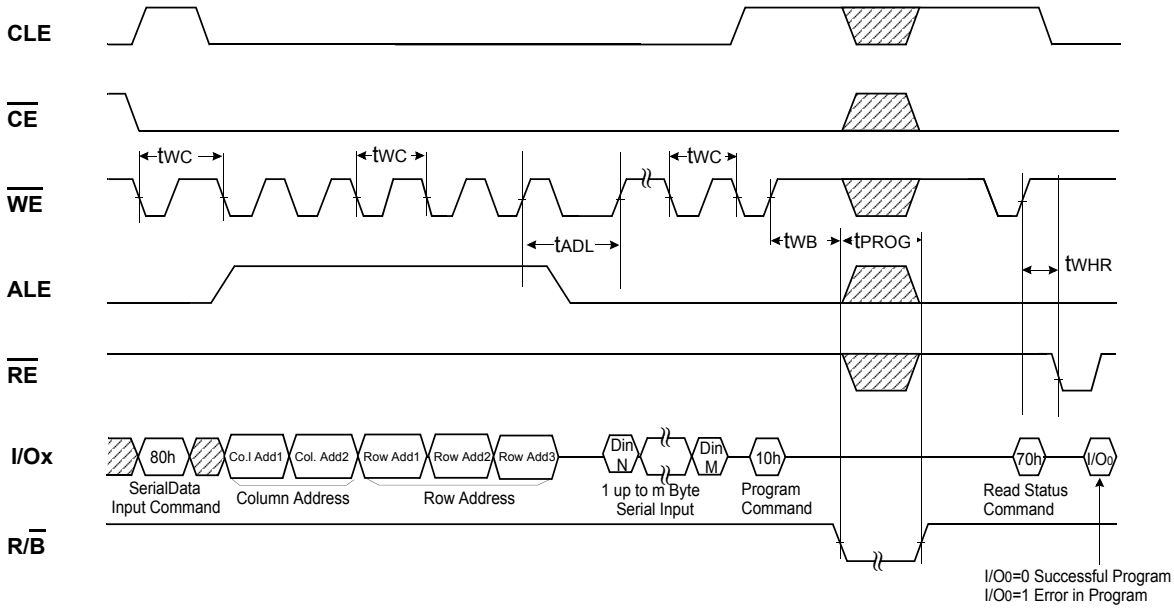
Read Operation(Intercepted by $\overline{CE}$)



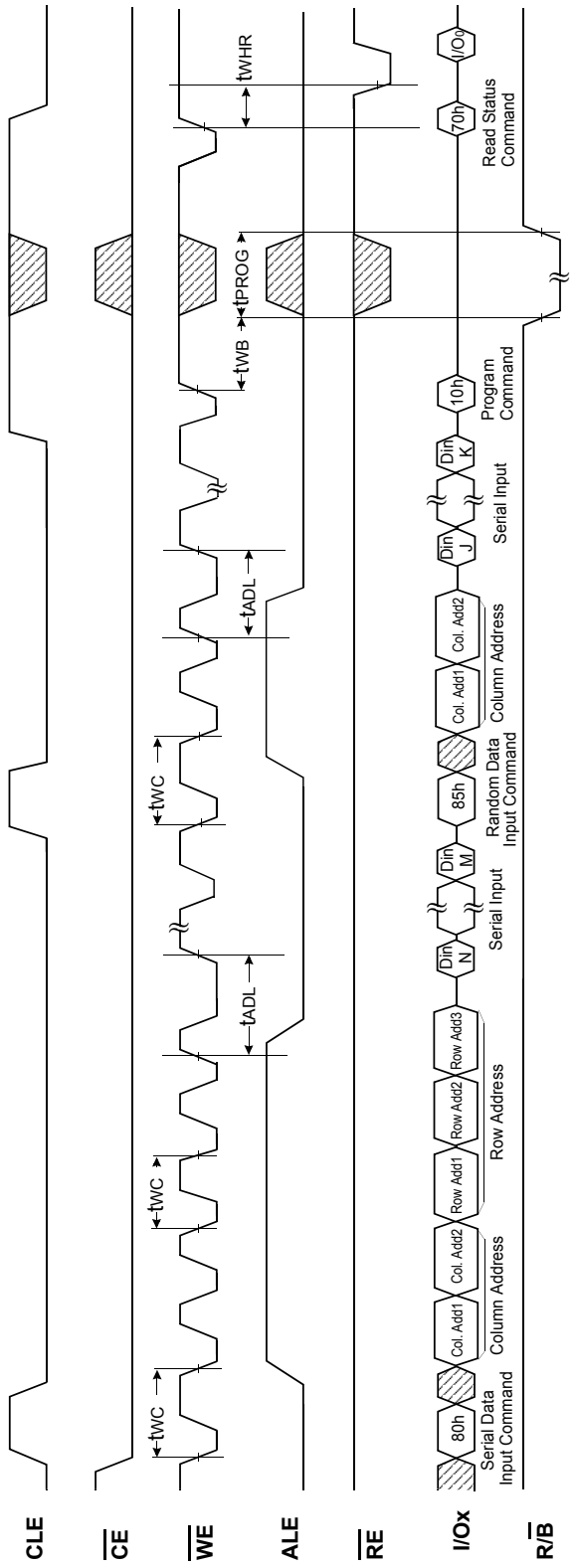
Random Data Output In a Page



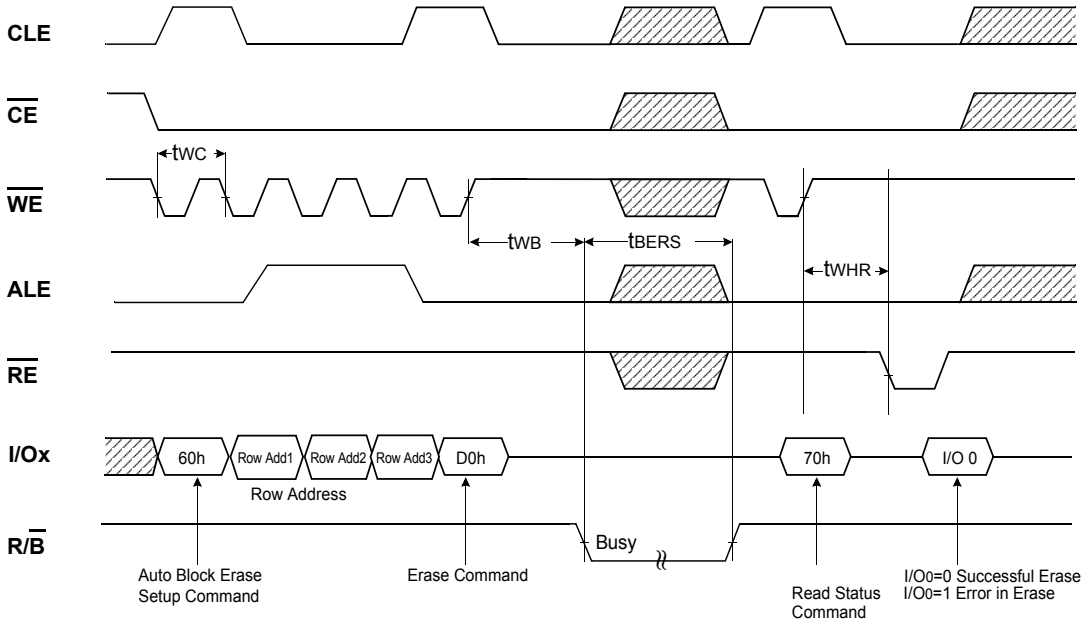
Page Program Operation



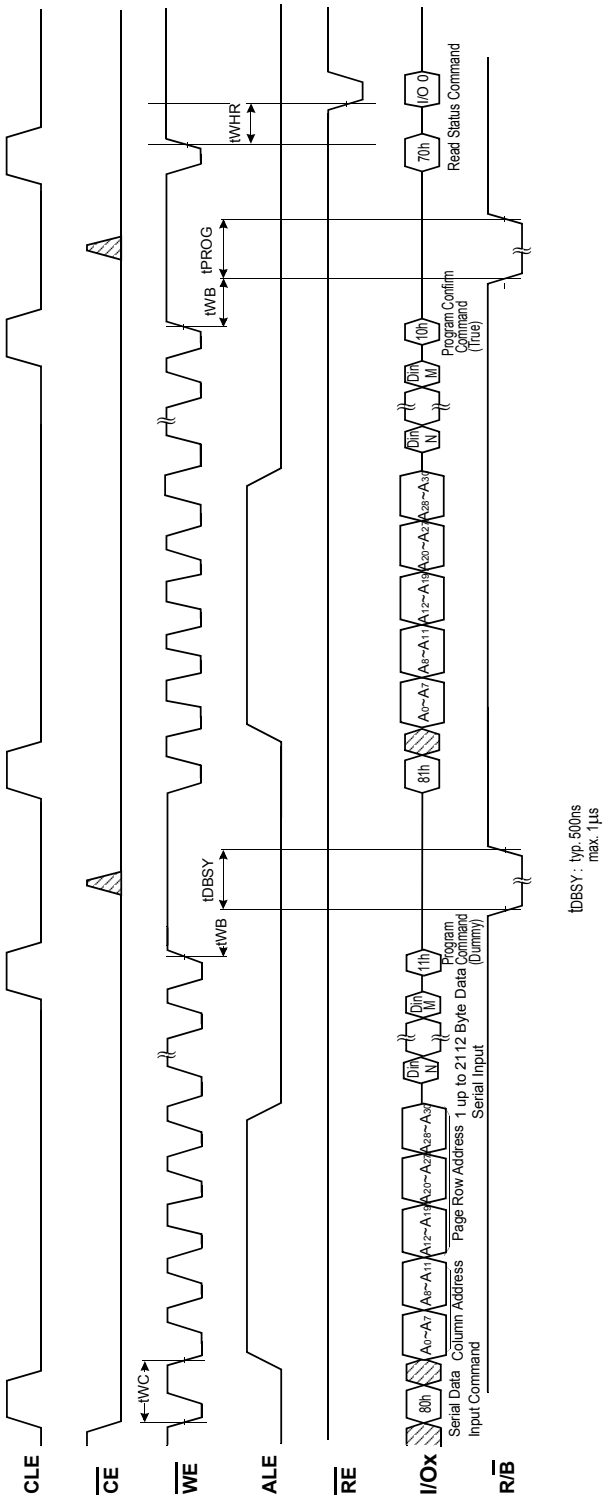
Page Program Operation with Random Data Input



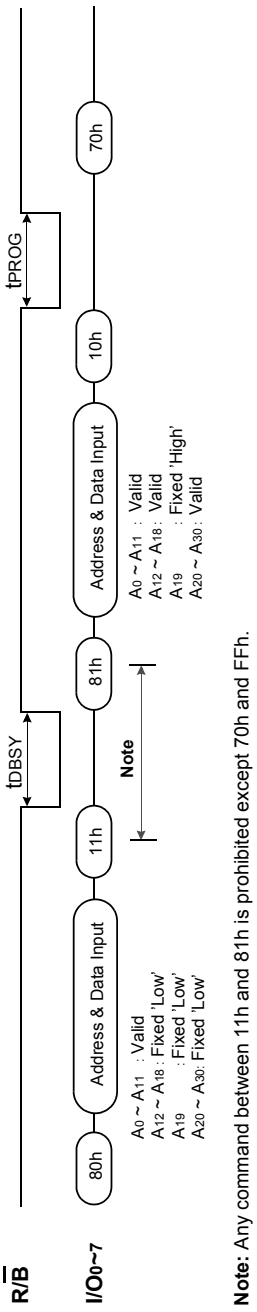
Block Erase Operation



Two-Plane Page Program Operation

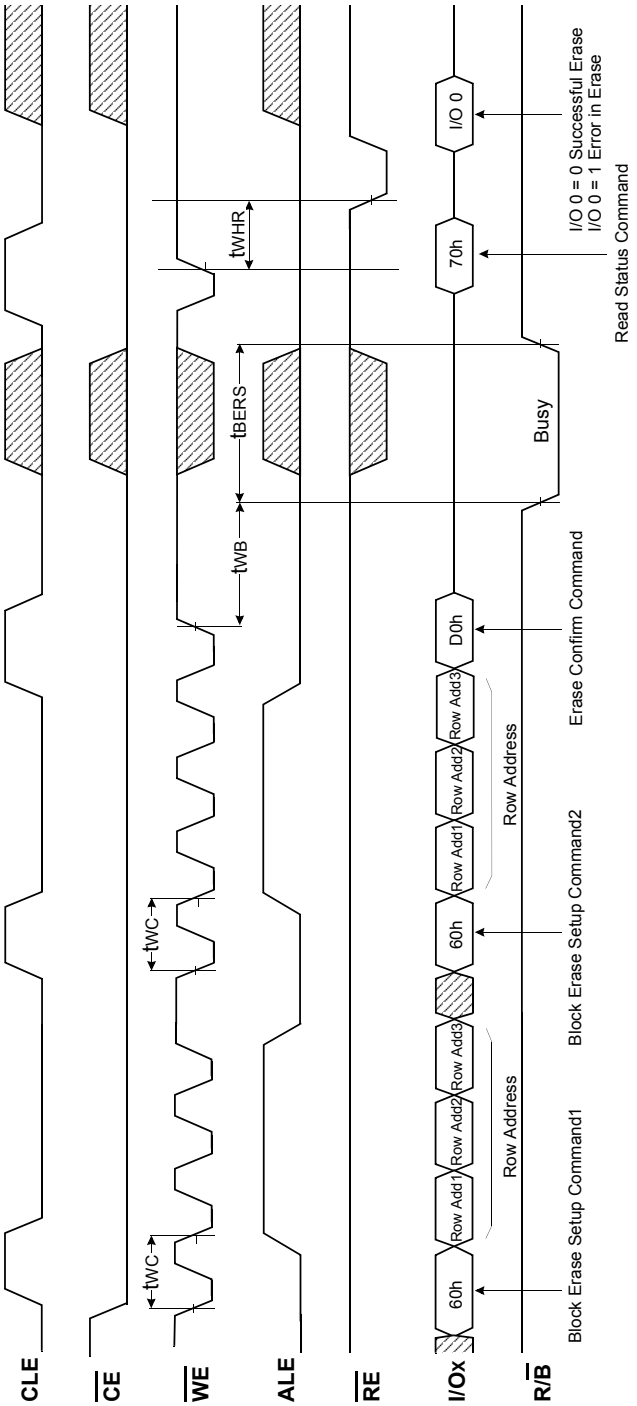


Ex.) Two-Plane Page Program

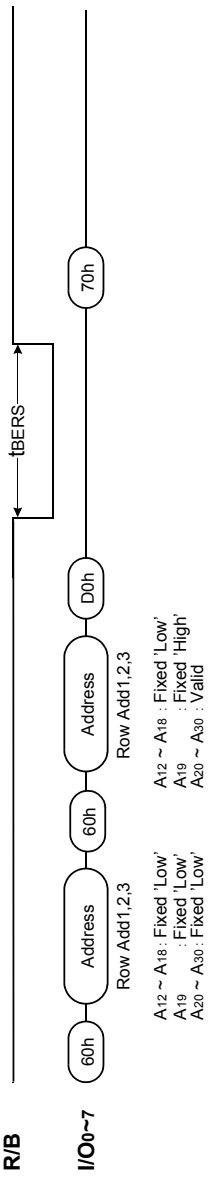


Note: Any command between 11h and 81h is prohibited except 70h and FFh.

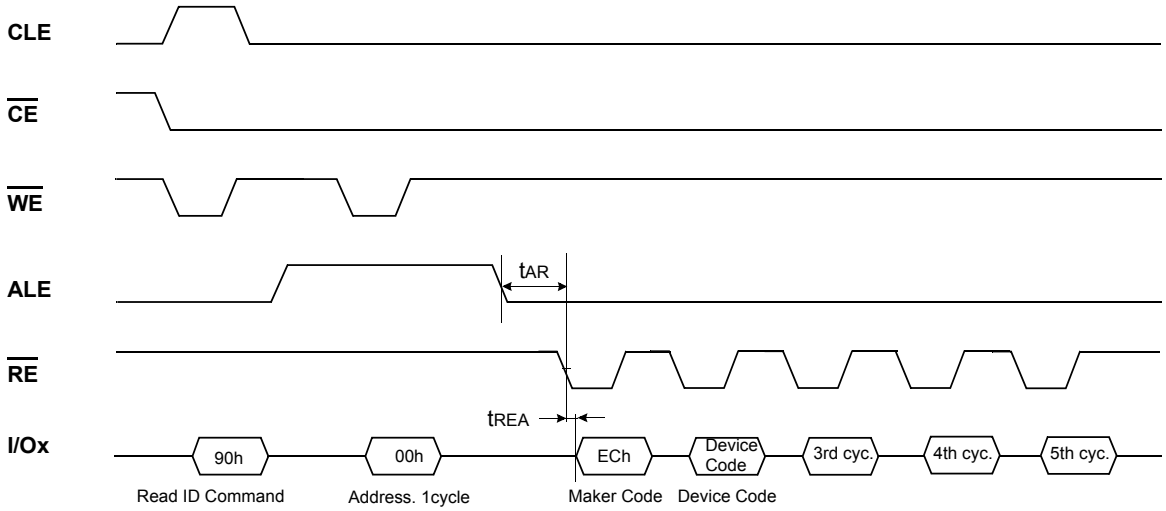
Two-Plane Block Erase Operation



Ex.) Address Restriction for Two-Plane Block Erase Operation



Read ID Operation



Device	Device Code(2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
K9G8G08U0M	D3h	14h	25h	64h
K9LAG08U1M	Same as each K9G8G08U0M in it			

ID Definition Table

90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programed Pages, etc
4th Byte	Page Size, Block Size, Spare Size, Organization, Serial Access Minimum
5th Byte	Plane Number, Plane Size

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Redundant Area Size (byte/512byte)	8 16					0 1	
Organization	x8 x16		0 1				
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (w/o redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved		0						0	0

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 60μs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

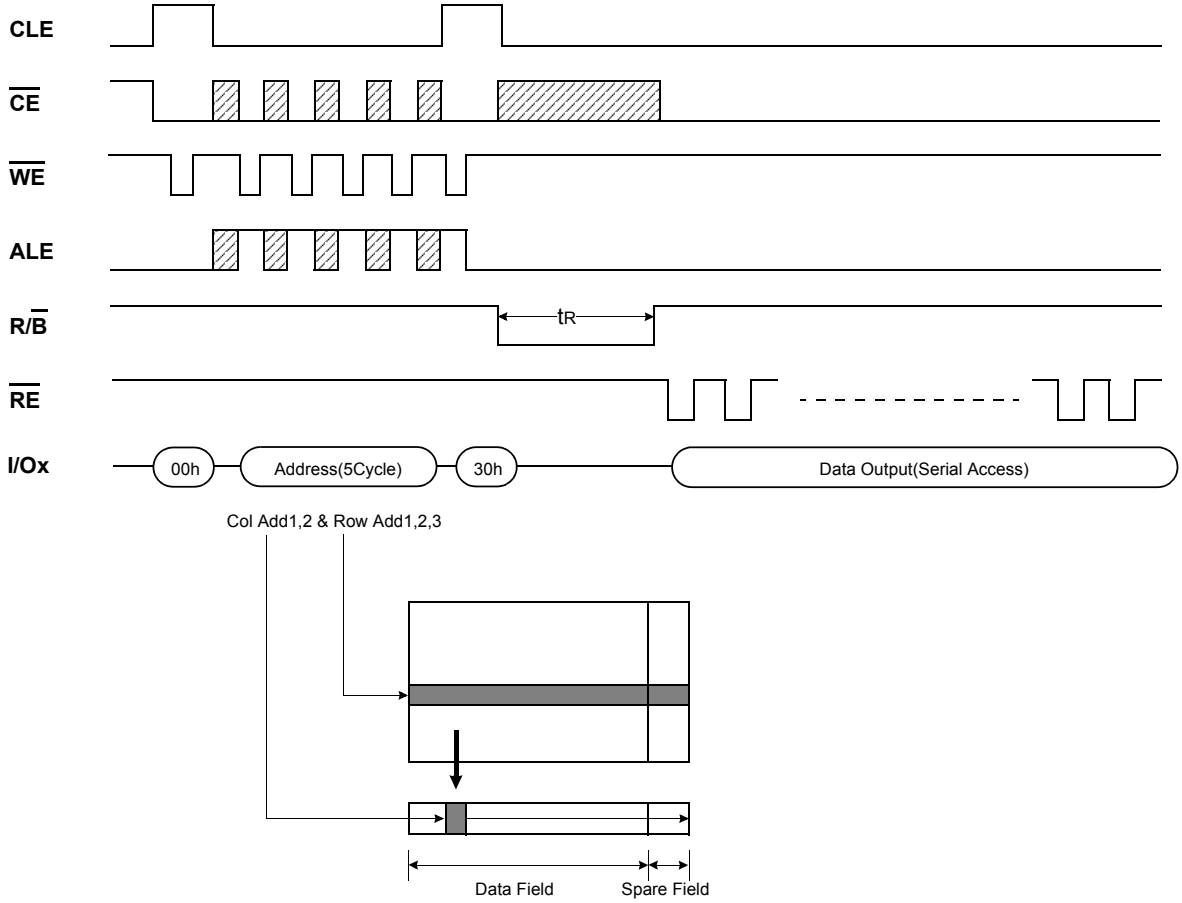
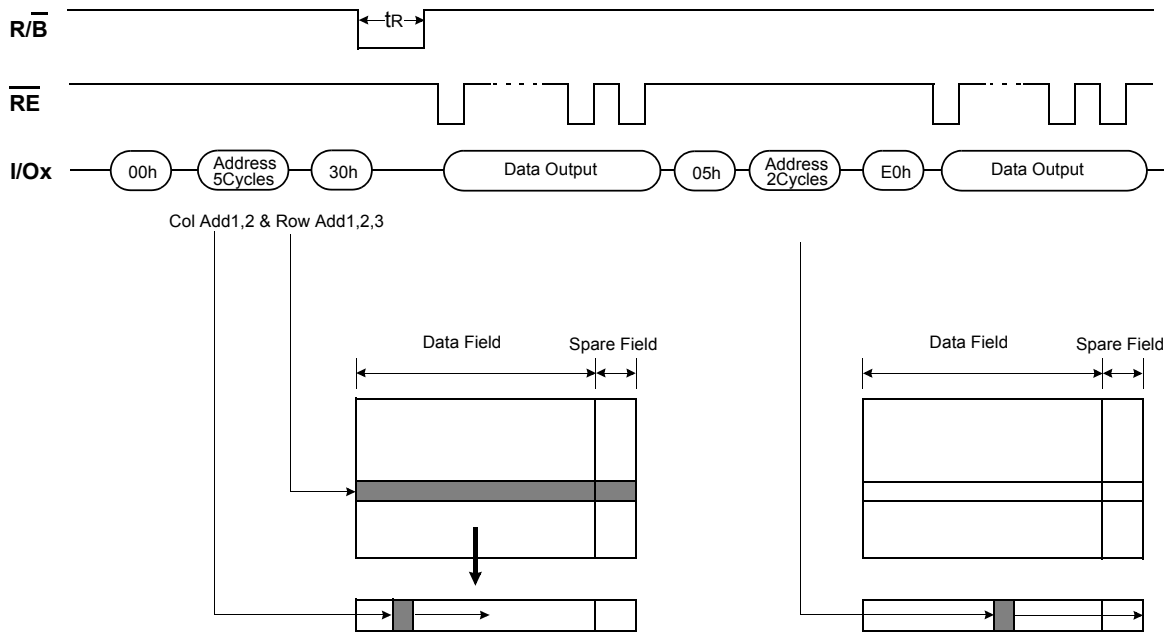


Figure 7. Random Data Output In a Page



PAGE PROGRAM

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 time for the page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

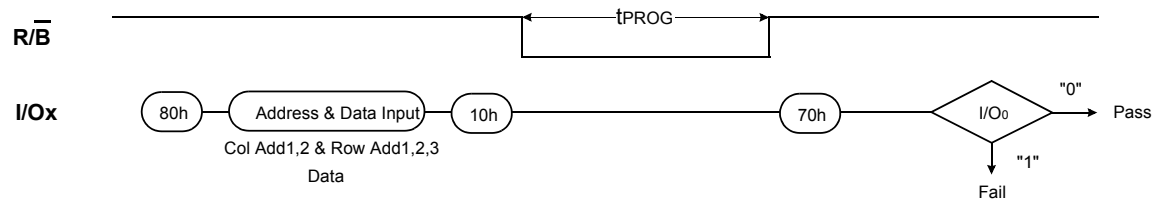


Figure 9. Random Data Input In a Page

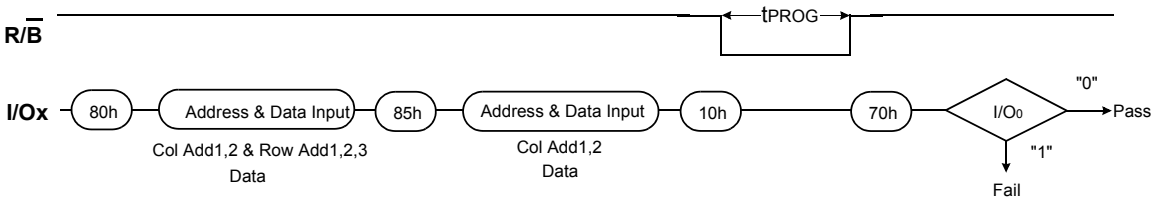


Table 2. Paired Page Address Information

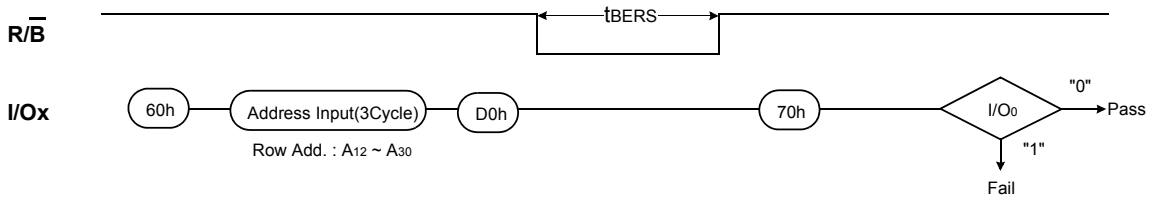
Paired Page Address		Paired Page Address	
00h	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

Note: When program operation is abnormally aborted (ex. power-down), not only page data under program but also paired page data may be damaged(Table 2).

BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{19} to A_{30} is valid while A_{12} to A_{18} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 10 details the sequence.

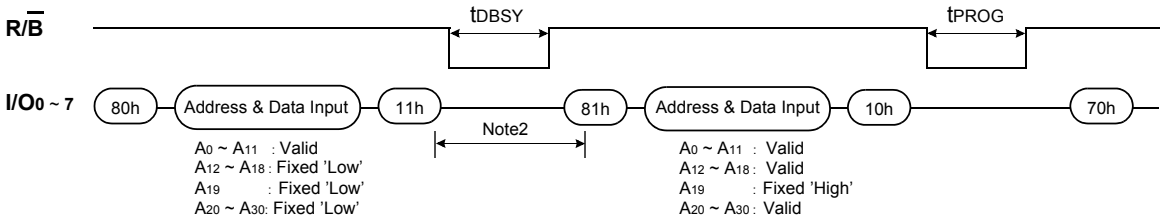
Figure 10. Block Erase Operation



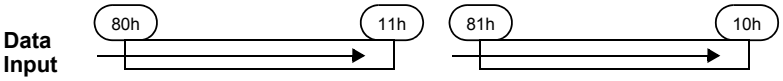
Two-Plane Page Program

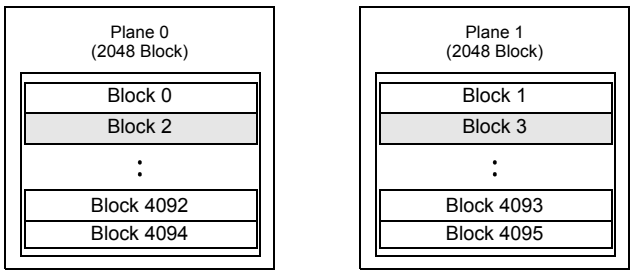
Two-Plane Page Program is an extension of Page Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.
After writing the first set of data up to 2112 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Althougth two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails.
Restriction in addressing with Two-Plane Page Program is shown in Figure11.

Figure 11. Two-Plane Page Program



NOTE : 1. It is noticeable that physically same row address is applied to two planes .
2. Any command between 11h and 81h is prohibited except 70h and FFh.

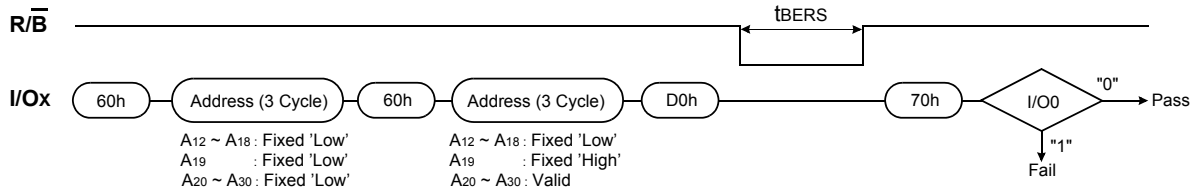




Two-Plane Block Erase

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/$\overline{B}$ pin or Ready/ Busy status bit (I/O 6).

Figure 12. Two-Plane Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table 3. Read Status Register Definition

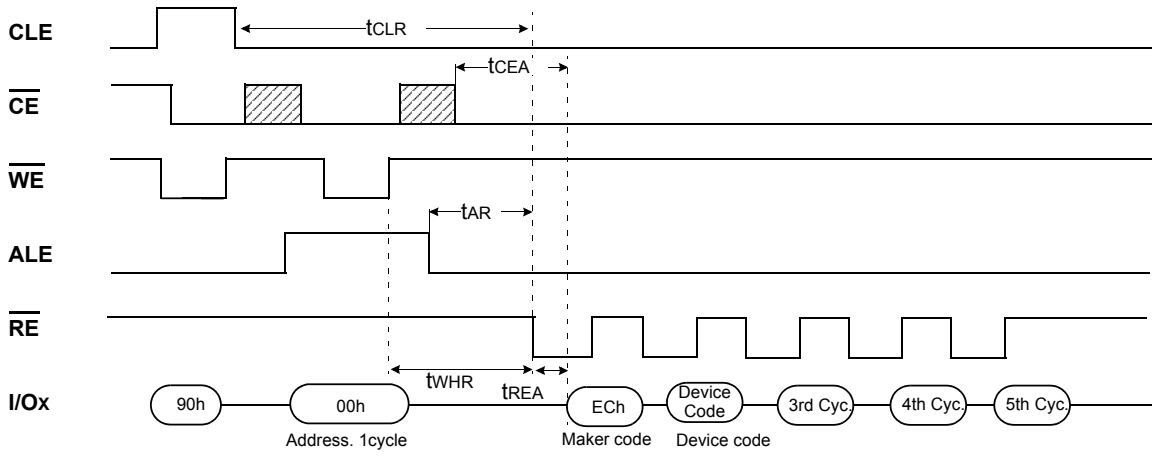
I/O No.	Page Program	Block Erase	Read	Definition	
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared	
I/O 2	Not use	Not use	Not use	Don't -cared	
I/O 3	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Not Use	Not Use	Not Use	Don't -cared	
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd cycle ID, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 13 shows the operation sequence.

Figure 13. Read ID Operation



Device	Device Code(2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
K9G8G08U0M	D3h	14h	25h	64h
K9LAG08U1M	Same as each K9G8G08U0M in it			

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to Table 4 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 14 below.

Figure 14. RESET Operation

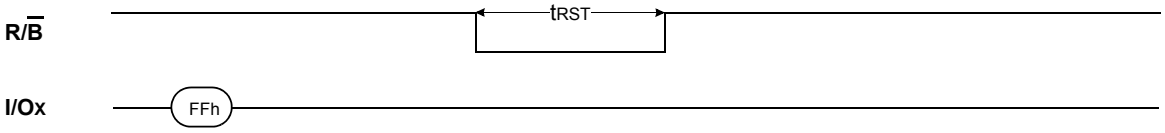


Table 4. Device Status

	After Power-up	**After Reset**
Operation mode	00h Command is latched	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 15). Its value can be determined by the following guidance.

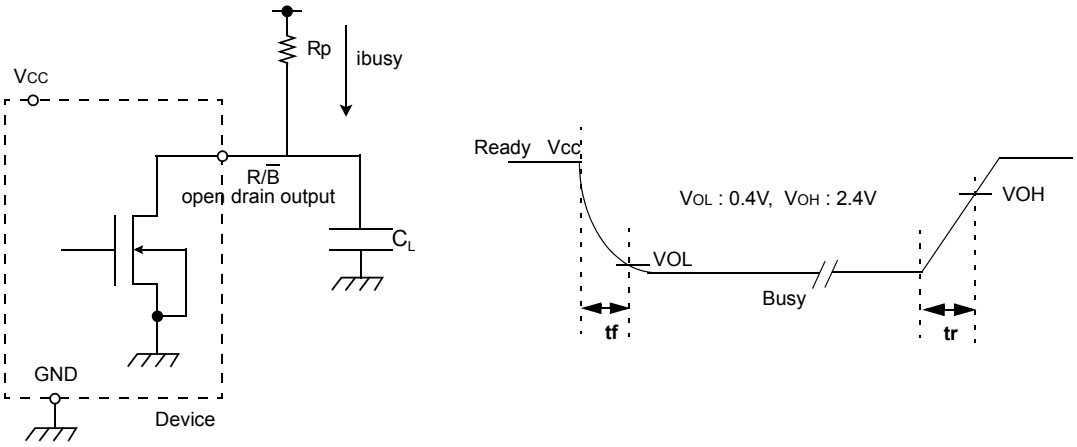
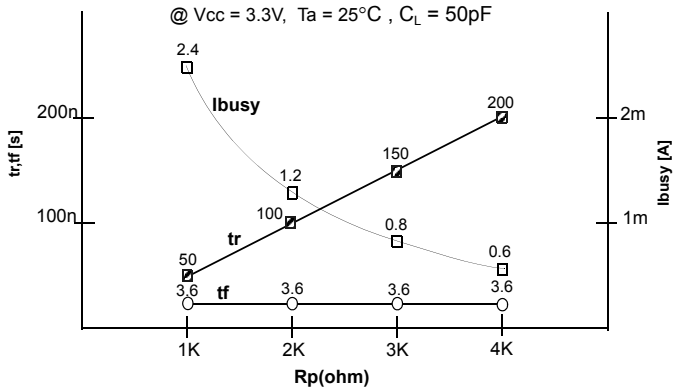


Figure 15. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr