QUALCOMM CDMA Technologies

MSM7627 Chipset Training

Baseband Topics

Qualcomm Confidential and Proprietary

Restricted Distribution. Not to be distributed to anyone who is not an employee of either Qualcomm or a subsidiary of Qualcomm without the express approval of Qualcomm's Configuration Management.

Not to be used, copied, reproduced in whole or in part, nor its contents revealed in any manner to others without the express written permission of Qualcomm.

QUALCOMM is a registered trademark of QUALCOMM Incorporated in the United States and may be registered in other countries. Other product and brand names may be trademarks or registered trademarks of their respective owners. CDMA2000 is a registered certification mark of the Telecommunications Industry Association, used under license. ARM is a registered trademark of ARM Limited. QDSP is a registered trademark of QUALCOMM Incorporated in the United States and other countries.

This technical data may be subject to U.S. and international export, re-export, or transfer ("export") laws. Diversion contrary to U.S. and international law is strictly prohibited.

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, CA 92121-1714
U.S.A.

Copyright © 2009 QUALCOMM Incorporated
All rights reserved.

Terms and Conditions of Usage

This document may contain information regarding parts and products whose manufacture, use, sale, offer for sale, or importation into the United States is subject to restrictions under one or more U.S. injunctions against QUALCOMM Incorporated. This document is not to be construed as an offer to sell such parts or products for use or importation into the U.S. This document is intended solely to provide technical information regarding technical recommendations and/or requirements regarding uses and configurations of those parts or products inside and outside the United States that are permitted by such injunctions. Recipient's download and/or use of the information in this document constitutes agreement with these terms.

Revision History

Revision	Date	Description
A	April 2009	Initial release

Agenda (1 of 2)

- **Feature comparison**
  - Chipset comparison for MSM7600™, MSM7625™, and MSM7627™ IC
  - Overview of engineering samples
- **System architecture**
- **Design considerations**
  - Voltage requirements
  - Power
  - Clocks
  - Boot options/security
  - Pin map
  - GPIO

Agenda (2 of 2)

- **RF analog interface**
  - GRFC
  - RF dedicated interface
  - PMIC interface
- **MSM7627 device interface**
  - EBI1
  - EBI2
  - MDDI
  - Parallel camera interface
  - Transport stream interface/UBM
  - LCD controller (RGB888)
  - HKADC/touchscreen
  - USB/USB-UICC/USIM/UART/SDIO/I2C/Keypad
  - BT
  - Audio
  - JTAG/ETM
- **MSM7627 heat dissipation modeling**
- **Reference Documents**

QUALCOMM
2010.07.13 at 18:46 PDT
ruijun.zhang-sh@...

MSM7627 Device Overview

MSM7627 Chipset Comparison (1 of 3)

Features	MSM7600	MSM7625	MSM7627
Process technology	65 nm CMOS (15 × 15 × 1.4 mm) 543 CSP	65 nm CMOS (11 × 11 × 1.05 mm) 456 NSP	65 nm CMOS (12 × 12 × 1.05 mm) 560 NSP
Processor	ARM1136-J™ 528 MHz/528 MHz* (apps) ARM926EJ-S™ 320 MHz/256 MHz* (modem) QDSP5000® 320 MHz/256 MHz* (apps) QDSP4000 122.88 MHz (modem)	ARM1136-J 528 MHz/528 MHz* (apps) ARM926EJ-S 320 MHz/256 MHz* (modem) QDSP5000 256 MHz (apps) QDSP4000 122.88 MHz (modem)	ARM1136JF-S 600 MHz (apps) ARM926EJ-S 400 MHz (modem) QDSP5000 320 MHz (apps) QDSP4000 122.88 MHz (modem)
Modem	IS-2000 CDMA 1X, IS-856 1xEV-DO Rev. A, WCDMA, GSM, GPRS, EDGE, DTM, HSDPA 7.2 Mbps, HSUPA 5.76 Mbps, Concurrency 7.2 Mbps DL + 2 Mbps UL	IS-2000 CDMA 1X, IS-856 1xEV-DO Rev. A, WCDMA, GSM, GPRS, EDGE, DTM, HSDPA 7.2 Mbps, HSUPA 5.76 Mbps, Concurrency 7.2 Mbps DL + 2 Mbps UL	IS-2000 CDMA 1X, IS-856 1xEV-DO Rev. A, WCDMA, GSM, GPRS, EDGE, DTM, HSDPA 7.2 Mbps, HSUPA 5.76 Mbps, Concurrency 7.2 Mbps DL + 2 Mbps UL
Rx enhancements	Equalizer, Rx diversity, SAIC	Equalizer, Rx diversity, SAIC	Equalizer, Rx diversity, SAIC
LCD support	16-bit/18-bit/24-bit (EBI2) 16-bit/18-bit/24-bit (MDDI)	16-bit/18-bit/24-bit (EBI2) 16-bit/18-bit/24-bit (MDDI) 16-bit/18-bit/24-bit LCD (RGB) controller	16-bit/18-bit/24-bit (EBI2) 16-bit/18-bit/24-bit (MDDI) 16-bit/18-bit/24-bit LCD (RGB) controller
MDDI support	Yes (two hosts and one client)	Yes (one host)	Yes (one host)
Broadcast interface	TSIF (DVB-H, ISDB-T, S-DMB)	TSIF (DVB-H, ISDB-T, S-DMB)	TSIF (DVB-H, ISDB-T, S-DMB)
Memory	Stacked: 256 Mbit 166 MHz DDR-SDRAM External: 32-bit 166 MHz DDR-SDRAM 8-bit/16-bit NAND flash 16-bit DeMUX OneNAND™	Stacked: N/A External: 32-bit 166 MHz DDR-SDRAM 8-bit/16-bit NAND flash 16-bit MUX OneNAND	Stacked: N/A External: 32-bit 200 MHz DDR-SDRAM 8-bit/16-bit NAND flash 16-bit MUX OneNAND
UART	Four (two HS and two standard)	Four (two HS and two standard)	Four (two HS and two standard)
SDIO	Four	Four	Four

Red text indicates different features than the MSM7600 device
Green text indicates different features than the MSM7625 device
.

MSM7627 Chipset Comparison (2 of 3)

Features	MSM7600	MSM7625	MSM7627
Qcamera™ (viewfinder frame rate)	8 megapixel support MDDI – 30 fps WVGA	5 megapixel support MDDI – 30 fps VGA LCDC – 30 fps WQVGA	8 megapixel support MDDI – 30 fps WVGA LCDC – 30 fps WVGA
OS	ARM11: L4, Windows Mobile®, Linux® ARM9™: L4	ARM11: L4, WinMob, Linux ARM9: L4	ARM11: L4, WinMob, Linux ARM9: L4
Qcamcorder™ (offline video encoding)	30 fps WVGA	24 fps QVGA	30 fps WVGA
Qtv™ (video decode)	30 fps WVGA streaming 30 fps VGA offline	15 fps WQVGA streaming 30 fps WQVGA offline	15 fps VGA streaming 30 fps WVGA offline
Qvideophone™ (video telephony)	15 fps QCIF	15 fps QCIF	15 fps QCIF
Audio/video decoders	MP3, AAC, AAC+, EAAC+, ADPCM, MPEG4, H263, H264, WMA v9, AMR-NB	MP3, AAC, AAC+, EAAC+, ADPCM, MPEG4, H263, H264, WMA v9, AMR-NB	MP3, AAC, AAC+, EAAC+, ADPCM, MPEG4, H263, H264, WMA v9, AMR-NB
2D/3D graphics acceleration	Hardware acceleration - 2 M - 4 M triangles/sec - 133 megapixels/sec	Not available	Adreno™ 200 WVGA 27 M triangles/sec 133 megapixels/sec fill rate Open GL®-ES 2.0/OpenVG 1.1/ SVG Tiny 1.2
Simultaneous polyphonic tones	128 polyphony Wavetable MIDI	128 polyphony Wavetable MIDI	128 polyphony Wavetable MIDI
Bluetooth®	BT 2.1 + EDR (BTS4025™ device)	BT 2.1 + EDR (BTS4025 device)	BT 2.1 + EDR (BTS4025 device)

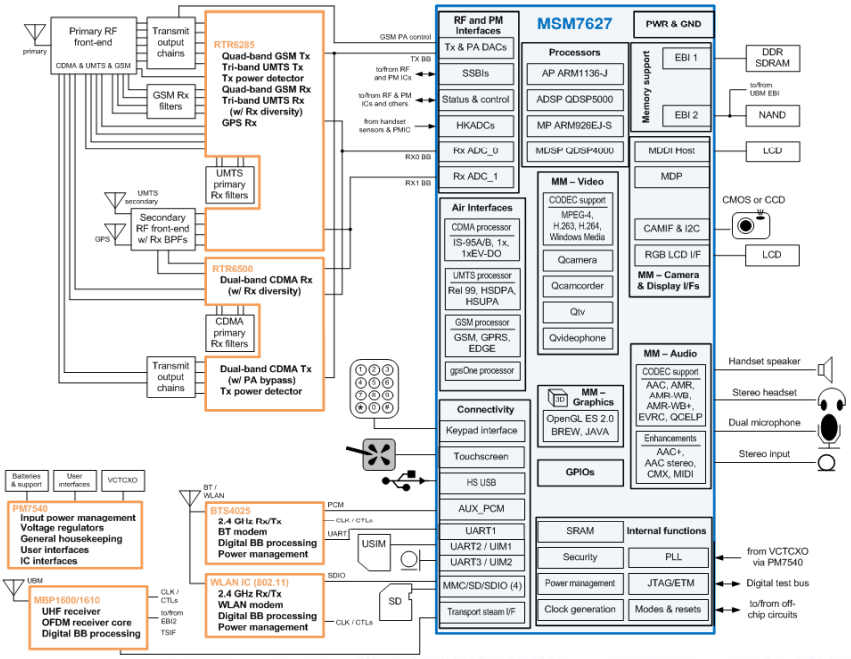
Red text indicates different features than the MSM7600 device
Green text indicates different features than the MSM7625 device
.

MSM7627 Chipset Comparison (3 of 3)

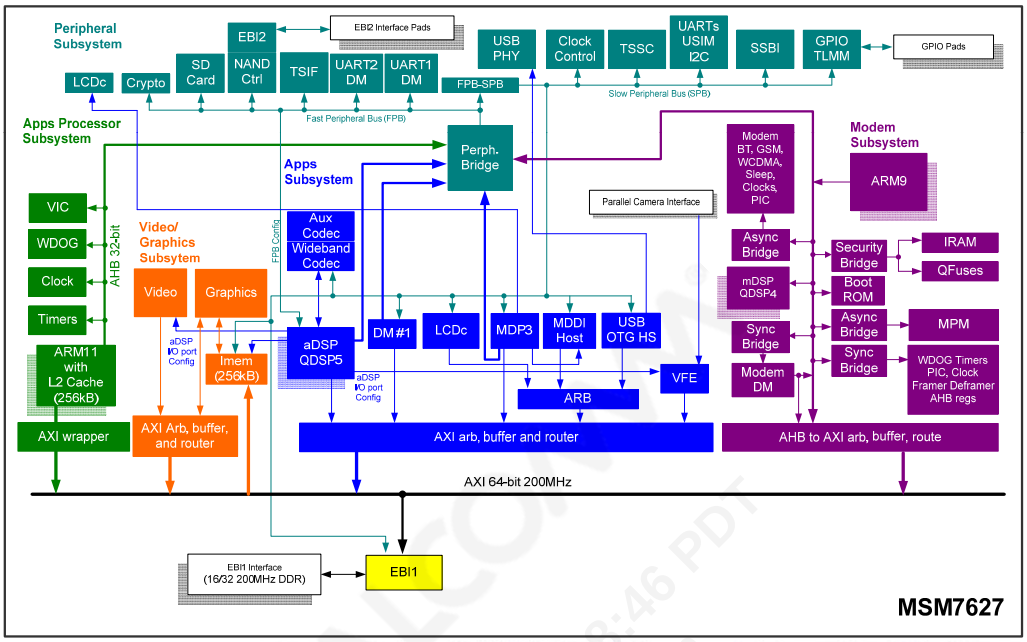
Features	MSM7600	MSM7625	MSM7627
USB	High-speed USB OTG (external PHY)	High-speed USB OTG (built-in PHY)	High-speed USB OTG (built-in PHY)
GPS	Standalone and assisted	Standalone and assisted	Standalone and assisted
USIM	Supports dual-voltage USIM via PMIC	Built-in support for dual-voltage USIM	Built-in support for dual-voltage USIM
UICC	One UICC	One UICC	One UICC
Digital rights management (DRM)	OMA DRM v2.0	OMA DRM v2.0	OMA DRM v2.0

Red text indicates different features than the MSM7600 device
Green text indicates different features than the MSM7625 device
.

MSM7627 Functional Block Diagram



System Architecture



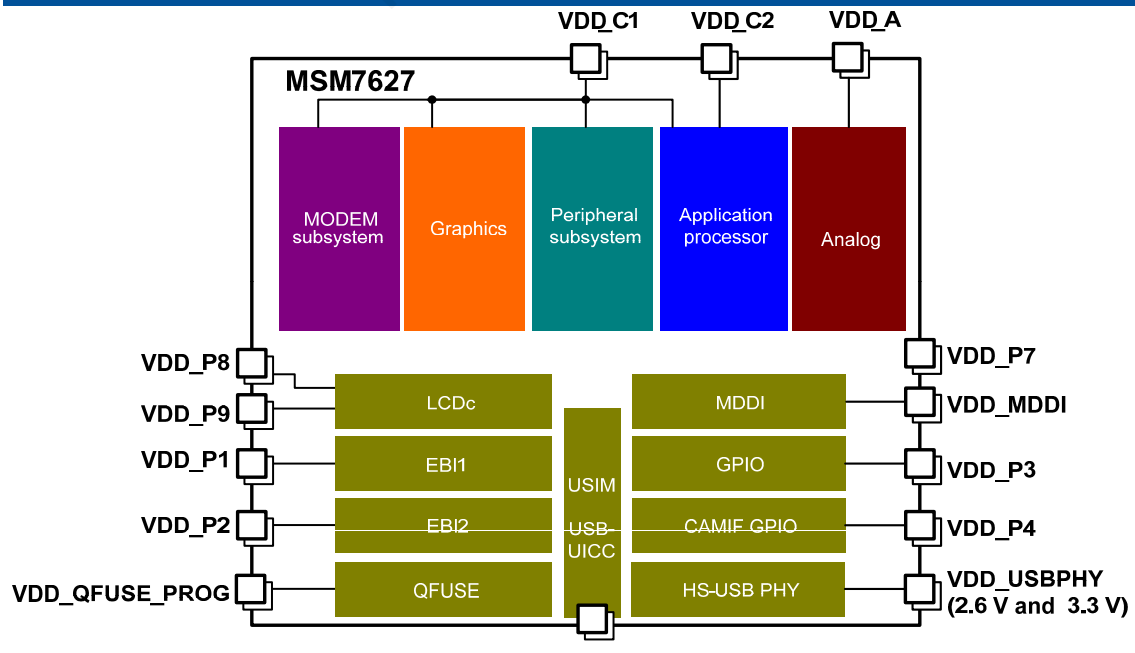
Engineering Sample

- Engineering sample (February 2009)
  - HS-USB leakage
  - Limitation of EBI2_CS3_N configuration as GPIO
  - Limitation while configuring GPIOs for LCDC mode
  - Audio distortion when VDD_USBPHY (3.3 V) is not supplied

Refer to the *MSM7627 Mobile Station Modem Device Revision Guide* (80-VM151-4) for more information.

MSM7627 Device Design Considerations

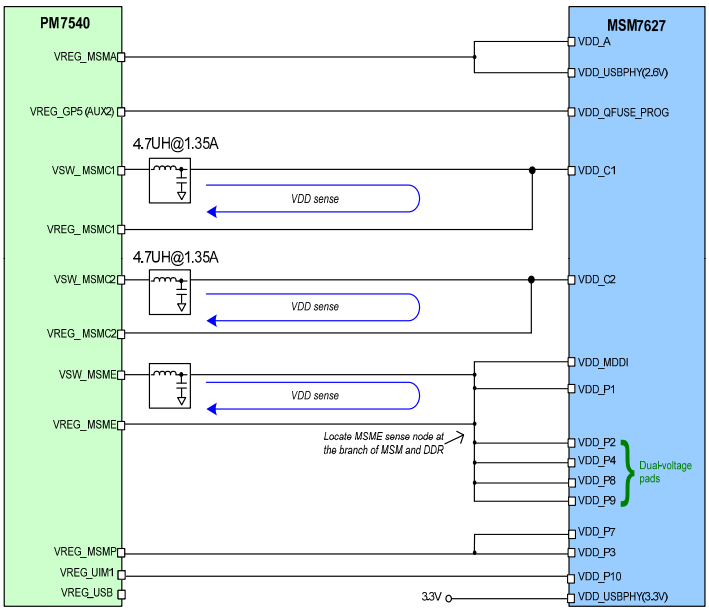
MSM7627 Power Supply



Voltage Requirements

Symbol	Description	Min	Typ	Max	Units
VDD_C1	Supply voltage for Mobile Station Modem (MSM™) digital core #1 (everything but ARM1136JF-S: High speed (AXI > 160 MHz) Normal operation (AXI ≤160 MHz) VDD minimization (retention state)	 TBD TBD TBD	 1.35 1.25 –	 TBD TBD –	V
VDD_C2	Supply voltage for MSM digital core #2 (ARM1136JF-S) High-speed (AXI > 160 MHz) Normal operation (AXI ≤160 MHz)	 TBD TBD	 1.35 1.25	 TBD TBD	V
VDD_A	Supply voltage for internal analog core	2.5	2.6	2.7	V
VDD_P1	Supply voltage P1 for EBI1 and peripheral interfaces	1.7	1.8	1.9	V
VDD_P2	Supply voltage P2 for EBI2 and peripheral interfaces	1.65 2.5	1.8 2.6	1.95 2.7	V V
VDD_P3	Supply voltage P3 for peripheral interfaces	2.5	2.6	2.69	V
VDD_P4	Supply voltage P4 for camera interface	1.65 2.5	1.8 2.6	1.95 2.7	V V
VDD_P7	Supply voltage P7 for internal reference	2.5	2.6	2.7	V
VDD_P8	Supply voltage P8 for LCDc interface	1.65 2.5	1.8 2.6	1.95 2.7	V V
VDD_P9	Supply voltage P9 for LCDc or EBI2 interface	1.65 2.5	1.8 2.6	1.95 2.7	V V
VDD_P10	Supply voltage P10 for USIM/USB-UICC interface Low voltage option High voltage option	 1.65 2.70	 1.80 2.85	 1.95 3.0	V
VDD_MDDI	Supply voltage for MDDI interface	1.65	1.8	1.95	V
VDD_QFUSE_PROG	Supply voltage for Qfuse programming	2.8	2.9	3.0	V
VDD_USBPHY (2.6 V)	Supply voltage for USB (HS) PHY interface	2.5	2.6	2.7	V
VDD_USBPHY (3.3 V)	Supply voltage for USB (HS) PHY interface	3.0	3.3	3.6	V

MSM7627/PM7540 Power-Supply Connections



The current rating for inductors on VDD_C1 and VDD_C2 should be 1.35 A; the other inductors are not necessarily to have 1.35 A current rating.

Although the average DC currents for VDD_C1 and VDD_C2 will be no more than 600 mA, peak currents could be much higher than that.

To be conservative, 1.35 A current rating inductors are recommended for now. More accurate values will be provided on base of measurements.

Refer to the *MSM7627 Baseband Reference Schematic* (80-VM151-41) for the recommended decoupling capacitor values and placements.

Powerup/Powerdown Sequence (1 of 2)

- **Powerup sequence (as controlled by the PM7540™ device):**

  1) VDD_C1: all digital core circuit except ARM1136J-FS

  2) VDD_C2*: application processor

  3) VDD_E: pad group EBI1 (EBI2**/MDDI and camera)

  4) VDD_P**: pad group GPIO (2.6 V domain/EBI2)

  5) VDD_A: pad group analog

Powerup/Powerdown Sequence (2 of 2)

- **Powerdown sequence (as controlled by the PM7540 device):**

  1) VDD_A: analog

  2) VDD_P**: pad group GPIO (2.6 V domain/EBI2)

  3) VDD_E: pad group EBI1 (EBI2**/MDDI and camera)

  4) VDD_C2*: application processor

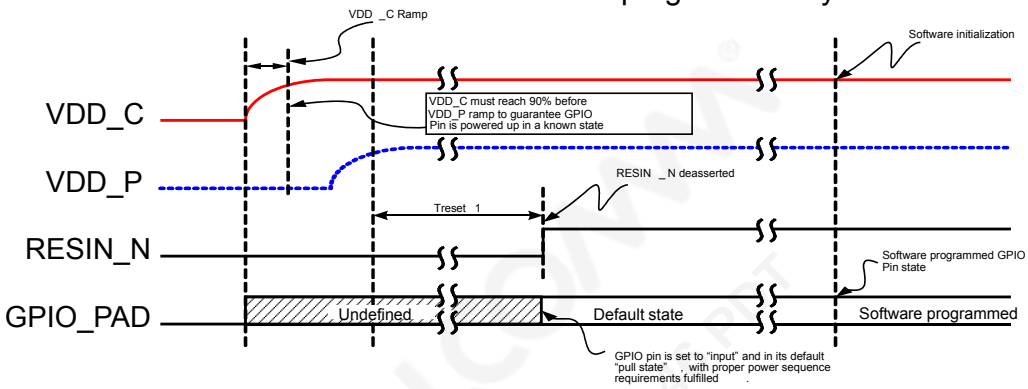
  5) VDD_C1: all digital core circuit except ARM1136J-FS

* The application processor (VDD_C2) power supply is controlled by the modem master.

** The EBI2 can be powered by either a 1.8 V or 2.6 V power rail.

GPIO Powerup States

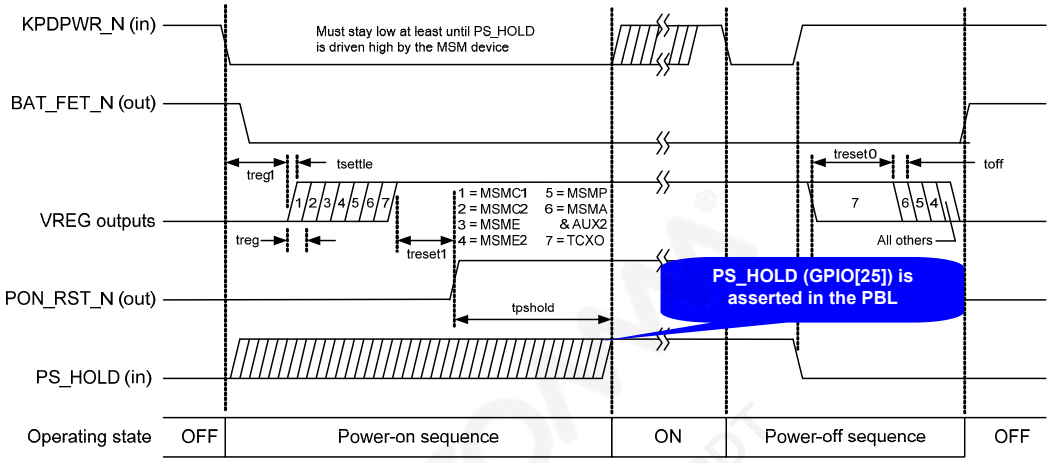
- A specific powerup sequence is required for the MSM7627 IC.
- If the powerup sequence is not achieved, GPIO pads may power up in undefined states.
- Qualcomm power management ICs, such as the PM7540 IC, ensure the proper supply sequence and states.
- The initial GPIO state is maintained until programmed by software.



Powerup Sequencing

- **The use of the Qualcomm PM7540 power management IC ensures the correct powerup sequence.**
- **When using the MSM7627 IC with the PM7540 IC, GPIO[25] is configured as the PS_HOLD signal by the software during boot up.**
- **After the voltage rails are brought up, PON_RST_N is deasserted by PM7540 IC, and then the MSM7627 IC asserts the PS_HOLD signal.**
  - This is done early in the boot process (PBL) to ensure that the PMIC does not turn the MSM device off.

PS_HOLD Assertion

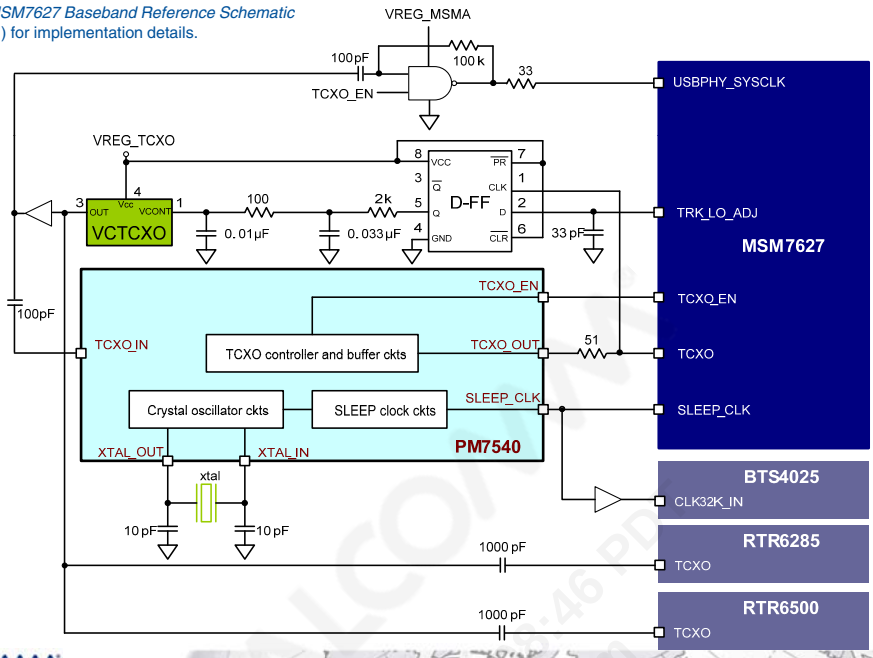


Clock

- **The MSM7627 system uses two external clocks:**
  - **19.2 MHz**
    - System clock
    - RF clock
    - HS-USBPHY clock
    - Refer to the *Voltage Controlled TCXO, 19.2 MHz Specifications* (80-V2896-1) for more details on VCTCXO requirements in a phone design.
  - **32.768 kHz**
    - Sleep clock
    - Refer to the *PM7540 Power Management IC Device Specification* (80-VD691-1) for complete specifications.

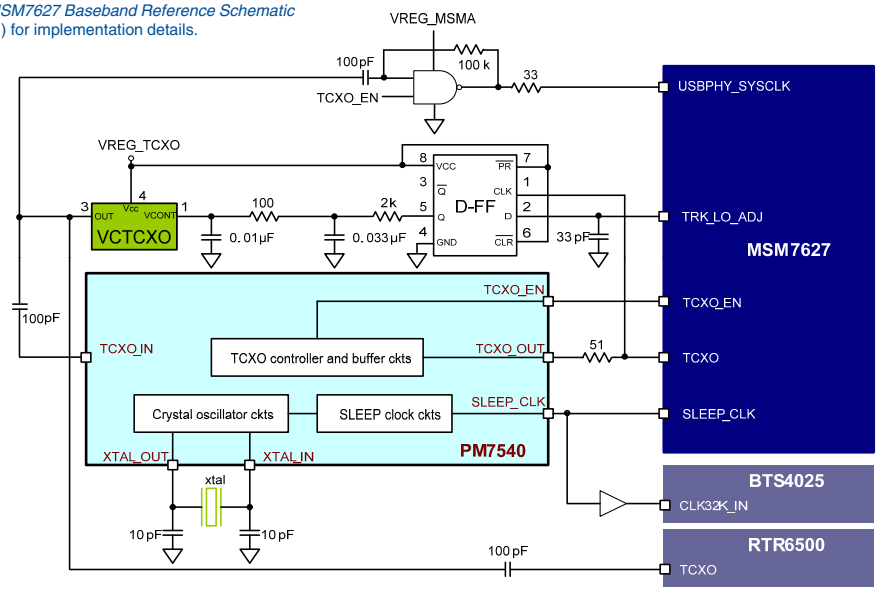
Clock Source Generation (Multimode)

Refer to the *MSM7627 Baseband Reference Schematic* (80-VM151-41) for implementation details.



Clock Source Generation (1x Only)

Refer to the *MSM7627 Baseband Reference Schematic* (80-VM151-41) for implementation details.



Secure Boot

- **A secure boot ensures that the MSM7627 IC boots from code which cannot be altered or hacked.**
- **A secure boot also enables the phone manufacturer and Qualcomm to ensure that their own code runs unchanged on the device.**
- **Hardware requirements for secure boot are as follows:**
  - Boot ROM (primary boot loader)
    - A secure boot capability is provided through an on-chip ROM. The MSM7627 IC has a built-in 64 KB of on-chip boot ROM. This ROM contains the primary boot loader (PBL).
    - This boot ROM is programmed in silicon – it **CANNOT** be changed for different configurations or for different uses by customers.
    - The PBL is mapped to address 0xFFFF0000.
  - Internal RAM (IRAM)
    - IRAM is a 4 KB-memory space used to load the basic configuration data.
  - Secondary boot loader (SBL)
    - The SBL is an external flash memory device.
    - The SBL could be implemented as a NAND or a SD device (software not supported).
    - Since SBL is external to the MSM7627 device, SBL contents **MUST** be authenticated by PBL before execution.

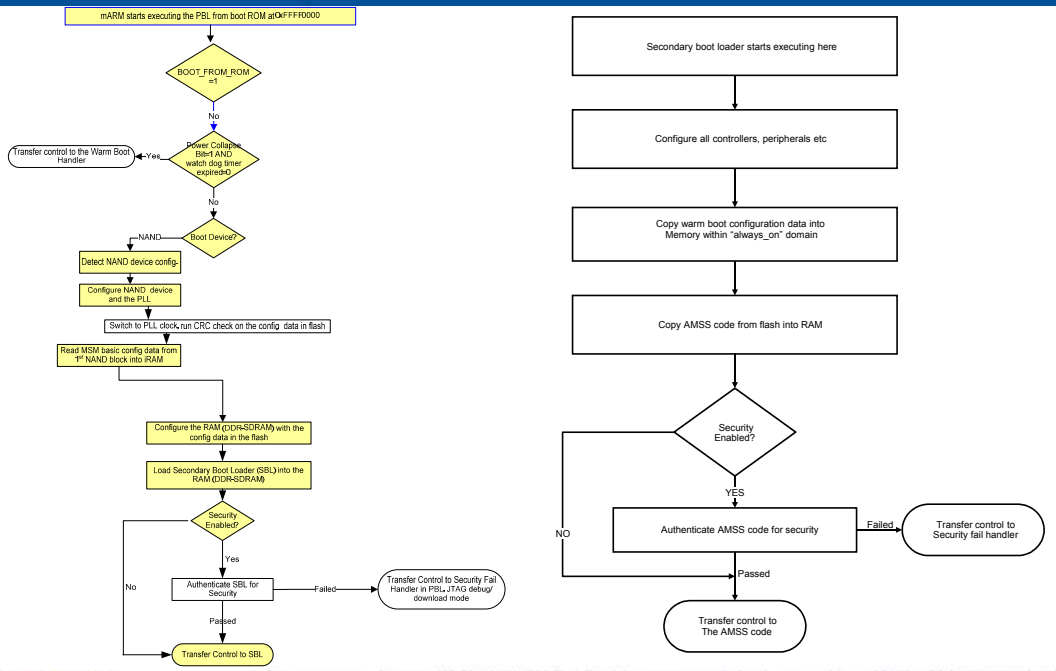
Configuring the MSM7627 Device in Secure Boot (1 of 2)

- **There are two ways to ensure that the MSM7627 IC boots in secure boot**:
  - External mode pin
  - On-chip Qfuses
- **External mode pin (BOOT_SCUR pin)**
  - GPIO[95] is used for this purpose.
  - If this pin is enabled (high), it forces the secondary boot loader or any subsequent code to be authenticated for security.
  - This pin setting is valid only if the security-enabled Qfuse is **NOT** blown.
- **On-chip Qfuse**
  - One-time programmable fuse
  - The FORCE_TRUSTED_BOOT Qfuse is used for the MSM7627 secure boot configuration.
  - If this Qfuse is blown, it forces the SBL and any subsequent code to be authenticated for security.
  - When the FORCE_TRUSTED_BOOT Qfuse is blown, the BOOT_SCUR pin setting is meaningless, and the BOOT_SCUR pin is available for use as GPIO[95].
  - It needs to be blown by the customer if a secure boot is deemed mandatory.
  - The Qfuse is blown through the software or JTAG.

Configuring the MSM7627 Device in Secure Boot (2 of 2)

- **QCT recommends connecting VDD_QFUSE_PRG to the PM7540 VREG_AUX2**
- **VDD_QFUSE_PRG must be connected to GND if Qfuse programming is not being performed**
- **Do not leave VDD_QFUSE_PRG floating**
- **Refer to *Application Note: MSM7xxx Qfuses and Security* (80-V9038-15) for more information.**

Secure Boot Process Flow

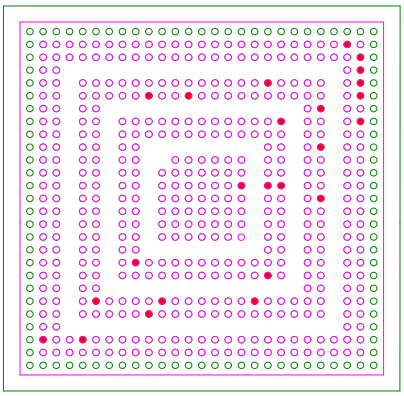


Boot Operation

- **Cold boot**
  - Occurs at initial powerup
  - Follows the PBL and SBL boot process flow from the previous slide
- **Warm boot**
  - A warm boot occurs when a device comes out of its shutdown (power-saving) mode.
  - The PBL executes and determines the system is powering up from power-saving mode and executes the warm-boot loader.
  - The system is reconfigured almost the same way as a cold boot, but the configuration comes from a small memory on the always-on domain.
  - Once the memory controllers are configured, data in the RAM can be accessed. The SBL does not need to be reloaded from the flash.

MSM7627 Package Design

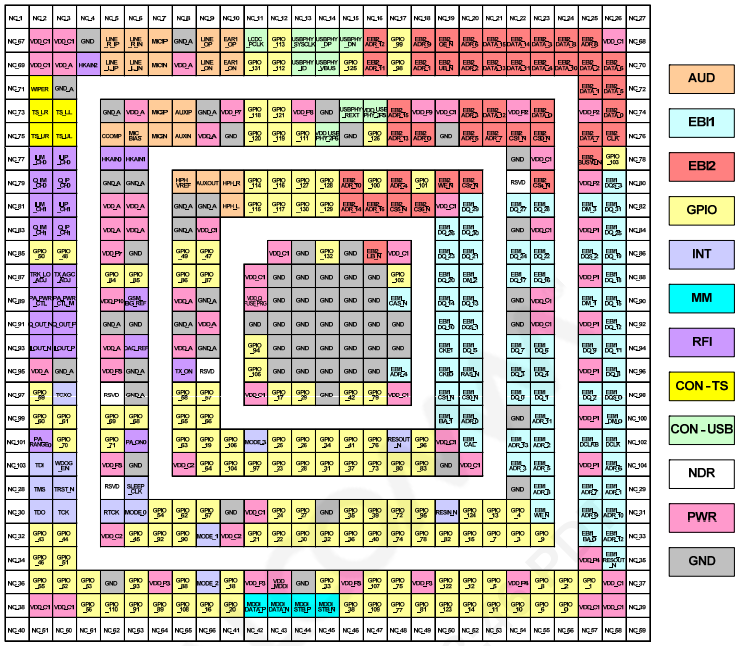
- **12 × 12 mm, 0.4 mm pitch, 560 pin, NSP package**
  - **Package size enlarged because of graphic core integration**
  - **104 NC pins to fill up the additional space while keeping 456 compatible with MSM7625**
- **No internal connection for pins on outer ring (104 NC pins)**
  - **Signals can route through these NC pins if necessary**
- **24 pins moved for better power distribution for graphic core**



MSM7627 Package with MSM7x25 Overlay

MSM7627 package
MSM7625 package
Updated Pins

MSM7627 Pin Map

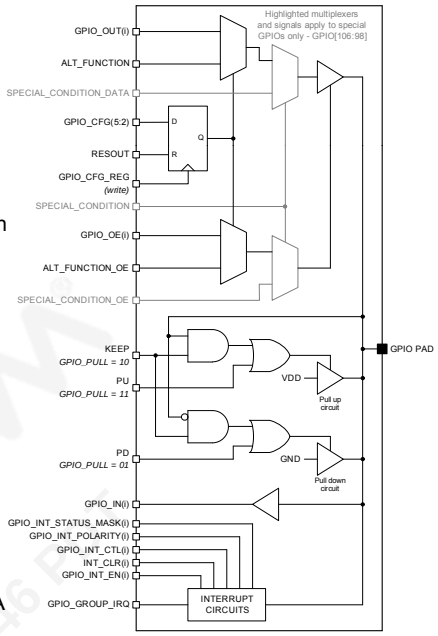


General Purpose Input/Output

- **The MSM7627 IC provides general purpose input/output (GPIO) pins which are software programmable.**
- **GPIO pads are assigned functions using AMSS software.**
- **Many pads can be assigned more than one function, depending on the application.**
- **GPIO pins can be configured as follows:**
  - B: Bidirectional with CMOS input
  - DI/DO: Digital input/output (CMOS)
  - H: High-voltage tolerant; allows digital input voltages up to 3.0 V
  - W: Input pad provides wake-up interrupt during deep-sleep mode
  - nppdpukp: Programmable pull resistor
- **Refer to the *MSM7627 Mobile Station Modem Device Specification* (80-VM151-1) for more information regarding GPIO pins and their functions.**

GPIO Pad Structure

- **Output configurations**
  - Normal GPIO output signal
  - Alternate GPIO output signal
  - Special GPIO signal
- **Input configuration**
  - Buffer
  - Interrupt: the input signal's (interrupt source) level or edge, with selectable polarity, is used to generate an interrupt.
- **Pull configurations**
  - Keeper
  - Pull up
  - Pull down
- **Programmable drive strengths**
  - Most of the GPIO pin's output drive strength is programmable from 2 to 16 mA, in 2 mA increments.
  - High voltage (3 V) GPIO pin's output drive strength is programmable from 2 to 8 mA, in 2 mA increments.
  - SDCC CLK GPIO pin's output drive strength is non-linear 4 mA to 7 mA. Refer to the *MSM7627 Mobile Station Modem Device Specification* (80-VM151-1) for more information.



Modem Power Manager

- **The modem power manager (MPM) is a MSM7627 IC feature that reduces the leakage current in phone designs during sleep mode.**
- **When the MPM feature is used, only a select number of GPIO pins can turn on the MSM device from sleep.**
  - 28 GPIO pins are capable of wake-up interrupt..
  - Other GPIO pins cannot be used as a wakeup-capable interrupt (only applicable if the MPM feature is enabled)
- **During power-saving mode, all pins in the MSM device will be held by the keeper.**
- **Keepers provide < 30 µA per pad of drive strength capability on all MSM pads.**
- **It is recommended to avoid using external pulls on the MSM device, which pull to the state opposite to that nominally found on the pin.**
  - Excessive DC current will be drawn in such a condition.
- **The noise coupling should also be kept ≤ 30 µA.**

MPM GPIO Pins

The GPIO pins which can detect an interrupt during MPM shutdown include:

GPIO pin	Alt. function
GPIO[114]	LCDC_BLUE[6]
GPIO[112]	UART3_RX LCDC_GREEN[0]
GPIO[94]	
GPIO[92]	SDC3_DATA[1]
GPIO[86]	UART3_RX UIM2_PWR_EN TSIF_DATA
GPIO[83]	PA_ON1
GPIO[71]	AUX_PCM_CLK SDAC_CLK GRFC[11] PA_ON2
GPIO[70]	AUX_PCM_SYNC SDAC_L_R_N GRFC[12] SYNC_TIMER1
GPIO[66]	SDC2_DATA[1]
GPIO[53]	SDC1_DATA[1]

GPIO pin	Alt. function
GPIO[49]	UART2_CTS_N UIM1_PWR_EN
GPIO[45]	UART1_RX UART1DM_RX TSIF_DATA
GPIO[42]	KEYPAD[0] ETM9_TRDATA0
GPIO[41]	KEYPAD[1] ETM_TRDATA[1]
GPIO[40]	KEYPAD[2] ETM_TRDATA[2]
GPIO[39]	ETM_TRDATA[3]
GPIO[38]	KEYPAD[4] ETM_TRDATA[4]
GPIO[37]	KEYPAD[5] ETM_TRDATA[5]
GPIO[36]	KEYPAD[6] ETM_TRDATA[6]
GPIO[29]	SYNC_TIMER2 CAM_AFC0 ETM9_PIPESTAT[0] ETM11_TRACEDATA0
GPIO[28]	ASYNC_TIMER2B CAM_AFC1 GP_MN ETM_GPIO_IRQ

GPIO pin	Alt. function
GPIO[27]	ASYNC_TIMER2A CAM_AFC2 GP_CLK ETM9_PIPESTAT1 ETM11_TRACECTL
GPIO[24]	PM_INT_N ETM_GPIO2_CS_N
GPIO[21]	UART2DM_RX SDC4_DATA[1] SDC3_DATA[5] ETM_KEYSENSE_IRQ
GPIO[20]	UART2DM_CTS_N SDC4_DATA[2] SDC3_DATA[6] ETM_TRDATA[14]
GPIO[19]	UART1_RI UART2DM_RFR_N SDC4_DATA[3] SDC3_DATA[7] ETM_TRDATA[15]
GPIO[18]	CAM_SHTR ASYNC_TIMER1B ETM_PIPESTATB2
GPIO[17]	CAM_FLASH ASYNC_TIMER1A ETM_PIPESTATB1

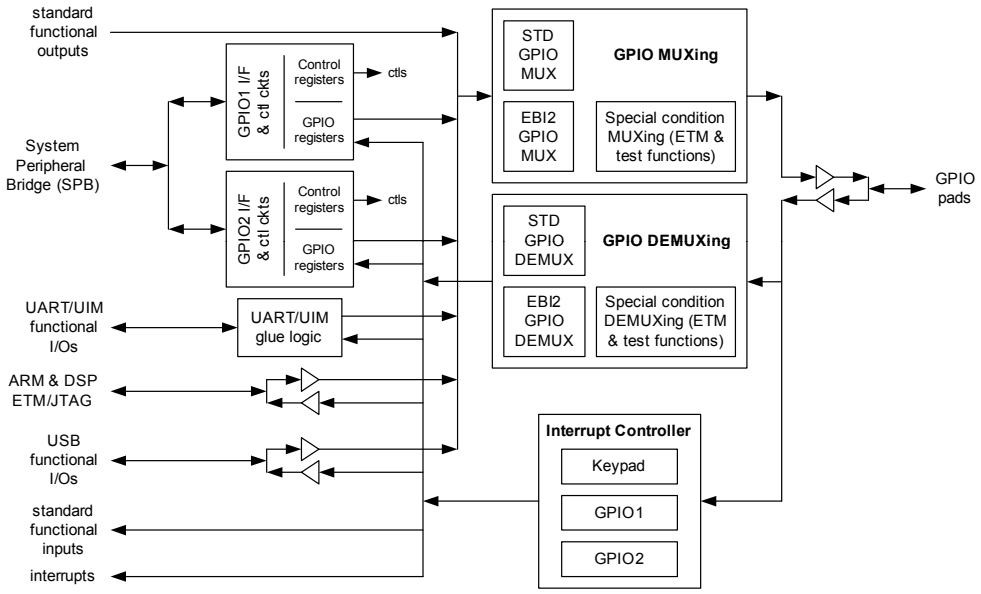
Top-level Mode Multiplexer

- **The top-level mode multiplexer (TLMM) provides a convenient mechanism for sharing multiple internal functions on the same set of GPIO pads.**
- **The mode assignment for each set of GPIOs is specified using a combination of input pin settings and software-programmed register settings.**
- **The use of TLMM allows for higher-level instructions, resulting in faster and easier GPIO assignments.**
  - Without TLMM, each GPIO pad would require individual programming.

TLMM Modes

- **TLMM provides three modes of software-controlled MUXing (or deMUXing) of the MSM7627 I/Os.**
  - **GPIO Group 1**: Most GPIOs fall into this category ([132:107], [97:43], and [15:0]). These GPIOs are configured as inputs on powerup, and then set by software to the desired functionality.
  - **GPIO Group 2**: These are primarily GPIOs used in ETM modes (GPIO[42:16]).
  - **Special Condition GPIO:**
    - **MPM:** GPIO[106:104] are used by the modem power manager during a chip power collapse
    - **EBI2**: GPIO[103:98] falls into this category; these GPIO pads are used for EBI2 functions on power up.

TLMM Architecture



GPIO Configuration

- **The MSM7627 IC GPIO pin functionality is controlled through the following registers:**
  - GPIO_OUT_x: contains output values for enabled GPIO pins
  - GPIO_OE_x: output enabled for GPIO pins
  - GPIOx_CFG: alternate functions, drive strength, pull configuration
    - GPIOx_PAGE is used to select the GPIO pin to configure.
  - GPIO_IN_x: Contains the GPIO input value

Note: Refer to the *MSM7627 Mobile Station Modem Software Interface Manual* (80-VM151-2) for more information about GPIO registers.

GPIO Programming (1 of 2)

GPIO programming is performed by two files:

- **TLMM.h: Configures GPIOs in the TLMM for use in certain modes of operation.**
  - **USIM, I²C, CAM IF, USB, BT**

- Example code

```
#elif defined (TLMM_UIM_USB_BT_MODE)
#define TLMM_USES_RUIM2
#define TLMM_USES_BT
#define TLMM_USES_USB
#define TLMM_USES_MMC1
```

- Function call

```
#if defined( TLMM_USES_RUIM2)
#define GPIO_84_SIGNAL      GPIO_IN_84
#elif defined( TLMM_USES_UART2)
#define GPIO_84_SIGNAL UART3_DP_TX_DATA
#else
#define GPIO_84_SIGNAL      GPIO_GENERIC_DEFAULT
#endif
```

GPIO Programming (2 of 2)

GPIO programming is performed by two files (cont.):

- **GPIO.h: This file lists all the declarations and functions necessary to support interaction with TLMM functions.**

- Example code

GPIO_OUT_84 = GPIO_OUT(84,4),

GPIO_IN_84 = GPIO_IN (84,4,GPIO_PULL_DOWN),

UART3_DP_TX_DATA = GPIO_ALT(84,4,1,GPIO_PULL_DOWN),

UIM2_DATA = GPIO_ALT(84,4,2,GPIO_NO_PULL)

GPIO Table (1 of 4)

GPIO	MSM7627 functions
132	**SPI_SCLK**
131	**SPI_CS**
130	**LCDC_GREEN[5]**
129	LCDC_DEN EBI2_ADR[23]
128	**LCDC_HSYNC** EBI2_ADR[22]
127	**LCDC_VSYNC** EBI2_ADR[21]
126	**LCDC_BLUE[0]** EBI2_ADR[20]
125	**LCDC_BLUE[1]** EBI2_ADR[19]
124	
123	UART1_TX
122	UART1_RX
121	**LCDC_GREEN[2]**
120	**LCDC_GREEN[3]**
119	**LCDC_GREEN[4]**

GPIO	MSM7627 functions
118	**LCDC_BLUE[2]**
117	**LCDC_BLUE[3]**
116	**LCDC_BLUE[4]**
115	**LCDC_BLUE[5]**
114	**LCDC_BLUE[6]**
113	**LCDC_BLUE[7]**
112	**LCDC_GREEN[0]** UART3_RX
111	UART3_TX **LCDC_GREEN[1]**
110	PA_ON2
109	SDC4_CLK
108	SDC4_DATA[0] UART2DM_TX SDC3_DATA[4]
107	SDC4_CMD
MPM_2	PMIC_SSBI MPM_GPIO[2]
MPM_1	TCXO_EN MPM_GPIO[1]
MPM_0	PA_RANGE1 MPM_GPIO[0] GP_PDM[0]

GPIO	MSM7627 functions
103	AUX_TCK EBI2_CS3_N **SPI_SDI**
102	AUX_TRST_N EBI2_CS2_N **SPI_SDO**
101	AUX_RTCK EBI2_RSVD
100	AUX_TDO EBI2_ADV_N **LCDC_RED[7]**
99	AUX_TDI EBI2_ADR[18] **LCDC_RED[6]**
98	AUX_TMS EBI2_ADR[17] **LCDC_RED[5]**
97	MDP_VSYNC_P
96	AUX_I2C_SDA
95	BOOT_SCUR AUX_I2C_SCL
94	
93	SDC3_DATA[0] AUDIO_CABLE_DET_N

Text highlighted in red indicates pins which are currently used on FFA.

Text highlighted in **bold** indicates pins which are different with FFA7625 default settings.

GPIO Table (2 of 4)

GPIO	MSM7627 functions
92	SDC3_DATA[1] MONO_STEREO_HS_N
91	SDC3_DATA[2]
90	SDC3_DATA[3]
89	SDC3_CMD CAMIF_RESET
88	SDC3_CLK **LCD_DAC_RESET_N**
87	UART3_TX UIM2_DATA USB_UICC_OE_N TSIF_SYNC
86	UART3_RX UIM2_PWR_EN TSIF_DATA
85	UART3_CTS_N UIM2_RESET USB_UICC_VM TSIF_EN
84	UART3_RFR_N UIM2_CLK USB_UICC_VP TSIF_CLK
83	PA_ON1 BT_WAKEUP

GPIO	MSM7627 functions
82	MDP_VSYNC_S
81	GRFC[0] – EXT_GPS_LNA_EN
80	GRFC[1] – GSM_PA_EN ASYNC_TIMER1B ASYNC_TIMER2B
79	GRFC[2] - GSM_PA_BAND
78	GRFC[3]
77	GRFC[4] ASYNC_TIMER1A ASYNC_TIMER2A
76	GRFC[5] SYNC_TIMER1 SYNC_TIMER2
75	GRFC[6] - ANT_SEL0
74	GRFC[7] - ANT_SEL1
73	GRFC[8] - ANT_SEL2
72	GRFC[9] - ANT_SEL3
71	GRFC[11] PA_ON2 AUX_PCM_SYNC SDAC_CLK
70	GRFC[12] AUX_PCM_SYNC SDAC_L_R_N SYNC_TIMER1

GPIO	MSM7627 functions
69	GRFC[13] AUX_PCM_DIN SDAC_MCLK TSIF_NULL
68	GRFC[14] AUX_PCM_DOUT SDAC_DOUT TSIF_ERROR
67	SDC2_DATA[0]
66	SDC2_DATA[1]
65	SDC2_DATA[2]
64	SDC2_DATA[3]
63	SDC2_CMD
62	SDC2_CLK
61	I2C_SDA
60	I2C_SCL
59	SSBI_2*
58	SSBI_1*
57	SSBI_0*
56	SDC1_CLK
55	SDC1_CMD
54	SDC1_DATA[0]

For detailed SSBI configuration for RTR6500/RTR6285, refer to *MSM7627 Baseband Reference Schematic* (80-VM151-41)

GPIO Table (3 of 4)

GPIO	MSM7627 functions
53	SDC1_DATA[1]
52	SDC1_DATA[2]
51	SDC1_DATA[3]
50	UART2_TX* UIM1_DATA
49	UART2_CTS_N* UIM1_PWR_EN **SDC1_CARD_DET**
48	UART2_RX UIM1_RESET
47	UART2_RFR_N UIM1_CLK
46	UART1_TX UART1DM_TX TSIF_SYNC
45	UART1_RX UART1DM_RX TSIF_DATA
44	UART1_CTS_N UART1DM_CTS_N TSIF_EN
43	UART1_RFR_N UART1DM_RFR_N TSIF_CLK

GPIO	MSM7627 functions
42	KEYPAD[0] ETM9_TRDATA[0] MSM_WAKES_BT
41	KEYPAD[1] ETM_TRDATA[1]
40	KEYPAD[2] ETM_TRDATA[2]
39	KEYPAD[3] ETM_TRDATA[3]
38	KEYPAD[4] ETM_TRDATA[4]
37	KEYPAD[5] ETM_TRDATA[5]
36	KEYPAD[6] ETM_TRDATA[6]
35	KEYPAD[7] ETM_TRDATA[7]
34	KEYPAD[8] ETM_TRDATA[8]
33	KEYPAD[9] ETM_TRDATA[9]
32	KEYPAD[10] ETM_TRDATA[10]
31	KEYPAD[11] ETM9_TRSYNC

GPIO	MSM7627 functions
30	SYNC_TIMER1 ETM_TRACECLK DRX_MODE_SELECT_A
29	ETM9_PIPESTAT[0] ETM11_TRDATA0 SYNC_TIMER2 CAM_AFC0
28	GP_MN ETM_GPIO_IRQ ASYNC_TIMER2B CAM_AFC1
27	GP_CLK ETM9_PIPESTAT[1] ETM11_TRACECTL ASYNC_TIMER2A CAM_AFC2
26	ETM_PIPESTAT[2]
25	PS_HOLD ETM_TRDATA[11]
24	PM_INT_N ETM_GPIO2_CS_N
23	ETM_TRDATA[12] DRX_MODE_SELECT_B
22	PA_ON1 ETM_TRDATA[13]
21	UART2DM_RX SDC4_DATA[1] SDC3_DATA[5] ETM_KEYSENSE_IRQ

UART2_TX and UART2_CTS_N have been switched on GPIO49 and GPIO50 compared with MSM7625 for enabling emergency download.

GPIO Table (4 of 4)

GPIO	MSM7627 functions
20	UART2DM_CTS_N SDC4_DATA[2] SDC3_DATA[6] ETM_TRDATA[14]
19	UART1_RI UART2DM_RFR_N SDC4_DATA[3] SDC3_DATA[7] ETM_TRDATA[15]
18	CAM_SHTR ASYNC_TIMER1B ETM_PIPESTATB2
17	CAM_FLASH ASYNC_TIMER1A ETM_PIPESTATB1
16	WDOG_STB MDP_VSYNC_E ETM_PIPESTATB0
15	CAMIF_MCLK
14	CAMIF_VSYNC_IN
13	CAMIF_HSYNC_IN
12	CAMIF_PCLK
11	CAMIF_DATA11
10	CAMIF_DATA10
9	CAMIF_DATA9

GPIO	MSM7627 functions
8	CAMIF_DATA8
7	CAMIF_DATA7
6	CAMIF_DATA6
5	CAMIF_DATA5
4	CAMIF_DATA4
3	CAMIF_DATA3
2	CAMIF_DATA2
1	CAMIF_DATA1
0	CAMIF_DATA0

GPIO Mux Table

GPIOs	Rail	Voltage(s)	FFA default	Alternate 1	Alternate 2	Comments
GPIO [87:86]	P10	2.85V/1.8V		UART3	UIM2	
GPIO [85:84]	P10	2.85V/1.8V	UICC-USB			
GPIO [50:47]	P10	2.85V/1.8V	UIM1	UART2		SIM card
GPIO [131]	P8	2.6V/1.8V		MISC		Miscellaneous interfaces
GPIO [132]	P9	2.6V/1.8V				
GPIO [121:111]	P8	2.6V/1.8V	LCDC			LCDC (RGB)
GPIO [130]	P9	2.6V/1.8V				
GPIO [129:125]	P9	2.6V/1.8V		EBI2 (addr)		LCDC (RGB) or EBI2
GPIO [100:98]	P2	1.8V				LCDC (RGB) or EBI2
GPIO [103:101]	P2	1.8V				EBI2
GPIO [110] GPIO [106:104]	P3	2.6V	PMIC, RF			BB-PMIC and RF interfaces
GPIO [124:122] GPIO [97, 94]	P3	2.6V		MISC		Miscellaneous interfaces
GPIO [93:88]	P3	2.6V		SDC3		
GPIO [83:72]	P3	2.6V	GRFC			General RF controls
GPIO [71:68]	P3	2.6V		AUX_PCM	SDAC	PCM or Stereo DAC
GPIO [67:62]	P3	2.6V		SDC2		BT/WLAN interface option
GPIO [61:60]	P3	2.6V	I2C			I2C bus
GPIO [59:57]	P3	2.6V	SSBI, RF			BB-RF interface
GPIO [56:51]	P3	2.6V	SDC1			SD card (4-bits)
GPIO [46:43]	P3	2.6V		UART1 / UART1DM	TSIF	BT/WLAN interface option
GPIO [42:31]	P3	2.6V	KEYPAD [0:11]			Keypad
GPIO [30:27]	P3	2.6V		TIMER1 / TIMER2		Async & sync timers
GPIO [26:22] GPIO[16]	P3	2.6V	PMIC, RF			BB-PMIC and RF interfaces
GPIO [109:107] GPIO [21:19]	P3	2.6V		SDC4 / SDC3 (bits [7:4])	UART2DM	
GPIO [18:17]	P3	2.6V	CAMIF (shutter, flash)			Camera shutter & flash
GPIO [15:0]	P4	2.6V/1.8V	CAMIF			Camera
GPIO [96] GPIO [95]	P4	2.6V/1.8V	-- BOOT_SCUR	AUX_I2C		

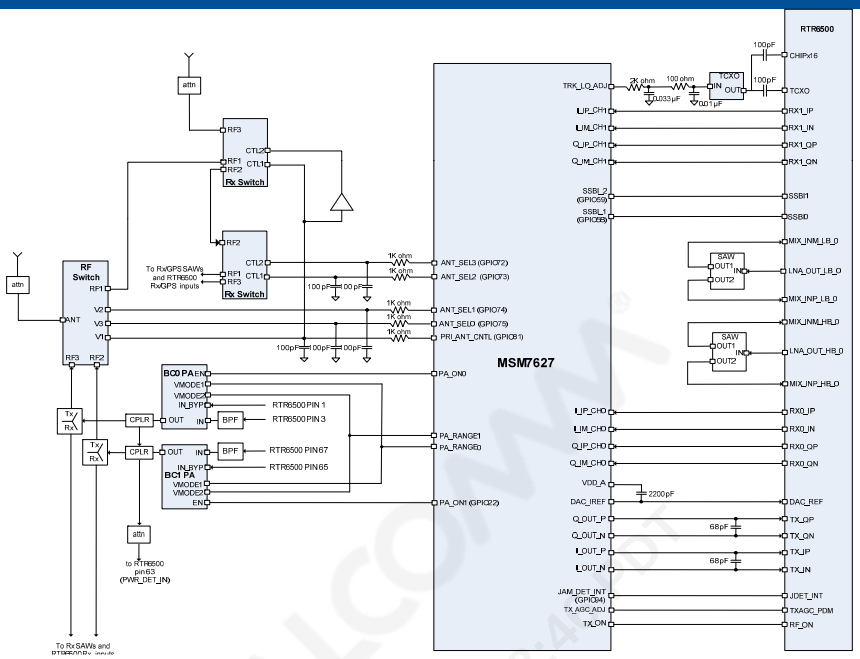
GPIO Design Considerations

- **USIM should use GPIO[50:47] since it is the software default**
  - Leave GPIO[87:84] and GPIO[49] open if supporting dual-voltage USIM.
- **PA_ON2 must use GPIO[110].**
- **I²C primarily uses GPIO[61:60] (2.6 V).**
  - AUX_I2C GPIO[96:95] (1.8 V/2.6 V) could be used for I²C only when EFUSE is blown
  - Only one I²C controller in the MSM device

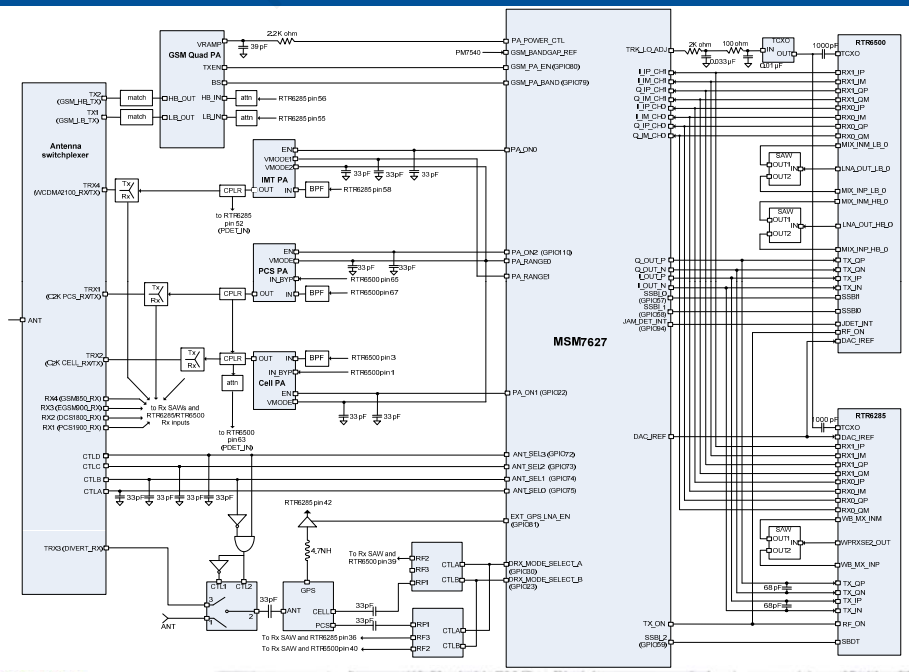
QUALCOMM 2010.07.13 ruijun.zhang-sim.com

MSM7627 RF Analog Interface

RF-Baseband Interface (1x only)



RF-Baseband Interface (Multimode)



General RF Control Signals

GRFC	MSM signal	RF signal name	Device connection: 1x Only	Device connection: Multi Mode	Description
	PA_ON	PA_ON0	BC0 PA	IMT PA	PA enable
	GPIO[22]	PA_ON1	BC1 PA	Cell PA	PA enable
	GPIO[110]	PA_ON2	N/A	PCS PA	PA enable
	PA_R0	PA_R0	BC0 & BC1 PA	IMT,PCS & Cell PA	power-mode selection
	GPIO[104]	PA_R1	BC0 & BC1 PA	IMT PA	power-mode selection
GRFC[9]	GPIO[72]	ANT_SEL3	DRX Switch	PRX Antenna Switch	Antenna SEL signals
GRFC[8]	GPIO[73]	ANT_SEL2			
GRFC[7]	GPIO[74]	ANT_SEL1	PRX Switch		
GRFC[6]	GPIO[75]	ANT_SEL0			
GRFC[10]	TX_ON	TX_ON	RTR6500	RTR6285 & RTR6500	RTR6500/6285 RF-enable signal
GRFC[2]	GPIO[79]	GSM_PA_BAND	N/A	GSM quad-band power amplifier	Quad-band GSM PA-band selection
GRFC[1]	GPIO[80]	GSM_PA_EN	N/A	GSM quad-band power amplifier	Quad-band GSM PA-enable signal
GRFC[0]	GPIO[81]	PRI_ANT_CTNL	PRX Switch	N/A	Antenna SEL signals
		EXT_GPS_LNA_EN	N/A	External LNA Module for GPS	GPS amplifier enable signal
	GPIO[30]	DRX_MODE_SELECT_A	N/A	DRX Switch	DRX Switch SEL signals
	GPIO[23]	DRX_MODE_SELECT_B			

MSM7627 Device Interfaces
Memory (EBI1 and EBI2)

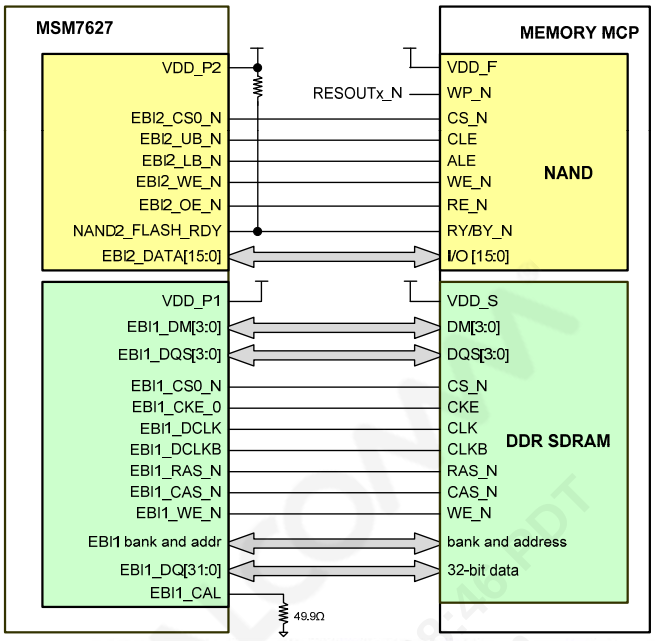
Supported Memory Configurations

- **Supported memory types**
  - External bus interface 1 (EBI1) supports high-speed, high-performance memory devices.
    - 32-bit DDR SDRAM (low-power DDR, 200 MHz)
  - External bus interface 2 (EBI2) supports lower-speed devices
    - 8-bit or 16-bit NAND (512 and 2048 bytes/page)
    - 16-bit, 18-bit or 24-bit LCD support
    - 16-bit OneNAND (MUXed mode only)
- **Primary memory configuration**
  - 8-bit NAND (EBI2) + 32-bit DDR SDRAM (EBI1)
  - Testing and verification to date was performed on NAND + DDR SDRAM configurations.
  - Tested devices are listed in flash_nand_xxx.c of the AMSS driver archive (xxx = manufacturer's name) of the AMSS driver's archive.

Memory Requirement

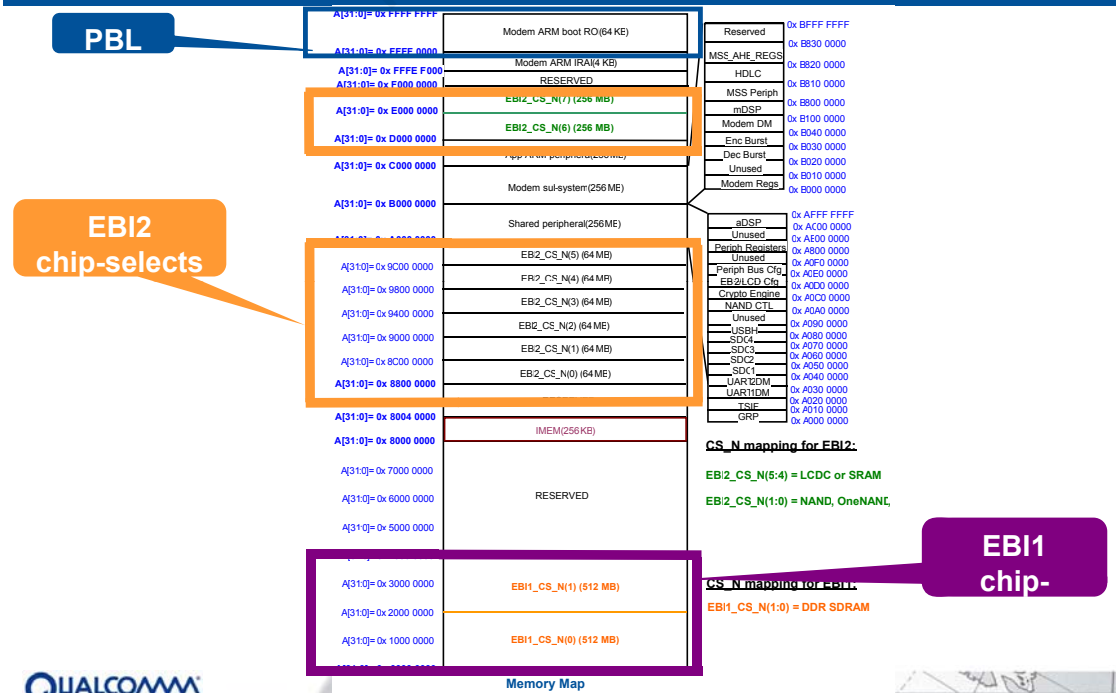
- **DDR SDRAM**
  - **JEDEC Standard JESD209A compliant**
  - **Meet with LPDDR400 timing requirement (Target)**
- **NAND**
  - **ONFI 1.0 compliant**
- **Synchronous OneNAND**
  - **Clock frequency at 100 MHz (Target)**

Typical Memory Connection



Qualcomm Confidential and Proprietary
MAY CONTAIN U.S. AND INTERNATIONAL EXPORT CONTROLLED INFORMATION

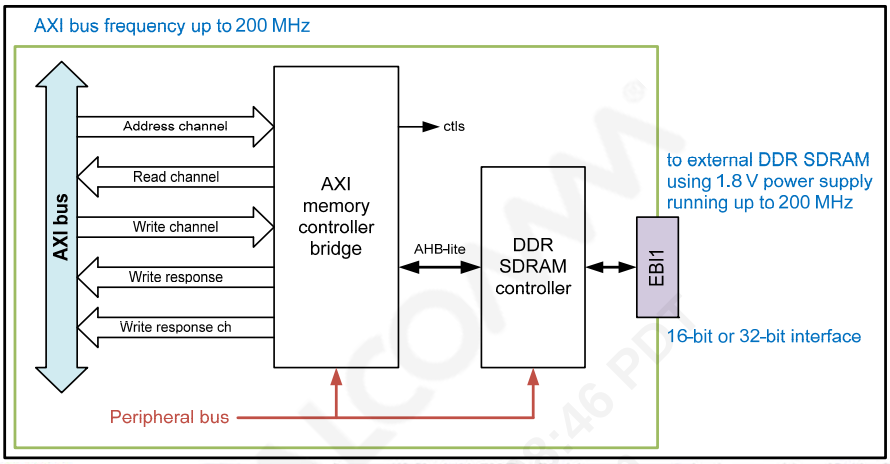
MSM7627 Memory Map



Qualcomm Confidential and Proprietary
MAY CONTAIN U.S. AND INTERNATIONAL EXPORT CONTROLLED INFORMATION

EBI1

- Features
  - Support only for low-power memories at 1.8 V I/O power supply
  - Bus frequencies up to 200 MHz (DDR SDRAM mode)
  - EBI1 auto-calibration
    - EBI1_CAL connected with ground through 49.9 Ω resistor for calibration
    - Close to MSM



EBI1 Pins

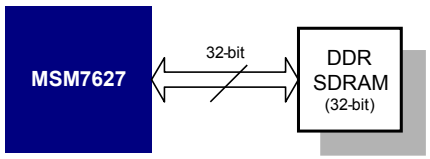
- 67 dedicated pins
- Supports DDR-SDRAM
- 2 chip selects
- 14 address lines, 32 data lines
- 1 calibration pin
- 1.8 V interface

EBI1 Pin Connections

Signal name	I/O	Voltage domain	Description	Comments
EBI1_ADR[13:0]	DO	P1	14-bit EBI1 address bus; ADR[13] is the MSB, ADR[0] is the LSB.	
EBI1_DQ[31:0]	B	P1	32-bit EBI1 data bus; DQ[31] is the MSB, DQ[0] is the LSB.	
Other EBI1 signaling				
EBI1_DQS[3:0]	B	P1	EBI1 data strobes	
EBI1_DM[3:0]	DO	P1	EBI1 data masks	
EBI1_DCLK	B	P1	Differential clock for DDR SDRAM	
EBI1_DCLKB	B	P1		
EBI1_CS1_N	DO	P1	DDR SDRAM chip select	
EBI1_CS0_N	DO	P1		
EBI1_CKE1	DO	P1	DDR clock enables	
EBI1_CKE0	DO	P1		
EBI1_RAS_N	DO	P1	DDR RAS_N	
EBI1_WE_N	DO	P1	EBI1 write enable	
EBI1_CAS_N	DO	P1	DDR CAS_N	
EBI1_BA[1]	DO	P1	Bank selection	
EBI1_BA[0]	DO	P1	Bank selection	
EBI1_CAL	AI	P1	EBI1 calibration pad	

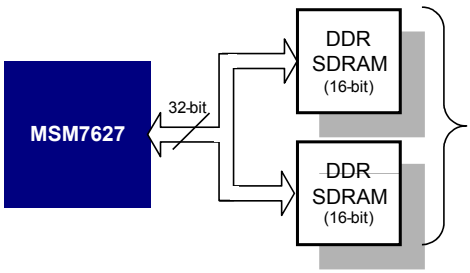
EBI1 Supported Configurations

Configuration 1



For 32-bit DDR SDRAM

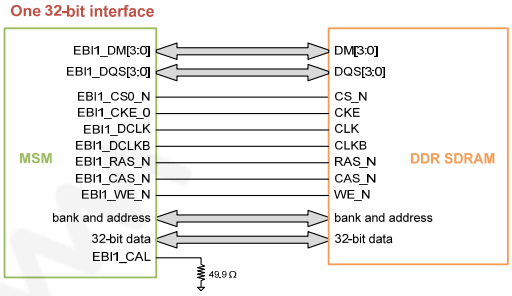
Configuration 2



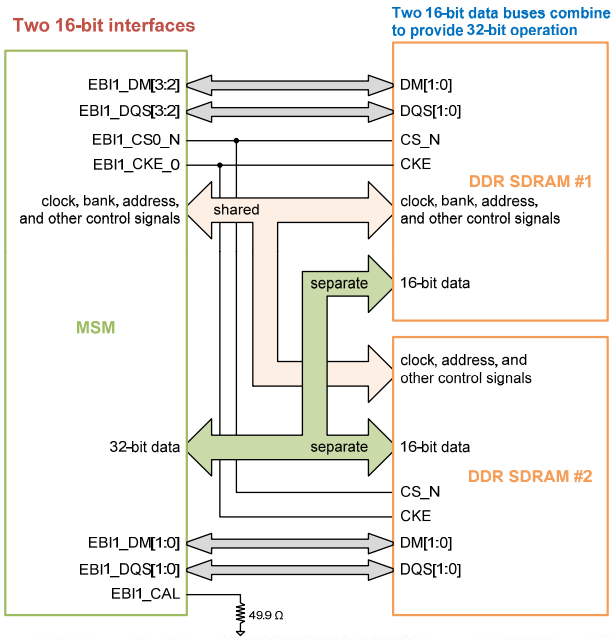
Two 16-bit DDR SDRAM combined for 32-bit operation. Bus loading may limit actual clock speed.

DDR SDRAM Support (1 of 2)

- **MSM7627 IC supports 32-bit external DDR SDRAM devices**.
- **MSM7627 IC supports self-refresh**.
  - One CKE for each chip-select signal
  - Each SDRAM can be powered down individually.
- **Supported configurations include**:
  - Single 32-bit DDR device
  - 32-bit DDR device (2 × 16-bit)
- **Due to extremely high data rates, hence timing is very crucial.**
  - Care must be taken during trace layout and design.
  - Refer to the *MSM7627 Mobile Station Modem User Guide* (80-VM151-3) for more information regarding design guidelines for the DDR SDRAM.

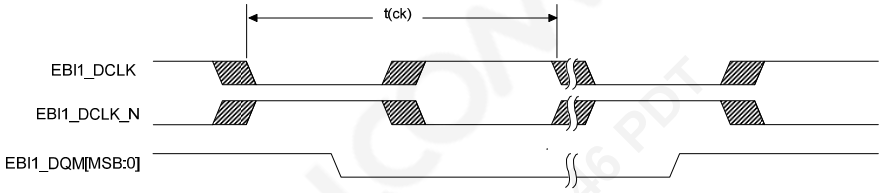


DDR SDRAM Support (2 of 2)



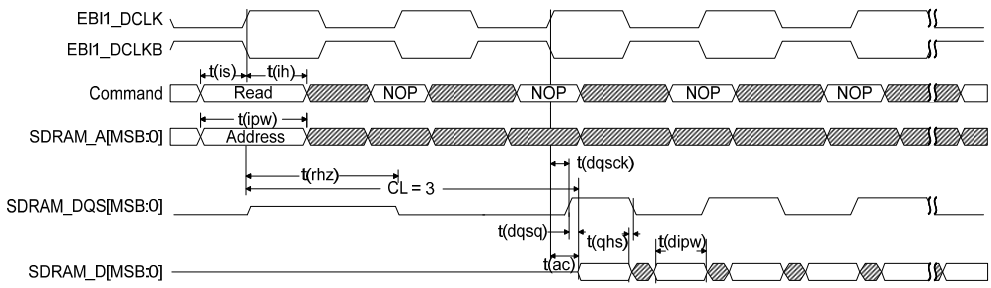
DDR SDRAM Clock

- The power supply of the DDR component needs sufficient decoupling capacitors. Refer to the *MSM7627 Baseband Reference Schematic* (80-VM151-41).
- EBI1_DCLK and EBI1_DCLKB are differential clock outputs.
- All address and control signals are sampled at the rising edge of DCLK and falling edge of DCLKB.
- All data signals are sampled at the crossing of DCLK and DCLKB.
- This effectively doubles the data rate, since the signal is sampled at both the rising and falling edges of the clock signal.

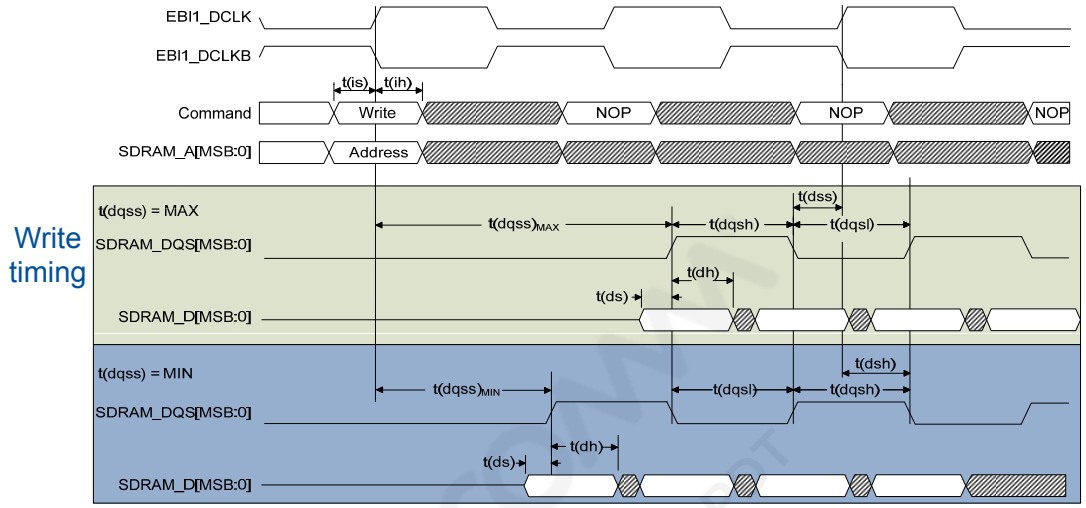


DDR SDRAM Access Timing (1 of 2)

Read timing



DDR SDRAM Access Timing (2 of 2)



DDR SDRAM Design Considerations

- The extremely high data rates demand very careful timing calculations and controlled impedance routing.
- Long PCB traces, excessive parasitic capacitance, or similar layout issues can degrade or violate signal integrity.
- The various DDR signals can be grouped into these categories:
  - Clocks
  - Data
  - Address/command
  - Control
  - Power
- Special considerations for each group need to be taken; some of the important considerations are listed in the following slides.

DDR Differential Clock Considerations

- Use controlled impedance lines for each of the two traces.
- Route the traces in parallel and close to each other.
  - If the trace width is W, spacing between the traces should be on the order of 2 W to 3 W.
- The differential clock traces must have nearly equal length.
  - Maintain the trace length difference to be less than **40** mil.
  - Complementary phase relationship between the two signals will be degraded if the traces are of different trace lengths.
    - This can impact the timing and duty cycle.
- Other layout considerations:
  - Route the clock pair on the same critical layer to ensure clocks have similar signal integrity.
  - Maintain a solid ground reference for routed clocks, thereby providing a low-impedance path for return currents.

DDR DQ and DQS Signal Considerations (1 of 2)

- **The MSM7627 device drives the DQS signal to capture data during reads, and the DDR device drives DQS during writes.**
- **The timing difference between DQ and DQS signals needs to be minimized. Trace matching is very important.**
- **DQ and DQS signals are divided into four groups.**
  - EBI1_DQS[3] ↔ EBI_DQ[31:24]
  - EBI1_DQS[2] ↔ EBI_DQ[23:16]
  - EBI1_DQS[1] ↔ EBI_DQ[15:8]
  - EBI1_DQS[0] ↔ EBI_DQ[7:0]

DDR DQ and DQS Signal Considerations (2 of 2)

- **Layout considerations:**
  - Every eight bits of data and the corresponding DQS signal MUST have similar trace characteristics:
    - Trace length differences must be less than **80** mil for the entire group.
    - Capacitive loading must be similar.
  - Make sure to reduce cross-talk noise from adjacent signals on DQS signals.
    - Maintain at least 4 W spacing between DQS and other non-data group signals.

Other DDR Design Considerations (1 of 2)

- All address/command and control signals should have similar trace characteristics (trace length, capacitance, etc.).
  - Distance from the capacitor to the power pins being bypassed must not exceed 150 mil
- Use distributed and balanced decoupling.
- Keep the VDD_MSME trace as wide a trace as possible, and isolate the trace as much as possible with adjacent ground trace segments.

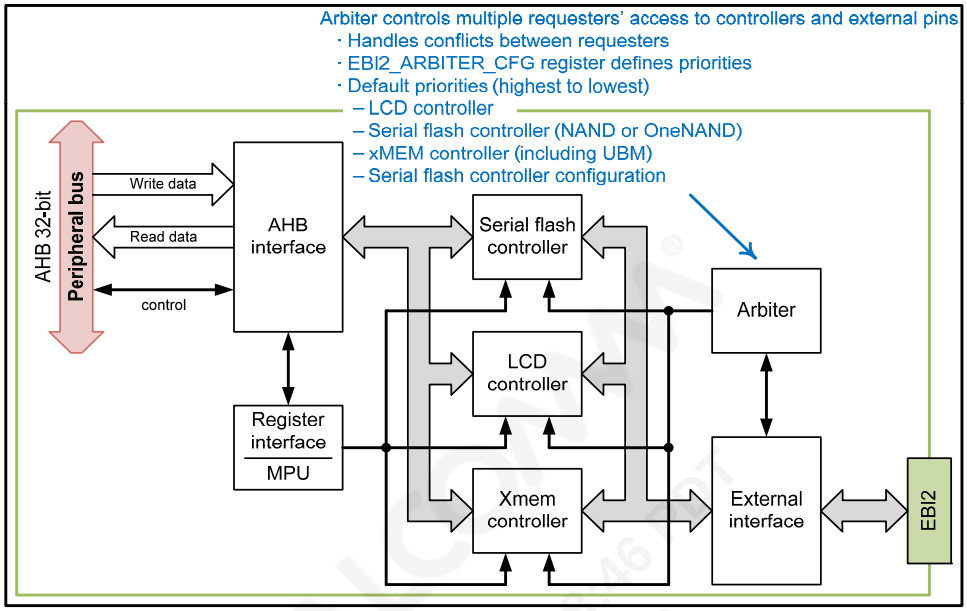
Other DDR Design Considerations (2 of 2)

- Provide a solid ground reference to all signals.
- Avoid crossing high-speed traces.
- Keep traces short and direct to minimize loss and undesired coupling.
- Refer to 80-V9038-54 (*DDR SDRAM DESIGN CONSIDERATIONS FOR MOBILE STATION MODEM(MSM) DEVICES) for more details.*

EBI2

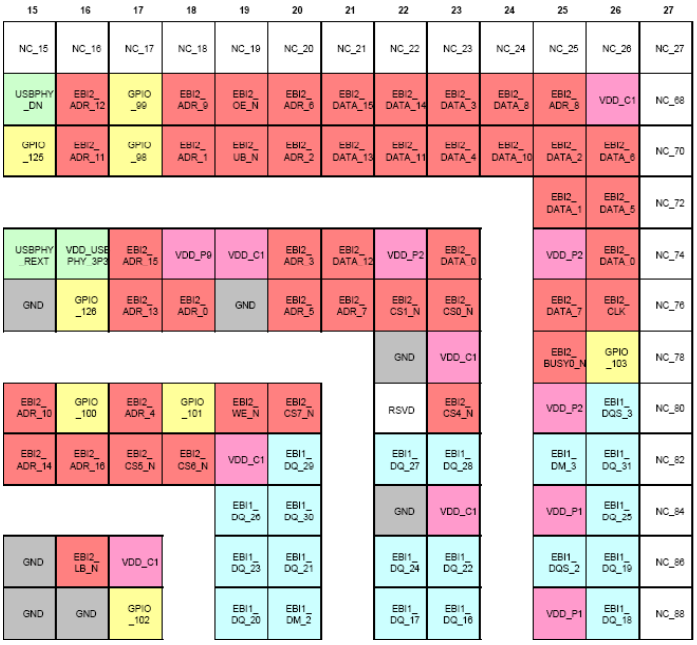
- **EBI2 provides support for slower peripheral devices.**
  - NAND flash memory
  - LCDs
  - Async devices
  - FLO receiver
  - OneNAND
- **The EBI2 controller includes three separate controllers:**
  - Serial flash controller
  - LCD controller
  - External memory controller
- **Supports 1.8 V or 2.6 V power supply voltages.**
- **Supports any generic external peripheral whose timing is similar to async memories.**

EBI2 High-Level Block Diagram



Qualcomm Confidential and Proprietary
MAY CONTAIN U.S. AND INTERNATIONAL EXPORT CONTROLLED INFORMATION

EBI2 Pins



- 51 dedicated pins
- Supports NAND, OneNAND, async/page mode memory devices, LCDs
- 8 chip-selects: 2 for NAND (OneNAND), 4 for async/page, and 2 for LCD
- 24 address lines, 16 data lines
- 1.8 V and 2.6 V interface

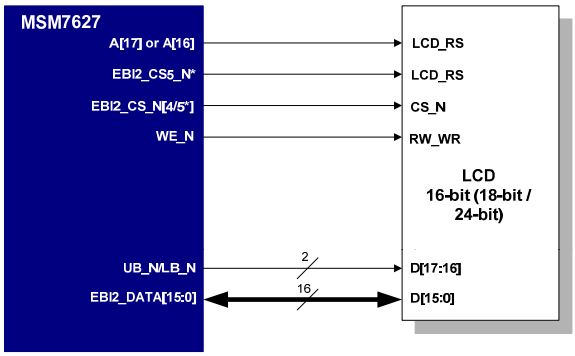
Qualcomm Confidential and Proprietary
MAY CONTAIN U.S. AND INTERNATIONAL EXPORT CONTROLLED INFORMATION

EBI2 Pin Connections

Signal name	I/O	Voltage domain	Description	Comments
EBI2_ADR[23:0]	B	P2	24-bit address bus; ADR[23] is the MSB, ADR[0] is the LSB.	
EBI2_DATA[15:0]	B	P2	16-bit data bus; DATA[15] is the MSB, DATA[0] is the LSB.	
Other EBI2 signaling				
EBI2_LB_N	DO	P2	Lower byte enable	Byte access of 16-bit memory
EBI2_UB_N	DO	P2	Upper byte enable	Byte access of 16-bit memory
EBI2_WE_N	DO	P2	Write enable	
EBI2_OE_N	DO	P2	Output enable	
EBI2_CS7_N	DO	P2	Chip select	
EBI2_CS6_N	DO	P2	Chip select	
EBI2_CS5_N	DO	P2	Chip select	Also used to select second LCD
EBI2_CS4_N	DO	P2	Chip select first LCD	
EBI2_CS3_N	DO	P2	Chip select	
EBI2_CS2_N	DO	P2	Chip select	
EBI2_CS1_N	DO	P2	Chip select second NAND	Chip select second OneNAND
EBI2_CS0_N	DO	P2	Chip select first NAND	Chip select first OneNAND
EBI2_BUSY0_N	DI	P2	Busy signal first NAND	
EBI2_CLK	DO	P2	EBI2 OneNAND clock	

LCD Device Support

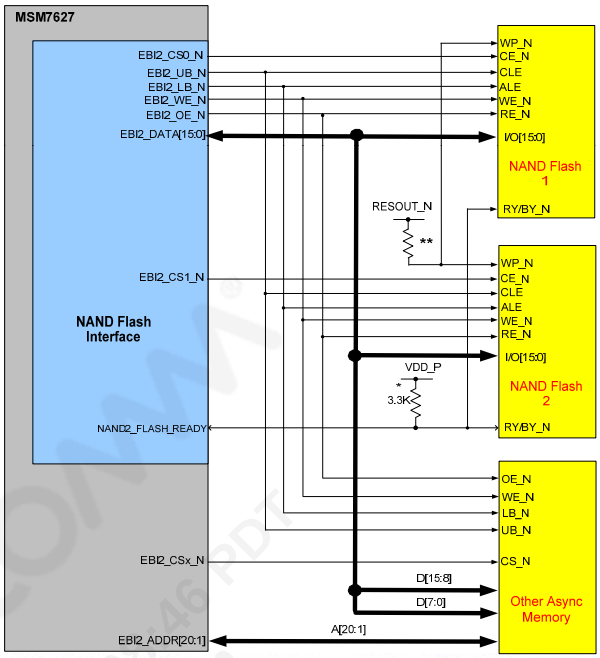
- **Supports 16-bit/18-bit/24-bit port-mapped LCDs**
- **Supports 16-bit read and 16-bit, 18-bit, and 24-bit writes through a parallel interface**
  - EBI2_UB/LB_N are used as LCD_DATA[17:16] for 18-bit LCD interface.
  - EBI2_UB/LB_N are used as LCD_DATA[17:16] and EBI2_ADR[6:1] are used as LCD_DATA[23:18] for 24-bit LCD interface.
- **Two chip selects available:**
  - EBI2_CS4_N (use A16 as LCD_RS for this chip select).
  - EBI2_CS5_N* (use A17 as LCD_RS for this chip select).
- **Intel timing**
  - Two chip selects are available.
- **Motorola timing**
  - One chip select is available (EBI2_CS4_N).
  - EBI2_CS5_N is used as LCD_EN.



***Note**: EBI2_CS5_N is not available in Motorola-style LCD devices; it is used as the LCD_EN signal.

NAND Memory Support

- **MSM7627 IC provides support for 8-bit and 16-bit NAND flash devices.**
- **Programmable page sizes of 512-byte and 2048-byte (256-byte is NOT supported).**
- **Hardware supports both MLC and SLC mass storage technologies.**
  - MLC NAND is not supported by software.
- **Error correction coding (ECC):**
  - 1-bit Reed-Solomon code is used to support SLC-based devices.
  - 4-bit Reed-Solomon code is used to support MLC-based devices.
  - For each 512 bytes of user data, 4 bytes of ECC is available.
    - For every 512 bytes of user data, there are 4 bytes of ECC data to recover 1 bit of user data.
- **NAND interface shares the EBI2 ports with other external SRAM devices.**
- **Two chip selects are available for NAND:**
  - EBI2_CS0_N
  - EBI2_CS1_N
- **Maximum addressable memory space of greater than 1 GByte.**
- **Note**: The MSM7627 does not support simultaneous NAND and OneNAND operation.

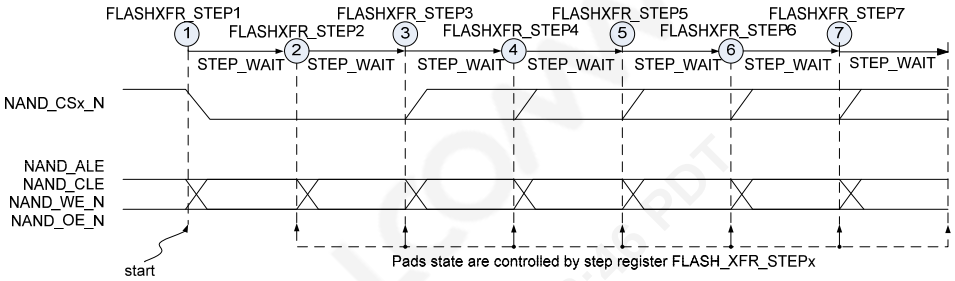


NAND Pin Connections

EBI2 pin	Direction	Voltage domain	NAND signal
EBI2_LB_N	DO	P2	NAND address latch enable
EBI2_HB_N	DO	P2	NAND command latch enable
EBI2_WE_N	DO	P2	NAND write enable
EBI2_OE_N	DO	P2	NAND output enable
EBI2_CS0_N	DO	P2	Chip select for first NAND
EBI2_CS1_N	DO	P2	Chip select for second NAND
EBI2_DATA[15:0]	B	P2	NAND data input/output [15:0]
EBI2_BUSY0_N	DI	P2	NAND ready/busy

NAND Interface Timing

- **Each access to NAND flash devices involves the controller executing a sequence of signal assertion and de-assertion, according to the timing requirements of the connected device.**
- **The transfer sequence is defined using registers FLASH_XFR_STEP(1 – 7).**
  - The register values dictate the signal status.
- **There are seven distinct configurations, including wait states:**
  - FLASH_XFR_STEP1 to FLASH_XFR_STEP7



NAND Flash Timing

- **Step configuration registers (FLASH_XFR_STEPn) are divided as follows:**
  - Bits [31:16]: Command and Address cycles
  - Bits [15:0]: Data cycles
- **If the step configuration is changed, then the timing parameters mapped to the registers can be adjusted accordingly.**

FLASH_XFR_STEPx (x = 1 to 7)			
Command/Address		Data	
31:30	CMD_SEQ_SETP_NUM	15:14	DATA_SEQ_STEP_NUMBER
29:26	CMD_STEP1_WAIT	13:10	DATA_STEP1_WAIT
25	CMD_AOUT_EN*	9	DATA_AOUT_EN*
24	CMD_DATA_EN	8	DATA_DATA_EN
23	CMD_CE_EN	7	DATA_CE_EN
22	CMD_CLE_EN	6	DATA_CLE_EN
21	CMD_ALE_PIN	5	DATA_ALE_PIN
20	CMD_WE_EN	4	DATA_WE_EN
19	CMD_RE_EN	3	DATA_RE_EN
18	CMD_WIDE	2	DATA_WIDE
17:16	RESERVED*	1:0	EXTA_READ_WAIT

* Not used

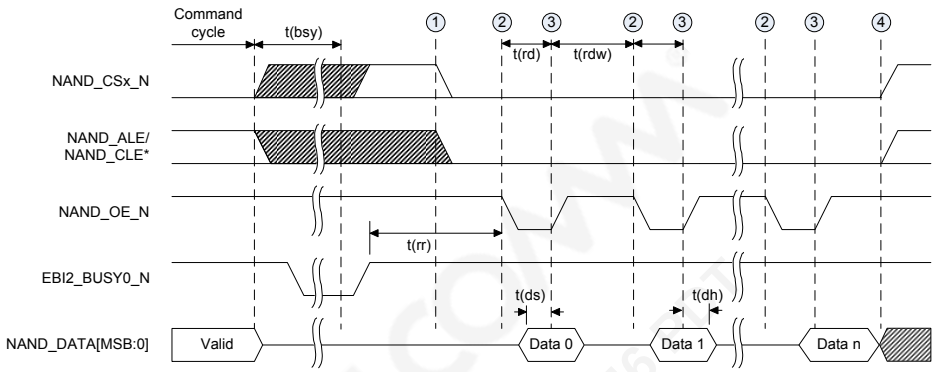
Notes:

1. ALE_PIN and CLE_EN bits are the "enable" control of the external pin. When set (1), the ALE and CLE are controlled by the NANDC sequencer. When clear (0), ALE and CLE are disabled (signal = low).
2. Read data wait can be incremented without changing the write data wait states using bits [1:0].

NAND Flash Timing Example

1. Assert CS_N (CS_N = 0).
2. Wait for CS_N-to-OE_N setup time for read from flash.
3. Assert OE_N (OE_N = 0) and read data.

Repeat for consecutive data reads.



* During data read wait period, ALE and CLE stay low only if NAND_CSx_N is driven low as required by the FLASH device.

OneNAND Support (1 of 3)

- **OneNAND is a NAND-type flash memory that operates through the NOR interface.**
- **Supported OneNAND configurations:**
  - Synchronous and asynchronous
  - 16-bit MUXed only OneNAND
- **Two chip selects are available for OneNAND:**
  - ONENAND_CS0_N (EBI2_CS0_N)
  - ONENAND_CS1_N (EBI2_CS1_N)
- **Simultaneous NAND and OneNAND operation is not supported.**
- **Boot from the OneNAND device is supported.**

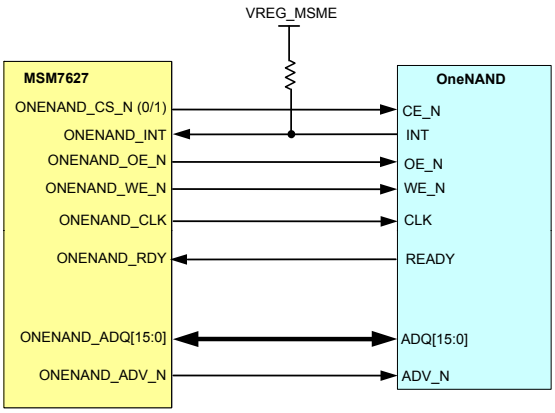
OneNAND Support (2 of 3)

OneNAND pin	EBI2 pin	Direction	Voltage domain	Description
ONENAND_CLK	EBI2_CLK	O	P2	Clock
ONENAND_INT	EBI2_BUSY0_N	I	P2	Interrupt
ONENAND_CS0_N	EBI2_CS0_N	O	P2	Chip select for first NAND
ONENAND_CS1_N	EBI2_CS1_N	O	P2	Chip select for second NAND
ONENAND_OE_N	EBI2_OE_N	O	P2	Output enable
ONENAND_WE_N	EBI2_WE_N	O	P2	Write enable
ONENAND_ADV_N	EBI2_LB_N	O	P2	Address valid detect
ONENAND_RDY	EBI2_ADR[9]	I	P2	Ready signal
ONENAND_ADQ[15:0]	EBI2_DATA[15:0]	B	P2	Multiplexed address/data bus [15:0]

Note: EBI2_ADV_N is not used for ONENAND_ADV_N.

OneNAND Support (3 of 3)

- **Dedicated configuration registers for each OneNAND chip select to allow different configurations for each chip select.**
- **The following operations are supported:**
  - Reset flash device
  - Read page
  - Program page
  - Erase block
  - Lock block
  - Unlock block
- **Memory protection unit (MPU) is available to secure multiple blocks in memory for security.**
  - Support for one OneNAND device

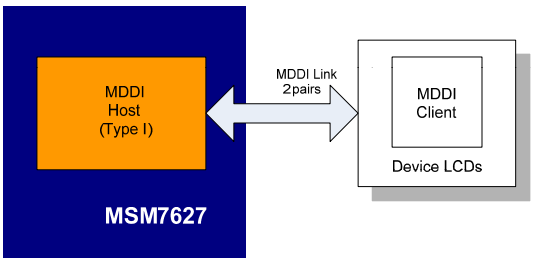


Note: 16-bit MUXed OneNAND interface example

MSM7627 Device Interfaces
MDDI

Mobile Display Digital Interface

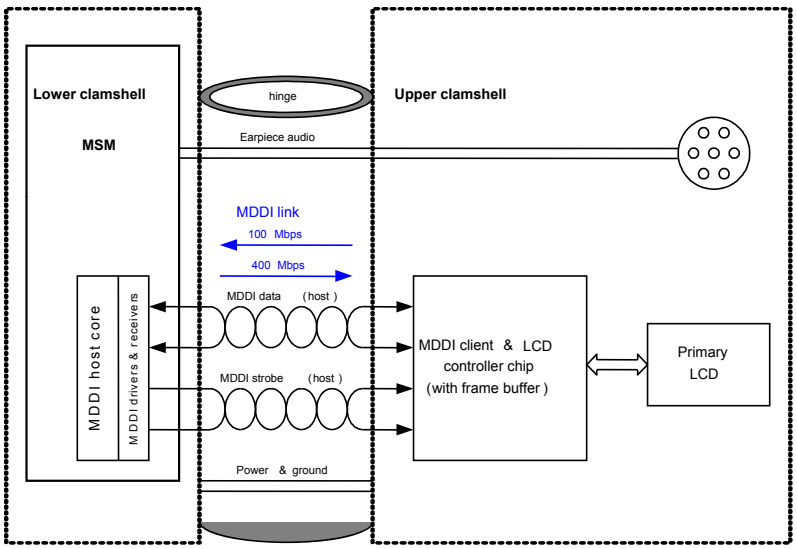
- **Mobile display digital interface (MDDI) is a cost-effective, low-power solution that enables high-speed, short-range communication between the MSM and display devices.**
- **The MSM7627 device has one dedicated MDDI interface.**
  - One host interfaces with LCD
- **One Type I MDDI host interface**
  - Two low-swing differential signal pairs (data and strobe)



MDDI Pin Connections

Signal name	I/O	Voltage	Description	Comments
Primary MDDI connections (LCD)				
MDDI_P_STB_N	AO	MDDI	LCD differential strobe pair	Low-swing differential signal; connects to MSM host; high-Z default state
MDDI_P_STB_P	AO	MDDI		
MDDI_P_DATA_N	AI, AO	MDDI	LCD differential data pair	Low-swing differential signal; connects to MSM host; high-Z default state
MDDI_P_DATA_P	AI, AO	MDDI		
MDDI power and ground				
VDD_MDDI		MDDI	MDDI power supply	From PM7540 IC; 1.8 V typ, programmable from 1.500 V to 3.050 V, in 50 mV steps
VSS_MDDI		GND	MDDI ground	

MDDI Flip-Phone Design



MDDI Vendors

MDDI vendor and part number	Status	Resolution primary (secondary)	Notes
Samsung S3CA460X ('MC4')	Available	QVGA	Media coprocessor and LCD controller IC QVGA
Samsung S6D0142	Available	QVGA	TFT LCD display driver with 320 × 240 262 k colors
Sharp LR38869 'Rodem'	Available	QVGA	
Rodem-WV	Available	WVGA	
Epson S1D13751		QVGA	Graphics engine and display driver MDDI
Epson L5F30376T0x		QVGA	1.98" TFT module
Epson L5F30415T0x		QVGA	2.22" TFT module
Renesas R61504	Available	QVGA	LCD IC controller with 16.77 M colors
Renesas		QVGA & WQVGA	Two MDDI driver ICs (COG)
Toshiba TC358720	Available	VGA (QCIF+)	Bridge chip, 'VeGA'
Toshiba TC358722	Available	WVGA	18 bpp

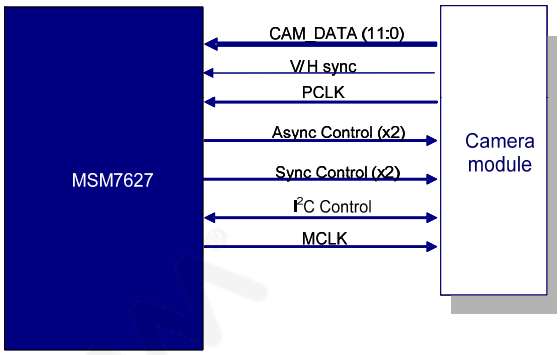
There are additional manufacturers with plans to produce MDDI displays up to VGA, including Sitronix and California Micro Devices.

2010.07.13 ruijun.zhang-sh.com

MSM7627 Device Interfaces
Parallel Camera

Camera Interface

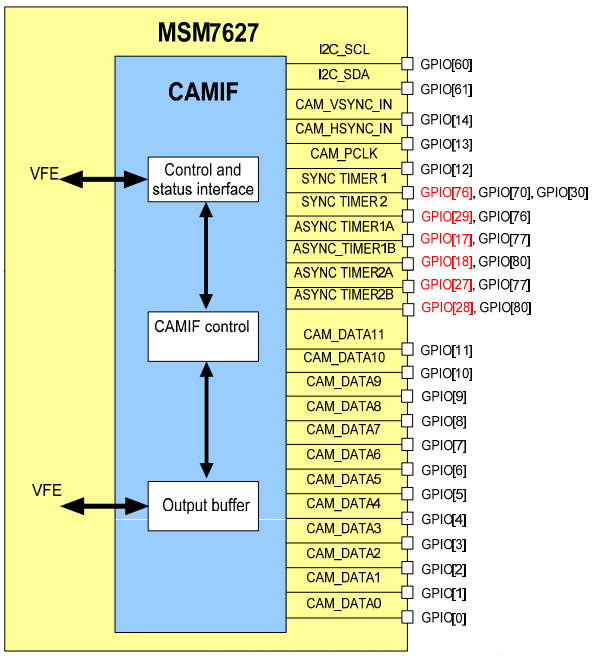
- **CAMIF_PCLK**
  - Up to 120 MHz
- **CAM_MCLK**
  - Generated by M/N counter
  - Can support several frequencies
- **CAMIF_VSYNC: frame sync input**
- **CAMIF_HSYNC: line sync input**
- **CAMIF_DATA: pixel data input**
- **Sync control: synchronous timer outputs (flash and mechanical shutter control)**
- **Async control: asynchronous timer outputs (auto-focus and zoom control)**
- **Camera module control through I²C interface**



Notes:
For 10/8-bit data input: use CAM_DATA[11:2] or CAM_DATA[11:4] respectively.

CAM_DATA[3:0] can be used as GPIOs if programmed
for noncamera function.

CAMIF Block Diagram



CAMIF Pin Connections (1 of 2)

Signal name	I/O	Voltage domain	Description	Comments
I2C_SDA GPIO[61]	B	P3	Serial control data	
I2C_SCL GPIO[60]	B	P3	Serial control clock	
CAM_VSYNC_IN GPIO[14]	DI	P4	Vertical sync	
CAM_HSYNC_IN GPIO[13]	DI	P4	Horizontal sync	
CAM_MCLK GPIO[15]	DO	P4	Master clock	
CAM_PCLK GPIO[12]	DI	P4	Pixel rate clock	
ASYNC_TIMER1A **GPIO[17]** GPIO[77]	DO	P3	Camera zoom and auto-focus control	
ASYNC_TIMER1B **GPIO[18]** GPIO[80]				
ASYNC_TIMER2A **GPIO[27]** GPIO[77]				
ASYNC_TIMER2B **GPIO[28]** GPIO[80]				

CAMIF Pin Connections (2 of 2)

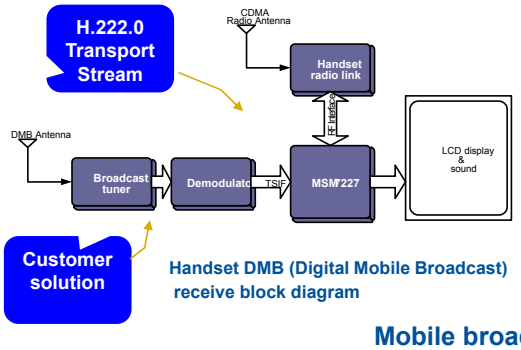
Signal name	I/O	Voltage domain	Description	Comments
SYNC_TIMER1 GPIO[70] **GPIO[76]** GPIO[30]	DO	P3	Camera flash and mechanical shutter control	
SYNC_TIMER2 **GPIO[29]** GPIO[76]				
CAM_DATA[11:0] GPIO[11:0]	DI	P4	Camera 12-bit data; Bit 11 is MSB; bit 0 is LSB	Bayer input data (preferred)
CAM_MRST	DO	---	Camera reset control signal	Can be software-controlled on any available GPIO

If a camera with other than 12-bit resolution is used, the MSB must be aligned between the MSM device and the camera, as shown in the table below:

Camera type	MSM signals	Camera signals
12-bit	CAM_DATA(11:0)	DATA(11:0)
10-bit	CAM_DATA(11:2)	DATA(9:0)
8-bit	CAM_DATA(11:4)	DATA(7:0)

MSM7627 Device Interfaces
Transport Stream Interface

Transport Stream Interface



Handset DMB (Digital Mobile Broadcast) receive block diagram

The handset's mobile broadcast implementation (see figure) that uses a separate, non-WCDMA radio link has its own antenna.

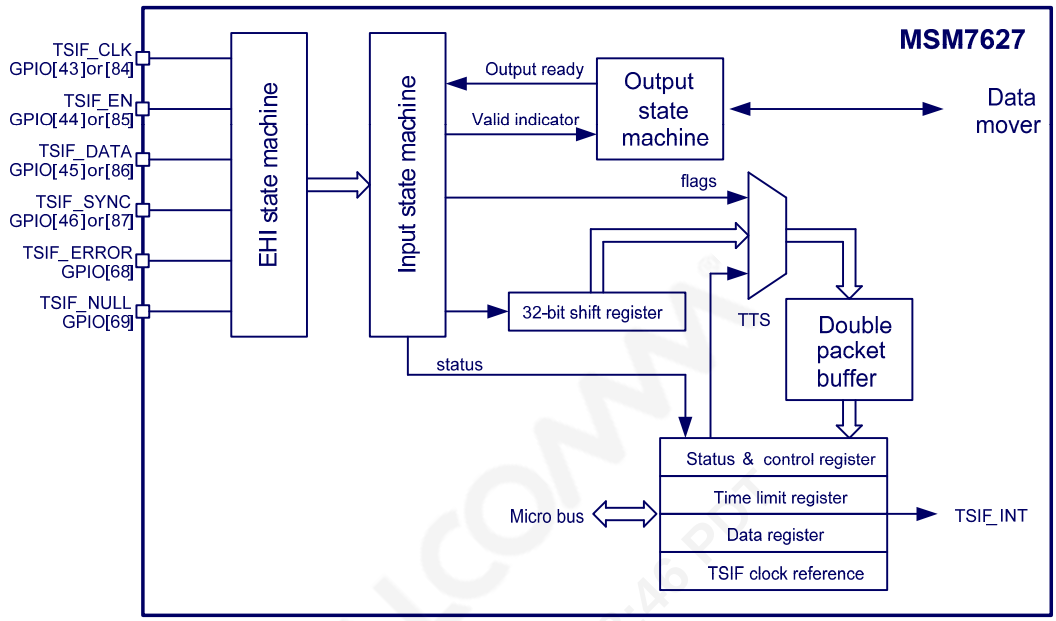
Depending on the standard used, the broadcast module may or may not output H.222.0 MPEG2 transport stream packets that the MSM7627 supports.

The transport stream interface (TSIF) in MSM7627 IC *ONLY* supports transport of TS packets from the broadcast module to the MSM device. Most DVB-H modules only support SDIO interface, which requires an OEM to provide their own driver.

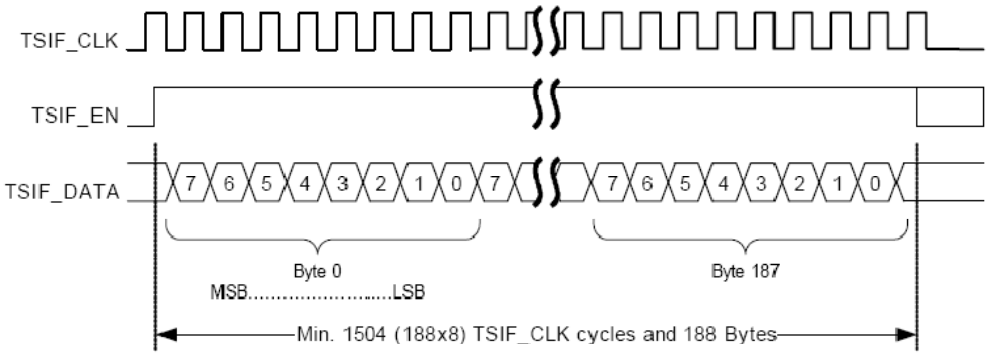
Mobile broadcast standard

Standard	Region	Technology and mode	Bandwidth	Band	Comments
ISDB-T Integrated service digital broadcasting – Terrestrial transmission (ARIB STD-B31)	Japan	OFDM	6 MHz or 6/13 MHz	UHF	Typical ISDB-T modules use TSIF.
S-DMB Satellite – digital mobile broadcast (ARIB STB-B41)	Korea	4XWCDMA	25 MHz	S-Band (2.6 GHz)	Typical S-DMB modules use TSIF.
DVB-H Digital video broadcast – handheld	US/Europe	COFDM	5, 6, 7, 8 MHz	UHF/VHF	Typical DVB-H modules do not support TSIF. DVB-H modules usually support SDIO output.

TSIF Block Diagram

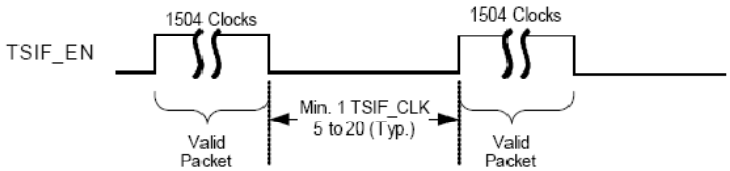


TSIF Signaling



Note: (1) TSIF_EN input can be programmed as "active low" or "active high" signal
(2) TSIF_EN and TSIF_DATA are sampled on either rising or falling TSIF_CLK edge.

TSIF Packet Timing



MSM7627 TSIF Features

- 3-pin or 6-pin serial interface
- Supports external clocks up to 4 MHz, with a maximum data rate of 0.5 MB per second.
- The data mover (DM) transfers HTS packets directly from the external interface to system memory.
- 4 bytes of additional information (time-stamp and flags) are provided with every HTS packet.
  - TSIF time stamp (TTS) is based on a 27 MHz TSIF clock reference (TCR).
- Enhanced fallback and/or debug support using a software-based copy mechanism when HTS packets are transferred directly from the external interface to system memory
- Reports the status of each HTS packet transferred to memory via the DM or software copy
- Optional interrupts for critical events: loss-of-sync, packet available, and packet overflow

Universal Broadcast Modem™ (1 of 2)

- The Qualcomm Universal Broadcast Modem (UBM™) provides a single-chip solution for the world's leading mobile broadcast standards. By combining digital and RF functionality into a single package, UBM chip is a size and cost-efficient solution. The Qualcomm UBM chipset family includes:
  - MBP1600 – supports wideband MediaFLO™, DVB-H, and ISDB-T
  - MBP1610 – supports MediaFLO in the US
- These chipsets are single-chip solution that includes RF and baseband processing. They are MSM-companion ICs that provide broadcast receive-only tuning, demodulation, and decoding capabilities.

Universal Broadcast Modem (2 of 2)

- There are two MBP/MSM interfaces: the MSM device's EBI2 and the TSIF. The MSM device's ARM always configures the MBP via EBI2. The interface used for physical layer data transport from the MBP1600 device to the MSM device depends on the broadcast standard being supported:
  - MediaFLO uses EBI2 only.
  - ISDB-T uses TSIF for data, EBI2 for control.
  - DVB-H uses EBI2 for control and by default for data,
    - Option of using TSIF for PSI/SI (program specific information/service information) control packet.
- The MediaFLO, DVB-H, and ISDB-T software protocol stacks (including video decoding and processing) are all handled within the MSM device.
- Contact support.cdmatech@qualcomm.com for inquiries regarding the UBM.

QUALCOMM 2010.07.13 ruijun.zhang-sim.com

MSM7627 Device Interfaces
LCD Controller (RGB Interface)

LCD Controller Overview (1 of 2)

- The MSM7627 device includes an integrated LCD controller, meant to directly drive an LCD panel/glass through the dedicated RGB interface.
- Reduces overall BOM and costs
  - No need for an external LCD controller IC
  - No need for integrated RAM on LCD panel
  - Compatible with many more high end resolution panels
- Supports up to a parallel RGB888 (24 bpp) output with PCLK up to 75 MHz
  - Output is programmable – RGB565, RGB666, or RGB888
  - PCLK frequency is also programmable through M/N dividers, with a maximum supported frequency of 75 MHz
  - Maximum resolution supported is FWVGA (864 × 480 or 480 × 864) at a refresh rate of 85 Hz

LCD Controller Overview (2 of 2)

- Programmable timing to support various panel's timing
  - Examples: HSYNC/VSYNC width, length, and skew; PCLK period; front and back porches; and display dimensions are all programmable.
  - Color correction capability (fully programmable 3 × 3 color correction matrix and a 256 entry per color gamma look-up table)
- Provides standard RGB interface timing – CSTN is not supported

LCD Controller Tuning (1 of 2)

- The behavior of the RGB interface must be tuned to match the panel of choice's characteristics
  - Parameters such as resolution, refresh rate, horizontal and vertical blanking and color depth, must all be identified, determined, and properly set in the relevant LCDC registers of the MSM7627 IC.
  - List of tunable parameters:
    - Data output format – RGB565, RGB666, RGB888
    - DCLK frequency – up to 48 MHz
    - HSYNC period (active and blanking) – 1 to 4095 DCLK cycles
    - HSYNC pulse width (length of 'inactive' interval) – 1 to 4095 DCLK cycles
    - VSYNC period (active and blanking) – 1 to 4095 HSYNC cycles
    - VSYNC pulse width (length of 'inactive' interval) – 1 to 4095 DCLK cycles
- **Note**: Refer to the *MSM7627 Mobile Station Modem Software Interface Manual* (80-VM151-2) for more details about LCDC registers and programmability, and to the *MSM7627 Mobile Station Modem Device Specification* (80-VM151-1) for more details about timing parameters and their allowed range.

LCD Controller Tuning (2 of 2)

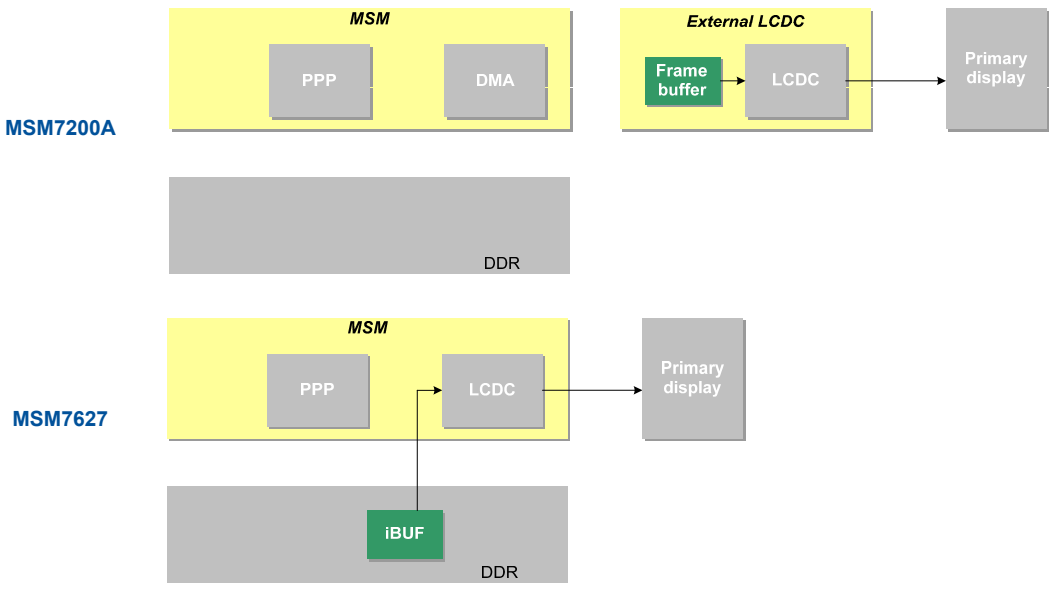
- List of tunable parameters (cont.):
  - Active horizontal and vertical display areas – start and end points can each assume a value from 1 to 4095 DCLKs or 1 to 4095 HSYNCs, respectively.
  - Front and back horizontal and vertical porches – Start and end points can each assume a value from 1 to 4095 DCLKs or 1 to 4095 HSYNCs, respectively.
  - Background color value
  - Skew between active VSYNC edge and first active HSYNC edge – 0 to 4095 DCLKs
  - Polarity of VSYNC, HSYNC, and DEN
  - Launching edge of DCLK
- **Note**: Refer to the *MSM7627 Mobile Station Modem Software Interface Manual* (80-VM151-2) for more details about LCDC registers and programmability, and to the *MSM7627 Mobile Station Modem Device Specification* (80-VM151-1) for more details about timing parameters and their allowed range.

LCD Controller Design Considerations (1 of 2)

- Meeting all required timing specifications of a chosen panel
  - As already described, the MSM7627 device's RGB interface is very flexible and tunable to meet the needs of typical LCD panels.
  - While output delays (and thus exact setup/hold windows) will only be provided upon completion characterization, there are design targets to ensure compatibility with the majority, if not all, of the LCD panels available.
    - Setup/hold windows are designed to be no less than worst case DCLK_CYC/2 – 2.5 ns. (Official specification numbers, once published, will supersede this target spec.)
- Power consumption
  - This consideration is only relevant if customers wish to keep the LCD "on" when the MSM goes into sleep mode.
  - In traditional cases for static screen updates, the external LCDC, with its integrated GRAM, automatically and continuously updates the LCD panel
  - When using the MSM7627 device's integrated LCD controller, the MSM device (and TCXO) must be turned on for every panel update, since it must read from the external RAM and send out the corresponding image to the LCD panel at every single refresh cycle
    - This prevents the MSM device from entering full sleep and low-power mode, which will increase the overall current consumption during sleep, thus reducing standby time.

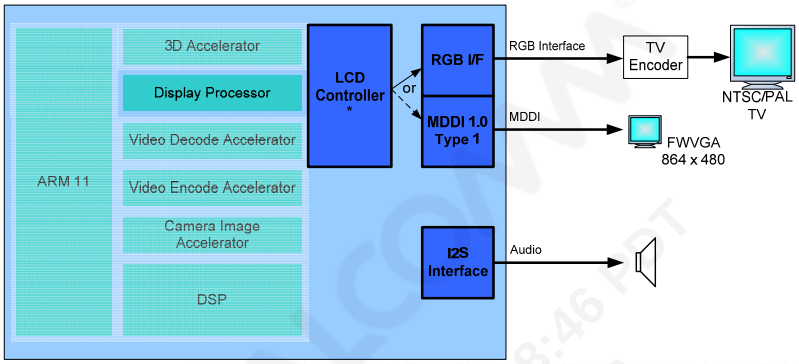
LCD Controller Design Considerations (2 of 2)

Example – static update of LCD panel



TV-out Connectivity

- TV-out function is possible to be supported with MSM7627 devices
  - External transition chip connection required
  - Software support is not available currently
  - Refer to TV OUT SOLUTIONS FOR MSM7x25 AND MSM7x27 (80-VC720-15) for more details



LCD Controller Connections

Signal name	EBI2 and GPIO signals	Voltage rail	Description
LCDC_RED[7:0]	GPIO[100:98],EBI2_ADR[16:12]	P9	8-bit red
LCDC_GREEN[7:0]	EBI2_ADR[11:10],GPIO[130,121:119,112:111]	P8, P9	8-bit green
LCDC_BLUE[7:0]	GPIO[126:125,118:113]	P8, P9	8-bit blue
LCDC_PCLK		P8	Clock
LCDC_VSYNC	GPIO[127]	P9	Vertical sync
LCDC_HSYNC	GPIO[128]	P9	Horizontal sync
LCDC_DEN	GPIO[129]	P9	Data enable

Note: P8 and P9 must be tied together to 1.8 V or 2.6 V.

If an LCD panel other than RGB888 is used, LSB must be aligned between the MSM device and the camera, as shown in this table:

LCD panel type	MSM signals	LCD panel signals	Comments
RGB888	LCDC_RED[7:0] LCDC_GREEN[7:0] LCDC_BLUE[7:0]	RED[7:0] GREEN[7:0] BLUE[7:0]	8-bit red 8-bit green 8-bit blue
RGB666	LCDC_RED[5:0] LCDC_GREEN[5:0] LCDC_BLUE[5:0]	RED[5:0] GREEN[5:0] BLUE[5:0]	6-bit red 6-bit green 6-bit blue
RGB565	LCDC_RED[4:0] LCDC_GREEN[5:0] LCDC_BLUE[4:0]	RED[4:0] GREEN[5:0] BLUE[4:0]	5-bit red 6-bit green 5-bit blue

MSM7627 Device Interfaces
HKADC

Housekeeping ADC

- **The MSM7627 IC has an on-chip 12-bit analog-to-digital converter**.
- **This housekeeping ADC (HKADC) is used for digitizing signals which support handset-level housekeeping functions**.
  - Battery voltage
  - Temperature
- **HKADC features**:
  - 12-bit successive approximation circuit
  - 10-bit accuracy
  - Nine inputs
    - Three inputs are available as general purpose inputs.
    - Five inputs are dedicated for touchscreen functions.
    - One reserved pin

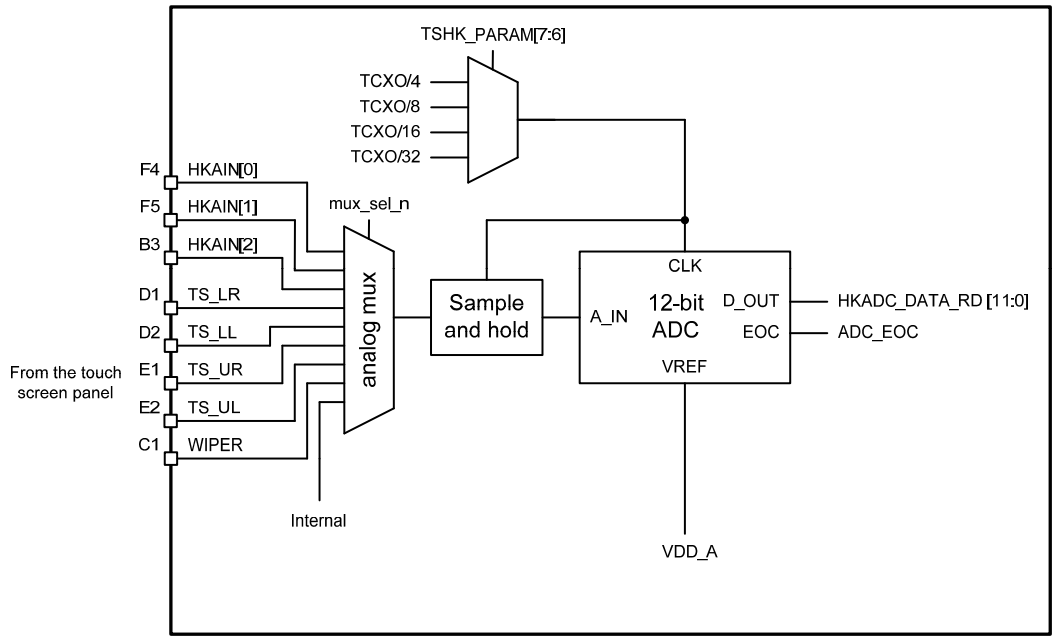
HKADC Connections

Signal name	I/O	Description	Comments
General housekeeping inputs			
HKAIN[0]	AI	Three general purpose inputs to the HKADC analog multiplexer	
HKAIN[1]	AI		
HKAIN[2]	AI		
Touch screen inputs			
TS_LR	AI, AO	5-wire LR; 4-wire Y-	
TS_LL	AI, AO	5 wire LL; 4-wire X-	
TS_UR	AI, AO	5-wire UR; 4-wire Y+	
TS_UL	AI, AO	5-wire UL; 4-wire X+	
WIPER	AI	5-wire back panel input	Not used for 4-wire

Note: If the 4-wire touchscreen interface is used, a wiper pin can be used as HKADC general input pins.

QUALCOMM CDMA Technologies

HKADC Connections

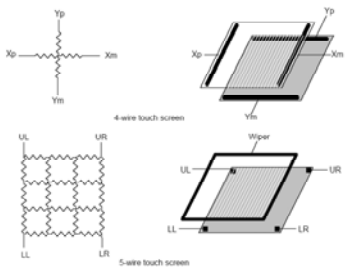


QUALCOMM CDMA Technologies

MSM7627 Device Interfaces
Touchscreen

Touchscreen Interface

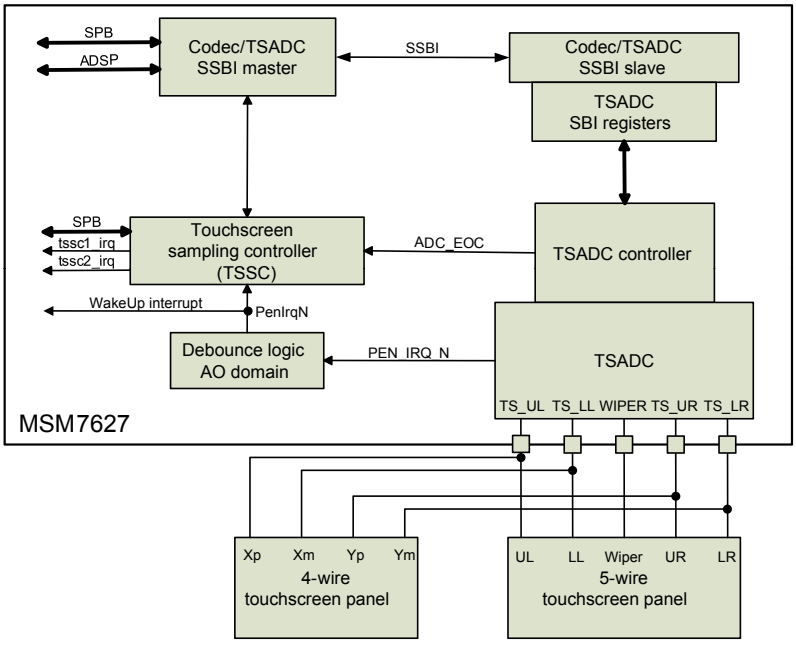
- The MSM7627 IC supports both 4-wire and 5-wire resistive touchscreen panels.
  - All resistive touchscreens use the voltage divider principle to generate voltages that represent X and Y coordinates.
  - The 4-wire consists of two resistive layers. The controller supplies voltages to one layer and reads the voltages from the second layer to determine the X and Y values.
  - The 5-wire works very similarly to the 4-wire. It consists of one conductive and one resistive layer. The controller alternates voltages between two of the four corners on the resistive layer and reads voltages on the conductive layer via wiper to determine the X and Y values.
  - The TSADC is a 12-bit successive approximation device.
  - The conversion result is sent to the touchscreen sampling controller (TSSC) via single-wire serial bus interface (SSBI), and the TSSC generates the necessary interrupts.
  - Detailed information on how the touchscreen interface works is included in the *Application Note: Touch Screen Operation for MSM7200 and MSM7500* (80-V9038-11).



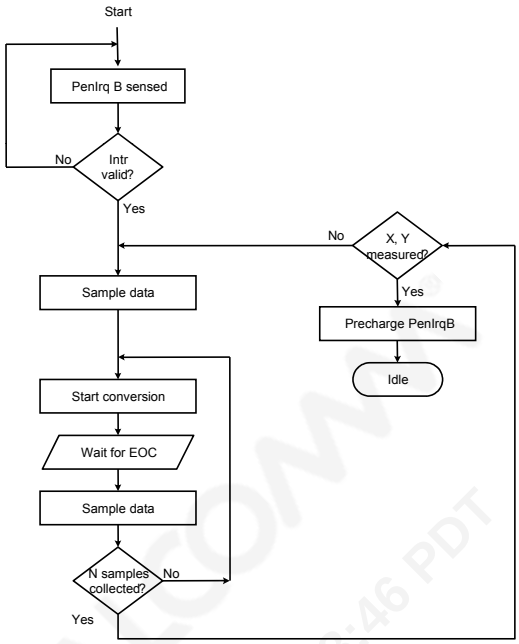
Touchscreen Features

- One interface supports both 4-wire and 5-wire resistive touch panels.
- Pen-down detection
- Programmable debounce logic
- Programmable number of samples (1, 4, 8, or 16)
- Programmable precharge and panel voltage-stabilization duration
- Programmable resolutions (8-bit, 10-bit, or 12-bit)
- Programmable sampling periods (3, 24, 36, and 48 clock cycles of a 2.4 MHz clock)
- Ratiometric conversion
- Touch pressure Z1 and Z2 measurement
- X and Y coordinate measurement

Touchscreen Interface Diagram



MSM7627 Touchscreen Operation Flow



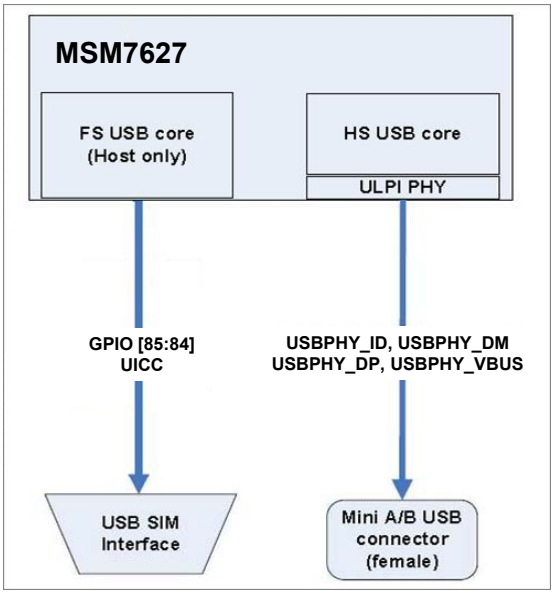
Touchscreen ADC Contention Issue

- **A contention issue arises when another ADC sampling request is trying to access the ADC controller while the touchscreen sampling is in process**.
  - If another ADC sampling request comes in when the touchscreen sampling process is in process (e.g., HDET, VBATT, etc.), the touchscreen sample will be corrupted, and a TSSC_ADC_EOC timeout error occurs.
  - The touchscreen sample is corrupted, and ADC is no longer sampling the touchscreen. TSSC is unaware of this and keeps waiting until the timeout occurs. The touchscreen operation is frozen.
- **A software workaround has been implemented.**
  - During touchscreen sampling activity, the ADC will not accept any other sampling requests.
  - Please consult with Qualcomm for further details.

HS-USB/USB-UICC/USIM/UART/SDIO/I²C/Keypad

MSM7627 USB Hardware Architecture

- Integrated HS USB LINK and PHY cores, interfaces to USB connector
  - Supports peripheral/host/OTG modes of operation
- Integrated FS USB core supports host-only mode of operation.
  - Used to interface with USB-UICC



HS-USB Connectivity

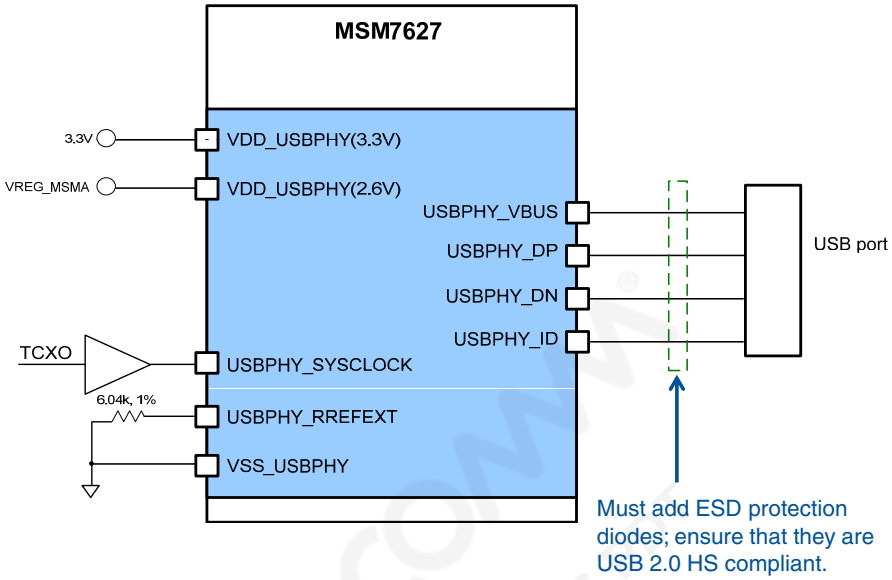
- **The MSM7627 IC supports one internal high-speed OTG port**.
- **Supported speeds**:
  - The MSM7627 HS-USB OTG core supports three speeds while acting as a host:
    - Low-speed (1.5 Mbps)
    - Full-speed (12 Mbps)
    - High-speed (480 Mbps)
- **High-speed USB**:
  - On-chip (internal) USB solution with built-in transceiver inside the MSM device.
  - HS-USB is on-the-go (OTG) compliant, and hence can be configured either as host or peripheral.
  - Supports 16 endpoint pairs:
    - 1 reserved for control IN/OUT
    - 15 can be used for bulk IN/OUT, interrupt IN/OUT, and isochronous IN/OUT

Note: There is no software support for isochronous IN/OUT.

USB Pin Connections

Signal name	I/O	Voltage	Description	Comments
High-speed OTG USB				
USBPHY_SYSCLK	AI	USBPHY	Buffered system clock signal from TCXO	
USBPHY_REXT	AI	USBPHY	External resistor connection for current reference	Shorted to ground through a 6.04 kΩ resistor.
USBPHY_ID	AI	USBPHY	USB ID signal	
USBPHY_DN	AI, AO	USBPHY	USB D- signal	
USBPHY_DP	AI, AO	USBPHY	USB D+ signal	
USBPHY_VBUS	AI, AO	USBPHY	USB VBUS signal	
Power and ground				
VDD_USBPHY(3.3V)			Power for 3.3 V power rail	
VDD_USBPHY(2.6V)			Power for 2.6 V power rail	
VSS_USBPHY			Ground	

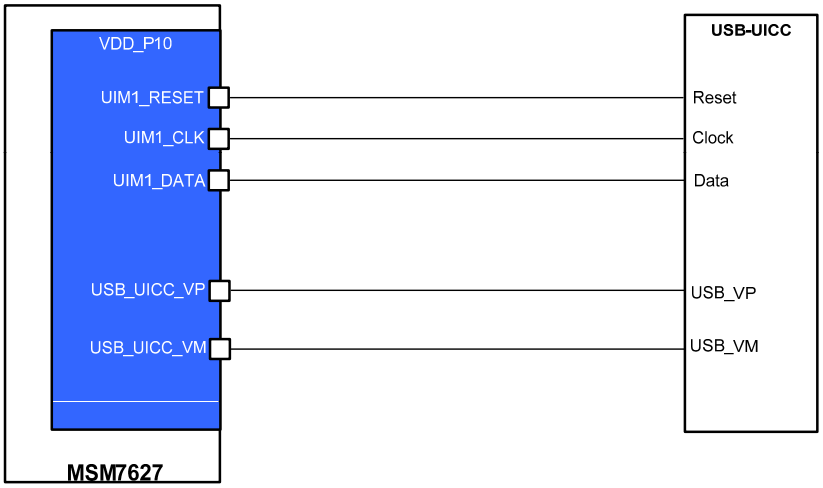
USB Block Diagram



For more details, please refer to *Application Note: USB Design Guidelines for Mobile Station Modem™ (MSM™) Devices* (80-VF815-19)

USB-UICC

- The MSM7627 device supports USB-UICC.
  - Enables the use of SIM cards with mass storage capability.

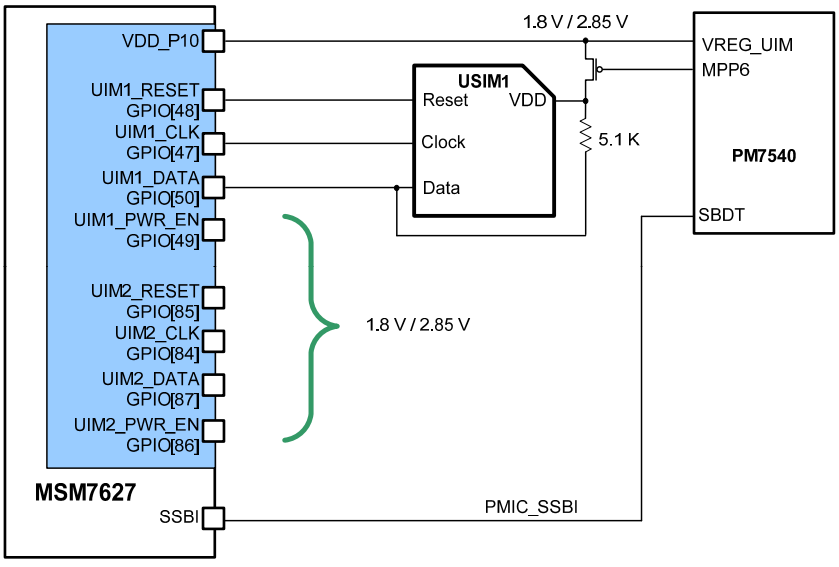


USIM

- MSM7627 supports 1.8 V/2.85 V dual-voltage USIM:
  - USIM signals can be connected directly to MSM; a level translator between the MSM and USIM is not required.
  - Two USIM interfaces; both use a separate VDD_P10 power rail.

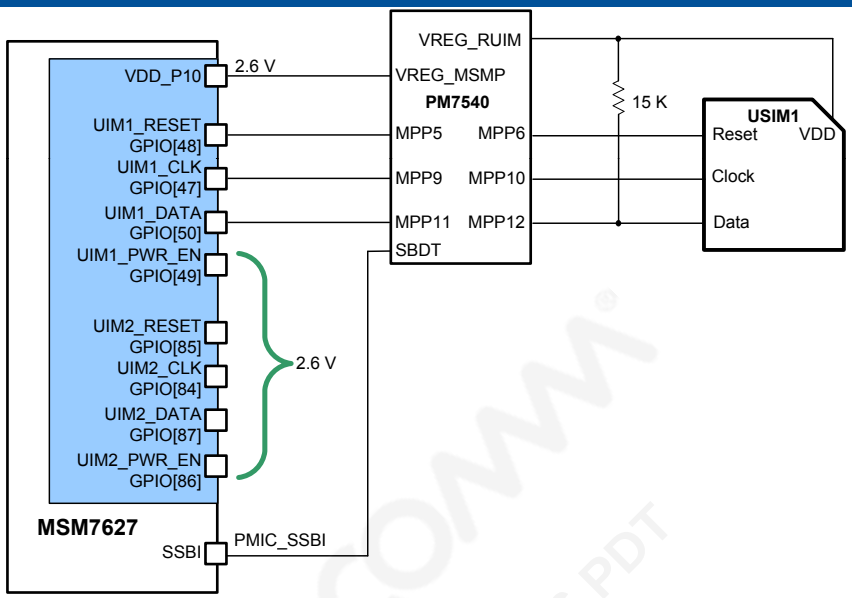
Signal name	I/O	Voltage	Description
USIM1			
UIM1_PWR_EN/GPIO[49]	DO	P10	Power enable
UIM1_RESET /GPIO[48]	DO	P10	Reset
UIM1_CLK/GPIO[47]	DO	P10	Clock
UIM1_DATA/GPIO[50]	B	P10	Data
USIM2			
UIM2_PWR_EN/GPIO[86]	DO	P10	Power enable
UIM2_RESET/GPIO[85]	DO	P10	Reset
UIM2_CLK/GPIO[84]	DO	P10	Clock
UIM2_DATA/GPIO[87]	B	P10	Data
Power			
VDD_P10		P10	Power

USIM Block Diagram (Primary Configuration)



SW can change the VREG_UIM voltage dynamically to match the USIM voltage type. Avoid using GPIO[87:84], GPIO[49] if the device supports dual-voltage USIM.

USIM Block Diagram (Alternative Configuration)



If USB-UICC is implemented, external level shifters are required for USB_UICC_VP and USB_UICC_VM.

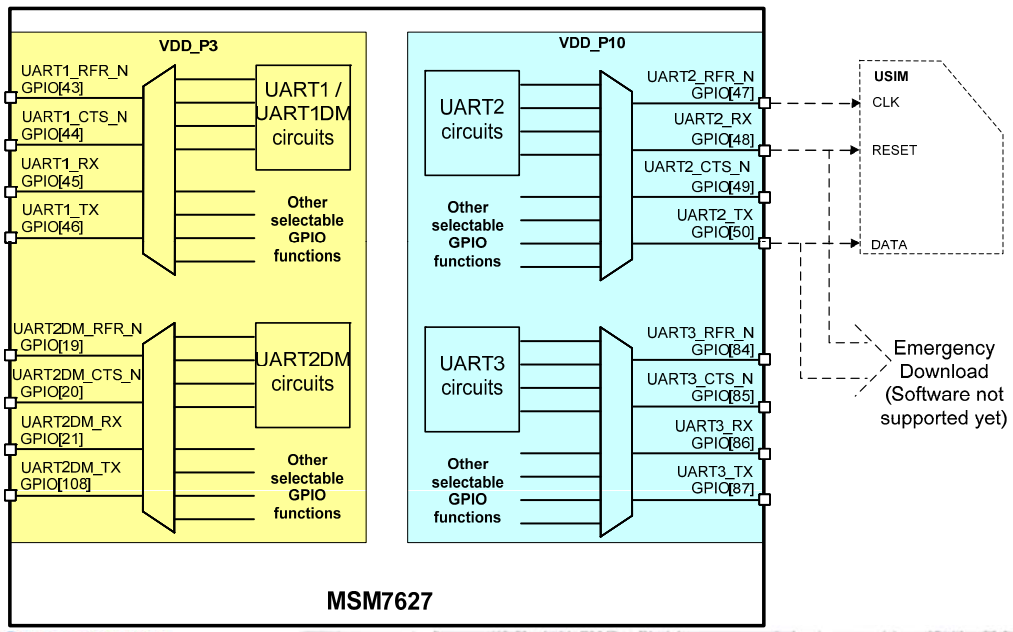
UART Connectivity (1 of 2)

- **The MSM7627 IC is capable of providing up to four UART ports.**
- **Each UART port communicates with serial data ports that conform to the RS-232 interface protocol.**
- **The UART port can be used for test and debug functions and can support additional interface functions, such as an external keypad or ringer.**
- **UART supported speeds**:
  - UART1
    - UART1 is capable of supporting a maximum transfer speed of up to 230 kbps.
  - UART2 and UART3
    - These two ports have smaller FIFOs; therefore, the supported speeds are much slower.
    - Supports a maximum speed of up to 115 kbps
    - UART2 must be used for USIM.

UART Connectivity (2 of 2)

- **High-speed UART**:
  - High-speed UART is achieved using UART1DM and UART2DM interfaces.
    - UART1DM is behind the UART1 interface.
    - UART2DM has its own set of GPIOs.
  - Maximum speeds up to 4 Mbps
- **UART features**:
  - The UART has several features that are common to both transmit and receive modes.
  - Hardware handshaking
  - Programmable parameters
    - Data size
    - Stop bits
    - Parity
    - Bit rate
    - Selectable clock source
- **All UART signals use GPIOs; this allows them to be configured for alternate functions.**
- **Emergency download supported in UART2 interface**

UART Pin Connections Diagram



UART Pin Connections (1 of 2)

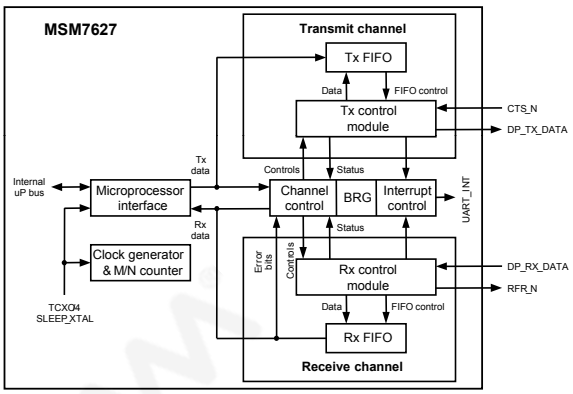
Signal name	I/O	Voltage	Description	Comments
UART1/UART1DM				
UART1_RFR_N GPIO[43]	O	P3	Ready for receiving	Shares the same GPIO as UART1DM
UART1_CTS_N GPIO[44]	DI	P3	Clear to send	Shares the same GPIO as UART1DM
UART1_RX GPIO[45]	DI	P3	Receive serial data input	Shares the same GPIO as UART1DM
UART1_TX GPIO[46]	O	P3	Transmit serial data output	Shares the same GPIO as UART1DM
UART2DM				
UART2DM_RFR_N GPIO[19]	O	P3	Ready for receiving	
UART2DM_CTS_N GPIO[20]	DI	P3	Clear to send	
UART2DM_RX GPIO[21]	DI	P3	Receive serial data input	
UART2DM_TX GPIO[108]	O	P3	Transmit serial data output	

UART Pin Connections (2 of 2)

Signal name	I/O	Voltage	Description	Comments
UART2				
UART2_RFR_N GPIO[47]	O	P10	Ready for receiving	USIM must use UART2.
UART2_CTS_N GPIO[49]	I	P10	Clear to send	USIM must use UART2.
UART2_RX GPIO[48]	I	P10	Receive serial data input	USIM must use UART2.
UART2_TX GPIO[50]	O	P10	Transmit serial data output	USIM must use UART2.
UART3				
UART3_RFR_N GPIO[84]	O	P10	Ready for receiving	
UART3_CTS_N GPIO[85]	I	P10	Clear to send	
UART3_RX GPIO[86]	I	P10	Receive serial data input	
UART3_TX GPIO[87]	O	P10	Transmit serial data output	

UART Block Diagram

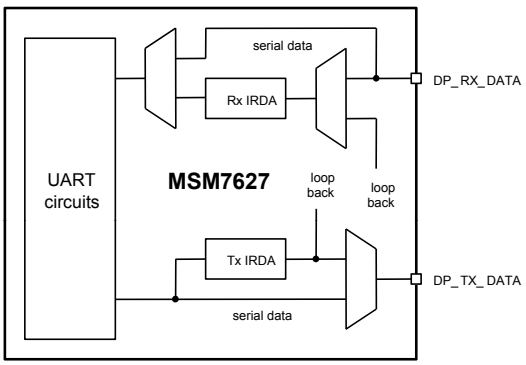
- The UART core consists of separate transmit and receive channels.
- The Tx and Rx data is processed with separate FIFOs.
  - Both Tx and Rx FIFOs are 512 bytes (UART1).
- Other support blocks include:
  - Clock source:
    - Each UART interface has its own clock source.
    - The UART clock is derived from the selected clock source.
    - The clock source is selected by setting the MISC_CLK_SEL1 register.
  - Bit rate generator (BRG):
    - The desired bit rate for the receive and transmit channels is selected using the UART_CSR register.
    - Each UART can be set independently.
    - Speeds range from 75 bps to 230 kbps and 1.152 Mbps.
  - Microprocessor interface
  - Interrupt control
- UART2 and UART3 interfaces have a 64-byte FIFO in the transmit and receive channels.
  - The speed of these two interfaces is much slower than UART1.



IrDA Through UART Interface

- The MSM7627 IC contains an IrDA transceiver that interfaces between the UART and RX_DATA/TX_DATA pins.
- The IrDA feature is available for both UARTDM interfaces (UART1DM, UART2DM).
- The IrDA feature is fully supported in hardware, but it is NOT supported by Qualcomm software.

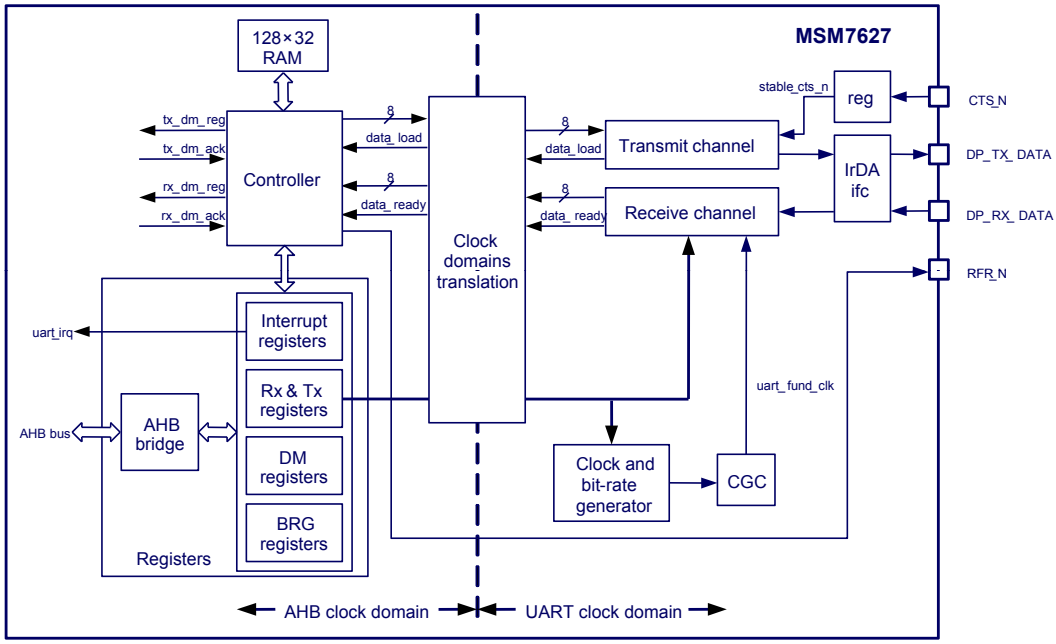
  Refer to the *MSM7627 Mobile Station Modem User Guide* (80-VM151-3) for information regarding the IrDA interface.
- IrDA Tx converts the serial data into IrDA format.
  - Logic 1 = 0
  - Logic 0 = 1 (pulse width = 3/16 bit rate)
- IrDA Rx converts IrDA data into serial bits.



UART1DM/UART2DM (UART1/UART2 Data Mover)

- **The MSM7627 IC needs to provide support for medium-rate IrDA (1.15 Mbps).**
- **The UART block is connected on the slow peripheral (microprocessor) bus and cannot provide such a high bandwidth.**
- **To support this data rate, the UART1DM and UART2DM block is implemented in the MSM7627 IC.**
- **The UART1DM and UART2DM are on the fast peripheral bus (AHB), and can support the high bandwidth required for medium-rate IrDA.**
- **UART1DM/UART2DM features:**
  - Support for medium-rate IrDA (1.15 Mbps)
  - Support for high-speed UART feature (up to 4 Mbps)
  - Separate Tx/Rx FIFOs (implemented in one SRAM)
    - Tx/Rx FIFOs share the same 512 byte memory.
  - 32-bit wide AHB interface
  - Rate-controlled data mover (separate channel for Rx/Tx)

UARTDM Architecture



UARTDM Operation (1 of 2)

Traditional UART transfer

1. Initialize UART.
2. UART sends an interrupt to CPU each time FIFO holds less than the preprogrammed number of characters. This interrupt signals the CPU that new data burst can be sent to UART Tx block.
3. UART transmits character-by-character until the Tx FIFO is empty.

UARTDM transfer

1. Initialize the UART.
2. Initialize the DM.
3. Enable the Tx-DM transfer mode.
4. UART sends a request to the DM when there is space available in Tx FIFO. The DM responds by sending the data burst via AHB bus to Tx FIFO. This continues until Tx FIFO is full.
5. UART transmits character-by-character until the Tx FIFO is empty.

UARTDM Operation (2 of 2)

- **UARTDM is connected to the AHB bus and includes two rate-controlled data mover interfaces (one for Tx and one for Rx).**
- **All configuration registers are in the AHB clock domain.**
- **Rx path is independent of Tx path. Therefore, the UART block can receive data during an active Tx transfer.**
- **Commonality is the shared SRAM between Tx/Rx FIFOs.**
  - Sharing occurs during the initialization phase.
  - Memory space is not necessarily shared equally.

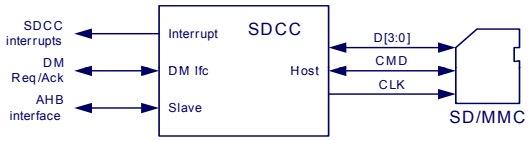
UARTDM IrDA

- **To support an IrDA medium data rate of 1.15 Mbps, UART must run at a high clock frequency of 18.4 MHz.**
- **The UART1DM CSR register needs to be set to determine the bit rate for Tx and Rx.**
- **The UART1DM_IRDA register enables the IrDA function. This register also controls the IrDA transceiver that optionally interfaces between the UART and the RX_DATA and TX_DATA pins.**
- **Refer to the *MSM7627 Mobile Station Modem Software Interface Manual* (80-VM151-2) for information regarding UART1DM and UART2DM registers and settings.**

SD Interface

- **MSM7627 IC supports MMC, SD, SDIO, and T-Flash.**
  - Supports 1-bit, 4-bit, and 8-bit modes.
  - Four SDC ports are available on the MSM7627 IC.
- **2.5 V to 3.0 V operation**

SDCC architecture

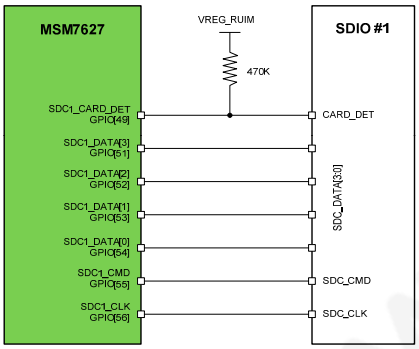


- **Supported standards**

	1-bit	4-bit	8-bit	Max. frequency of operation (MHz)	Notes
SDIO v2.0	Yes	Yes	N/A	50	2, 3
SD v2.0	Yes	Yes	N/A	50	2, 3
MMC v4.2	Yes	Yes	Yes	52	2, 3

Notes:
1. Please check with the Qualcomm Software team for software driver availability.
2. All speed classes mentioned under these specification are supported.
3. Boot-up from embedded SD/embedded MMC is not supported in hardware.
4. Refer to the *Application Note: MultiMedia Card/Secure Digital Card* (80-V7837-1) for more details.

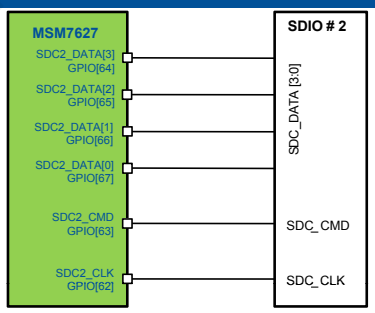
SDC1 Connections



Signal name	I/O	Voltage	Description	Comments
SDC1				
GPIO[51] (SDC1_DATA[3])	B	P3	SDC1 data bit #3	Primary SDC data bus 10 k – 100 k external PUs are required for SD cards on DATA and CMD signals. 50 k – 100 k external PUs are required for MMC cards on DATA and CMD signals. If MSM internal PUs are used, OEMs may need to keep only placeholders for the external PUs.
GPIO[52] (SDC1_DATA[2])	B	P3	SDC1 data bit #2	
GPIO[53] (SDC1_DATA[1])	B	P3	SDC1 data bit #1	
GPIO[54] (SDC1_DATA[0])	B	P3	SDC1 data bit #0	
GPIO[55] (SDC1_CMD)	B	P3	SDC1 command and response bit	
GPIO[56] (SDC1_CLK)	DO	P3	SDC1 clock	
GPIO[49] (SCD1_CARD_DET)	DI	P10	SDC1 card detection	

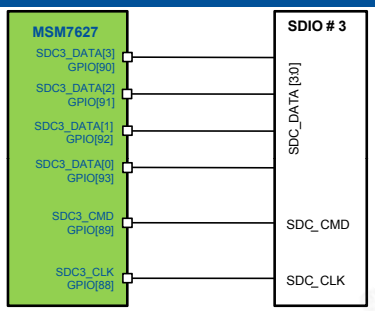
Reference: *Application Note: MMC/SD* (80-V7837-1), Section 3.9 FAQ.

SDC2 Connections



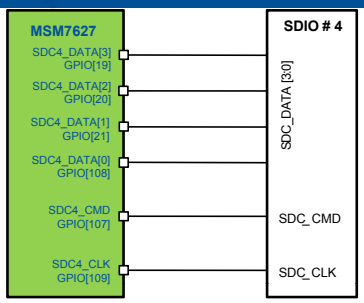
Signal name	I/O	Voltage	Description	Comments
SDC2				
GPIO[64] SDC2_DATA[3]	B	P3	SDC2 data bit #3	10 k – 100 k external PUs are required for SD cards on DATA and CMD signals. 50 k – 100 k external PUs are required for MMC cards on DATA and CMD signals. If MSM internal PUs are used, OEMs may need to keep only placeholders for the external PUs. Reference: *Application Note: MMC/SD* (80-V7837-1), Section 3.9 FAQ.
GPIO[65] SDC2_DATA[2]	B	P3	SDC2 data bit #2	
GPIO[66] SDC2_DATA[1]	B	P3	SDC2 data bit #1	
GPIO[67] SDC2_DATA[0]	B	P3	SDC2 data bit #0	
GPIO[63] SDC2_CMD	B	P3	SDC2 command and response bit	
GPIO[62] SDC2_CLK	DO	P3	SDC2 clock	

SDC3 Connections



Signal name	I/O	Voltage	Description	Comments
SDC3				
GPIO[90] SDC3_DATA[3]	B	P3	SDC3 data bit #3	Can be combined with SDC4 to enable an 8-bit SD interface. 10 k – 100 k external PUs are required for SD cards on DATA and CMD signals. 50 k – 100 k external PUs are required for MMC cards on DATA and CMD signals. If MSM internal PUs are used, OEMs may need to keep only placeholders for the external PUs. Reference: *Application Note: MMC/SD* (80-V7837-1), Section 3.9 FAQ.
GPIO[91] SDC3_DATA[2]	B	P3	SDC3 data bit #2	
GPIO[92] SDC3_DATA[1]	B	P3	SDC3 data bit #1	
GPIO[93] SDC3_DATA[0]	B	P3	SDC3 data bit #0	
GPIO[89] SDC3_CMD	B	P3	SDC3 command and response bit	
GPIO[88] SDC3_CLK	DO	P3	SDC3 clock	

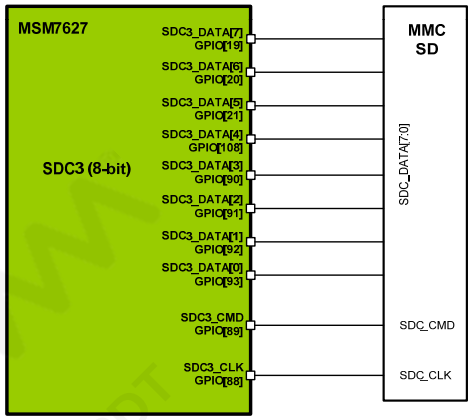
SDC4 Connections



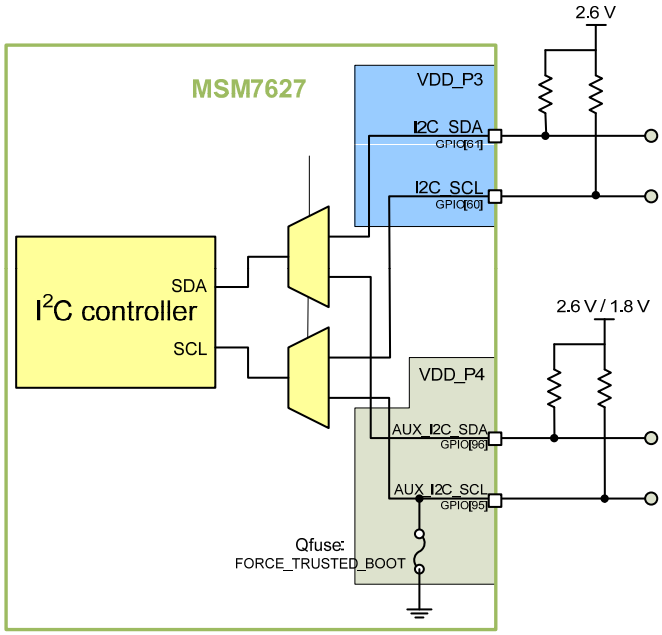
Signal name	I/O	Voltage	Description	Comments
SDC4				
GPIO[19] SDC4_DATA[3]	B	P3	SDC4 data bit #3	Can be combined with SDC3 to enable an 8-bit SD interface. 10 k – 100 k external PUs are required for SD cards on DATA and CMD signals. 50 k – 100 k external PUs are required for MMC cards on DATA and CMD signals. If MSM internal PUs are used, OEMs may need to keep only placeholders for the external PUs. Reference: *Application Note: MMC/SD* (80-V7837-1), Section 3.9 FAQ.
GPIO[20] SDC4_DATA[2]	B	P3	SDC4 data bit #2	
GPIO[21] SDC4_DATA[1]	B	P3	SDC4 data bit #1	
GPIO[108] SDC4_DATA[0]	B	P3	SDC4 data bit #0	
GPIO[107] SDC4_CMD	B	P3	SDC4 command and response bit	
GPIO[109] SDC4_CLK	O	P3	SDC4 clock	

SDC3 8-bit Interface

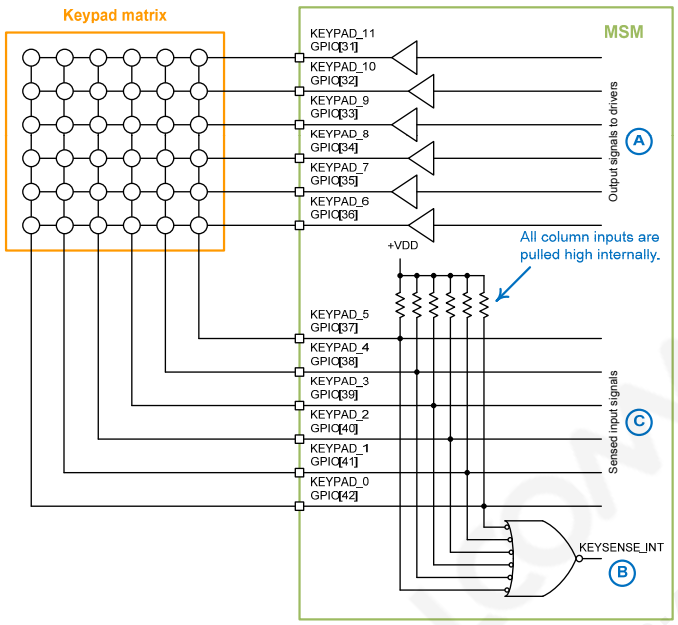
Signal name	I/O	Voltage	Description
SDC3 (8-bit)			
GPIO[19] SDC3_DATA[7]	B	P3	SDC3 data bit #7
GPIO[20] SDC3_DATA[6]	B	P3	SDC3 data bit #6
GPIO[21] SDC3_DATA[5]	B	P3	SDC3 data bit #5
GPIO[108] SDC3_DATA[4]	B	P3	SDC3 data bit #4
GPIO[90] SDC3_DATA[3]	B	P3	SDC3 data bit #3
GPIO[91] SDC3_DATA[2]	B	P3	SDC3 data bit #2
GPIO[92] SDC3_DATA[1]	B	P3	SDC3 data bit #1
GPIO[93] SDC3_DATA[0]	B	P3	SDC3 data bit #0
GPIO[89] SDC3_CMD	B	P3	SDC3 command and response bit
GPIO[88] SDC3_CLK	DO	P3	SDC3 clock



I²C and AUX_I2C Interface



Keypad Interface

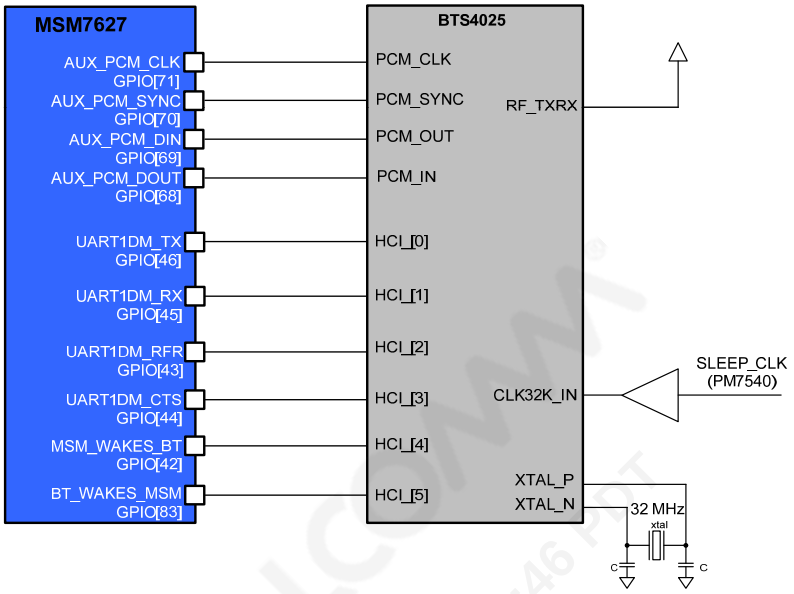


- Any keypad button press is detected by OR-ing all column signals together using a set of KEYPAD pins.
  - Before a keypad button is pressed, all rows are driven low. (A)
  - When a keypad button is pressed, its corresponding column is pulled low (since all rows are low).
  - The KEYSENSE_INT signal is asserted whenever any keypad button, from any column, is pressed. (B)
- When the interrupt signal is received, the MSM device begins scanning the keypad.
  - During a scan, each row is sequentially driven low, one at a time. (A)
  - As each row is driven low, the columns are sensed. (C)
  - The precise keypad button being pressed is revealed when that button's column reads low while that button's row is driven low.

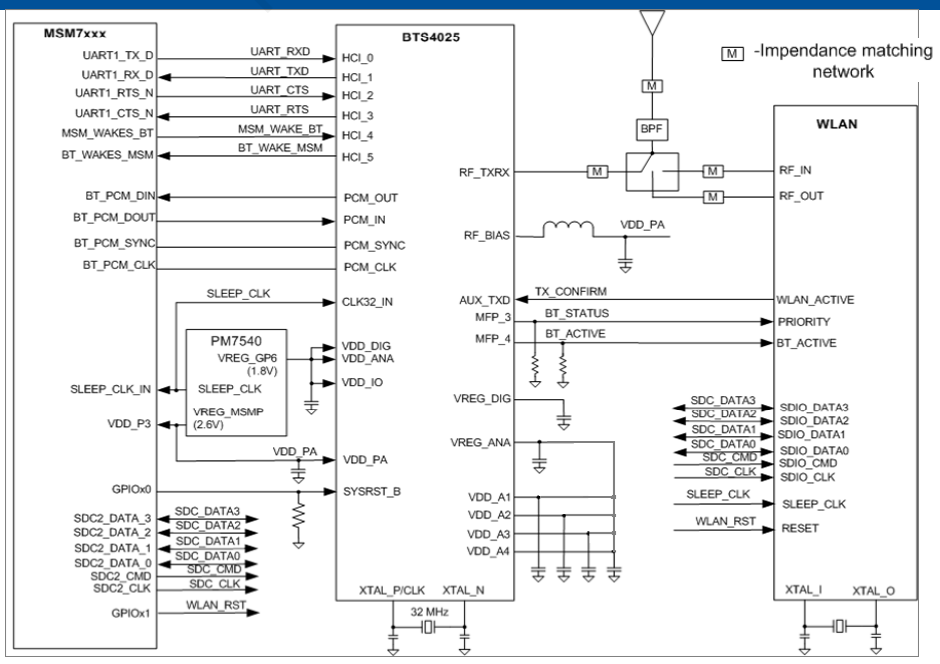
2010.07.13 ruijun.zhang-sh@...

MSM7627 Device Interfaces
Bluetooth (BTS4025™ Device)

Bluetooth – BTS4025 Device



BTS4025 and WLAN Interface



Bluetooth – BTS4025 Features

- **0.13 µm CMOS system-on-chip (SoC) with integrated baseband and 2.4 GHz radio for Bluetooth V2.1 wireless technology applications with EDR up to 3 Mbps**
- **Interface using UART1DM (data) and PCM (audio)**
- **Supports 802.11 (WiFi) coexistence**
- **Two clock sources required:**
  - 32 MHz master reference clock provides timing source for all nonsleep operational functions
  - 32.768 kHz sleep clock provides timing during sleep mode to minimize DC power consumption
- **No RF tuning required in production**
- **Integrated front-end regulator (LDO) for direct battery connection**

QUALCOMM
2010.07.13 18:08:46 PDT
ruijun.zhang-sh@...

MSM7627 Device Interfaces
Audio

Audio (1 of 2)

- **The MSM7627 IC audio frontend includes the following**:
  - Stereo wideband codec
  - PCM interface
  - Additional DSP audio processing
- **Stereo wideband codec**
  - MSM7627 IC supports stereo wideband sampling in both Tx and Rx paths.
  - Stereo music/ringer melody applications through line-in inputs
  - Supports 8 kHz voice-band applications on forward link
  - Software-selectable sampling rate up to 48 kHz in receive path**
- **PCM interface**
  - The PCM interface allows for an external codec to be used instead of the internal codec.
  - Supports I²S modes that allow an external stereo DAC to be used.

** Refer to the software release plan for details about sample rate support

Audio (2 of 2)

- **Additional DSP audio processing**
  - Additional gains
  - Filtering voice call enhancements

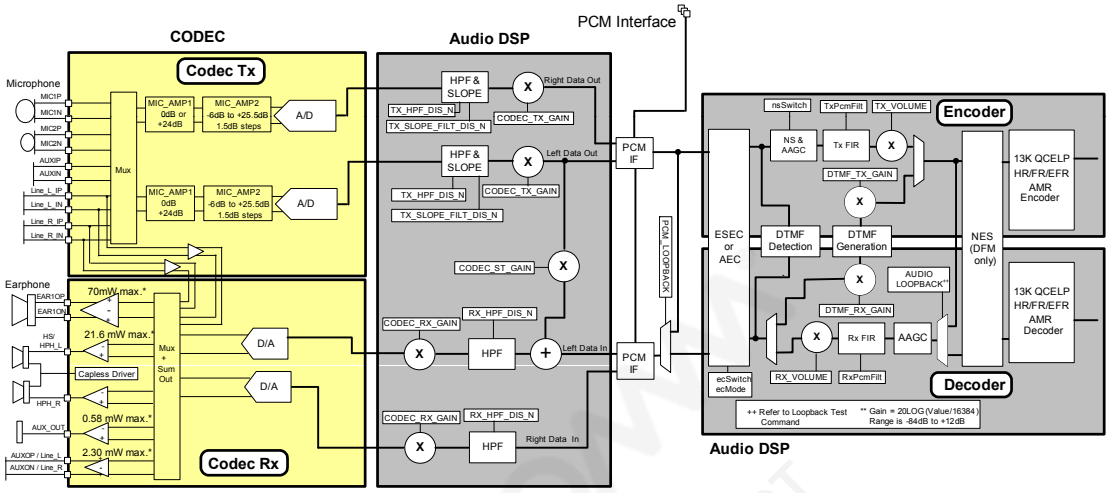
Audio Front End – Tx Features

- **Tx (ADC) features**:
  - Stereo wideband sampling (stereo ADC), two differential MIC inputs, one differential AUX input, stereo differential line-inputs
  - MICAMP1 software-adjustable 0 dB or +24 dB gain
  - MICAMP2 (internal) software-adjustable -6 dB to +25.5 dB, in steps of 1.5 dB
  - CodecTxGain, TxVolume software-adjustable from -84 dB to +12 dB, in steps of 1 dB
  - CodecStGain adds a portion of Tx audio into Rx path with software-selectable gain from -96 dB to +12 dB, in steps of 1 dB (includes a 12 dB offset).
  - TxSlope provides pre-emphasis for high-frequency audio.
  - TxPcmFilter – flexible 13-tap software-adjustable filter
  - TxHPF – 30 dB attenuation below 120 Hz

Audio Front End – Rx Features

- **Rx (DAC) features**:
  - Integrated stereo DAC, one mono differential earphone output, legacy or OCL stereo headset output (stereo single-ended or mono differential), single-ended mono AUX output, and dedicated stereo line-output
  - 13-bit/16-bit DAC with a typical 88 dB dynamic range
  - Rx sampling rates: 8, 16, 22.05, 24, 32, 44.1, and 48 kHz (The rate support varies between voice and playback; check the software release plan.)
  - Supports summing an external device's stereo (left, right) single-ended analog signal into earphone outputs.
  - CodecRxGain, RxVolume software-adjustable from -84 dB to +12 dB in steps of 1 dB
  - RxPcmFilter – similar to TxPcmFilter
  - RxHPF – similar to TxHPF

Stereo Wideband Codec and Audio DSP



Note: Internal loopbacks exist to drive speakers for the external input device or for signal-level verification: AUX-PGA, CodecStGain, PCM, and audio loopbacks.

Additional Audio DSP Blocks (1 of 2)

- **Enhanced echo canceller (EC)**
  Application Note: Enhanced Echo Canceller and Noise Suppression Tuning (CL93-V1638-2)
  - Cancels acoustic feedback between a loudspeaker and a microphone
  - Problems that are usually related to echo canceller: no double-talk or reduced double-talk, unexplained Tx muting, and volume variations
  - Supports full-duplex speakerphone mode
- **Noise suppressor (NS)**
  Application Note: Noise Suppressor for DMSS Software (80-V2312-1)
  - Intended to remove continuous sounds that have no value in transmitting to the far-end user – automobile noise (engine noise, tire noise) and continuous tones (whistles, horns)
  - On Tx link only
  - Typically turned on for most phone modes. Does not require special tuning.
  - Possible problems: may not let tones or other test audio be transmitted, may cause unexpected volume variations if the test lab has a changing acoustic environment; should be one of the first things to disable if unexplained volume issues occur with audio

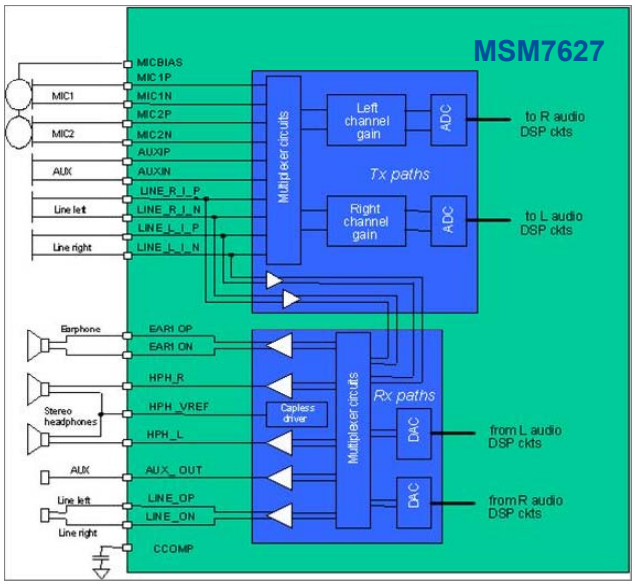
Additional Audio DSP Blocks (2 of 2)

- **PureVoice Audio AGC™**
  ***Application Note: Audio AGC for DMSS Software* (CL93-V2586-1)**
  - Intended to make sound volume more uniform on Tx and Rx sides (independently controlled Tx and Rx) and remove unnecessary low-level noise
  - By using static gain feature, can give greater control of gains
  - Possible problems fixed by audio AGC: large variations in sound levels and inability to hear soft sounds
  - This issue is discussed in greater detail later in this presentation.
- **Audio front-end features – comfort noise**
  - Intended for use when muting the audio on the TX path
  - On Tx path only
  - When muting the microphone, a white noise of equivalent level to the measured background noise will play, instead of just pure silence.

Audio Connections

MSM7627 audio connections fall into seven categories:

- Microphone inputs
- Auxiliary inputs
- Line inputs
- Earphone outputs
- Stereo headphone outputs
- Auxiliary outputs
- Line outputs



Audio Pin Connections (1 of 2)

Signal name	I/O	Voltage	Description	Comments
Microphone inputs				
MIC1P	AI	Analog	Microphone #1 differential positive (+) input	
MIC1N	AI	Analog	Microphone #1 differential negative (-) input	
MIC2P	AI	Analog	Microphone #2 differential positive (+) input	
MIC2N	AI	Analog	Microphone #2 differential negative (-) input	
MICBIAS	AI, AO	Analog	Microphone bias supply	No decoupling cap
Auxiliary input				
AUXIP	AI	Analog	Auxiliary differential positive (+) input	
AUXIN	AI	Analog	Auxiliary differential negative (-) input	
Line inputs				
LINE_R_I_P	AI	Analog	Right channel stereo function with three options	Options: 1) Line in 2) Microphone 3) Summing function to Rx
LINE_R_I_N	AI	Analog		
LINE_L_I_P	AI	Analog	Left channel stereo function with three options	
LINE_L_I_N	AI	Analog		

Audio Pin Connections (2 of 2)

Signal name	I/O	Voltage	Description	Comments
Earphone outputs				
EAR1OP	AO	Analog	Earphone differential positive (+) output	
EAR1ON	AO	Analog	Earphone differential negative (-) output	
Stereo headphone outputs				
HPH_R	AO	Analog	Stereo headphone right output or negative (-) headphone out	
HPH_L	AO	Analog	Stereo headphone left output or positive (+) headphone out	
HPH_VREF	AI	Analog	Headphone common mode voltage	Capless mode
Auxiliary output				
AUX_OUT	AO	Analog	Auxiliary output to car kit, PMIC, or external speaker	Single-ended
Line outputs				
LINE_OP	AO	Analog	Positive (+) line (LINE_OUT_L) output or stereo left channel output	
LINE_ON	AO	Analog	Negative (-) line (LINE_OUT_R) output or stereo right channel output	
Other audio-related pin				
CCOMP	AI	Analog	External decoupling cap for codec voltage reference	0.1 µF recommended

Audio Summary

Item	MSM7627 IC
Tx differential inputs	Five pairs
Tx codec ADC path	Mono/stereo
Rx codec DAC path	Mono/stereo
Rx max sampling rate	48 kHz
Tx ADC max resolution	16 bit
Tx MIC_AMP1 gain	Internal gain: 0 dB or +24 dB
Tx MIC_AMP2 gain	Internal gain: +25.5 to -6 dB, in 1.5 dB steps
AUX PGA path gain settings	+11.5 to -24.5 dB, in 3 dB steps
HPH driver	Cap-coupled and capless modes
Headset switch detect (HSSD)	In standby and sleep modes via an interrupt
Line out and AUX_OUT	Line out and AUX_OUT

PCM Interface (1 of 2)

- **Two PCM interface modes are supported**:
  - Auxiliary PCM running at 128 kHz (default)
  - Primary PCM running at 2.048 MHz
  - API to call is snd_set_device
  - Pins used for AUX_PCM can be used to interface with an external stereo DAC (SDAC – details on the next page).
  - Refer to the *Application Note: External PCM Interface* (80-V7143-1) for more PCM interface details and implementation.
- **Auxiliary PCM**
  - Communicates with an external codec
  - 8-bit μ-law and 8-bit A-law codecs are supported
  - Uses standard long-sync timing and a 128 kHz clock

PCM Interface (2 of 2)

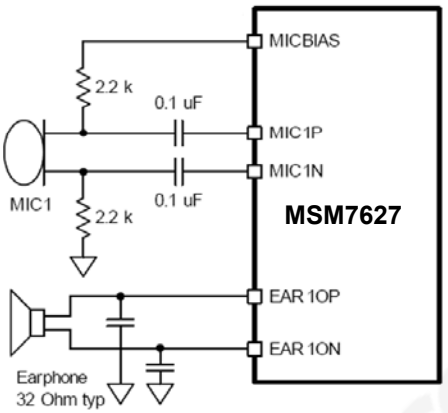
- **Primary PCM**
  - Supports 16-bit linear, 8-bit μ-law, and 8-bit A-law codecs
  - 2.048 MHz PCM data and short sync timing
  - Can be configured and controlled two ways:
    - Direct register access (CODEC_CTL register)
    - aDSP codec configuration commands (the preferred method)

Interfacing With External Stereo DAC

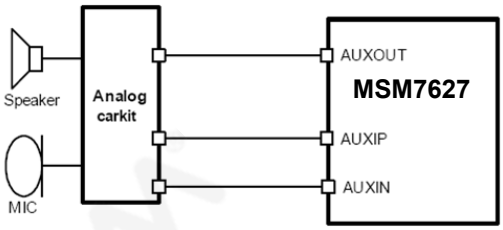
- **The MSM7627 pins used for AUX_PCM can also be used to interface with external stereo DAC (SDAC) to play stereo sound or music (MP3 or MIDI, for example)**.
  - I^2S used to transfer audio data for this interface. Currently, this can only be used as output mode to SDAC.
- **The following pins are used**:
  - SDAC_DOUT: Serial PCM data stream for both channels are output from the MSM device through this pin.
  - SDAC_L_R_N: This signal specifies the present data stream's intended stereo channel.
    - Left channel = 1
    - Right channel = 0
  - SDAC_CLK: Bit clock generated by the MSM7627 IC
  - SDAC_MCLK: An optional clock output from the MSM device to the external stereo DAC

External Analog Interface (1 of 7)

- Handset

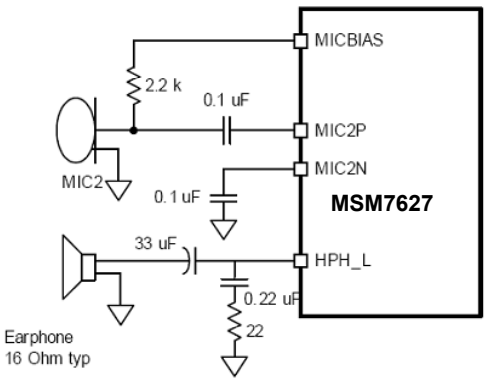


- AUX interface (car kit)

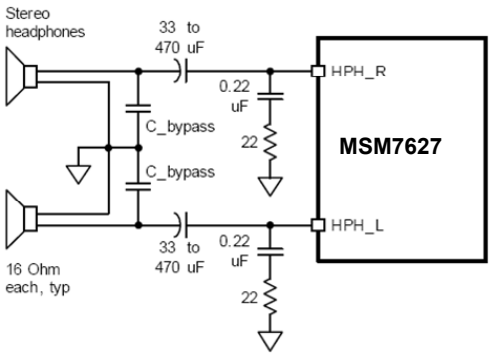


External Analog Interface (2 of 7)

- Headset
  - Mono single-ended

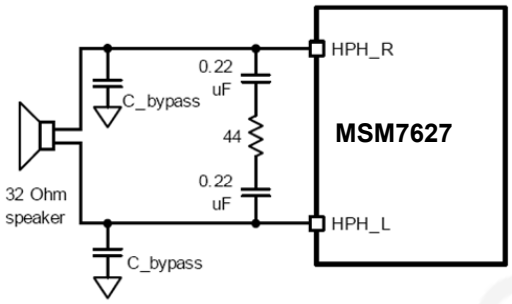


  - Stereo single-ended

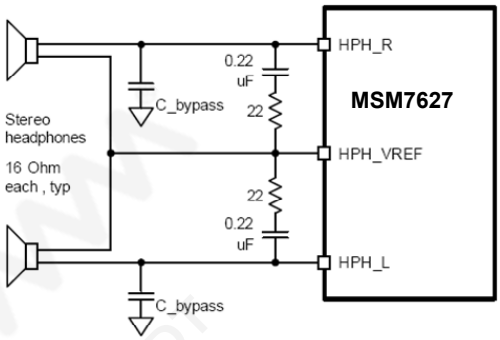


External Analog Interface (3 of 7)

- Mono differential

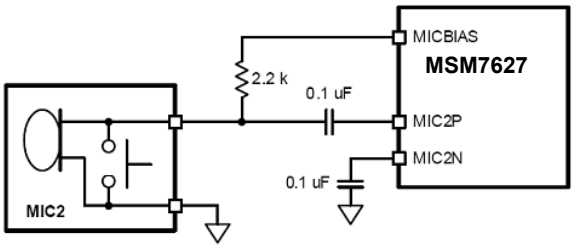


- Stereo single-end capless

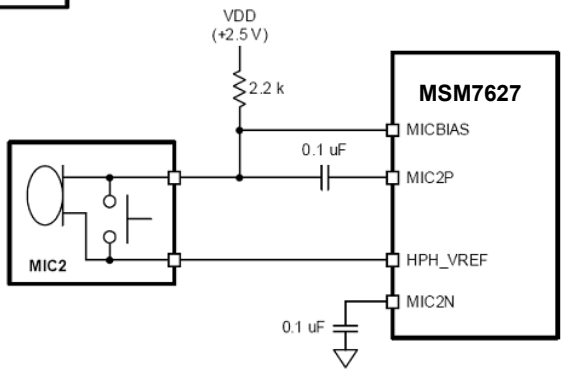


External Analog Interface (4 of 7)

- Headset switch detect (HSSD)



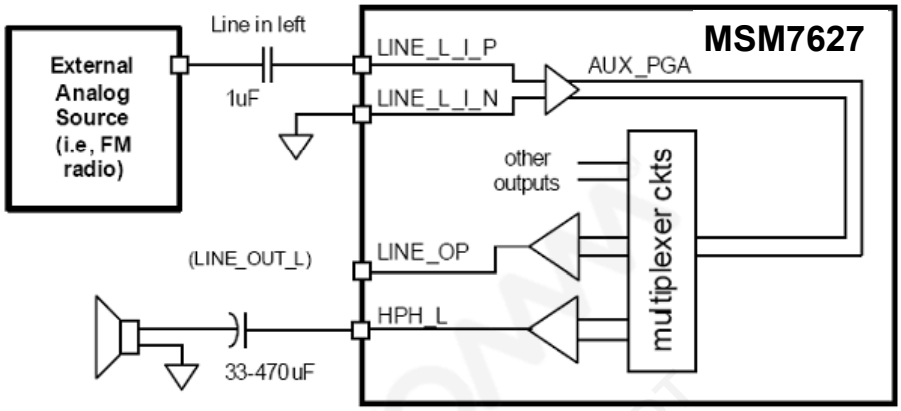
- HSSD using capless driver



Note: MIC inputs must be in single-ended mode to enable HSSD.

External Analog Interface (5 of 7)

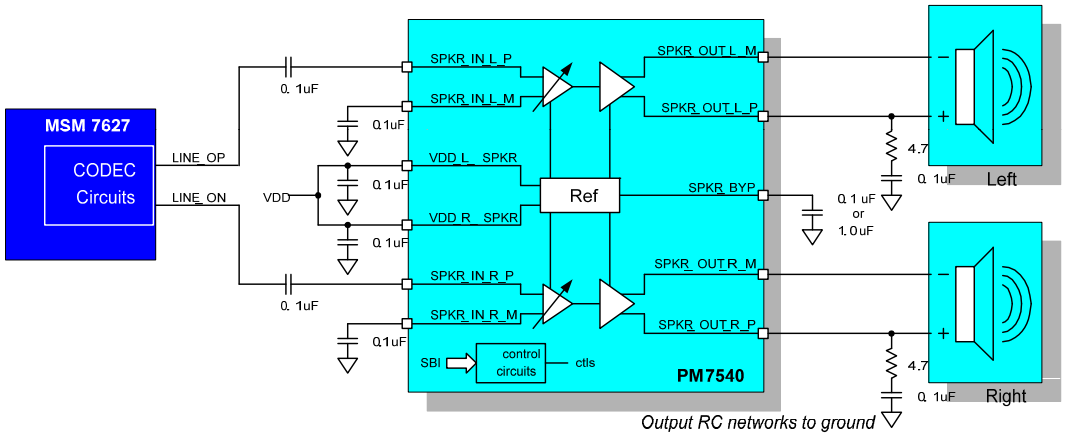
- Line input to output audio



Note: The analog audio signal can be routed to any output amplifiers (EAR1O, EAR20, HPH, AUXO); not limited to just HPH.

External Analog Interface (6 of 7)

- Interface to external speaker amplifier (PM7540 IC)



Output RC networks to ground must be connected to the plus pins (each speaker channel).

External Analog Interface (7 of 7)

- **Interface to external speaker amplifier (PM7540 IC)**
  - PM7540 input: Stereo single-ended/differential or mono differential
    - Stereo single-ended inputs can be summed together and output in mono.
  - PM7540 output: Stereo differential delivering 500 mW to each 8 Ω speaker
    - Can also be configured as mono or dual mono sound.
  - Interface recommendations
    - Set the MSM device digital gains and PMIC speaker analog gain appropriately to ensure the speaker amps do not saturate.
    - Set the analog high-pass filter corner according to the resonant frequency of the fair-field speaker transducer
    - Corner can be changed by either changing capacitor or by using the PM7540 IC's new variable input impedance feature.
    - For more information, see the *PM7540 Power Management IC User Guide* (80-VD691-3).

QUALCOMM
2010.07.13 at 18:08:46 PDT
ruijun.zhang-sh@...

MSM7627 Device Interfaces
JTAG and ETM

MSM7627 Debug and Test

- **MSM7627 IC provides two debugging methods**:
  - JTAG
  - ETM
- **Joint Test Action Group (JTAG)**
  - Aids in board-level testing and debugging
  - The JTAG interface allow test instructions and data to be shifted into the MSM device, and the test results to be read out in a serial format.
- **Embedded Trace Macrocell (ETM)**
  - Enables tracing while running ARM® processors at high speed

JTAG Debug and Test

- **The MSM7627 IC provides two separate JTAG ports (primary and auxiliary ports):**
  - The primary JTAG port is a dedicated port.
  - The auxiliary JTAG port is available through configurable GPIO pins.
- **These JTAG pins communicate with the ARM9 and ARM11 cores, depending upon the mode setting**.
  - The JTAG mode is selected by setting the MODE[3:0] pins.
- **MSM7627 JTAG features**:
  - Provides JTAG access to both ARM9 and ARM11 microprocessors.
    - Using daisy-chained ARM9 + ARM11 mode on the primary JTAG port
    - Using two separate JTAG ports with ARM9 on the primary and ARM11 on the auxiliary JTAG port
- **WDOG_EN can expire during JTAG operation**.
  - Disable by grounding pin or through software.
- **Refer to the *Application Note: JTAG Setup Procedure on MSM7500/MSM7200* (80-V9038-13) for more information about how to use the JTAG interface with the MSM7627 device**.

JTAG Connectivity Modes

Mode pins [3:0]	Phone mode and JTAG selection
0000	Native, ARM9 on primary JTAG, ARM11 on AUX JTAG
0001	**TLMM_INT_JTAG_CTL** register specifies the internal version of the MODE pin value for the Primary JTAG port. **TLMM_INT_JTAG_CTL** settings: 0000: ARM9 only 0001: ARM9 + ARM11 daisy-chained*

The four mode pins are V10, AD8, AB8, and AB9 (MSB to LSB).

* ARM9 must enable ARM11 through software to enable daisy-chain mode.

** A separate TAP controller is required for the MSM in boundary-scan mode.

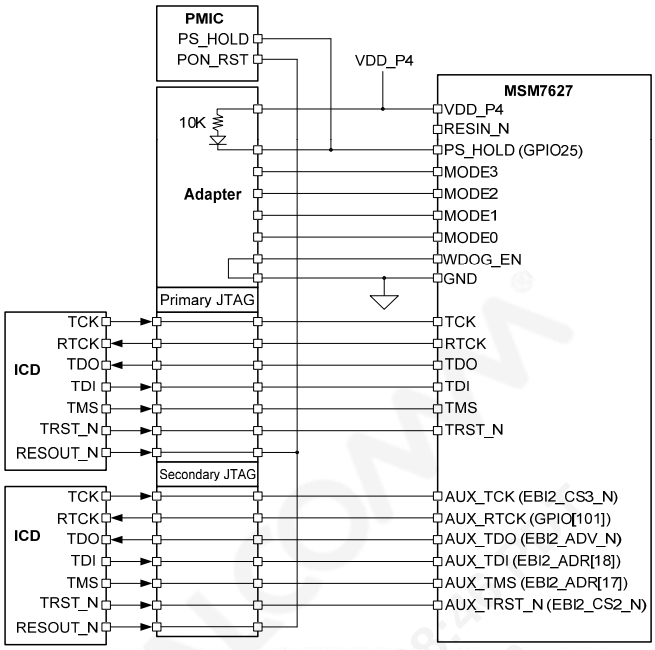
Note: The modes listed above have not been fully tested.

JTAG Pin Connections

Signal name	I/O	Voltage	Description	Comments
Primary interface – dedicated pins				
TRST_N	DI	P3	JTAG reset	
TCK	DI	P3	JTAG clock input	
TMS	DI	P3	JTAG mode select	
TDI	DI	P3	JTAG data input	
TDO	Z	P3	JTAG data output	
RTCK	DO	P3	JTAG return clock	
Secondary interface – configurable GPIO pins				
AUX_TRST_N	DI	P2	Auxiliary JTAG reset	EBI2_CS2_N
AUX_TCK	DI	P2	Auxiliary JTAG clock input	EBI2_CS3_N
AUX_TMS	DI	P2	Auxiliary JTAG mode sel	EBI2_ADR[17]
AUX_TDI	DI	P2	Auxiliary JTAG data input	EBI2_ADR[18]
AUX_TDO	Z	P2	Auxiliary JTAG data output	EBI2_ADV_N
AUX_RTCK	DO	P2	Auxiliary JTAG return clock	GPIO[101]
Mode control pins				
MODE3 MODE2 MODE1 MODE0	DI DI DI DI	P3 P3 P3 P3		Determines the IC operating mode

Note: when internal LCDC used, AUX_JTAG pins are lost.

Example JTAG Connection

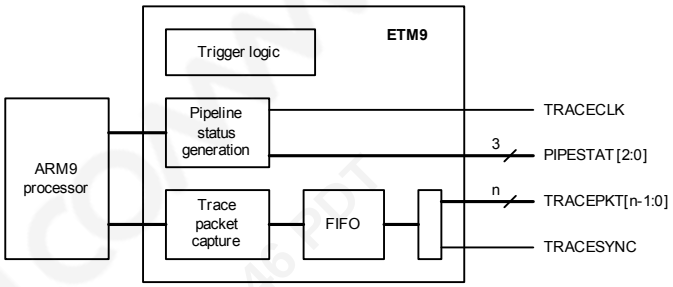


MSM7627 ETM Features

- **The MSM7627 is a dual-processor MSM device:**
  - ARM9
  - ARM11
- **Separate ETM block for each processor:**
  - ETM9
  - ETM11
- **The ETM consists of two parts:**
  - Trace port – This port broadcasts trace information (instruction or data trace).
  - Triggering facilities – These control the ETM to filter and control trace operations.
- **ETM architecture is different for the ARM9 compared to the ARM11:**
  - ETM is designed to be connected directly to the ARM core that it is tracing.

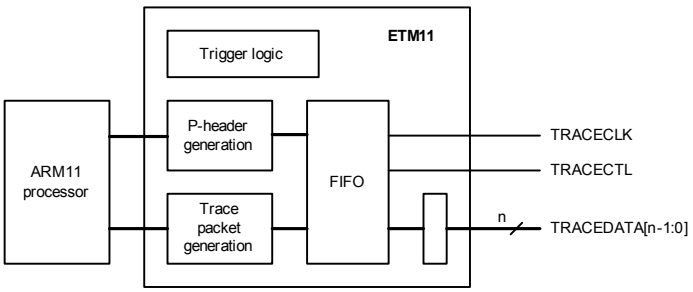
ETM9 Architecture

- **ETM9 architecture has a trace port that includes four signals:**
  - PIPESTAT (2:0): Pipeline status pins
  - TRACEPKT: Trace packet port (4/8/16 pins)
  - TRACESYNC: Trace packet synchronization pin
  - TRACECLK: Clock signal



ETM11 Architecture

- **The major differences between ETM11 and ETM9 are:**
  - ETM11 removes the PIPESTAT signals.
  - ETM11 trace-port protocol enables the trace port and the core to run at different speeds.
  - Trace data is collected on both clock edges.

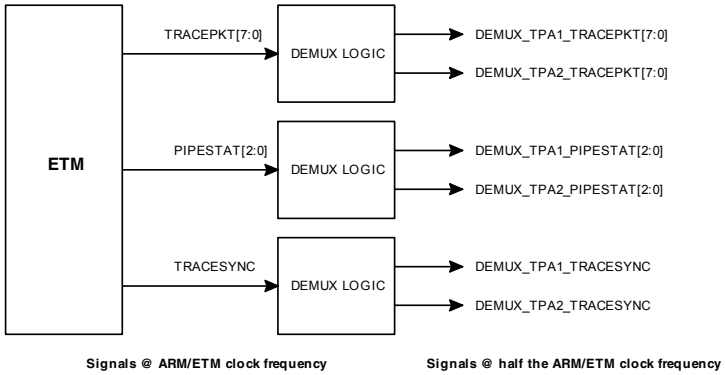


ETM9 Modes

- **MSM7627 IC supports several different ETM9 configurations and modes.**
- **The configuration options supported by MSM7627 ETM9 include:**
  - 16-bit normal mode: ETM pins are toggled at ARM9's maximum clock rate.
    - 21 pins are needed.
    - 1 trace port analyzer is needed.
  - 8-bit deMUXed mode: This mode is used when at-speed core operation is required and 16-bit mode is not available due to I/O speed limitations.
    - 25 pins are needed.
    - ARM9/ETM9 speed: 192 MHz
    - Pin speed: 192/2 MHz
    - Two trace port analyzers are needed.
  - Both ETM9 modes listed above are still being verified for the maximum supported clock rate.

8-bit DeMUXed ETM9 Mode

- This mode is used only when at-speed core operation is required and 16-bit mode is unavailable due to I/O speed limitations.
- Number of pins is doubled, so 8-bit trace is used instead of 16-bit trace.
- 25 pins are required.
- Requires two trace port analyzers.



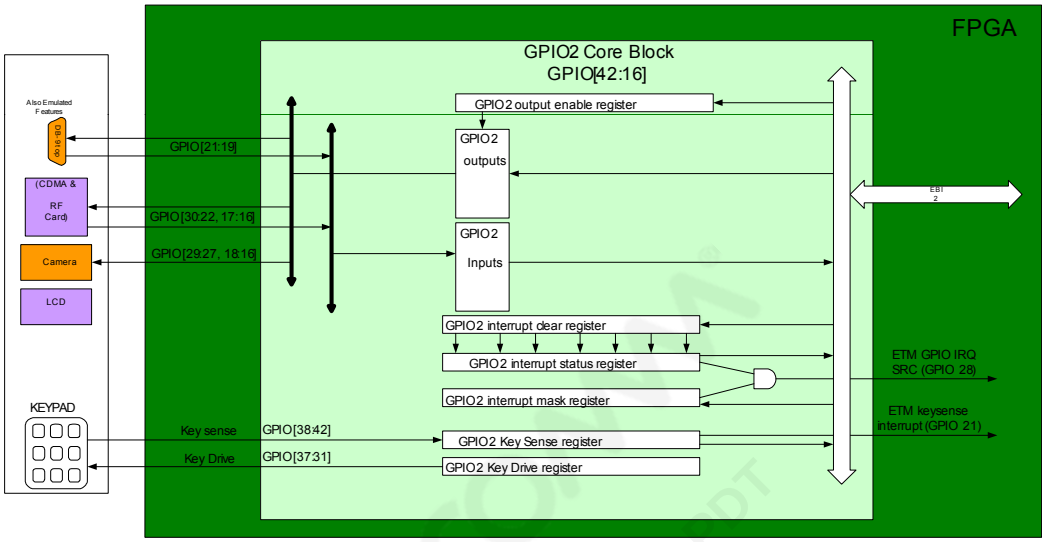
ETM Pin Connections

Signal name	I/O	Voltage	Description	Comments
ETM_TRDATA[15:0]	O	P3	16-bit ETM trace data; DATA[15] is the MSB, DATA[0] is the LSB.	133 MHz clock rate; 10 pF max load capacitor
ETM_TRACECLK GPIO[30]	O	P3	ETM trace clock	133 MHz clock rate; 10 pF max load capacitor
ETM9_TRACESYNC GPIO[31]	O	P3	Trace sync in ETM9	
ETM9_PIPESTAT0 ETM11_TRACEDATA0 GPIO[29]	O	P3	ETM9 pipestat0 … or … ETM11 trace data0	
ETM9_PIPESTAT1 ETM11_TRACECTL GPIO[27]	O	P3	ETM9 pipestat1 … or … ETM11 trace control	
ETM9_PIPESTAT2 GPIO[26]	O	P3	ETM9 only – pipestat2	
ETM9_PIPESTATB0 GPIO[16]	O	P3		Reserved for deMUX mode; 133 MHz clock rate; 10 pF max load capacitor
ETM9_PIPESTATB1 GPIO[17]	O	P3		
ETM9_PIPESTATB2 GPIO[18]	O	P3		
ETM9_TRACESYNCB DP_ETM_TRACECLK_B GPIO[82]	O	P3	ETM9 trace sync … or … Dual port ETM trace clock	
ETM_GPIO_CS_N GPIO[24]	I	P3		
ETM_KEYSENSE_IRQ GPIO[21]	I	P3		
ETM_GPIO_IRQ GPIO[28]	O	P3		

ETM GPIO Emulation

- During ETM mode, the MSM7627 GPIO [16:42] and GPIO [82] are used for ETM signals.
- When these GPIO pins are used in ETM mode, the alternate functionality is lost.
- The displaced functionality behind the ETM pins that functionally used the GPIO is replicated off-chip by FPGAs.
- These GPIOs are emulated using the EBI2 memory-mapped interface.

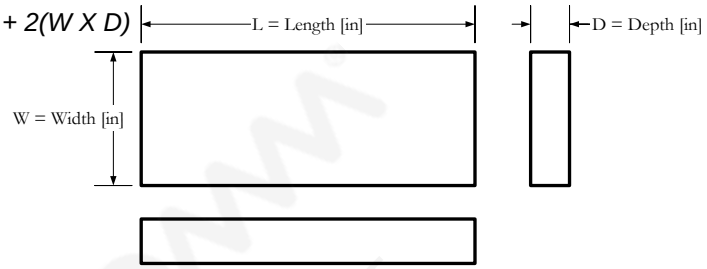
ETM GPIO Emulation: Example



MSM7627 Heat Dissipation Modeling

Heat Dissipation Modeling (1 of 2)

- **Modeling for temperature rising on UE surface**
  - Key parameters
    - Total power dissipation
    - Surface area
- **Step 1: Calculate surface area**
  - $A_{surface} = 2(L \times W) + 2(L \times D) + 2(W \times D)$



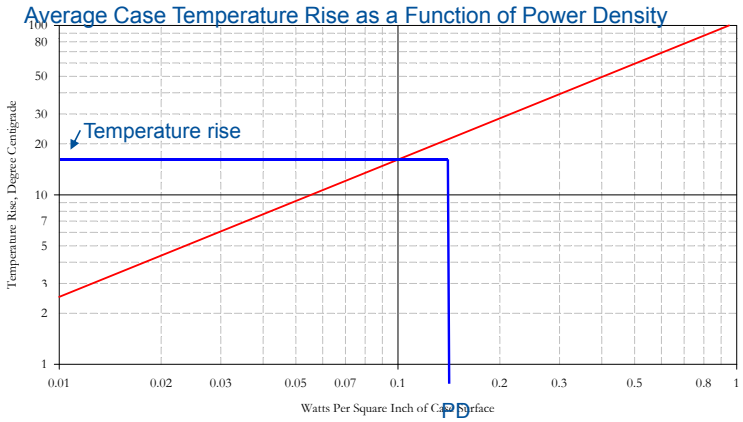
- **Assumption**
  - Mono-block form factor
  - At room temperature (25°C)
  - Total power-dissipation range (1.5 W to 4.5 W)

Heat Dissipation Modeling (2 of 2)

Step 2: Calculate surface power densityc

- $PD_{surface} = P_{average} / A_{surface}$

Step 3: Determine surface temperature from T_rise model



Graph derived from model

See the Application Note for detail

Reference Documents

Reference Documents (1 of 2)

MSM7627 Baseband Documents:

80-VM151-1	*MSM7627 MOBILE STATION MODEM DEVICE SPECIFICATION*
80-VM151-2	*MSM7627 MOBILE STATION MODEM SOFTWARE INTERFACE*
80-VM151-3	*MSM7627 MOBILE STATION MODEM USER GUIDE*
80-VM151-4	*MSM7627 MOBILE STATION MODEM DEVICE REVISION GUIDE*
80-VM151-6	*MSM7625 TO MSM7627 MIGRATION GUIDE*
80-VM151-41	*MSM7627 BASEBAND REFERENCE SCHEMATIC*
80-VM151-1A	*MSM7227/MSM7627 PIN ASSIGNMENT SPREADSHEET*

Application Notes and Guidelines:

80-V9038-15	*MSM7XXX QFUSES AND SECURITY*
80-VN499-7	*CONFIGURATION OF INPUT PINS DURING DEVICE SLEEP*
80-V9038-54	*DDR SDRAM DESIGN CONSIDERATIONS FOR MOBILE STATION MODEM(MSM) DEVICES*
80-V5557-1	*CAMERA INTERFACE ON MSM DEVICES*
80-V9038-11	*TOUCH SCREEN OPERATION FOR MSM7200 AND MSM7500*
80-VF815-19	*USB DESIGN GUIDELINES FOR MOBILE STATION MODEM (MSM) DEVICES*
80-V7837-1	*MULTIMEDIACARD SECURE DIGITAL CARD*
80-VM151-11	*USB AUDIO ELECTRICAL SPECIFICATION & SOFTWARE INTERFACE FOR QSD8X50/MSM7X25/MSM6246/MSM6290*
80-VE797-11	*FLUENCE ELECTRO-ACOUSTICAL DESIGN GUIDELINES*

QUALCOMM 2010.07.13 at 08:46 PDT ruijun.zhang-sim.com