QUALCOMM® CDMA Technologies

MSM7625 Mobile Station Modem

Device Specification (Advance Information)

80-VJ153-1 Rev. C

November 11, 2008

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Revision history

Revision	Date	Description
A	June 2008	Initial release
B	October 2008	Global: updated Chapter 4, Chapter 5, and Chapter 6 to reflect a global change Qualcomm is making to all products regarding device ordering information, package and carrier information, and the barcode label (see the text below for more details) Chapter 1, *Introduction* ■ Section 1.1, *Documentation overview*: updated summaries for chapters 4 through 6 to reflect new organization and content (see details below) Chapter 2, *Pin Definitions*: updated almost all of the content in this chapter Chapter 3, *Electrical Specifications* ■ Table 3-1, *Absolute maximum ratings*: added USB VBUS voltage (USBPHY_VBUS) value ■ Table 3-2, *Recommended operating conditions*: corrected description of VDD minimization and modified high-speed values for the V_{DD_C1} entry, removed power-collapsing value from the V_{DD_C2} entry, removed the USBPHY_VBUS entry, and modified table note #3 ■ Section 3.1.4, *DC characteristics*: updated cross-references in Table 3-4 and Table 3-5 notes ■ Table 3-10, *Sleep clock timing parameters*: updated the units for the *t(xoh)* and *t(xol)* entries ■ Replaced old EBI1 and EBI2 sections (Sections 3.2.5 to 3.2.7) with new Section 3.2.5 (*EBI1*) and Section 3.2.6 (*EBI2 timing*) ■ Table 3-24, *JTAG interface timing*: updated the TDI input hold time [t(htdi)] value to 25 ns ■ Table 3-26, *LCD controller interface timing*: updated t(adw) and t(adh) values and modfied table note #1 accordingly Chapter 4, *Device Marking and Ordering Information* (updated title) ■ Removed paragraph in Chapter 4 introduction ■ Moved Section 4.1, *Device physical dimensions* to Section 5.1 ■ Table 4-1, *Part marking line descriptions*: added supply source code (F) values in line 3, updated an assembly site code (A) value in line 4 (corrected Amkor location), and added the product revision (RR) values in line 4 ■ Updated Figure 4-2, *Example device identification code*, and the text immediately after this figure ■ Moved Section 4.4, *Device moisture sensitivity level (MSL)* to Section 6.1.2 ■ Moved Section 4.5, *Device thermal characteristics* to Section 3.1.3

Revision	Date	Description
B (cont'd)	October 2008	Chapter 5, *Package and Carrier Information* (updated title) ■ Switched the order of Chapter 5 and Chapter 6. Chapter 5 is now titled *Package and Carrier Information*, and Chapter 6 is now titled *PCB Mounting Guidelines* ■ Updated text in Chapter 5 introduction ■ Updated Figure 5-1, *456 NSP (11 x 11 x 1.05 mm) outline drawing* ■ Reorganized and revised text in Section 5.2, *Tape and reel information* ■ Added Section 5.3, *Barcode label and packing for shipment*: replaced all barcode and packing information (previously in Sections 6.2 through 6.4) with a reference to *IC Packing Methods and Materials Specification* (80-VK055-1) Chapter 6, *PCB Mounting Guidelines* ■ Corrected lead-free information in Chapter 6 introduction ■ Moved *Storage conditions, unpacking, and handling* to Section 6.1 ■ Updated Section 6.1.2, *Device moisture sensitivity level (MSL)* ■ Updated Figure 6-1, *456 NSP land pattern drawing* ■ Updated Figure 6-2, *456 NSP solder stencil design* Chapter 7, *Part Reliability Test Specification* (updated title) ■ Table 7-1, *Stress tests for the MSM7625 device*: added table entry for physical dimensions test
C	November 2008	Chapter 1, *Introduction* (Removed OTG from USB descriptions) ■ Figure 1-1, Changed HS-USB-OTG into HS-USB ■ Section 1.3.1, Removed USB-OTG description ■ Section 1.3.12, Removed OTG ■ Section 1.3.13, Updated audio codecs, Qtv, Qvideophone, and CMX • Added QCELP, EVRC, AMR-NB to Audio Codecs • Replaced Windows Media with Windows Audio v9, and Windows Audio ProPlus v10 from Qtv • Removed G.711 from Qvideophone • Added PMD/ADPCM/PNG/SAF/Multisequencer to CMX ■ Table 1-2, Removed USB-OTG row Chapter 2, *Pin Definitions* ■ Table 2-2, Updated alternate function, signal names, and descriptions • Removed DATA from the name of UART signals • RTR_SSBI to SSBI_RTR • Updated USB3_DATA_VP and USB3_SE_VM descriptions (removed "single ended data")

1 Introduction

1.1 Documentation overview

Technical information for the MSM7625™ Mobile Station Modem™ (MSM™) device is primarily covered by four documents (Table 1-1). Each is a self-contained document, but a thorough understanding of the device and its applications requires familiarization with all four documents. The device description provided in the next section is a good place to start. All released MSM7625 documents are posted on the CDMA Tech Support website (https://support.cdmatech.com) and are available for download.

Table 1-1 Primary MSM7625 documentation

Document number	Title/description
80-VJ153-1 (this document)	*MSM7625 Mobile Station Modem Device Specification* Conveys all MSM7625 device electrical and mechanical specifications. Additional material includes pin assignment definitions, PCB mounting specifications, packing methods and materials, and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-VJ153-2	*MSM7625 Mobile Station Modem Software Interface Manual* Provides detailed information about the MSM7625 device software interface and its clocks, security, user interface, and registers.
80-VJ153-3	*MSM7625 Mobile Station Modem User Guide* Provides detailed descriptions of all MSM7625 device functions and interfaces, including its various operating modes.
80-VJ153-4	*MSM7625 Mobile Station Modem Device Revision Guide* Provides a history of MSM7625 device revisions and changes to its device specification. It explains how to identify the various device revisions, discusses known issues (or bugs) for each revision and how to work around them, and lists performance specification changes between each revision of the device specification (80-VJ153-1).

This MSM7625 device specification is organized as follows:

Chapter 1: Provides an overview of the MSM7625 documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2: Defines the device pin assignments.

Chapter 3: Defines the device electrical performance specifications, including absolute maximum and recommended operating conditions.

Chapter 4: Provides the visible markings and ordering information for the MSM7625 device.

Chapter 5: Describes the physical dimensions and the tape and reel packaging of the MSM7625 device.

Chapter 6: Provides specifications for mounting MSM7625 parts.

Chapter 7: Presents MSM7625 device reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 Concise device description

The Convergence Platform continues to evolve with the latest addition to this great product line. The MSM7625 (Figure 1-1) not only offers the capability of high-performance applications, it also provides worldwide phone coverage on a single device:

- CDMA 1xRTT plus CDMA2000 1xEV-DO Rev. A
- WCDMA Release-99 plus HSDPA and HSUPA
- GSM/GPRS/EDGE

With the MSM7625 device, more powerful business and user applications are possible, while allowing the user to access the widest range of wireless networks.

Wireless devices enabled by the Convergence Platform chipsets will leverage the convenience of consumer electronics to support:

- Point-to-point video telephony for on-the-go (OTG) conferencing
- Downloadable feature-length movies via Unicast services for extended viewing of the latest releases
- Streaming TV and video clips via multicasting services to keep users up-to-date on their particular areas of interest while they are on the go
- Multimedia consumers' everyday use, including music, streaming video, photos, and more

With the Convergence Platform, camera phones can rival the resolution of all but a few high-end digital still cameras. They can store and manipulate images in the handset, and then transmit them with cable-modem speed.

The key appeal of the Convergence Platform-enabled devices is their ability to seamlessly connect to the indispensable electronics that people use every day. Integrated USB, MDDI, and LCDC can drive computers, printers, video projectors, televisions, and other external devices. The highly integrated Qualcomm chipset solutions cut bill-of-material (BOM) costs, power consumption, and time-to-market, enabling manufacturers to build attractive and sleek form factors that mirror the incredible performance of the Convergence Platform chipset inside.

The MSM7625 chipset and system software solution is the next generation of the Convergence Platform; it builds on Qualcomm's years of systems expertise and field experience with CDMA, WCDMA, GSM, and GPS technologies. Qualcomm works with its partners to develop products that meet the exact needs of the growing wireless market, providing its customers with complete, verifiable solutions, including fully segmented product families, systems software, testing, and support.

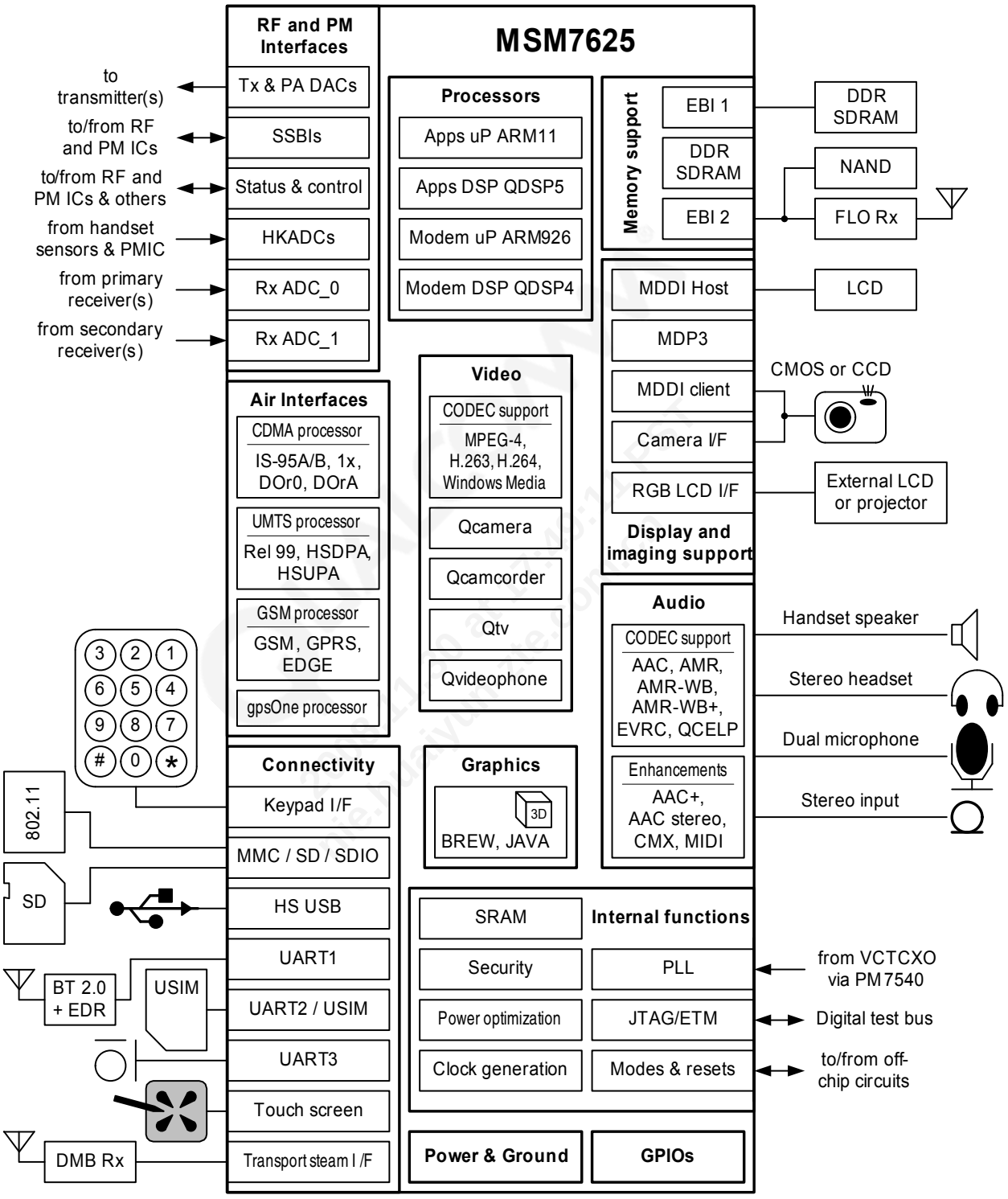


Figure 1-1 MSM7625 functional block diagram

The MSM7625 device integrates the ARM1136-J™ and ARM926EJ-S™ processor cores, offering the ARM® Jazelle™ Java® hardware accelerator: one low-power, high-performance QDSP5000™ application digital signal processor (aDSP) and one QDSP4000™ modem digital signal processor (mDSP) core; hardware acceleration for video, imaging, and graphics; and a wideband stereo codec to support enhanced digital audio applications. The hardware acceleration eliminates the need for the multimedia companion processors normally required for video and audio-based applications that support MP3 music files, a MIDI synthesizer, and video and still-image recording and playback. By removing the need for costly applications coprocessors and memory subsystems, the MSM7625 solution reduces BOM costs and increases standby and talk times.

The MSM7625 device supports CDMA (1x and DO), WCDMA (Release-99, HSDPA, and HSUPA), and GSM/GPRS/EDGE; these enable rich wireless multimedia services, such as high-speed upload of multimedia files and attachments, interactive gaming, and a variety of IP-based services such as the voice over Internet (VoIP) protocol. Real-time conversational services such as push-to-talk, video telephony, and instant multimedia (an extension of push-to-talk that combines immediate voice with simultaneous delivery of video and pictures) are also supported.

Very high peak data rates are supported: 7.2 Mbps on the downlink (DL) and 5.76 Mbps on the uplink (UL) using HSDPA/HSUPA; or 3.1 Mbps on the downlink and 1.8 Mbps on the uplink using DOrA. Such high data rates enable network operators to provide an even broader range of wireless multimedia and other data services for consumers and enterprise customers. HSDPA/HSUPA and DOrA are optimized for packet data service, and provide some of the lowest costs per bit when compared with other wireless wide area network (WAN) technologies. The MSM7625 solution integrates powerful application processors into the Qualcomm market-proven wireless modem, offering increased processing capacity combined with lower power consumption. With the MSM7625 chipset solution, handset manufacturers can design sleek, converged consumer wireless devices that boast the industry's most advanced image quality and resolution to provide enhanced 3D animation, gaming, streaming video, video conferencing, MediaFLO™, and more.

The MSM7625 has the following encoding characteristics:

- MPEG-4/H.263 encoding performance is 24 fps @QVGA.
- H.264 encoding is not available.
- AAC audio-only encoding (video + AAC audio is not available).
- Camera multishot is not available.

MSM7625 chipset solution benefits

- Integrates dedicated hardware cores and an applications processor into the MSM device — offers superior image quality and resolution for mobile devices and extended application time.
- Provides longer run time for mobile devices compared with other industry solutions that use companion processors.
- Offers a higher degree of integration (digital and analog functions on a single chip) and dedicated hardware cores, which decrease power consumption and size while increasing performance and quality.

- Eliminates the need for intermediate frequency (IF) components, decreasing printed circuit board (PCB) area and reducing time-to-market and BOM costs.
- Enables a wide variety of location-based services and applications, including points of interest, personal navigation, friend finder, and position stamping of images and videos taken by the user.
- Has a single platform that provides dedicated support for all market-leading voice and audio codecs and other multimedia formats to support carrier deployments around the world.
- Offers a high-quality digital still-image camera (DSC) performance with up to 5 megapixel resolution.
- Offers MDDI and LCDC ports to seamless connect embedded LCDs, cameras, and external projectors.
- Provides ample processing power to support third-party operating systems.

Qualcomm provides a complete software suite and advance mobile subscriber software (AMSS) for building handsets based on the MSM7625 chipset. AMSS software is designed to run on a Subscriber unit reference platform™ (SURF™) phone platform, an optional development platform optimized to assist in evaluating, testing, and debugging AMSS software.

Launchpad™ Suite of Technologies

The Launchpad Suite of Technologies offers wireless operators and manufacturers a cost-effective, scalable, and timely solution for providing advanced wireless data services. This seamlessly integrated solution enables advanced next-generation applications and services that incorporate multimedia, position location, connectivity, and customized user interface and storage capabilities. Launchpad features are available for each Qualcomm chipset, closely matching the specific functionality and cost-target objectives agreed upon in joint product planning with manufacturers and wireless service operators worldwide.

The MSM7625 solution supports the advanced feature set of the Qualcomm Launchpad Suite of Technologies, including streaming video and audio, enhanced MIDI audio, spatialized and positional audio, still-image and video encoding and decoding, Java acceleration, and a 5-megapixel camera interface. The MSM7625 solution also integrates gpsOne® functionality to support assisted and standalone GPS — enabling a wide variety of location-based services and applications, including points of interest, personal navigation, and friend finder.

gpsOne technology

gpsOne technology merges GPS satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs well even in very challenging environmental conditions where conventional GPS receivers fail. It provides a platform to enable wireless operators to address both location-based services and emergency mandates, such as the United States FCC E911 mandate.

When a request for position location is issued in mobile-assisted mode, the available network information is provided to the location server (e.g., cell-ID), and assistance is requested from the location server. The location server sends the assistance information to the handset. The handset/mobile unit measures the GPS observables and provides the GPS measurements along with available network data (that is appropriate for the given air interface technology) to the location server. The location server then calculates the position location and returns the results to the requesting entity.

In mobile-based mode, the assistance data provided by the location server encompasses not only the information required to assist the handset in measuring the satellite signals, but also the information required to calculate the handset's position. Therefore, rather than provide the GPS measurements and available network data back to the location server, the mobile calculates the location on the handset and passes the results to the requesting entity.

In standalone (autonomous) mode, the handset demodulates the data directly from the GPS satellites. This mode has some reduced cold-start sensitivity, and a longer time to first fix as compared with the assisted modes. However, it requires no server interaction and works in out-of-network coverage situations.

This combination of GPS measurements and available network information provides:

- High-sensitivity solution that works in all terrains: indoor, outdoor, urban, and rural
- High availability that is enabled by using both satellite and network information

Therefore, while network solutions typically perform poorly in rural areas and areas of poor cell geometry/density, and while unassisted, GPS-only solutions typically perform poorly indoors, the Qualcomm gpsOne solution provides optimal time-to-fix, accuracy, sensitivity, availability, and reduced network utilization in both of these environments, depending on the given condition.

The gpsOne solution in assisted modes provides a cold-start GPS sensitivity improvement of approximately 20 to 30 dB over unassisted, conventional GPS receivers.

Compared to network solutions that require equipment at each cell site, the gpsOne solution integrates a complete GPS receiver in every MSM7625 chipset. This means that each handset is capable of position location without requiring expensive cell site equipment. This solution not only can be used to help operators address the FCC E911 mandate in the United States (and mandates planned for other countries), but also provides a ubiquitous platform for location-based applications. The gpsOne solution enables consumer-priced, position-capable handsets for location-based services worldwide.

radioOne® technology

The MSM7625 device interfaces directly with the Qualcomm new radioOne RF ASICs. radioOne is a revolutionary technology for CDMA and UMTS transceivers that use a zero intermediate frequency (ZIF) architecture, or direct conversion. Direct conversion eliminates the need for large IF surface acoustic wave (SAW) filters and additional IF circuitry, which significantly reduces the handset BOM parts count. This reduction in the parts count facilitates production of multiband and multimode handsets in smaller form factors. radioOne technology also incorporates the frequency synthesis and passive elements used in converting baseband signals to and from the RF bands. External UHF oscillators are fully integrated to enable operation on systems around the world with simplified parts procurement.

The BREW® solution

The MSM7625 device includes support for the Qualcomm BREW solution. BREW is a complete product and business system for the development and over-the-air deployment of data services on wireless devices. The BREW solution provides the necessary tools and value-added services to developers, device manufacturers, and wireless operators for application development and distribution, device configuration, and billing/payment.

MediaFLO

MediaFLO is an end-to-end solution that enables multicasting of high-quality video, audio, clipcast media, and IP data-casting to a large number of mobile users. The forward-link only (FLO™) air interface implements the physical layer of the MediaFLO system. An overview of the MediaFLO system and FLO technology is available at www.mediaFLO.com. The following standard for MediaFLO operation can be used as reference:

TIA-1099: *Forward Link Only Air Interface Specification for Terrestrial Mobile Multimedia Multicast*

SecureMSM™ Platform V3

The MSM7625 device includes support for the SecureMSM security solution. The SecureMSM security solution incorporates the following features:

- Secure boot — protects against reflashing attacks:
  - Trusted third-party certificate authority (GeoTrust) provides code-signing service to manufacturers and to Qualcomm.
  - Strong 2048-bit RSA keys
  - Enables manufacturers and Qualcomm to ensure that their own code is running unchanged on the device.
- Secure component framework:
  - Capabilities-based architecture (access control for resource)
  - Partitioned software provides isolation of compromise/subvert.
  - Only known, trusted processes are permitted to access materials in the secure file system (SFS).
- Secure storage:
  - 128-bit hardware key for (AES) encryption of SFS
  - Operations using a hardware key are run in on-chip RAM, making observation extremely difficult.
- Unchangeable hardware ID is unique to each MSM device.

The result is a very robust platform securing OMA DRM v2.0 services, CPRM, and e-commerce transactions.

1.3 Device features

This section lists MSM7625 device features, beginning with its general features and continuing with features organized according to its major functions.

1.3.1 General MSM7625 device features

The MSM7625 system solution consists of the MSM7625, RTR6500™, RTR6285™, and PM7540™ ICs, plus AMSS™ system software with the SURF7625™ platform available for development.

- CDMA 1xRTT plus CDMA2000 1xEV-DO Rev. A
- WCDMA Release-99 plus HSDPA and HSUPA
- GSM/GPRS/EDGE
- High-performance ARM1136-J application processor running at up to 528 MHz
- High-performance ARM926EJ-S modem processor running at up to 256 MHz
- Java hardware acceleration for faster Java-based games and other applets
- Support for Bluetooth® 2.0 EDR via an external Bluetooth System-on-Chip (SoC)
- High-speed, serial mobile display digital interface that optimizes the interconnection cost between the MSM device and the LCD panel
- Receive diversity support for CDMA and WCDMA modes, which provides improved capacity and data throughput
- Built-in high-speed USB core and PHY
- Integrated wideband stereo codec for digital audio applications
- Direct interface to digital camera module with video front-end (VFE) image processing
- GPS position location capabilities
- Vocoder support (EVRC, 13k QCELP®, GSM-HR, FR, EFR, AMR, AMR-WB/+, and 4GV™)
- Advanced 11 mm × 11 mm × 1.05 mm, 0.4 mm pitch, 456-pin nano-scale package (NSP)

1.3.2 CDMA 1X (IS-2000) features supported

- Fast 800 Hz forward power control
- Quasi-orthogonal functions
- Supplemental channel (SCH) support
- CDMA2000 1X forward quick paging channel (F-QPCH)
- Convolutional and turbo codes on SCH
- Radio link protocol (RLP3)

1.3.3 CDMA 1xEV-DO (IS-856) features

- High-speed peak data rates of 3.1 Mbps on the downlink and 1.8 Mbps on the uplink
- Handoffs between IS-2000 and IS-856 systems
- Slotted-mode operation for reduced power consumption
- Platinum broadcast supporting 1.5 Mbps multicast services on the downlink via OFDM® overlay

1.3.4 WCDMA Release-99 features

The MSM7625 device supports Release-99, June 2004 of the WCDMA FDD standard, including the following features:

- All modes and data rates for WCDMA frequency division duplex (FDD), with the following restrictions:
  - The downlink (DL) supports the following specifications:
    - Up to four physical channels, including the broadcast channel (BCH), if present
    - Up to three dedicated physical channels (DPCHs)
    - Spreading factor (SF) range support from 4 to 256
    - Support for the following transmit diversity modes:
      - Space-time transmit diversity (STTD)
      - Time-switched transmit diversity (TSTD)
      - Closed-loop feedback transmit diversity (CLTD)
  - The uplink (UL) supports the following specifications:
    - The uplink provides the following UE support:
      - One physical channel, eight TrCH, and 16 TrBks starting at any frame boundary
      - A maximum data rate of 384 kbps
    - Full SF range support from 4 to 256
- SMS (CS and PS)
- PS data rate: 384 kbps DL/384 kbps UL
- CS data rate: 64 kbps DL/64 kbps UL
- AMR (all rates)

1.3.5 HSDPA features

The MSM7625 device supports the Release 5, December 2004 standard for HSDPA, including the following features:

- HS-DSCH (HS-SCCH, HS-PDSCH, and HS-DPCCH) and the Release-99 transport channels as defined in 3GPP specifications
- A maximum of four simultaneous HS-SCCH channels as defined in the 3GPP specifications
- A maximum of 10 HS-PDSCH channels, both QPSK and 16 QAM modulation and UE category 6 in software release 2.0, and category 8 in software release 3.0
- CQI and ACK/NACK on HS-DPCCH channel as defined in the 3GPP specifications
- All incremental redundancy versions for HARQ as defined in the 3GPP specifications
- Can switch between HS-PDSCH and DPCH channel resources as directed by the network
- Can be configured to support any of the two power classes 3 or 4 as defined in the 3GPP R5 specifications (25.101)
- Network activation of compressed mode by SF/2 or HLS on the DPCH for conducting inter-frequency or inter-RAT measurements when the HS-DSCH is active
- STTD on both associated DPCH and HS-DSCH simultaneously
- CLTD mode 1 on the DPCH when the HS-PDSCH is active
- STTD on HS-SCCH when either STTD or CLTD mode 1 are configured on the associated DPCH
- TFC selection limitation on the UL factoring in transmissions on the HS-DPCCH as required in TS 25.133
- HSDPA enables PS data speeds up to 7.2 Mbps on the downlink

1.3.6 HSUPA features

The MSM7625 device supports the Release 6, March 2006 standard for HSUPA, including the following features:

- N E-AGCH, E-RGCH and E-HICH channels for downlink as defined in the 3GPP specifications. E-RGCH and E-HICH supports serving and non-serving radio links, with up to four radio links in the E-DCH active set.
- STTD on all HSUPA downlink channels
- CLTD mode 1 on HS-PDSCH and DPCH along with HSUPA channels
- All incremental redundancy versions for HARQ and maximum number of HARQ retransmissions as defined in 3GPP specifications
- E-DCH channel on the uplink as defined in the 3GPP specifications with support for up to four E-DPDCH channels
- E-DCH data rates of up to 5.76 Mbps for 2ms TTI (UE category 6) uplink
- HSUPA channels simultaneously with Release-99 and HSDPA channels as defined in the 3GPP specifications

- Switch between HSUPA channels and DPCH channel resources as directed by the network
- Handover using compressed mode with simultaneous E-DCH and HS-DSCH interactive/background and streaming QoS classes

1.3.7 GSM features

The following GSM modes and data rates are supported by the MSM7625 hardware. Support modes conform to Release-99 (R99) specification of subfeature.

- Voice features
  - FR
  - EFR
  - AMR
  - HR
  - A5/1 and A5/2 ciphering
- Circuit-switched data features
  - 9.6 k
  - 14.4 k
  - Fax
  - Transparent and non-transparent modes for CS data and fax
  - No subrates are supported

1.3.8 GPRS features

- Packet-switched data (GPRS)
- DTM (simple class A) operation
- Multislot class 12 data services
- CS schemes — CS1, CS2, CS3, and CS4
- GEA1, GEA2, and GEA3 ciphering
- Maximum of four Rx timeslots per frame

1.3.9 EDGE features

- EDGE E2 power class for 8 PSK
- DTM (simple class A), multislot class 12
- Downlink coding schemes: CS 1-4, MCS 1-9
- Uplink coding schemes: CS 1-4, MCS 1-9
- BEP reporting

- SRB loopback and test mode B
- 8-bit and 11-bit RACH
- PBCCH support
- One-phase/two-phase access procedures
- Link adaptation and IR
- NACC, extended UL TBF

1.3.10 Position location features

- Next-generation gpsOne solution with an enhanced GPS engine
- Enhanced filtering software optimizes GPS accuracy and availability
- Full integration with Windows® Mobile, Java®, and BREW-based development environments
- MS-assisted, MS-based, MS-assisted/hybrid, and standalone GPS modes
- gpsOneXTRA Assistance™ for enhanced standalone GPS performance
- Support for UMTS control plane, GSM control plane, and OMA SUPL 1.0 user plane assisted-GPS protocols

1.3.11 Microprocessor and memory subsystem

- High-performance ARM1136-J application processor:
  - ARM architecture v6
  - 32-kB instruction and 32-kB data cache
  - 4 kB level-one tightly-coupled memory (TCM)
  - 8-stage pipeline, branch prediction with return stack
  - Supports the ARM and Thumb instruction sets, and Jazelle technology to enable direct execution of Java bytecodes
  - Low-interrupt latency
- Industry standard ARM926EJ-S embedded microprocessor subsystem
  - 16-kB instruction and 16-kB data cache
  - ARM version 5TEJ instructions
  - Higher performance five-stage pipeline, Harvard-cached architecture
  - Higher internal CPU clock rate with on-chip cache

- Enhanced memory support
  - 128-MHz bus clock for DDR SDRAM
  - Dual-memory buses separating the high-speed memory subsystem (EBI1) from low-speed peripherals (EBI2) such as LCD panels
  - 1.8-V or 2.6-V memory interface support (excluding EBI1 and SMI)
  - NAND/OneNAND™ flash memory interface
  - Boot from NAND/OneNAND
- Internal watchdog and sleep timers

1.3.12 Supported connectivity features

- High-speed USB port with built-in PHY
- Four universal asynchronous receiver transmitter (UART) serial ports
- Two USIM ports (via UART)
- Two high-speed UARTs (DM via UART)
- Four SD/mini SD/SDIO card ports
- Parallel LCD interface
- RGB888 interface (LCD controller)
- General-purpose I/O pins
- High-speed serial MDDI port that optimizes the interconnection cost between the MSM device and the LCD panel.
- Capable of supporting broadcast technologies, including the Qualcomm FLO technology, DVB-H, and ISDB-T.

1.3.13 Supported multimedia features

- Additional general-purpose MIPS:
  - One QDSP5000 aDSP
  - Dedicated hardware accelerators and compression engines
- Improved Java, BREW, and game performance
- Various accessories via USB host connectivity
  - Integrated USB host controller functionality
- Compelling visual and audio applications:
  - High-quality digital camera processing, supporting CCD or CMOS image sensors up to 5 megapixels
  - Dedicated support for market-leading codecs such as MPEG-4, H.263, H.264, and Windows Media

- Integrated stereo wideband codec for music/digital clips
- CMX® — 128 polyphonic MIDI wavetable synthesizer
- Audio codecs: MP3, QCELP, EVRC, AMR-NB, AMR-WB/+, AAC, aacPlus™, enhanced aacPlus, and Windows Audio
- Streaming video (Qtv™)
  - WQVGA at 30 frames per second (fps) playback and 15 fps streaming
  - Support for various video codecs formats: MPEG-4, H.263, H.264, and Windows Media
  - AMR-NB, AMR-WB/+, AAC, AAC Plus, Enhanced aacPlus, Windows Audio v9, and Windows Audio ProPlus v10
- Video (Qcamcorder™)
  - QVGA video encode and decode at 24 fps
  - MPEG-4 and H.263
  - QCELP, AMR-NB, and EVRC
- Video telephony services (Qvideophone™)
  - Video telephony at 15 fps, QCIF resolution
  - H.263 profile 0/3 (Level 10), MPEG simple profile
  - EVRC and AMR-NB

- High-speed broadcast services over 1xEV-DO Gold/Platinum multicast
  - Enables TV-like functionality on a handset
- CMX (enhanced audio engine that enables time-synchronization of MIDI, audio, images, animation, text, and LED/vibrate)
  - 128 poly
  - Playback of following formats:
    - MIDI
    - General MIDI
    - SP-MIDI
    - SMAF (up to MA-5 audio only)
    - PMD/XMF/DLS
    - ADPCM
    - PNG/SAF
    - Multisequencer
  - Scalable vector graphics (SVG) Tiny 1.2
- Enhanced sound
  - QConcert™ (spatialized audio)

- QAudioFX™ (3D positional audio for gaming)

1.3.14 Audio processing features

- Integrated wideband stereo codec
  - 16-bit DAC with typical 88 dB dynamic range
  - Sampling rates up to 48 kHz on the speaker path and 48 kHz on the microphone path
  - Supports summing of an external device's stereo single-ended analog signal
  - Supports summing of an I2S digital audio signal
  - Supports headset switch press detection
- Enhanced Acoustic echo cancellation for full duplex calls
- PureVoice Audio AGC™
- Internal vocoder supporting 13 kbps PureVoice®

1.4 Terms and acronyms

Table 1-2 defines abbreviations commonly used throughout this document.

Table 1-2 Terms and acronyms

Term	Definition
4GV	4th generation vocoder
AAGC	Audio automatic gain control
ADC	Analog-to-digital converter
aDSP	Applications digital signal processor
AEC	Acoustic echo cancellation
AGC	Automatic gain control
AMR	Adaptive multi-rate (vocoder)
AMSS	Advanced Mobile Subscriber Station (software)
BER	Bit error rate
Bps	Bits per second
BT	Bluetooth
CAGC	CDMA AGC
CDMA	Code Division Multiple Access
CELP	Code excited linear prediction
CIF	Common intermediate format (352 × 288 image resolution)
CMX®	Compact Media Extension (registered by Qualcomm)
Codec	Coder-decoder
CRC	Cyclic redundancy code
DAC	Digital-to-analog converter
DDR	Dual data rate

Table 1-2 Terms and acronyms (cont.)

Term	Definition
DRM	Digital rights management
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution
ETM	Embedded trace macrocell
EVRC	Enhanced variable rate codec
FLO	Forward link only
FPS	Frames per second
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GSM	Global system for mobile communications
HSDPA	High-speed downlink packet access
HSUPA	High-speed uplink packet access
IF	Intermediate frequency
ISM	Internal stacked memory
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	Kilobits per second
LCD	Liquid crystal display
LSBit or LSByte	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MDDI	Mobile display digital interface
MDP	Mobile display processor
mDSP	Modem digital signal processor
MIDI	Musical instrument digital interface
MMC	Multimedia card
MPEG	Motion picture experts group
MSBit or MSByte	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
MSM	Mobile Station Modem (trademarked by Qualcomm)
NSP	Nano-scale package
OMA	Open Mobile Alliance
PA	Power amplifier
PCM	Pulse-coded modulation
PDM	Pulse-density modulation

Table 1-2 Terms and acronyms (cont.)

Term	Definition
PM	Power management
QCELP	Qualcomm Code Excited Linear Prediction
QCIF	Quarter common intermediate format (176 pixels/line, 144 lines/frame)
QCT	Qualcomm CDMA Technologies
QLIC	Quasi-linear interference cancellation
radioOne	Zero-IF (ZIF) radio architecture
RLP	Radio link protocol
RTR	Radio frequency transceiver
RUIM	Removable user identity module
SD	Secure digital
SDAC	Stereo digital-to-analog converter
SDRAM	Synchronous dynamic random access memory
SFS	Secure file system
SIM	Subscriber identity module
SoC	System-on-Chip
Sps	Symbols per second (or samples per second)
SURF	Subscriber unit reference platform
TAP	Test access port
TCXO	Temperature-compensated crystal oscillator
UART	Universal asynchronous receiver transmitter
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USIM	UMTS subscriber identity module
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator
WCDMA	Wideband Code Division Multiple Access
ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-3 defines special marks used in this document.

Table 1-3 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, GPIO_INT [7:0] may indicate a range that is 8 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The highly integrated MSM7625 device is available in the 456-pin nano-scale package (456 NSP); its pins serve a wide variety of purposes. This chapter:

- Defines the parameters used to describe the I/Os
- Provides concise functional descriptions of each pin
- Provides an illustration of the pin assignments

2.1 I/O parameter definitions

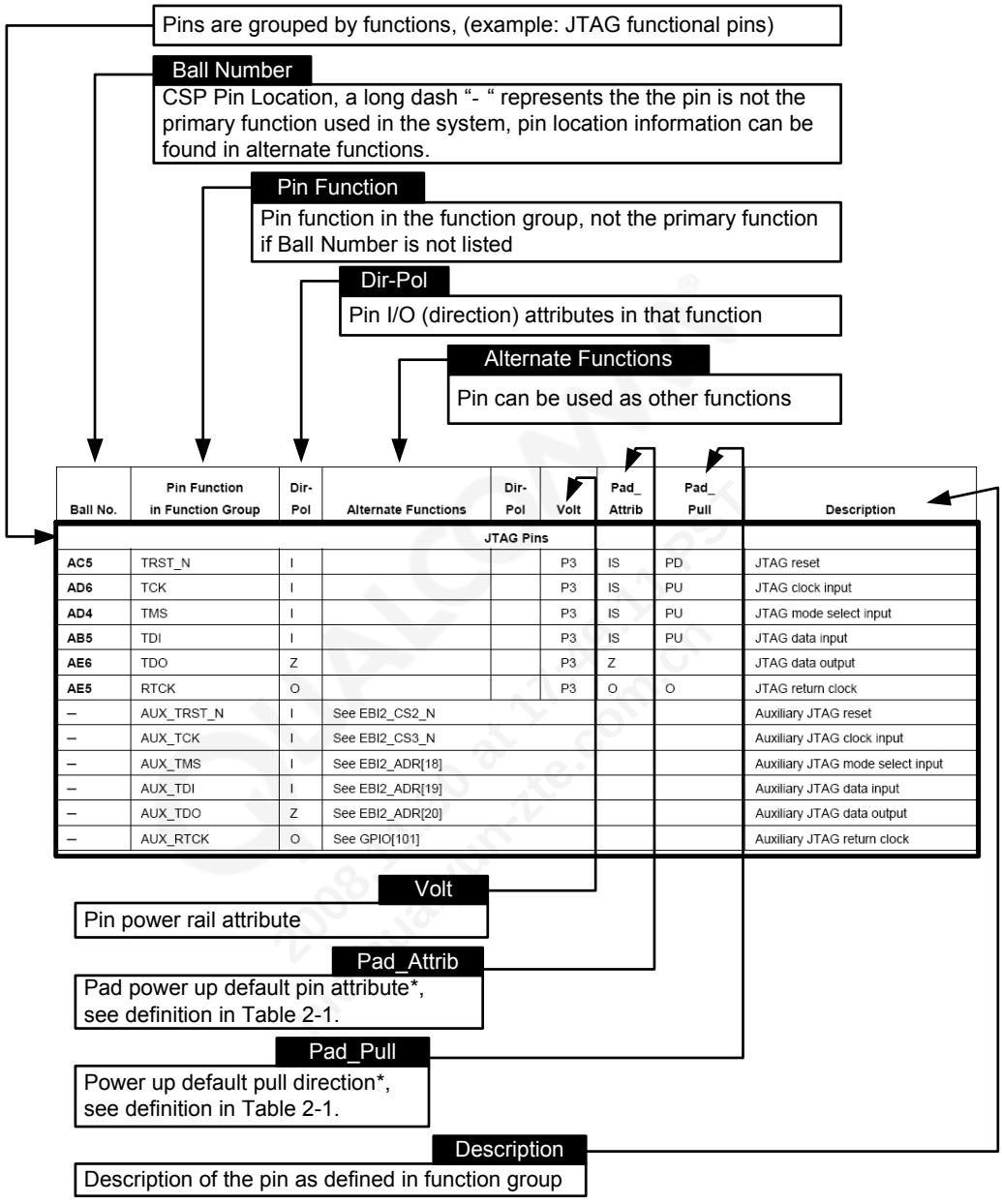
Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad type	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional with CMOS input
BS	Bidirectional with Schmitt trigger
H	High-voltage tolerant; allows digital input voltages up to 3.0 V.
I	CMOS input
O	CMOS output
S	Schmitt trigger input
W	Input pad provides wake-up interrupt during deep-sleep mode.
Z	High-Z output
Pad pull/keep details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP:pdpukp = default no-pull with programmable options following the colon (:) PD:nppukp = default pull-down with programmable options following the colon (:) KP:nppdpu = default keeper with programmable options following the colon (:) PU:nppdkp = default pull-up with programmable options following the colon (:)
K	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
Pad voltage groupings	
P1	Tied to pad group 1 that uses supply voltage V_{DD_P1} (1.8 V)
P2	Tied to pad group 2 that uses supply voltage V_{DD_P2} (1.8 V or 2.6 V)
P3	Tied to pad group 3 that uses supply voltage V_{DD_P3} (2.6 V)
P4	Tied to pad group 4 that uses supply voltage V_{DD_P4} (1.8 V or 2.6 V)
P7	Tied to pad group 7 that uses supply voltage V_{DD_P7} (2.6 V)
P8	Tied to pad group 8 that uses supply voltage V_{DD_P8} (1.8 V or 2.6 V)
P9	Tied to pad group 9 that uses supply voltage V_{DD_P9} (1.8 V or 2.6 V)
P10	Tied to pad group 10 that uses supply voltage V_{DD_P10} (1.8 V or 3.0 V)
USBPHY	Pad group that uses supply voltage V_{DD_USBPHY} (2.6 V and 3.3 V)
Output current drive strength	
EBI1 pads	Pads for EBI1 are tailored for the 1.8-V interface and are source terminated. At the pads, after the source termination, the drive strength at I_{OL}, I_{OH} is equivalent to a range of 1.45 to 2.5 mA in non-linear steps when the JEDEC standard range (90% / 10%) is followed.
3.0 V (H) pads	Programmable drive strength, 2 to 8 mA in 2 mA steps
Others[1]	Programmable drive strength, 2 to 16 mA in 2 mA steps

1. Digital pads other than EBI1 pads or high-voltage tolerant pads.



Ball No.	Pin Function in Function Group	Dir-Pol	Alternate Functions	Dir-Pol	Volt	Pad_ Attrib	Pad_ Pull	Description
JTAG Pins								
AC5	TRST_N	I			P3	IS	PD	JTAG reset
AD6	TCK	I			P3	IS	PU	JTAG clock input
AD4	TMS	I			P3	IS	PU	JTAG mode select input
AB5	TDI	I			P3	IS	PU	JTAG data input
AE6	TDO	Z			P3	Z		JTAG data output
AE5	RTCK	O			P3	O	O	JTAG return clock
–	AUX_TRST_N	I	See EBI2_CS2_N					Auxiliary JTAG reset
–	AUX_TCK	I	See EBI2_CS3_N					Auxiliary JTAG clock input
–	AUX_TMS	I	See EBI2_ADR[18]					Auxiliary JTAG mode select input
–	AUX_TDI	I	See EBI2_ADR[19]					Auxiliary JTAG data input
–	AUX_TDO	Z	See EBI2_ADR[20]					Auxiliary JTAG data output
–	AUX_RTCK	O	See GPIO[101]					Auxiliary JTAG return clock

* Must meet proper power up/down sequence requirements

Figure 2-1 Pin table definition

Table 2-2 Functional pin descriptions for the MSM7625 device

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
Clocks								
T2	TCXO	I			P3	AI	-	TCXO clock input
Y5	SLEEP_CLK	I			P3	IS	-	Low-power sleep controller crystal oscillator input. Digital sleep clock
Modes and resets								
AA18	RESIN_N	I			P3	IS		Hardware reset input to system
V16	RESOUT_N	O			P3	O		Reset output generated by synchronized RESIN_N and by WDOG_RESET. The rising edge of RESOUT_N is delayed from the rising edge of RESIN_N by a few microprocessor clocks.
AC25	EBI1_RESOUT_N	O			P1	O		Duplicated RESOUT_N, same voltage level as the first external memory interface. Connected to pad_group1.
W2	WDOG_EN	I			P3	IS	PU	Watchdog timer enable input
V10	MODE3	I			P3	IS	PD: nppukp	Determines operating mode of the chip. PJtag = primary JTAG port AJtag = auxiliary JTAG port "+" indicates daisy chaining MODE[3: 0]: 0000 Native, ARM9 on PJtag; ARM11 on AJtag 0001 Native, ARM9 + ARM11 on PJtag 0010--1111 Reserved
AD8	MODE2	I			P3	IS	PD: nppukp	
AB8	MODE1	I			P3	IS	PD: nppukp	
AB9	MODE0	I			P3	IS	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
	BOOT_SCUR	I	See GPIO[95].	B	P4	B	PD: nppukp	Determines boot mode of the chip: 0: Boot in non-secure mode 1: Boot in secure mode (boot code is authenticated) This pin is only meaningful if the security enable fuse is not blown. Once blown, the pin can be used as GPIO[95].
JTAG pins								
Y2	TRST_N	I			P3	IS	PD	JTAG reset
AA2	TCK	I			P3	IS	PU	JTAG clock input
Y1	TMS	I			P3	IS	PU	JTAG mode select input
W1	TDI	I			P3	IS	PU	JTAG data input
AA1	TDO	Z			P3	Z		JTAG data output
AA4	RTCK	O			P3	O	O	JTAG return clock
	AUX_TRST_N	I	See EBI2_CS2_N.					Auxiliary JTAG reset
	AUX_TCK	I	See EBI2_CS3_N.					Auxiliary JTAG clock input
	AUX_TMS	I	See EBI2_ADR[17].					Auxiliary JTAG mode select input
	AUX_TDI	I	See EBI2_ADR[18].					Auxiliary JTAG data input
	AUX_TDO	Z	See EBI2_ADV_N.					Auxiliary JTAG data output
	AUX_RTCK	O	See GPIO[101].					Auxiliary JTAG return clock
Modem power manager (MPM)								
V9	MPM_GPIO[2]	B	SSBI_PMIC GPIO[106]	B B	P3	B	PD: nppukp	
R10	MPM_GPIO[1]	B	TCXO_EN GPIO[105]	O B	P3	B	PU: nppdkp	
W9	MPM_GPIO[0]	B	PA_RANGE1 GP_PDM[0] GPIO[104]	O Z B	P3	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
PLL test raw clock source								
T4	PLL_TEST_SE	B			P3	B	PD: nppukp	This can be used as an alternative raw clock source for internal clock generation.
External bus interface 1								
V19	EBI1_ADR[14]	O			P1	O		EBI1 address bus
V21	EBI1_ADR[13]	O			P1	O		
AB25	EBI1_ADR[12]	O			P1	O		
U22	EBI1_ADR[11]	O			P1	O		
AA25	EBI1_ADR[10]	O			P1	O		
AA24	EBI1_ADR[9]	O			P1	O		
Y22	EBI1_ADR[8]	O			P1	O		
Y24	EBI1_ADR[7]	O			P1	O		
W25	EBI1_ADR[6]	O			P1	O		
W22	EBI1_ADR[5]	O			P1	O		
R16	EBI1_ADR[4]	O			P1	O		
W21	EBI1_ADR[3]	O			P1	O		
V22	EBI1_ADR[2]	O			P1	O		
Y25	EBI1_ADR[1]	O			P1	O		
U19	EBI1_ADR[0]	O			P1	O		
H25	EBI1_DQ[31]	B			P1	BS	NP: pdpukp	EBI1 data bus
J19	EBI1_DQ[30]	B			P1	BS	NP: pdpukp	
H19	EBI1_DQ[29]	B			P1	BS	NP: pdpukp	
H22	EBI1_DQ[28]	B			P1	BS	NP: pdpukp	
H21	EBI1_DQ[27]	B			P1	BS	NP: pdpukp	
J18	EBI1_DQ[26]	B			P1	BS	NP: pdpukp	
J25	EBI1_DQ[25]	B			P1	BS	NP: pdpukp	
K21	EBI1_DQ[24]	B			P1	BS	NP: pdpukp	
K18	EBI1_DQ[23]	B			P1	BS	NP: pdpukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
K22	EBI1_DQ[22]	B			P1	BS	NP: pdpukp	
K19	EBI1_DQ[21]	B			P1	BS	NP: pdpukp	
L18	EBI1_DQ[20]	B			P1	BS	NP: pdpukp	
K25	EBI1_DQ[19]	B			P1	BS	NP: pdpukp	
L25	EBI1_DQ[18]	B			P1	BS	NP: pdpukp	
L21	EBI1_DQ[17]	B			P1	BS	NP: pdpukp	
L22	EBI1_DQ[16]	B			P1	BS	NP: pdpukp	
M25	EBI1_DQ[15]	B			P1	BS	NP: pdpukp	
M19	EBI1_DQ[14]	B			P1	BS	NP: pdpukp	
N22	EBI1_DQ[13]	B			P1	BS	NP: pdpukp	
N25	EBI1_DQ[12]	B			P1	BS	NP: pdpukp	
P25	EBI1_DQ[11]	B			P1	BS	NP: pdpukp	
N18	EBI1_DQ[10]	B			P1	BS	NP: pdpukp	
P24	EBI1_DQ[9]	B			P1	BS	NP: pdpukp	
R25	EBI1_DQ[8]	B			P1	BS	NP: pdpukp	
P21	EBI1_DQ[7]	B			P1	BS	NP: pdpukp	
P22	EBI1_DQ[6]	B			P1	BS	NP: pdpukp	
P19	EBI1_DQ[5]	B			P1	BS	NP: pdpukp	
R22	EBI1_DQ[4]	B			P1	BS	NP: pdpukp	
R21	EBI1_DQ[3]	B			P1	BS	NP: pdpukp	
T24	EBI1_DQ[2]	B			P1	BS	NP: pdpukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
T22	EBI1_DQ[1]	B			P1	BS	NP: pdpukp	
T21	EBI1_DQ[0]	B			P1	BS	NP: pdpukp	
J22	EBI1_DQS[3]	B			P1	BS	NP: pdpukp	Data strobe
K24	EBI1_DQS[2]	B			P1	BS	NP: pdpukp	
N19	EBI1_DQS[1]	B			P1	BS	NP: pdpukp	
T25	EBI1_DQS[0]	B			P1	BS	NP: pdpukp	
H24	EBI1_DM[3]	O			P1	O		Data mask
L19	EBI1_DM[2]	O			P1	O		
M24	EBI1_DM[1]	O			P1	O		
U25	EBI1_DM[0]	O			P1	O		
V25	EBI1_DCLK	O			P1	B		Differential clock for DDR SDRAM
V24	EBI1_DCLKB	O			P1	B		
T18	EBI_CS1_N	O			P1	O		Chip select for DDR SDRAM
T19	EBI_CS0_N	O			P1	O		
P18	EBI1_CKE1	O			P1	O		DDR clock enable
R18	EBI1_CKE0	O			P1	O		
R19	EBI1_RAS_N	O			P1	O		DDR RAS_N
AA22	EBI1_WE_N	O			P1	O		Write enable
M18	EBI1_CAS_N	O			P1	O		
U18	EBI1_BA[1]	O			P1	O		Bank selection
AB24	EBI1_BA[0]	O			P1	O		Bank selection
External bus interface 2								
	Ball no. - H13	O	GPIO[129]	B	P9	B	PD: nppukp	
	Ball no. - G13	O	GPIO[128]	B	P9	B	PD: nppukp	
	Ball no. - G12	O	GPIO[127]	B	P9	B	PD: nppukp	
	Ball no. - E15	O	GPIO[126]	B	P9	B	PD: nppukp	
	Ball no. - B14	O	GPIO[125]	B	P9	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
A16	EBI2_ADR[18]	O	GPIO[99] AUX_TDI LCDC_RED[6]	B I O	P9	B	NP: pdpukp	
B16	EBI2_ADR[17]	O	GPIO[98] AUX_TMS LCDC_RED[5]	B I O	P9	B	NP: pdpukp	
H15	EBI2_ADR[16]	O	LCDC_RED[4]	O	P9	B		
D16	EBI2_ADR[15]	O	LCDC_RED[3]	O	P9	B		
H14	EBI2_ADR[14]	O	LCDC_RED[2]	O	P9	B		
E16	EBI2_ADR[13]	O	LCDC_RED[1]	O	P9	B		
A15	EBI2_ADR[12]	O	LCDC_RED[0]	O	P9	B		
B15	EBI2_ADR[11]	O	LCDC_GREEN[7]	O	P9	B		
G14	EBI2_ADR[10]	O	LCDC_GREEN[6]	O	P9	B		
A17	EBI2_ADR[9]	O			P2	B		
D18	EBI2_ADR[8]	O			P2	B		
E20	EBI2_ADR[7]	O			P2	B		
A19	EBI2_ADR[6]	O			P2	B		
E19	EBI2_ADR[5]	O	LCD_DATA[23]	O	P2	B		Enabled through EBI2 control registers
G16	EBI2_ADR[4]	O	LCD_DATA[22]	O	P2	B		
D19	EBI2_ADR[3]	O	LCD_DATA[21]	O	P2	B		
B19	EBI2_ADR[2]	O	LCD_DATA[20]	O	P2	B		
B17	EBI2_ADR[1]	O	LCD_DATA[19]	O	P2	B		
E17	EBI2_ADR[0]	O	LCD_DATA[18]	O	P2	B		
A20	EBI2_DATA[15]	B	NAND_IO[15] ONENAND_ADQ[15]		P2	B	NP: pdpukp	EBI2 data bus
A21	EBI2_DATA[14]	B	NAND_IO[14] ONENAND_ADQ[14]		P2	B	NP: pdpukp	
B20	EBI2_DATA[13]	B	NAND_IO[13] ONENAND_ADQ[13]		P2	B	NP: pdpukp	
D20	EBI2_DATA[12]	B	NAND_IO[12] ONENAND_ADQ[12]		P2	B	NP: pdpukp	
B21	EBI2_DATA[11]	B	NAND_IO[11] ONENAND_ADQ[11]		P2	B	NP: pdpukp	
B23	EBI2_DATA[10]	B	NAND_IO[10] ONENAND_ADQ[10]		P2	B	NP: pdpukp	
E25	EBI2_DATA[9]	B	NAND_IO[9] ONENAND_ADQ[9]		P2	B	NP: pdpukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
A23	EBI2_DATA[8]	B	NAND_IO[8] ONENAND_ADQ[8]		P2	B	NP: pdpukp	
E24	EBI2_DATA[7]	B	NAND_IO[7] ONENAND_ADQ[7]		P2	B	NP: pdpukp	
C25	EBI2_DATA[6]	B	NAND_IO[6] ONENAND_ADQ[6]		P2	B	NP: pdpukp	
D25	EBI2_DATA[5]	B	NAND_IO[5] ONENAND_ADQ[5]		P2	B	NP: pdpukp	
B22	EBI2_DATA[4]	B	NAND_IO[4] ONENAND_ADQ[4]		P2	B	NP: pdpukp	
A22	EBI2_DATA[3]	B	NAND_IO[3] ONENAND_ADQ[3		P2	B	NP: pdpukp	
B24	EBI2_DATA[2]	B	NAND_IO[2] ONENAND_ADQ[2]		P2	B	NP: pdpukp	
C24	EBI2_DATA[1]	B	NAND_IO[1] ONENAND_ADQ[1]		P2	B	NP: pdpukp	
D22	EBI2_DATA[0]	B	NAND_IO[0] ONENAND_ADQ[0]		P2	B	NP: pdpukp	
K15	EBI2_LB_N	O	NAND_ALE LCD_DATA[16] ONENAND_ADV_N	O O	P2	O		Low-byte enable (byte access of 16-bit memory)
B18	EBI2_UB_N	O	NAND_CLE LCD_DATA[17]	O O	P2	O		Upper-byte enable (byte access of 16-bit memory)
G18	EBI2_WE_N	O	NAND_WE_N ONENAND_WE_N		P2	O		Write enable
A18	EBI2_OE_N	O	NAND_OE_N ONENAND_OE_N		P2	O		Output enable
G15	EBI2_ADV_N	O	GPIO[100] AUX_TDO LCDC_RED[7]	B Z O	P9	B	PU: nppdkp	
F22	EBI2_CS7_N	O			P2	O	NP: pdpukp	Chip select for general-purpose asynch memory device
H17	EBI2_CS6_N	O			P2	O	NP: pdpukp	
H16	EBI2_CS5_N	O	LCD_EN LCD_CS1_N	O O	P2	O	NP: pdpukp	Chip select for general-purpose asynch memory device Chip select for second LCD
G22	EBI2_CS4_N	O	LCD_CS0_N	O	P2	O	NP: pdpukp	Chip select for first LCD

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
F25	EBI2_CS3_N	O	GPIO[103] AUX_TCK	B I	P2	B	NP: pdpukp	Chip select for general-purpose asynch memory device
L16	EBI2_CS2_N	O	GPIO[102] AUX_TRST_N	B I	P2	B	NP: pdpukp	Chip select for general-purpose asynch memory device
E21	EBI2_CS1_N	O	NAND_CS1_N ONENAND_CS1_N	O	P2	B	NP: pdpukp	Chip select for second NAND
E22	EBI2_CS0_N	O	NAND_CS0_N ONENAND_CS0_N	O	P2	B	NP: pdpukp	Chip select for first NAND
F24	EBI2_BUSY0_N	I	NAND_RY/BY_N ONENAND_INT		P2	I	PU: nppdkp	Busy signal NAND device
G25	EBI2_CLK	O	ONENAND_CLK		P2	B		EBI2 clock
MDDI primary (LCD) interface pins								
AE13	MDDI_P_STB_N	O			1.8	AO		LCD differential strobe pair
AE12	MDDI_P_STB_P	O			1.8	AO		
AE11	MDDI_P_DATA_N	B			1.8	AIO		LCD differential data pair
AE10	MDDI_P_DATA_P	B			1.8	AIO		
LCDC interface								
A10	LCDC_PCLK	O			P8	IS	PD: nppukp	
General-purpose I/O and interrupt pins								
K13	GPIO[132]	B			P9	B	NP: pdpukp	
B10	GPIO[131]	B			P8	B	NP: pdpukp	
H12	GPIO[130]	B	LCDC_GREEN[5]	O	P9	B	NP: pdpukp	
H13	GPIO[129]	B	LCDC_DEN EBI2_ADR[23]	O B	P9	B	PD: nppukp	
G13	GPIO[128]	B	LCDC_HSYNC EBI2_ADR[22]	O B	P9	B	PD: nppukp	
G12	GPIO[127]	B	LCDC_VSYNC EBI2_ADR[21]	O B	P9	B	PD: nppukp	
E15	GPIO[126]	B	LCDC_BLUE[0] EBI2_ADR[20] AUX_TDO	O B O	P9	B	PD: nppukp	
B14	GPIO[125]	B	LCDC_BLUE[1] EBI2_ADR[19]	O B	P9	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
AA19	GPIO[124]	B-W			P3	B-W	NP: pdpukp	
AE18	GPIO[123]	B			P3	B	NP: pdpukp	
AD18	GPIO[122]	B			P3	B	NP: pdpukp	
D11	GPIO[121]	B	LCDC_GREEN[2]	O	P8	B	PU: nppukp	
E10	GPIO[120]	B	LCDC_GREEN[3]	O	P8	B	PD: nppukp	
E11	GPIO[119]	B	LCDC_GREEN[4]	O	P8	B	PD: nppukp	
D10	GPIO[118]	B	LCDC_BLUE[2]	O	P8	B	PD: nppukp	
H11	GPIO[117]	B	LCDC_BLUE[3]	O	P8	B	PD: nppukp	
G11	GPIO[116]	B	LCDC_BLUE[4]	O	P8	B	PD: nppukp	
H10	GPIO[115]	B	LCDC_BLUE[5]	O	P8	B	PD: nppukp	
G10	GPIO[114]	B-W	LCDC_BLUE[6]	O	P8	B	PD: nppukp	
A11	GPIO[113]	B	LCDC_BLUE[7]	O	P8	B	PD: nppukp	
B11	GPIO[112]	B-W	UART3_RX LCDC_GREEN[0]	I O	P8	B	PD: nppukp	
E9	GPIO[111]	B	UART3_TX LCDC_GREEN[1]	O O	P8	B	PD: nppukp	
AE4	GPIO[110]	B	PA_ON2	O	P3	B	PD: nppukp	
AE15	GPIO[109]	B	SDC4_CLK	O	P3	B	PD: nppukp	
AE7	GPIO[108]	B	SDC4_DATA[0] UART2DM_TX SDC3_DATA[4]	B O B	P3	B-H	PD: nppukp	
AD15	GPIO[107]	B	SDC4_CMD	B	P3	B-H	PD: nppukp	
	GPIO[106]	B-W	MPM_GPIO[2] SSBI_PMIC	B B	P3	See MPM_GPIO[2].		
	GPIO[105]	B-W	MPM_GPIO[1] TCXO_EN	B O	P3	See MPM_GPIO[1].		

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
	GPIO[104]	B-W	MPM_GPIO[0] PA_RANGE1 GP_PDM[0]	B O B	P3	See MPM_GPIO[0].		
	GPIO[103]	B	EBI2_CS3_N AUX_TCK	O	P2	See EBI2_CS3_N.		
	GPIO[102]	B	EBI2_CS2_N AUX_TRST_N	O	P2	See EBI2_CS2_N.		
G17	GPIO[101]	B	MDP_VSYNC_P_B AUX_RTCK	B O	P2	B	PU: nppdkp	
	GPIO[100]	B	EBI2_ADV_N AUX_TDO LCDC_RED[7]	O Z O	P9	See EBI2_ADV_N.		
	GPIO[99]	B	EBI2_ADR[18] AUX_TDI LCDC_RED[6]	O I O	P9	See EBI2_ADR[18].		
	GPIO[98]	B	EBI2_ADR[17] AUX_TMS LCDC_RED[5]	O I O	P9	See EBI2_ADR[17].		
W10	GPIO[97]	B	MDP_ VSYNC_P	B	P3	B	PD: nppukp	
V17	GPIO[96]	B	AUX_I2C_SDA	B	P4	B	PD: nppukp	
W18	GPIO[95]	B	BOOT_SCUR AUX_I2C_SCL	I B	P4	B	PD: nppukp	
P10	GPIO[94]	B-W		I	P3	B-W	PD: nppukp	
AD5	GPIO[93]	B	SDC3_DATA[0]	B	P3	B-H	PD: nppukp	
AB6	GPIO[92]	B-W	SDC3_DATA[1]	B	P3	B-HW	PD: nppukp	
AE5	GPIO[91]	B	SDC3_DATA[2]	B	P3	B-H	PD: nppukp	
AB7	GPIO[90]	B	SDC3_DATA[3]	B	P3	B-H	PD: nppukp	
AE6	GPIO[89]	B	SDC3_CMD	B	P3	B-H	PD: nppukp	
AD7	GPIO[88]	B	SDC3_CLK	O	P3	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
L8	GPIO[87]	B	UART3_TX UIM2_DATA USB3_OE_INT_N USB3_OE_INT TSIF_SYNC JOYSTICK_W	O B O O I O	P10	B	PD: nppukp	USB3 is used for USB-UICC only.
L7	GPIO[86]	B-W	UART3_RX UIM2_PWR_EN TSIF_DATA JOYSTICK_E	I O I O	P10	B-W	PD: nppukp	
L5	GPIO[85]	B	UART3_CTS_N UIM2_RESET TSIF_EN JOYSTICK_S USB3_SE0_VM	I O I O B	P10	B	PD: nppukp	USB3 is used for USB-UICC only.
L4	GPIO[84]	B	UART3_RFR_N UIM2_CLK TSIF_CLK JOYSTICK_N USB3_DAT_VP	O O I O B	P10	B	PD: nppukp	USB3 is used for USB-UICC only.
W17	GPIO[83]	B-W	JOYSTICK_C PA_ON1	I O	P3	B-W	PD: nppukp	
AB18	GPIO[82]	B	MDP_VSYNC_S ETM9_TRACECLKB	B O	P3	B	PD: nppukp	
AE17	GPIO[81]	B	GRFC[0]	O	P3	B	PD: nppukp	
W16	GPIO[80]	B	GRFC[1] ASYNC_TIMER1B ASYNC_TIMER2B	O O O	P3	B	PD: nppukp	
T15	GPIO[79]	B	GRFC[2]	O	P3	B	PD: nppukp	
AB17	GPIO[78]	B	GRFC[3]	O	P3	B	PD: nppukp	
AE16	GPIO[77]	B	GRFC[4] ASYNC_TIMER1A ASYNC_TIMER2A	O O O	P3	B	PU: nppdkp	
V15	GPIO[76]	B	GRFC[5] SYNC_TIMER1 SYNC_TIMER2	O O O	P3	B	PU: nppdkp	
AD16	GPIO[75]	B	GRFC[6]	O	P3	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
AB16	GPIO[74]	B	GRFC[7]	O	P3	B	PD: nppukp	
W15	GPIO[73]	B	GRFC[8]	O	P3	B	PD: nppukp	
AA16	GPIO[72]	B	GRFC[9]	O	P3	B	PD: nppukp	
V4	GPIO[71]	B-W	AUX_PCM_CLK SDAC_CLK GRFC[11] PA_ON2	B O O O	P3	B-W	PD: nppukp	
V2	GPIO[70]	B-W	AUX_PCM_SYNC SDAC_L_R_N GRFC[12] SYNC_TIMER1	B O O O	P3	B-W	PD: nppukp	
U4	GPIO[69]	B	AUX_PCM_DIN SDAC_MCLK TSIF_NULL GRFC[13]	B O I O	P3	B	PD: nppukp	
U5	GPIO[68]	B	AUX_PCM_DOUT SDAC_DOUT TSIF_ERROR GRFC[14]	B O I O	P3	B	PD: nppukp	
AA8	GPIO[67]	B	SDC2_DATA[0]	B	P3	B-H	PD: nppukp	
U8	GPIO[66]	B-W	SDC2_DATA[1]	B	P3	B-HW	PD: nppukp	
U7	GPIO[65]	B	SDC2_DATA[2]	B	P3	B-H	PD: nppukp	
W8	GPIO[64]	B	SDC2_DATA[3]	B	P3	B-H	PD: nppukp	
V7	GPIO[63]	B	SDC2_CMD	B	P3	B-H	PD: nppukp	
AA7	GPIO[62]	B	SDC2_CLK	O	P3	B	PD: nppukp	
U2	GPIO[61]	B	I2C_SDA	B	P3	B	PU: nppdkp	
U1	GPIO[60]	B	I2C_SCL	B	P3	B	PU: nppdkp	
T1	GPIO[59]	B	SSBI_RTR	B	P3	B	PD: nppukp	
T7	GPIO[58]	B	EXT_GPS_LNA_EN	B	P3	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
T8	GPIO[57]	B	SSBI_TX	B	P3	B	PD: nppukp	
AE3	GPIO[56]	B	SDC1_CLK	O	P3	B	PD: nppukp	
AD4	GPIO[55]	B	SDC1_CMD	B	P3	B-H	PD: nppukp	
AA6	GPIO[54]	B	SDC1_DATA[0]	B	P3	B-H	PD: nppukp	
AD3	GPIO[53]	B-W	SDC1_DATA[1]	B	P3	B-HW	PD: nppukp	
AD2	GPIO[52]	B	SDC1_DATA[2]	B	P3	B-H	PD: nppukp	
AC2	GPIO[51]	B	SDC1_DATA[3]	B	P3	B-H	PD: nppukp	
K1	GPIO[50]	B	UART2_TX UIM1_DATA	O B	P10	B	PD: nppukp	
K7	GPIO[49]	B-W	UART2_RX UIM1_PWR_EN	I O	P10	B-W	PD: nppukp	
K2	GPIO[48]	B	UART2_CTS_N UIM1_RESET	I O	P10	B	PD: nppukp	
K8	GPIO[47]	B	UART2_RFR_N UIM1_CLK	O O	P10	B	PD: nppukp	
AC1	GPIO[46]	B	UART1_TX UART1DM_TX TSIF_SYNC	O O I	P3	B	PD: nppukp	
AB5	GPIO[45]	B-W	UART1_RX UART1DM_RX TSIF_DATA	I I I	P3	B-W	PD: nppukp	
AB2	GPIO[44]	B	UART1_CTS_N UART1DM_CTS_N TSIF_EN	I I I	P3	B	PD: nppukp	
AB1	GPIO[43]	B	UART1_RFR_N UART1DM_RFR_N TSIF_CLK	O O I	P3	B	PU: nppdkp	
T14	GPIO[42]	B-W	KEYPAD[0] ETM9_TRACEDATA0	B O	P3	B-W	PU: nppdkp	
V14	GPIO[41]	B-W	KEYPAD[1] ETM_TRACEDATA[1]	B O	P3	B-W	PU: nppdkp	
AB15	GPIO[40]	B-W	KEYPAD[2] ETM_TRACEDATA[2]	B O	P3	B-W	PU: nppdkp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
AA15	GPIO[39]	B-W	KEYPAD[3] ETM_TRACEDATA[3]	B O	P3	B-W	PU: nppdkp	
AE14	GPIO[38]	B-W	KEYPAD[4] ETM_TRACEDATA[4]	B O	P3	B-W	PU: nppdkp	
W14	GPIO[37]	B-W	KEYPAD[5] ETM_TRACEDATA[5]	B O	P3	B-W	PU: nppdkp	
AB14	GPIO[36]	B-W	KEYPAD[6] ETM_TRACEDATA[6]	B O	P3	B-W	PU: nppdkp	
AA14	GPIO[35]	B	KEYPAD[7] ETM_TRACEDATA[7]	B O	P3	B	PD: nppukp	
V13	GPIO[34]	B	KEYPAD[8] ETM_TRACEDATA[8]	B O	P3	B	PD: nppukp	
AD13	GPIO[33]	B	KEYPAD[9] ETM_TRACEDATA[9]	B O	P3	B	PD: nppukp	
AB13	GPIO[32]	B	KEYPAD[10] ETM_TRACEDATA[10]	B O	P3	B	PD: nppukp	
W13	GPIO[31]	B	KEYPAD[11] ETM9_TRACESYNC	B O	P3	B	PD: nppukp	
AB12	GPIO[30]	B	ETM_TRACECLK SYNC_TIMER1	O O	P3	B	PU: nppdkp	
T12	GPIO[29]	B-W	SYNC_TIMER2 ETM9_PIPESTAT[0] ETM11_TRACEDATA0	O O O	P3	B-W	PD: nppukp	
W12	GPIO[28]	B-W	ASYNC_TIMER2B GP_MN ETM_GPIO_IRQ	O B I	P3	B-W	PD: nppukp	
AA12	GPIO[27]	B-W	ASYNC_TIMER2A GP_CLK ETM9_PIPESTAT1 ETM11_TRACECTL	O O O O	P3	B-W	PD: nppukp	
V12	GPIO[26]	B	ETM9_PIPESTAT2	O	P3	B	PD: nppukp	
V11	GPIO[25] PS_HOLD	B O	ETM_TRACEDATA[11]	O	P3	B	PD: nppukp	This GPIO pin is reserved for PS_HOLD function and should not be used for other GPIO functions.
AA11	GPIO[24]	B-W	PM_INT_N ETM_GPIO2_CS_N	I O	P3	B-W	PD: nppukp	
W11	GPIO[23]	B	ETM_TRACEDATA[12]	O	P3	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
AB11	GPIO[22]	B	PA_ON1 ETM_TRACEDATA[13]	O O	P3	B	PD: nppukp	
AB10	GPIO[21]	B-W	UART1_DCD UART2DM_RX SDC4_DATA[1] SDC3_DATA[5] ETM_KEYSENSE_IRQ	I I B B I	P3	B-HW	PD: nppukp	
AE9	GPIO[20]	B-W	UART1_DTR UART2DM_CTS_N SDC4_DATA[2] SDC3_DATA[6] ETM_TRACEDATA[14]	I I B B O	P3	B-HW	PD: nppukp	
AA10	GPIO[19]	B-W	UART1_RI UART2DM_RFR_N SDC4_DATA[3] SDC3_DATA[7] ETM_TRACEDATA[15]	O O B B O	P3	B-HW	PD: nppukp	
AD9	GPIO[18]	B-W	ASYNC_TIMER1B ETM9_PIPESTATB2	O O	P3	B-W	PU: nppdkp	
T11	GPIO[17]	B-W	ASYNC_TIMER1A ETM9_PIPESTATB1	O O	P3	B-W	PD: nppukp	
AE8	GPIO[16]	B	WDOG_STB MDP_VSYNC_E ETM9_PIPESTATB0	O B O	P3	B	PU: nppdkp	
AB19	GPIO[15]	B	CAM_MCLK	O	P4	B	PD: nppukp	
AE19	GPIO[14]	B	CAM_VSYNC	I	P4	B	PD: nppukp	
AA20	GPIO[13]	B	CAM_HSYNC	I	P4	B	PD: nppukp	
AD19	GPIO[12]	B	CAM_PCLK	I	P4	B	PD: nppukp	
AE20	GPIO[11]	B	CAM_DATA[11]	I	P4	B	PD: nppukp	
AE21	GPIO[10]	B	CAM_DATA[10]	I	P4	B	PD: nppukp	
AB22	GPIO[9]	B	CAM_DATA[9]	I	P4	B	PD: nppukp	
AD22	GPIO[8]	B	CAM_DATA[8]	I	P4	B	PD: nppukp	
AB20	GPIO[7]	B	CAM_DATA[7]	I	P4	B	PD: nppukp	

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
AE22	GPIO[6]	B	CAM_DATA[6]	I	P4	B	PD: nppukp	
AD20	GPIO[5]	B	CAM_DATA[5]	I	P4	B	PD: nppukp	
AA21	GPIO[4]	B	CAM_DATA[4]	I	P4	B	PD: nppukp	
AB21	GPIO[3]	B	CAM_DATA[3]	I	P4	B	PD: nppukp	
AD23	GPIO[2]	B	CAM_DATA[2]	I	P4	B	PD: nppukp	
AD24	GPIO[1]	B	CAM_DATA[1]	I	P4	B	PD: nppukp	
AE23	GPIO[0]	B	CAM_DATA[0]	I	P4	B	PD: nppukp	
High-speed USB PHY interface								
A12	USBPHY_SYSCLOCK	I			USB PHY	AI		PHY interface REFEXT, SYSCLOCK and ID: Capable of 2.6 V operation only. VBUS: 5.25 V tolerant
D14	USBPHY_REFEXT	I			USB PHY	AIO		
B12	USBPHY_ID	I			USB PHY	AIO		
A14	USBPHY_DN	B			USB PHY	AIO		
A13	USBPHY_DP	B			USB PHY	AIO		
B13	USBPHY_VBUS	B			USB PHY	AIO		
TXDAC interface								
P2	I_OUT_P	O			A	AO	-	Non-inverted current mode output from the I transmit DAC.
P1	I_OUT_N	O			A	AO	-	Inverted current mode output from the I transmit DAC.
N2	Q_OUT_P	O			A	AO	-	Non-inverted current mode output from the Q transmit DAC.
N1	Q_OUT_N	O			A	AO	-	Inverted current mode output from the Q transmit DAC.
P5	DAC_IREF	I				AI	-	Input reference to set the gain of the I&Q transmit DACs.

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
RF Tx interface								
	PA_ON2	O	See GPIO[110]/GPIO[71]					Control signal that controls the power amplifier. PA_ON is high only when the RF power amplifier is needed for transmission. Supports up to two power amplifiers. PAs are powered off on hardware reset.
	PA_ON1	O	See GPIO[83]/GPIO[22]					
V5	PA_ON0	O			P3	O		
R7	TX_ON	O	GRFC[10]	O	P3	O		By using TX_ON, we can turn on/off Tx IF separately from PA_ON. (PA needs longer warmup time, so this feature could reduce the current consumption of Tx IF part.) Output goes low on hardware reset.
	PA_RANGE1	O	See MPM_GPIO[0].					These are digital outputs from the transmit AGC circuit that can be used to alter the subscriber transmit power amplifier characteristics. These pins are PA_RANGE by default; the web registers for pdm_to_pa_range must be set to use the alternate function.
V1	PA_RANGE0	O	GP_PDM1	B	P3	B	PD: nppukp	
	TCXO_EN	O	See MPM_GPIO[1].					Enables TCXO and related circuitry.
L1	TRK_LO_ADJ	O			P3	Z	PD: nppukp	PDM output from the frequency tracking circuit that sets the subscriber VHF and UHF frequencies.
L2	TX_AGC_ADJ	O			P3	Z	PD: nppukp	PDM output from the transmit AGC circuit to control the transmit output power.
PA control DAC interface								
M2	PA_POWER_CTL_M				A	AO		Output (-) from the PA power control DAC.

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
M1	PA_POWER_CTL				A	AO		Output from the PA power control DAC. Analog pin to control GSM PA. (single-ended input)
M5	GSM_BANDGAP_REF	I			A	AIO		Bandgap reference input
Analog RF Rx interface								
F2	I_IP_CH0	I			A	AI		Ch 0 differential analog I signal (+)
F1	I_IM_CH0	I			A	AI		Ch 0 differential analog I signal (-)
G2	Q_IP_CH0	I			A	AI		Ch 0 differential analog Q signal (+)
G1	Q_IM_CH0	I			A	AI		Ch 0 differential analog Q signal (-)
H2	I_IP_CH1	I			A	AI		Ch 1 differential analog I signal (+)
H1	I_IM_CH1	I			A	AI		Ch 1 differential analog I signal (-)
J2	Q_IP_CH1	I			A	AI		Ch 1 differential analog Q signal (+)
J1	Q_IM_CH1	I			A	AI		Ch 1 differential analog Q signal (-)
Internal codec signals								
A6	MIC1P	I			A	AI		Mic 1 input (+)
B6	MIC1N	I			A	AI		Mic 1 input (-)
D6	MIC2P	I			A	AI		Mic 2 input (+)
E6	MIC2N	I			A	AI		Mic 2 input (-)
D7	AUXIP	I			A	AI		Auxiliary input (+)
E7	AUXIN	I			A	AI		Auxiliary input (-)
A4	LINE_R_I_P	I			A	AI		Stereo function with three options (all right channel): 1) Line in 2) Microphone 3) Summing function to Rx
A5	LINE_R_I_N	I			A	AI		
B4	LINE_L_I_P	I			A	AI		Stereo function with three options (all left channel): 1) Line in 2) Microphone 3) Summing function to Rx
B5	LINE_L_I_N	I			A	AI		

Table 2-2 Functional pin descriptions for the MSM7625 device (cont.)

Ball no.	Pin function in function group	Dir-Pol	Alternate functions	Dir-Pol	Volt	Pad_ attrib	Pad_ pull	Description
A8	LINE_OP	O			A	AO		Line output (+ve) or stereo left channel line output.
B8	LINE_ON	O			A	AO		Line output (-ve) or stereo right channel line output.
A9	EAR1OP	O			A	AO		Earphone 1 amplifier output (+)
B9	EAR1ON	O			A	AO		Earphone 1 amplifier output (-)
G8	AUX_OUT	O			A	AO		Auxiliary output to carkit, PM7500™, or external speaker (single-ended)
E5	MICBIAS	O			A	AO		Microphone bias supply output, no decoupling capacitors.
E4	CCOMP	I			A	AI		External decoupling capacitor input for codec voltage reference.
G9	HPH_R	O			A	AO		Stereo headphone right output.
H9	HPH_L	O			A	AO		Stereo headphone left output.
G7	HPH_VREF	I			A	AI		Headphone common mode voltage.
General-purpose ADC signal								
B3	HKAIN[2]	I			A	AI		Analog MUX input channels to the on-chip housekeeping ADC.
F5	HKAIN[1]	I			A	AI		
F4	HKAIN[0]	I			A	AI		
Touchscreen								
D1	TS_LR	B			A	AIO		Touchscreen Y- (LR)
D2	TS_LL	B			A	AIO		Touchscreen X- (LL)
E1	TS_UR	B			A	AIO		Touchscreen Y+ (UR)
E2	TS_UL	B			A	AIO		Touchscreen X+ (UL)
C1	WIPER	I			A	AI		Touchscreen back panel input
Reserved								
R8	Reserved	I						Pin can be left floating

Table 2-3 MSM7625 power and ground pins

Ball no.	Pad name	Description
Digital power/GND		
A1, A2, A24, A25, B1, B25, G19, H18, J8, K11, K16, L10, M22, T10, T16, V8, V18, W19, AD1, AD25, AE1, AE2, AE24, AE25	VDD_C1	VDD for MSM digital core (except for ARM11 core)
G21	VDD_C1_SENSE	
W7, AA5, AB4	VDD_C2	VDD for ARM11 digital core
Y4	VDD_C2_SENSE	
J24, L24, N24, R24, U24, W24	VDD_P1	EBI1 (pad group 1) power
D21, D24, G24	VDD_P2	EBI2 (pad group 2) power
AD6, AD10, AD14, AD17, R4, W4	VDD_P3	Pad group 3 power
AC24, AD21	VDD_P4	Pad group 4 (camera) power
D12	VDD_P8	LCDC (pad group 8) power. If LCDC interface is used, this pad must be the same power rail as VDD_P9.
D17	VDD_P9	LCDC or EBI2 (pad group 9) power. If LCDC interface is used, this pad must be the same power rail as VDD_P8. If LCDC interface is not used, this pad must be the same power rail as VDD_P2 (EBI2).
M4	VDD_P10	Pad group 10 (USIM and USB-UICC)
D15	VDD_USBPHY (3.3 V)	USB PHY pad group (3.3 V)
E13	VDD_USBPHY (2.6 V)	USB PHY pad group (2.6 V)
M21, E12, E14, E18, F21, J21, K5, K12, K14, L11, L12, L13, L14, L15, M11, M12, M13, M14, M15, M16, N5, N10, N11, N12, N13, N14, N15, N16, N21, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, T13, U21, W5, Y21, AA9, AA13, AA17	GND	VSS for MSM digital core, EBI1, EBI2, pad group 3, pad group 4, pad group 8, pad group 9, pad group 10, USBPHY
D13	GND	USBPHY ground
AD11	VDD_MDDI	MDDI power and ground
AD12	GND	
M10	VDD_QFUSE_PROG	Qfuse program power
Analog power/GND		
B2	VDD_A	Touchscreen power and ground
C2	GND	
N8, P7, R1	VDD_A	Analog power and ground for PLL
N7, P8, R2, R5, T5	GND	

Table 2-3 MSM7625 power and ground pins (cont.)

Ball no.	Pad name	Description
H4, H5, J4, J5	VDD_A	Baseband sigma-delta modulator power and ground
G4, H7, H8, J7	GND	
D5	VDD_A	Codec power and ground
A3	GND	
D4	GND_RET	
D9, K4	VDD_P7	Pad group 7 (internal reference)
P4	VDD_A	Tx DAC
M7	VDD_A	PA control DAC
B7	VDD_A	Earphone
E8	VDD_A	Stereo DAC
A7, D8, G5, M8, N4	GND	Analog ground

Table 2-4 Pin descriptions by function

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
Keypad interface						
KEYPAD[11]	O	GPIO[31]	B	P3	PD: nppukp	Force/drive line
KEYPAD[10]	O	GPIO[32]	B	P3	PD: nppukp	Force/drive line
KEYPAD[9]	O	GPIO[33]	B	P3	PD: nppukp	Force/drive line
KEYPAD[8]	O	GPIO[34]	B	P3	PD: nppukp	Force/drive line
KEYPAD[7]	O	GPIO[35]	B	P3	PD: nppukp	Force/drive line
KEYPAD[6]	B	GPIO[36]	B	P3	PU: nppdkp	Optional force/drive or sense line
KEYPAD[5]	B	GPIO[37]	B	P3	PU: nppdkp	Optional force/drive or sense line
KEYPAD[4]	B	GPIO[38]	B	P3	PU: nppdkp	Sense line
KEYPAD[3]	B	GPIO[39]	B	P3	PU: nppdkp	Sense line
KEYPAD[2]	B	GPIO[40]	B	P3	PU: nppdkp	Sense line
KEYPAD[1]	B	GPIO[41]	B	P3	PU: nppdkp	Sense line
KEYPAD[0]	B	GPIO[42]	B	P3	PU: nppdkp	Sense line
UART1DM interface						
UART1DM_RFR_N	O	GPIO[43]	B	P3	PU: nppdkp	Ready to receive
UART1DM_CTS_N	I	GPIO[44]	B	P3	PD: nppukp	Clear to send
UART1DM_RX	I-W	GPIO[45]	B	P3	PD: nppukp	Receive serial data input
UART1DM_TX	O	GPIO[46]	B	P3	PD: nppukp	Transmit serial data output
UART2DM interface						
UART2DM_RFR_N	O	GPIO[19]	B	P3	PD: nppdkp	Ready to receive

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
UART2DM_CTS_N	I	GPIO[20]	B	P3	PD: nppukp	Clear to send
UART2DM_RX	I	GPIO[21]	B	P3	PD: nppukp	Receive serial data input
UART2DM_TX	O	GPIO[108]	B	P3	PD: nppukp	Transmit serial data output
UART1 interface						
UART1_RFR_N	O	GPIO[43]	B	P3	PU: nppdkp	Ready to receive
UART1_CTS_N	I	GPIO[44]	B	P3	PD: nppukp	Clear to send
UART1_RX	I	GPIO[45]	B	P3	PD: nppukp	Receive serial data input
UART1_TX	O	GPIO[46]	B	P3	PD: nppukp	Transmit serial data output
UART2/UIM interface						
UART2_RFR_N	O	GPIO[47] UIM1_CLK	B O	P10	PD: nppukp	Ready to receive
UART2_CTS_N	I	GPIO[48] # UIM1_RESET #	B O	P10	PD: nppukp	Clear to send
UART2_RX	I	GPIO[49] # UIM1_PWR_EN #	B O	P10	PD: nppukp	Receive serial data input
UART2_TX	O	GPIO[50] UIM1_DATA	B B	P10	PD: nppukp	Transmit serial data output 3 V tolerant input
UART3/UIM2 interface						
UART3_RFR_N	O	GPIO[84] UIM2_CLK	B O	P10	PD: nppukp	Ready to receive
UART3_CTS_N	I	GPIO[85] # UIM2_RESET #	B O	P10	PD: nppukp	Clear to send
UART3_RX	I	GPIO[86] # UIM2_PWR_EN # // GPIO[112] //	B O B	P10	PD: nppukp	Receive serial data input
UART3_TX	O	GPIO[87] UIM2_DATA // GPIO[111] //	B B B	P10	PD: nppukp	Transmit serial data output 3 V tolerant input
Transport stream interface (digital mobile broadcast)						
TSIF_CLK	I	GPIO[43] // GPIO[84] //	B	P3	PU: nppdkp	Clock
TSIF_EN	I	GPIO[44] // GPIO[85] //	B	P3	PD: nppukp	Enable
TSIF_DATA	I	GPIO[45] // GPIO[86] //	B	P3	PD: nppukp	Data
TSIF_SYNC	I	GPIO[46] // GPIO[87] //	B	P3	PD: nppukp	Synchronization for beginning of packet
TSIF_ERROR	I	GPIO[68]	B	P3	PD: nppukp	Packet error flag
TSIF_NULL	I	GPIO[69]	B	P3	PD: nppukp	Discrimination flag

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
USB3 transceiver interface						
USB3_DAT_VP	B	GPIO[84]	B	P10	PD: nppukp	Differential plus (+) for USB3 interface. USB3 is used for USB-UICC only.
USB3_SE0_VM	B	GPIO[85]	B	P10	PD: nppukp	Differential minus (-) for USB3 interface. USB3 is used for USB-UICC only.
USB3_OE_INT_N	O	GPIO[87] USB3_OE_INT	B	P10	PD: nppukp	Active low output used to enable or disable the D+ and D- pins of the transceiver. USB3 is used for USB-UICC only.
Secure digital 1 interface						
SDC1_DATA[3]	B	GPIO[51]	B	P3	PD: nppukp	Secure digital data
SDC1_DATA[2]	B	GPIO[52]	B	P3	PD: nppukp	Secure digital data
SDC1_DATA[1]	B	GPIO[53]	B	P3	PD: nppukp	Secure digital data
SDC1_DATA[0]	B	GPIO[54]	B	P3	PD: nppukp	Secure digital data
SDC1_CMD	B	GPIO[55]	B	P3	PD: nppukp	Secure digital command
SDC1_CLK	O	GPIO[56]	B	P3	PD: nppukp	Secure digital clock
Secure digital 2 (SDC2) interface						
SDC2_DATA[3]	B	GPIO[64]	B	P3	PD: nppukp	Secure digital data
SDC2_DATA[2]	B	GPIO[65]	B	P3	PD: nppukp	Secure digital data
SDC2_DATA[1]	B	GPIO[66]	B	P3	PD: nppukp	Secure digital data
SDC2_DATA[0]	B	GPIO[67]	B	P3	PD: nppukp	Secure digital data
SDC2_CLK	O	GPIO[62]	B	P3	PD: nppukp	Secure digital clock
SDC2_CMD	B	GPIO[63]	B	P3	PD: nppukp	Secure digital command
Secure digital 3 (SDC3) interface						
SDC3_DATA[3]	B	GPIO[90]	B	P3	PD: nppukp	Secure digital data
SDC3_DATA[2]	B	GPIO[91]	B	P3	PD: nppukp	Secure digital data
SDC3_DATA[1]	B	GPIO[92]	B	P3	PD: nppukp	Secure digital data
SDC3_DATA[0]	B	GPIO[93]	B	P3	PD: nppukp	Secure digital data
SDC3_CLK	O	GPIO[88]	B	P3	PD: nppukp	Secure digital clock
SDC3_CMD	B	GPIO[89]	B	P3	PD: nppukp	Secure digital command
Secure digital 4 (SDC4) interface						
SDC4_DATA[3]	B	GPIO[19]	B	P3	PD: nppdkp	Secure digital data
SDC4_DATA[2]	B	GPIO[20]	B	P3	PD: nppdkp	Secure digital data

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
SDC4_DATA[1]	B	GPIO[21]	B	P3	PD: nppdkp	Secure digital data
SDC4_DATA[0]	B	GPIO[108]	B	P3	PD: nppukp	Secure digital data
SDC4_CLK	O	GPIO[109]	B	P3	PD: nppukp	Secure digital clock
SDC4_CMD	B	GPIO[107]	B	P3	PD: nppukp	Secure digital command
SSBI interface						
SSBI_TX	O	GPIO[57]	B	P3	PD: nppukp	
SSBI_RX	B	GPIO[58]	B	P3	PD: nppukp	
SSBI_RTR	B	GPIO[59]	B	P3	PD: nppukp	
SSBI_PMIC	O	MPM_GPIO[2]	B	P3	PD: nppukp	SSBI for the PM7540 device
I²C interface						
I2C_SDA	B	GPIO[61]	B	P3	PU: nppdkp	I2C serial bus data
I2C_SCL	B	GPIO[60]	B	P3	PU: nppdkp	I2C serial bus clock
AUX_I2C_SDA	B	GPIO[96]	B	P4	PD: nppdkp	I2C serial bus data
AUX_I2C_SCL	B	GPIO[95]	B	P4	PD: nppdkp	I2C serial bus clock
Aux codec/PCM/stereo DAC interface						
AUX_PCM_DOUT	O	GPIO[68] {SDAC_DOUT}	B O	P3	PD: nppukp	PCM clock for auxiliary codec port PCM data output for stereo DAC port
AUX_PCM_DIN	I	GPIO[69] {SDAC_MCLK}	B O	P3	PD: nppukp	PCM data output for auxiliary codec port PCM data strobe for stereo DAC port
AUX_PCM_SYNC	O	GPIO[70] {SDAC_L_R_N}	B O	P3	PD: nppukp	PCM data input for auxiliary codec port PCM left/right strobe for stereo DAC port
AUX_PCM_CLK	B	GPIO[71] {SDAC_CLK}	B O	P3	PD: nppukp	PCM data strobe for auxiliary codec port PCM clock for stereo DAC port
AUX JTAG interface						
AUX_TRST_N	I	EBI2_CS2_N GPIO[102]	O B	P2	NP: pdpukp	Auxiliary JTAG reset
AUX_TCK	I	EBI2_CS3_N GPIO[103]	O B	P2	NP: pdpukp	Auxiliary JTAG clock
AUX_TMS	I	EBI2_ADR[17] GPIO[98]	O B	P9	NP: pdpukp	Auxiliary JTAG mode select
AUX_TDI	I	EBI2_ADR[18] GPIO[99]	O B	P9	NP: pdpukp	Auxiliary JTAG data input

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
AUX_TDO	O	EBI2_ADV_N GPIO[100]	O B	P9	PU: nppdkp	Auxiliary JTAG data output
AUX_RTCK	O	GPIO[101]	B	P2	PU: nppdkp	Auxiliary JTAG data output
GSM interface						
GRFC[14]	O	GPIO[68]	B	P3		
GRFC[13]	O	GPIO[69]	B	P3		
GRFC[12]	O	GPIO[70]	B	P3		
GRFC[11]	O	GPIO[71]	B	P3		
GRFC[10]	O	TX_ON	O	P3		
GRFC[9]	O	GPIO[72]	B	P3	PD: nppukp	
GRFC[8]	O	GPIO[73]	B	P3	PD: nppukp	
GRFC[7]	O	GPIO[74]	B	P3	PD: nppukp	
GRFC[6]	O	GPIO[75]	B	P3	PD: nppukp	
GRFC[5]	O	GPIO[76]	B	P3	PU: nppdkp	
GRFC[4]	O	GPIO[77]	B	P3	PU: nppdkp	
GRFC[3]	O	GPIO[78]	B	P3	PD: nppukp	
GRFC[2]	O	GPIO[79]	B	P3	PD: nppukp	
GRFC[1]	O	GPIO[80]	B	P3	PD: nppukp	
GRFC[0]	O	GPIO[81]	B	P3	PD: nppukp	
Camera interface						
CAM_DATA[11]	I	GPIO[11]	B	P4	PD: nppukp	Parallel camera interface pixel data input
CAM_DATA[10]	I	GPIO[10]	B	P4	PD: nppukp	
CAM_DATA[9]	I	GPIO[9]	B	P4	PD: nppukp	
CAM_DATA[8]	I	GPIO[8]	B	P4	PD: nppukp	
CAM_DATA[7]	I	GPIO[7]	B	P4	PD: nppukp	
CAM_DATA[6]	I	GPIO[6]	B	P4	PD: nppukp	
CAM_DATA[5]	I	GPIO[5]	B	P4	PD: nppukp	
CAM_DATA[4]	I	GPIO[4]	B	P4	PD: nppukp	
CAM_DATA[3]	I	GPIO[3]	B	P4	PD: nppukp	
CAM_DATA[2]	I	GPIO[2]	B	P4	PD: nppukp	
CAM_DATA[1]	I	GPIO[1]	B	P4	PD: nppukp	
CAM_DATA[0]	I	GPIO[0]	B	P4	PD: nppukp	
CAM_PCLK	I	GPIO[12]	B	P4	PD: nppukp	Clocks pixel input clock: data, vsync, and hsync signals
CAM_HSYNC_IN	I	GPIO[13]	B	P4	PD: nppukp	Parallel camera horizontal sync input

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
CAM_VSYNC_IN	I	GPIO[14]	B	P4	PD: nppukp	Parallel camera vertical sync input
CAM_MCLK	O	GPIO[15]	B	P4	PD: nppukp	Synchronization clock for sensors without their own
SYNC_TIMER1	O	GPIO[70] //GPIO[76]// //GPIO[30]//	B	P3	PD: nppukp	Camera control, synchronous timer output 1
SYNC_TIMER2	O	GPIO[29] //GPIO[76]//	B	P3	PD: nppukp	Camera control, synchronous timer output 2
ASYNC_TIMER1A	O	GPIO[17] //GPIO[77]//	B	P3	PD: nppukp	Camera control, asynchronous timer output 1 (line A)
ASYNC_TIMER1B	O	GPIO[18] //GPIO[80]//	B	P3	PU: nppdkp	Camera control, asynchronous timer output 1 (line B)
ASYNC_TIMER2A	O	GPIO[27] //GPIO[77]//	B	P3	PD: nppukp	Camera control, asynchronous timer output 2 (line A)
ASYNC_TIMER2B	O	GPIO[28] //GPIO[80]//	B	P3	PD: nppukp	Camera control, asynchronous timer output 2 (line B)
LCDC						
LCDC_RED[7]	O	GPIO[100]	B	P9	PU: nppdkp	
LCDC_RED[6]	O	GPIO[99]	B	P9	NP: pdpukp	
LCDC_RED[5]	O	GPIO[98]	B	P9	NP: pdpukp	
LCDC_RED[4]	O	EBI2_ADR[16]	B	P9		
LCDC_RED[3]	O	EBI2_ADR[15]	B	P9		
LCDC_RED[2]	O	EBI2_ADR[14]	B	P9		
LCDC_RED[1]	O	EBI2_ADR[13]	B	P9		
LCDC_RED[0]	O	EBI2_ADR[12]	B	P9		
LCDC_BLUE[7]	O	GPIO[113]	B	P8	PD: nppukp	
LCDC_BLUE[6]	O	GPIO[114]	B	P8	PD: nppukp	
LCDC_BLUE[5]	O	GPIO[115]	B	P8	PD: nppukp	
LCDC_BLUE[4]	O	GPIO[116]	B	P8	PD: nppukp	
LCDC_BLUE[3]	O	GPIO[117]	B	P8	PD: nppukp	
LCDC_BLUE[2]	O	GPIO[118]	B	P8	PD: nppukp	
LCDC_BLUE[1]	O	GPIO[125]	B	P9	PD: nppukp	
LCDC_BLUE[0]	O	GPIO[126]	B	P9	PD: nppukp	
LCDC_GREEN[7]	O	EBI2_ADR[11]	B	P9		
LCDC_GREEN[6]	O	EBI2_ADR[10]	B	P9		

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
LCDC_GREEN[5]	O	GPIO[130]	B	P9	NP: pdpukp	
LCDC_GREEN[4]	O	GPIO[119]	B	P8	PD: nppukp	
LCDC_GREEN[3]	O	GPIO[120]	B	P8	PD: nppukp	
LCDC_GREEN[2]	O	GPIO[121]	B	P8	PU: nppdkp	
LCDC_GREEN[1]	O	GPIO[111]	B	P8	PD: nppukp	
LCDC_GREEN[0]	O	GPIO[112]	B	P8	PD: nppukp	
LCDC_PCLK	O			P8	PD: nppukp	
LCDC_VSYNC	O	GPIO[127]	B	P9	PD: nppukp	
LCDC_HSYNC	O	GPIO[128]	B	P9	PD: nppukp	
LCDC_DEN	O	GPIO[129]	B	P9	PD: nppukp	
ETM						
ETM_TRACEDATA[15]	O	GPIO[19]	B	P3		
ETM_TRACEDATA[14]	O	GPIO[20]	B	P3		
ETM_TRACEDATA[13]	O	GPIO[22]	B	P3		
ETM_TRACEDATA[12]	O	GPIO[23]	B	P3		
ETM_TRACEDATA[11]	O	GPIO[25]	B	P3		
ETM_TRACEDATA[10]	O	GPIO[32]	B	P3		
ETM_TRACEDATA[9]	O	GPIO[33]	B	P3		
ETM_TRACEDATA[8]	O	GPIO[34]	B	P3		
ETM_TRACEDATA[7]	O	GPIO[35]	B	P3		
ETM_TRACEDATA[6]	O	GPIO[36]	B	P3		
ETM_TRACEDATA[5]	O	GPIO[37]	B	P3		
ETM_TRACEDATA[4]	O	GPIO[38]	B	P3		
ETM_TRACEDATA[3]	O	GPIO[39]	B	P3		
ETM_TRACEDATA[2]	O	GPIO[40]	B	P3		
ETM_TRACEDATA[1]	O	GPIO[41]	B	P3		
ETM9_TRACEDATA0	O	GPIO[42]	B	P3		
ETM11_TRACEDATA0	O	GPIO[29]	B	P3		ETM11 TRACEDATA0
ETM11_TRACECTL	O	GPIO[27]	B	P3		ETM11 TRACECTL
ETM_TRACECLK	O	GPIO[30]	B	P3		ETM trace clock
ETM9_TRACESYNC	O	GPIO[31]	B	P3		Trace sync in ETM9
ETM9_PIPESTAT0	O	GPIO[29]	B	P3		ETM9 only
ETM9_PIPESTAT1	O	GPIO[27]	B	P3		ETM9 only
ETM9_PIPESTAT2	O	GPIO[26]	B	P3		ETM9 only

Table 2-4 Pin descriptions by function (cont.)

Function	Dir-Pol	MSM pad name // optional second port //	Dir-Pol	Volt	Pad-attrib	Description
ETM_TRACECLKB	O	GPIO[82]	B	P3		ETM trace clock for dual-processor mode
ETM9_PIPESTATB0	O	GPIO[16]	B	P3		Reserved for ETM9 deMUX mode
ETM9_PIPESTATB1	O	GPIO[17]	B	P3		Reserved for ETM9 deMUX mode
ETM9_PIPESTATB2	O	GPIO[18]	B	P3		Reserved for ETM9 deMUX mode
ETM9_TRACESYNCB	O	GPIO[82]	B	P3		Reserved for ETM9 deMUX mode
ETM_GPIO2_CS_N	O	GPIO[24]	B	P3		GPIO emulation chip select to SURF FPGA
ETM_GPIO_IRQ	I	GPIO[28]	B	P3		GPIO emulation summary IRQ for GPIO[42: 16] from SURF FPGA
ETM_KEYSENS_IRQ	I	GPIO[21]	B	P3		GPIO emulation IRQ for KEYSENSE detect from SURF FPGA
ETM_GPIO_SHDW_IRQ	I	GPIO[87]	B	P3		Shadow GPIO emulation summary IRQ for GPIO[42: 16] from SURF FPGA

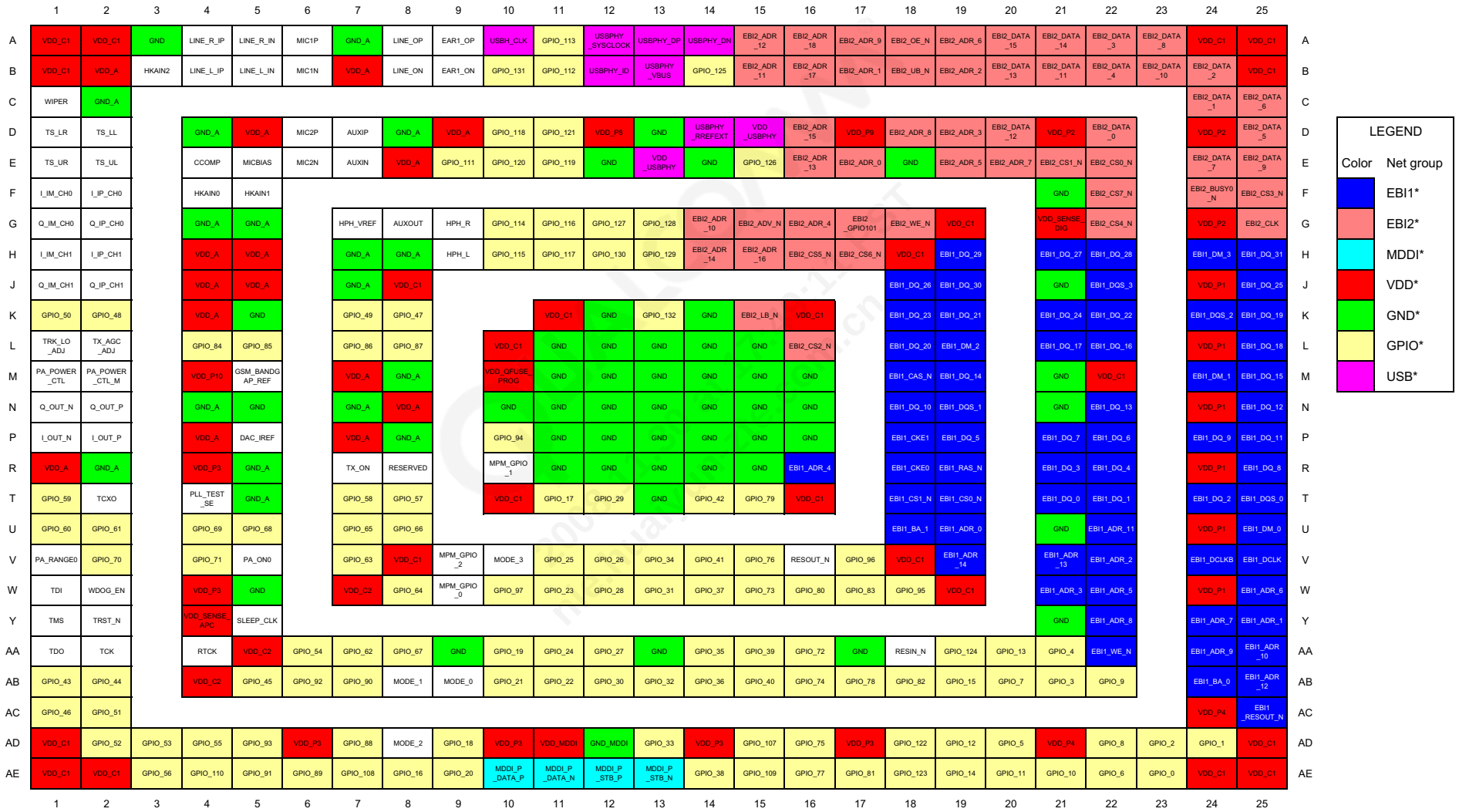


Figure 2-2 Pinout for the MSM7625 device

3 Electrical Specifications

3.1 DC electrical specifications

3.1.1 Absolute maximum ratings

Operating the MSM7625 device under conditions that exceed those listed in Table 3-1 may result in damage to the device. Absolute maximum ratings are limiting values and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the MSM7625 device under any of the conditions listed in Table 3-1 is not implied. Exposure to absolute maximum ratings for extended periods of time may affect the device's reliability.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min	Max	Units
T_S	Storage temperature	-65	+150	°C
T_J	Junction temperature		+125	°C
V_I	Voltage on any input or output pin	-0.5	V_{DD}+0.5	V
$V_{DD\_A,P}$	Supply voltage (analog, pad)	-0.3	3.0	V
V_{DD_C}	Supply voltage (core)	-0.3	2.3	V
USBPHY_VBUS	USB VBUS voltage		6.0	V
I_{IN}	Latch-up current	-150	150	mA
V_{ESDHBM}	Electrostatic discharge voltage (human body model)		2000	V
V_{ESDCDM}	Electrostatic discharge voltage (charge device model)		500	V

3.1.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Units
T_C	Operating temperature (case)	-30		90	°C
V_{DD_C1}[3]	Supply voltage for MSM digital core #1 (everything but ARM11)				
	High speed (ARM11 > 384 MHz)	1.27	1.35	1.45	V
	Normal operation (ARM11 <= 384 MHz)[2]	1.17	1.25	1.45	V
	VDD minimization (retention state)	0.75			V
V_{DD_C2}[3]	Supply voltage for MSM digital core #2 (ARM11)				
	High speed (ARM11 > 384 MHz)	1.27	1.35	1.45	V
	Normal operation (ARM11 <= 384 MHz)[2]	1.17	1.25	1.45	V
V_{DD_A}	Supply voltage for internal analog core	2.5	2.6	2.7	V
V_{DD_P1}	Supply voltage P1 for EBI1 and peripheral interfaces	1.7	1.8	1.9	V
V_{DD_P2}[1]	Supply voltage P2 for EBI2 and peripheral interfaces	1.65	1.8	1.95	V
		2.5	2.6	2.7	V
V_{DD_P3}	Supply voltage P3 for peripheral interfaces	2.5	2.6	2.7	V
V_{DD_P4}[1]	Supply voltage P4 for camera interface	1.65	1.8	1.95	V
		2.5	2.6	2.7	V
V_{DD_P7}	Supply voltage P7 for internal reference	2.5	2.6	2.7	V
V_{DD_P8}[1]	Supply voltage P8 for LCDC interfaces	1.65	1.8	1.95	V
		2.5	2.6	2.7	V
V_{DD_P9}[1]	Supply voltage P9 for LCDC or EBI2 interfaces	1.65	1.8	1.95	V
		2.5	2.6	2.7	V
V_{DD_P10}	Supply voltage P10 for USIM and USB-UICC	1.65		3.0	V
V_{DD_MDDI}	Supply voltage for MDDI interface	1.65	1.8	1.95	V
VDD_USBPHY (3.3 V)	Supply voltage for USB (HS) PHY interface	3.0	3.3	3.6	V
VDD_USBPHY (2.6 V)	Supply voltage for USB (HS) PHY interface	2.5	2.6	2.7	V
$V_{DD\_QFUSE\_PROG}$	Supply voltage for Qfuse programming	2.8	2.9	3.0	V

Notes:

1. This voltage must match the external device voltage. It is a dual-voltage pin and can be either 1.8 VDC nominal or 2.6 VDC nominal.
2. ARM11 (V_{DD_C2}) can operate at a lower voltage when the operating frequency is scaled down.
3. The MSM7625 chipset must implement PM7540 device's V_{DD_C1} and V_{DD_C2} local voltage-sensing capability in order to guarantee performance. Refer to the *MSM7625 Baseband Reference Schematic* (80-VJ153-41) for more information on voltage sensing.

Designers should use a programmable voltage regulator such as the PM7540 device for V_{DD_C1} and V_{DD_C2}. This allows the best flexibility for using the same design for future pin-compatible MSM devices that may require a lower V_{DD_C}.

3.1.3 Device thermal characteristics

The MSM7625 device in its 456 NSP package has typical thermal resistances as listed in Table 3-3.

Table 3-3 Device thermal resistance

Parameter		Comments	Typ	Units	Notes
θ_{JA}	Thermal resistance, J-to-A	Junction to ambient (still air)	22.8	°C/W	1, 2
θ_{JC}	Thermal resistance, J-to-C	Junction to case	3.9	°C/W	2, 3

Notes:
1. Thermal resistance, θ_{JA} from junction to ambient is calculated based on maximum die junction and total package power dissipation; ambient temperature is 85 °C.
2. $\theta_{JA,C}$ will vary based on the power consumption of the dies. The specified $\theta_{JA,C}$ was calculated using power consumption estimates of 625 mW for the digital die and 200 mW for the analog die.
3. Junction-to-case thermal resistance, θ_{JC}, applies to situations in which all or nearly all of the heat is flowing out of top of the package.

3.1.4 DC characteristics

Table 3-4 DC characteristics (for V_{DD_PX} = 1.8 V)

Symbol	Description	Min	Max	Units	Notes
V_{IH}	High-level input voltage, CMOS/Schmitt	0.65 • V_{DD_Px}	V_{DD_Px} + 0.3	V	
V_{IL}	Low-level input voltage, CMOS/Schmitt	-0.3	0.35 • V_{DD_Px}	V	
V_{SHYS}	Schmitt hysteresis voltage	100		mV	
I_{IH}	Input high leakage current	-	1	µA	1, 3
I_{IL}	Input low leakage current	-1		µA	2, 4
I_{IHPD}	Input high leakage current with pull-down	3	30	µA	1, 3, 5
I_{ILPU}	Input low leakage current with pull-up	-30	-3	µA	2, 4, 5
V_{OH}	High-level output voltage, CMOS, when driving pin at rated drive strength	V_{DD_Px}-0.45	V_{DD_Px}	V	6, 7
V_{OL}	Low-level output voltage, CMOS, when driving pin at rated drive strength	0	0.45	V	6, 7
I_{OZH}	High-level, three-state leakage current		1	µA	1
I_{OZL}	Low-level, three-state leakage current	-1		µA	2
I_{OZHPD}	High-level, three-state leakage current with pull-down	5	30	µA	1, 5

Table 3-4 DC characteristics (for V_{DD_PX} = 1.8 V) (cont.)

Symbol	Description	Min	Max	Units	Notes
I_{OZLPU}	Low level, three-state leakage current with pull-up	-30	-5	µA	2, 5
I_{OZHKP}	High-level, three-state leakage current with keeper	-15	-3	µA	3
I_{OZLKP}	Low level, three-state leakage current with keeper	3	15	µA	4
I_{ISL}	Sleep xtal input leakage	-0.15	0.15	µA	
I_{IHVKP}	High voltage tolerant input leakage with keeper	-1		µA	
C_{IN}	Input capacitance		7	pF	8

Notes:
1. Pin voltage = V_{DD_P} (max) and V_{DD_P} = V_{DD_P} (max).
2. Pin voltage = V_{SS} and V_{DD_P} = V_{DD_P} (max).
3. For keeper pins, pin voltage = V_{DD_P} (max) - 0.45 V.
4. For keeper pins, pin voltage = 0.45 V and V_{DD_P} = V_{DD_P} (max).
5. Refer to Table 2-2 for pull-up, pull-down, and keeper information on pins.
6. Refer to Table 2-2 for I_{OH} and I_{OL} rated drive strength (current) for output pins (at V_{DD_P} = V_{DD_P} [min]).
7. The default drive strength and the programmable range are included in Table 2-1.
8. The input capacitance value is guaranteed by design, but is not 100% tested.

Table 3-5 DC characteristics (for V_{DD_PX} = 2.6 V)

Symbol	Description	Min	Max	Units	Notes
V_{IH}	High-level input voltage, CMOS/Schmitt	0.65 • V_{DD_Px}	V_{DD_Px} + 0.3	V	
V_{IL}	Low-level input voltage, CMOS/Schmitt	-0.3	0.35 • V_{DD_Px}	V	
V_{SHYS}	Schmitt hysteresis voltage	150		mV	
I_{IH}	Input high leakage current		1	µA	1, 3
I_{IL}	Input low leakage current	-1		µA	2, 4
I_{IHPD}	Input high leakage current with pull-down	10	60	µA	1, 3, 5
I_{ILPU}	Input low leakage current with pull-up	-60	-10	µA	2, 4, 5
V_{OH}	High-level output voltage, CMOS, when driving pin at rated drive strength	V_{DD_Px}-0.45	V_{DD_Px}	V	6, 7
V_{OL}	Low-level output voltage, CMOS, when driving pin at rated drive strength	0	0.45	V	6, 7
I_{OZH}	High-level, three-state leakage current		1	µA	1
I_{OZL}	Low-level, three-state leakage current	-1		µA	2
I_{OZHPD}	High-level, three-state leakage current with pull-down	10	60	µA	1, 5
I_{OZLPU}	Low level, three-state leakage current with pull-up	-60	-10	µA	2, 5
I_{OZHKP}	High-level, three-state leakage current with keeper	-25	-5	µA	3
I_{OZLKP}	Low level, three-state leakage current with keeper	5	25	µA	4

Table 3-5 DC characteristics (for V_{DD_PX} = 2.6 V) (cont.)

Symbol	Description	Min	Max	Units	Notes
I_{ISL}	Sleep xtal input leakage	-0.15	0.15	µA	
I_{IHVKP}	High voltage tolerant input leakage with keeper	-1	1	µA	
C_{IN}	Input capacitance		7	pF	8
$V_{TCXOHDC}$	High-level input voltage, TCXO DC input	0.65 • V_{DD_A}	V_{DD_A} + 0.3	V	
$V_{TCXOLDC}$	Low-level input voltage, TCXO DC input	-0.3	0.35 * V_{DD_A}	V	
V_{TCXOAC}	Peak-to-peak input voltage, TCXO AC input	0.5	V_{DD_A} + 0.3	V	
$I_{TCXOIHDC}$	Input high leakage with pull-down, TCXO DC input	5	45	µA	1,3

Notes:
1. Pin voltage = V_{DD_P} (max) and V_{DD_P} = V_{DD_P} (max).
2. Pin voltage = V_{SS} and V_{DD_P} = V_{DD_P} (max).
3. For keeper pins, pin voltage = V_{DD_P} (max) - 0.45 V.
4. For keeper pins, pin voltage = 0.45 V and V_{DD_P} = V_{DD_P} (max).
5. Refer to Table 2-2 for pull-up, pull-down, and keeper information on pins.
6. Refer to Table 2-2 for I_{OH} and I_{OL} rated drive strength (current) for output pins (at V_{DD_P} = V_{DD_P} (min)).
7. The default drive strength and the programmable range are included in Table 2-1.
8. Input capacitance value is guaranteed by design, but is not 100% tested.

Table 3-6 DC characteristics for EBI1 DDR SDRAM interface at 1.8 V

Symbol	Description	Min	Max	Units	Notes
V_{IH}	High-level input threshold, CMOS/Schmitt	0.8 • V_{DD_Px}	V_{DD_Px} + 0.3	V	
V_{IL}	Low-level input threshold, CMOS/Schmitt	-0.3	0.20 • V_{DD_Px}	V	
I_{IH}	Input high-leakage current		1	µA	1
I_{IL}	Input low-leakage current	-1		µA	2
I_{IHPD}	Input high-leakage current with pull-down	50	300	µA	1
I_{ILPU}	Input low-leakage current with pull-up	-300	-50	µA	2
V_{OH}	High-level output voltage, CMOS, when driving pin at rated drive strength	0.9 • V_{DD_Px}	V_{DD_Px} + 0.3	V	
V_{OL}	Low-level output voltage, CMOS, when driving pin at rated drive strength	-0.3	0.10 • V_{DD_Px}	V	
I_{OH}	High-level output current, CMOS, default setting	2.05		mA	4
I_{OL}	Low-level output current, CMOS, default setting	2.05		mA	4
I_{OZH}	High-level, three-state leakage current		1	µA	
I_{OZL}	Low-level, three-state leakage current	-1	-	µA	
C_{IN}	Inputs capacitance		3	pF	3

Table 3-6 DC characteristics for EBI1 DDR SDRAM interface at 1.8 V (cont.)

Symbol	Description	Min	Max	Units	Notes
C_{IO}	I/O, DQS, DQ, or clock capacitance		5	pF	3

Notes:
1. Pin voltage (V_{DD_P}) = 1.9 V.
2. Pin voltage = V_{ss} and V_{DD_P} = 1.9 V.
3. Per pin on one memory package; input capacitance value is guaranteed by design, but not 100% tested.
4. The minimum specification is based on the default EBI1 DDR SDRAM drive strength with a bit setting of "100"

V_{OL} and V_{OH} are linear functions for the amount of drive strength used, as shown in Figure 3-1. They can also be calculated using the following equations:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

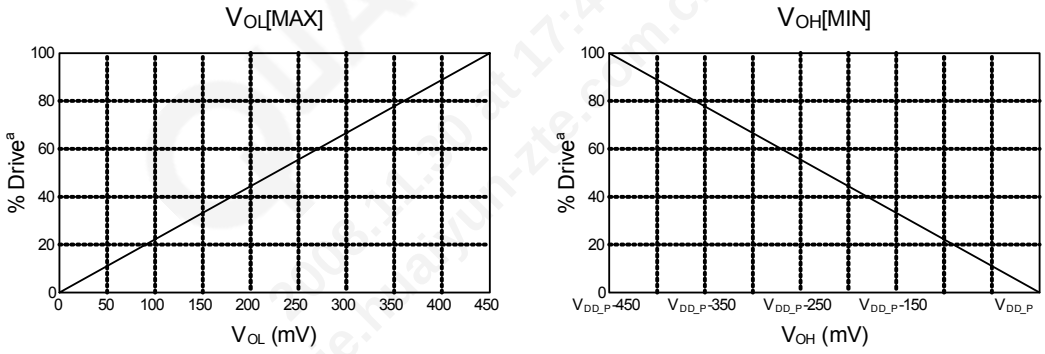


Figure 3-1 IV curve for V_{OL} and V_{OH} for V_{DD_PX} = 1.8 V or 2.6 V

NOTE See Table 2-1 for maximum drive strength and for appropriate voltage range.

3.1.5 Power consumption characteristics

Power consumption characteristics will be provided in a future release of this document.

3.1.6 Power sequencing

The PM7540 IC includes power-on circuits that provide the proper power sequencing for the MSM7625 chipset. The required power-up sequence is:

1. VDD_C1 (modem subsystem)
2. VDD_E (pad group EBI1/EBI2/MDDI/camera)
3. VDD_P (pad group GPIO)
4. VDD_A (pad group analog)

Comments regarding this sequence:

- VDD_C2 is decoupled from the power-up sequence and can be powered up by software when the MSM device has completed the boot process.
- All other power supplies can be powered on by software after the sequence is completed.
- EBI2 pad group can be powered on by 1.8 V or 2.6 V power rail.
- Core voltage needs to come up first so that internal circuits can take control of the I/O(s) and pads.
- VDD_QFUSE_PROG voltage must come up after the end of the power-up sequence listed above. It must be the last power rail to come up in order to prevent accidental blowing of Qfuses.
- If the pad_voltage comes on first, there may be large leakage due to the large driver transistors and the output drivers being stuck in unknown states, until Core_vdd comes on.
- Pad_voltage needs to precede analog voltage as SSBI is initialized to default before Analog_voltage comes up. (Note: The Analog section is controlled by SSBI.)
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when Core_VDD reaches 90% of its value, the next domain can start ramping up.
- The steps in the power-down sequence are executed in the reverse order of those in the power-up sequence.

See the *PM7540 Power Management IC User Guide* (80-VD691-3) for additional details.

3.2 Timing characteristics

3.2.1 Timing diagrams

The timing diagrams (Figure 3-2) illustrate the signals on the external bus as a function of time, as measured by the AHB bus clock (HCLK). Throughout this chapter, the term *HCLK* refers to the AHB bus-clock cycle and refers to T, unless otherwise specified. A clock extends from one rising HCLK edge to the next rising HCLK edge. For each signal in the timing diagrams, the high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state. When both the high and low levels are shown, the meaning depends on the signal. A single signal indicates “Don’t care.” In the case of bus activity, if both high and low levels are shown, the processor or external interface is driving a value that may or may not be valid.

Waveform	Description
	Don't care or bus is driven.
	Signal is changing from low to high.
	Signal is changing from high to low.
	Bus is changing from invalid to valid.
	Bus is changing from Hi-Z to valid.
	Denotes multiple clock periods.

Figure 3-2 Timing diagram waveforms

3.2.2 Rise and fall time

The tester that characterizes the MSM7625 device has an actively terminated load. This makes rise and fall transitions quicker (essentially mimicking a no-load condition as suggested in Figure 3-3). ***For this reason, the bus rise or fall time must be added to parameters that start timing at the MSM7625 device and terminate at the memory device.*** One of these parameters is the chip select to data valid on a read cycle. An example of this is **t**(csdv) in EBI2 asynchronous memory timing. Table 3-7 shows the capacitive load derating factor for EBI1 and EBI2.

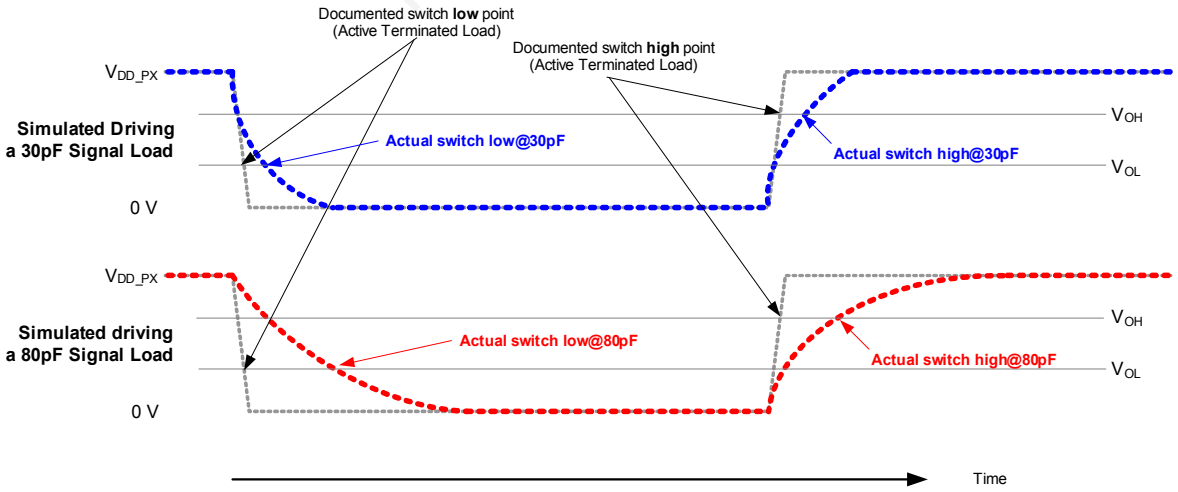


Figure 3-3 Rise and fall time in different load conditions

Table 3-7 Capacitive load derating factor

Symbol	EBI 1			Units
	EBI1_SDRAM_IO_DRVRx settings			
	000	100	111	
t(r) (0-90%)	0.16	0.11	0.10	ns/pF
t(f)(100-10%)	0.17	0.12	0.10	ns/pF
Symbol	**EBI 2 (pad voltage = 1.8 V)**			**Units**
	EBI2_IO_DRVRx_CFG settings			
	000	100	111	
t(r) (0-65%)	0.44	0.09	0.06	ns/pF
t(r) (0-90%)	0.76	0.15	0.10	ns/pF
t(f) (100-35%)	0.45	0.09	0.06	ns/pF
t(f)(100-10%)	0.74	0.15	0.10	ns/pF
Symbol	**EBI 2 (pad voltage = 2.6 V)**			**Units**
	EBI2_IO_DRVRx_CFG settings			
	000	100	111	
t(r) (0-65%)	0.29	0.07	0.04	ns/pF
t(r) (0-90%)	0.53	0.11	0.08	ns/pF
t(f) (100-35%)	0.31	0.07	0.04	ns/pF
t(f)(100-10%)	0.52	0.11	0.07	ns/pF

3.2.3 Pad design methodology

The MSM7625 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_PX} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case process/voltage/temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

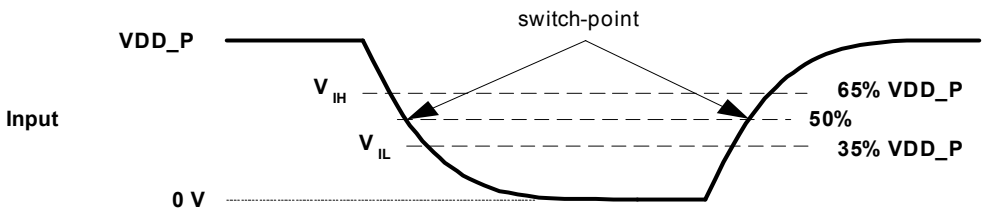


Figure 3-4 MSM7625 input signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero-DC-load outputs are estimated to be:

- V_{OH} ~ V_{DD_PX} - 50 mV or more
- V_{OL} ~ 50 mV or less

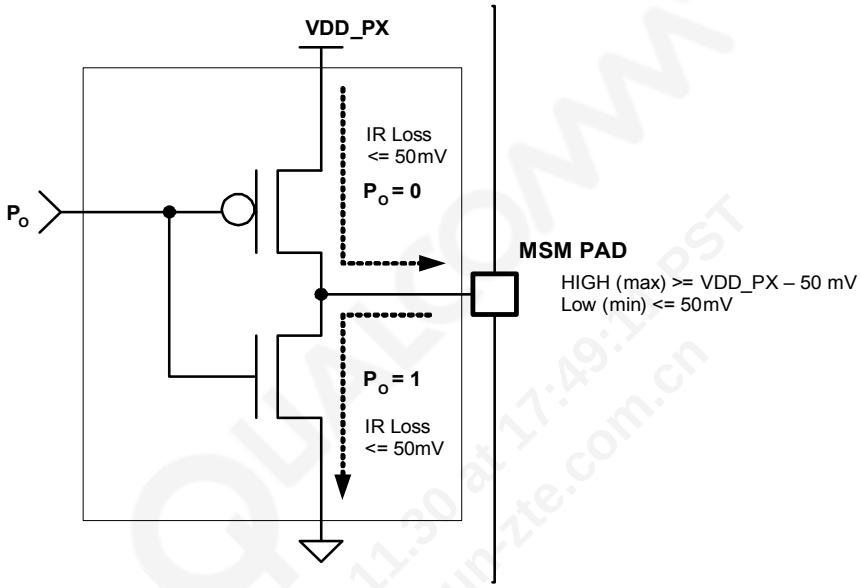


Figure 3-5 MSM7625 output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

The output driver rise time (**t**(r)) or fall time (**t**(f)) is a function of the phone board loading. EBI1 loading should be on the order of 20 pF (or less for a phone design with a single external memory device), but could be as high as 30 pF (assuming that phone designs have tight geometries and layout, and that the memory subsystem is treated as a lumped model load as opposed to a transmission line load).

NOTE EBI1 phone board loading should be limited to 30 pF or less. [1]

Bidirectional pins (such as the microprocessor databus) include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

In addition to being bidirectional, databus pins also include pad keepers. These keepers are weak flip-flops (easily over-driven by an external source) on the pad side of the structure to encourage an otherwise undriven pad voltage to migrate to a power or ground rail, either to help ensure hold-time requirements or to minimize power consumption within otherwise undriven pad structures. Keepers have the following impacts on the physical interface:

- External sources driving these pins must overcome the keepers in order to drive a logic level on such pins. The amount of current required must be greater than the maximum I_{OZLKP} values listed within the tables of Section 3.1.4.
- When an external source releases control of such pins, the keepers tend to hold the last logic level on the pins (subject to system-level leakages and capacitive loading effects). The minimum I_{OZLKP} current values may be sustained indefinitely without upsetting the state of the keeper.

3.2.4 Clocks

3.2.4.1 TCXO timing

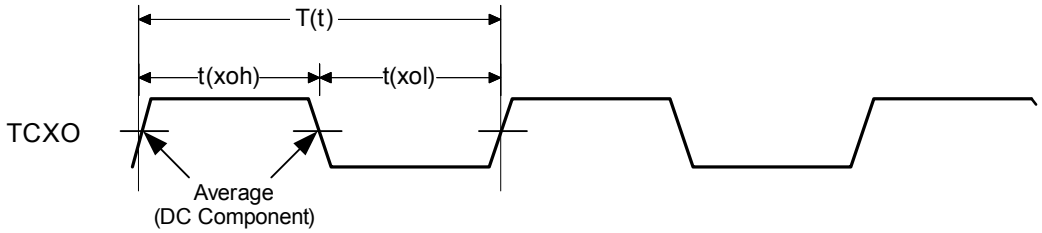


Figure 3-6 TCXO timing parameters

1. Memory vendors intending to support these products are encouraged to provide accurate timing information for the capacitive load levels. For example, vendors should provide timing values for 10 pF, 20 pF, 30 pF, and 40 pF loading during EBI1 operation, or should provide an accurate and reasonable means of calculating/derating the timing parameters for the corresponding load levels.

Table 3-8 TCXO timing parameters[1]

Symbol	Parameter	Min	Typ	Max	Units
t(xoh)	TCXO logic high	22.6		29.5	ns
t(xol)	TCXO logic low	22.6		29.5	ns
1/T(t)	Frequency (19.2 MHz must be used.)		19.2		MHz
T(t)	TCXO clock period		52.083		ns

1. Refer to *Voltage Controlled TCXO, 19.2 MHz Specifications* (80-V2896-1) for more details on VCTCXO requirements in a phone design.

3.2.4.2 Microprocessor clock

Table 3-9 MCLK timing parameters

Symbol	Parameter	Min	Max	Units
MCLK9	ARM9 microprocessor clock frequency		See Notes 1 and 2.	MHz
MCLK11	ARM11 microprocessor clock frequency		See Notes 1 and 2.	MHz

Notes:
1. The maximum MCLK frequency supported is the maximum frequency defined by the latest of the AMSS7625 software.
2. MCLK9 and MCLK11 are MSM7625 internal clock signals.

3.2.4.3 Sleep clock

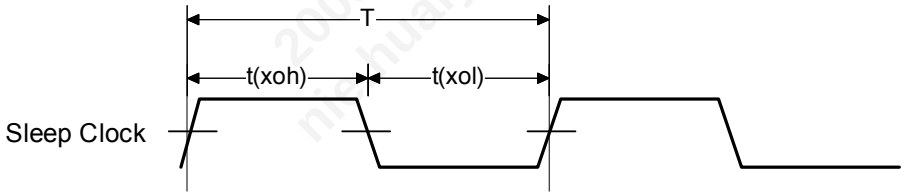


Figure 3-7 Sleep clock timing parameters

Table 3-10 Sleep clock timing parameters

Symbol	Parameter	Min	Typ	Max	Units
t(xoh)	Sleep clock logic high	4.58		25.94	µs
t(xol)	Sleep clock logic low	4.58		25.94	µs
T(t)	Sleep clock period		30.518		µs
1/T(t)	Frequency		32.768		kHz

3.2.5 EBI1

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse and hold time numbers may get better.

3.2.5.1 EBI1 pad drive strengths

Pads for EBI1 are tailored for the 1.8 V interface and are source-terminated. Before the source termination, the pad drive strength is 10-24 mA in 2-mA steps. But at the pads, after the source termination, the drive strength @ $I_{OL,}$ I_{OH} is equivalent to 1.45-2.5 mA in non-linear steps when the JEDEC standard range (90–10%) is followed.

3.2.5.2 DDR SDRAM

For any timing analysis, the measurement point for all signals is @ 50% V_{DD_P}. All output timing parameters represent the point of the output signal transition (additional delays due to signal rise/fall times for a specific bus load have to be accounted for). Timing symbols (for example: $\mathbf{t}_{IS}$) in the DDR section are made to match the JEDEC standard. The representation of the symbol is different than the timing symbols used in other sections of this document.

3.2.5.2.1 DDR SDRAM clock (EBI1_DCLK and EBI1_DCLKB)

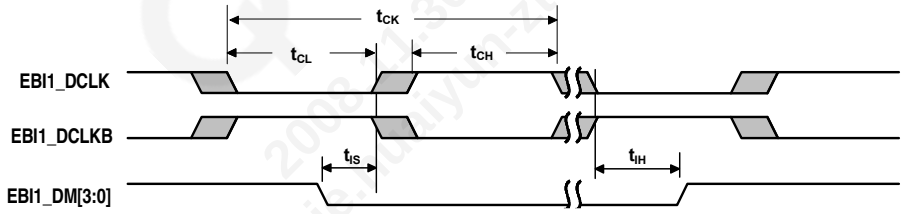


Figure 3-8 DDR SDRAM EBI1_DCLK and EBI1_DCLKB

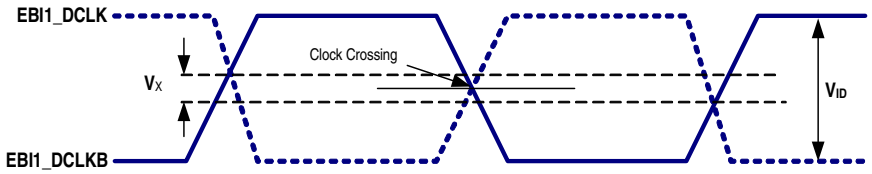


Figure 3-9 Differential clock signal

Table 3-11 DDR SDRAM timing parameters

Symbol	Parameter	Min	Max	Unit
$1/\mathbf{t}_{CK}$	DDR clock frequency	9.6	160	MHz
	Duty cycle	45	55	%
$\mathbf{V}_X$	Differential clock crossover-point relative to VSS	0.40 • V_{DD_Px}	0.60 • V_{DD_Px}	V
$\mathbf{V}_{ID}$	AC differential output voltage	1	—	V

3.2.5.3 DDR SDRAM timing

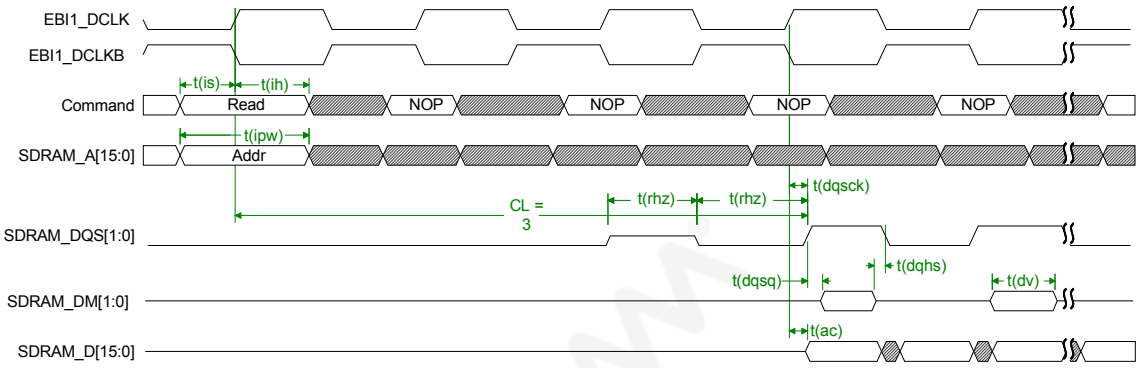


Figure 3-10 DDR SDRAM read timing

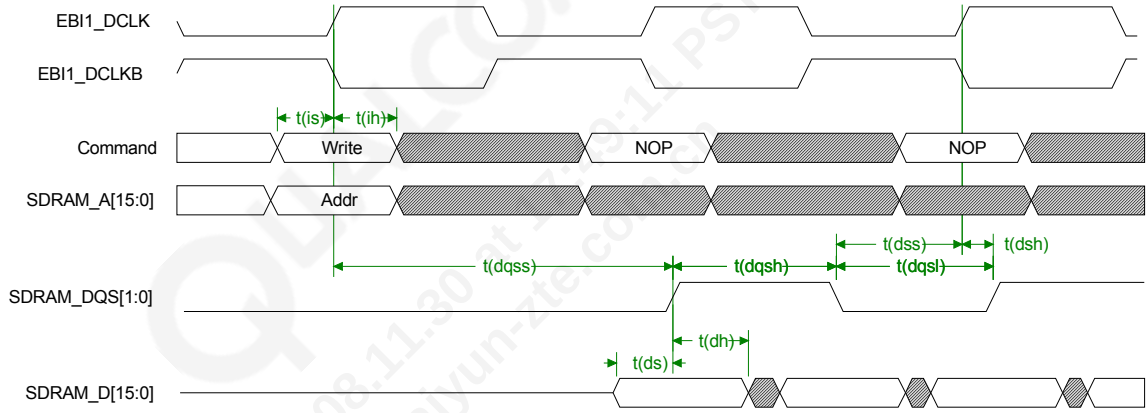


Figure 3-11 DDR SDRAM write timing

Table 3-12 DDR SDRAM memory specification

Symbol	Description	Min	Max	Unit
t_{IS}	Address and control input setup time before CK	1.1	—	ns
t_{IH}	Address and control input hold time after CK	1.1	—	ns
t_{AC}	DQ access time from clock	2	5.5	ns
t_{DIPW}	DQ and DM minimum pulse width	2.1	—	ns
t_{IPW}	Address and control input minimum pulse width	2.7	—	ns
t_{TDIFF}[1]	Allowed input transition slew rate from VIL to VIH (differential clock)	1	—	V/ns
t_T	Allowed input transition time from VIL to VIH (any input except differential clock)	1	—	V/ns
Read cycle				
t_{DQSCK}	DQS access time from clock	2	5.5	ns
t_{DQSQ}[2]	DQS to DQ skew limit	—	0.5	ns
t_{RPRE}	Read preamble	0.9	1.1	t_{CK}

Table 3-12 DDR SDRAM memory specification (cont.)

Symbol	Description	Min	Max	Unit
t_{QHS}	Data hold skew factor	—	0.65	ns
t_{DV}[2]	DQ/DQS data valid window	3	—	ns
t_{RHZ}[3, 4]	Read Hi-Z before preamble	1	2	t_{CK}
Write cycle				
t_{DS}	DQ and DM input setup time before DQS	0.6	—	ns
t_{DH}	DQ and DM input hold time after DQS	0.6	—	ns
t_{DQSH}[2]	DQS input high-level width	0.4	0.6	t_{CK}
t_{DQSL}[2]	DQS input low-level width	0.4	0.6	t_{CK}
t_{DQSS}[2]	First DQS latching transition	0.75	1.25	t_{CK}
t_{DSS}[2]	DQS falling edge to CK setup time	0.2	—	t_{CK}
t_{DSH}[2]	DQS falling edge hold time after CK	0.2	—	t_{CK}

1. Parameters are as defined in the JEDEC specification.
2. DQS lines must be well-isolated to reduce any noise induced into them.
3. Parameter is not in JEDEC standard, but an Mobile Station Modem™ (MSM™) device-specific behavior.
4. Parameters provided here are design targets and subject to change without notice.

3.2.6 EBI2

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse and hold time numbers may improve.

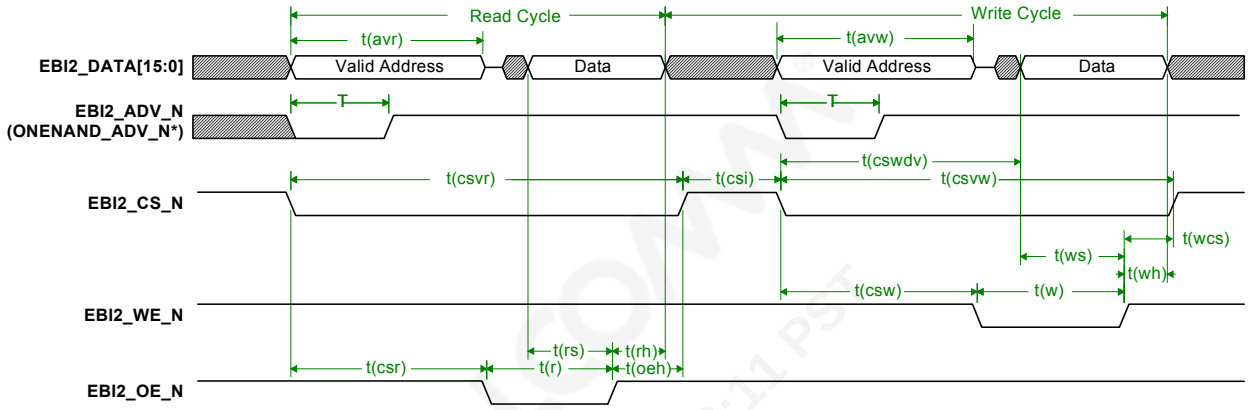
Table 3-13 EBI2 timing

Symbol	Write cycle	Read cycle
w	EBI2_XMEM_CSn_CFG0[7:4] = write wait	EBI2_XMEM_CSn_CFG0[3:0] = read wait
a_h	EBI2_XMEM_CSn_CFG1[5] = ADDR_HOLD_ENA	EBI2_XMEM_CSn_CFG1[5] = ADDR_HOLD_ENA
i	EBI2_XMEM_CSn_CFG0[23:16] = initial latency write	EBI2_XMEM_CSn_CFG0[15:8] = initial latency read
h	EBI2_XMEM_CSn_CFG0[27:24] = hold write	EBI2_XMEM_CSn_CFG1[27:24] = hold read
r	EBI2_XMEM_CSn_CFG0[31:28] = recovery [1]	EBI2_XMEM_CSn_CFG0[31:28] = recovery[1]
a_{or}	—	EBI2_XMEM_CSn_CFG1[17:16] = ADV_OE_RECOVERY
T	1 EBI2 clock cycle	

1. Recovery cycles are only inserted under certain circumstances as described in the corresponding software interface document. Precharge cycles and recovery cycles may also impact the chip-select high time as described in the corresponding MSM software interface document.

3.2.6.1 EBI2 asynchronous memory interface (including OneNAND asynchronous interface)

EBI2_DATA[15:0] of any waveforms in this section can be either data or address for address/data multiplexed interface. For de-MUXed interface, EBI2_ADR and EBI2_DATA should be used for address and data, respectively.



*For asynchronous OneNAND interface, ONENAND_ADV_N should be used on behalf of EBI2_ADV_N.

Figure 3-12 Asynchronous 16-bit read-write accesses

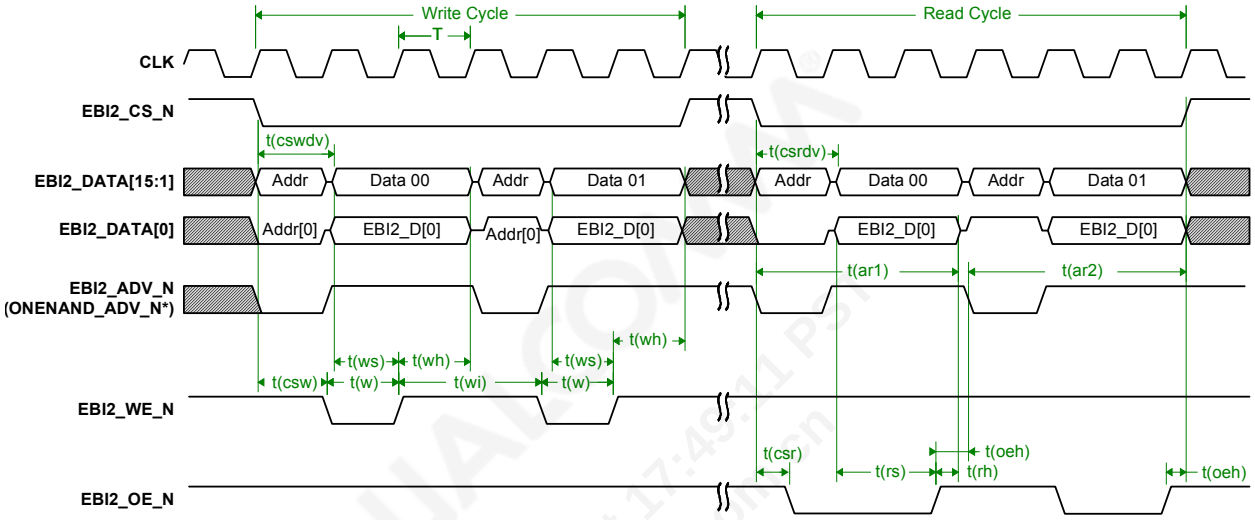
NOTE For greater hold times, setting ADDR_HOLD_ENA = 1 implies that the address will be held for one extra cycle after ADV_N rise.

Table 3-14 EBI2 asynchronous 16-bit access timing

Symbol	Description	Min	Max	Unit
Write cycle				
t(csvw)	Write cycle chip-select active	(w+i+h+1)T-3		ns
t(csw)	Chip-select active to write active	T-3		ns
t(cswdv)	Chip-select active to data valid	T-3		ns
t(w)	Write active	(w+i)T-3		ns
t(wcs)	Write inactive to chip-select inactive	(h)T-3		ns
t(avw)	Write cycle address valid	$(1+a_h)$T-3		ns
t(ws)	Write cycle data setup	(w+i)T-3		ns
t(wh)	Write data hold	(h)T-3		ns
Read cycle				
t(avr)	Read cycle address valid	$(1+a_h)$T-3		ns
t(r)	Read active	(w+i)T-3		ns
t(csvr)	Read cycle chip-select active	(w+i+1)T-3		ns
t(csr)	Chip-select active to read active	$(1+a_{or})$T-3		ns
t(csi)	Chip-select inactive	(r)T-3		ns
t(oeh)	Read inactive to chip-select inactive	(h)T-3		ns

Table 3-14 EBI2 asynchronous 16-bit access timing (cont.)

Symbol	Description	Min	Max	Unit
t(rh)	Read-data hold	0		ns
t(rs)	Read-data setup	20		ns



*For asynchronous OneNAND interface, ONENAND_ADV_N should be used on behalf of EBI2_ADV_N.

Figure 3-13 Asynchronous bus-sized access to 16-bit memory

Table 3-15 EBI2 asynchronous bus-sized access timing

Symbol	Description	Min	Max	Unit
Write cycle				
t(csw)	Chip-select active to write active	T-3		ns
t(w)	Write active	(i+w)T-3		ns
t(wi)	Write inactive	(1+h)T-3		ns
t(ws)	Write data setup	(i+w)T-3		ns
t(wh)	Write data hold time	(h)T-3		ns
t(cswdv)	Chip-select active to data valid	T-3		ns
Read cycle				
t(ar1)	Address valid to end of 1st read	(i+w+r)T-3		ns
t(ar2)	Address valid to end of 2nd read	(i+w)T-3		ns
t(csr)	Chip-select active to 1st read active	$(1+a_{or})$T-3		ns
t(rs)	Read-data setup	20		ns
t(oeh)	Read inactive to chip-select inactive	(h)T-3		ns
t(rh)	Read-data hold	0		ns
t(csrdv)	Chip-select active to data valid	(i+w)T-3		ns
t(adv)	Address valid to data valid			

3.2.6.2 EBI2 LCD interface

3.2.6.2.1 LCD interface write timing (with LCD_EN)

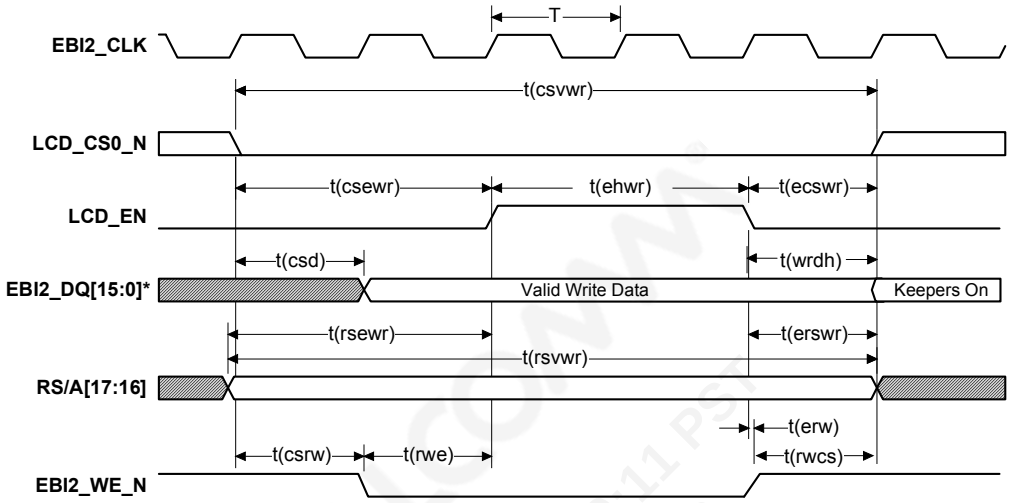


Figure 3-14 LCD interface write timing (with LCD_EN)

Table 3-16 LCD write timing (with LCD_EN)[1]

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(csvwr)	Chip-select active	(s+w+h)T-1	—	ns
t(rsvwr)	Address/RS valid	(r+c+s+w+h)T-5	—	ns
t(wrdh)	Write data hold	T-5	—	ns
t(csewr)	Chip-select active to LCD_E active	(e)T-5	—	ns
t(rsewr)	RS/address valid to LCD_E active	(c+e)T-5	—	ns
t(ehwr)	LCD_E active	(p)T-1	—	ns
t(csd)	Chip-select active to data valid	T-5	—	ns
t(ecswr)	LCD_E inactive to chip-select inactive	(s+w+h-e-p) T-5	—	ns
t(erswr)	LCD_E inactive to RS/address invalid	(s+w+h-e-p) T-5	—	ns
t(csrw)	Chip-select active to R/W low	T-5	—	ns
t(rwe)	WE_N low to LCD_E active	(e-s)T-5	—	ns
t(erw)	LCD_E inactive to R/W high	(s+w-e-p)T-5	—	ns

Table 3-16 LCD write timing (with LCD_EN)[1] (cont.)

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(rwcs)	R/W high to chip-select	-5	—	ns

1. T = EBI2_CLK = HCLK/2 cycle.
   c: ADDR_CS_SETUP = (EBI2_LCD_CFG0[29:25]+1) setup time from address to chip-select.
   s: CS_WR_RD_SETUP = (EBI2_LCD_CFG0[14:10]+1) chip-select to write/read setup time.
   w: WR_ACTIVE = (EBI2_LCD_CFG0[24:20]+1) write-enable signal assertion time.
   h: WR_CS_HOLD = (EBI2_LCD_CFG0[19:15]+1) write to chip-select hold time.
   p: WRENBL_ACTIVE = (EBI2_LCD_CFG1[9:5]+1) read enable assertion time.
   e: CS_WRENBL_SETUP = (EBI2_LCD_CFG1[4:0]+1) chip-select to the enable assertion during write.
   r: LCD_RECOV_CYCLES = (EBI2_LCD_CFG1[31:27]+1) LCD recovery cycles.

3.2.6.2.2 LCD interface read timing (with LCD_EN)

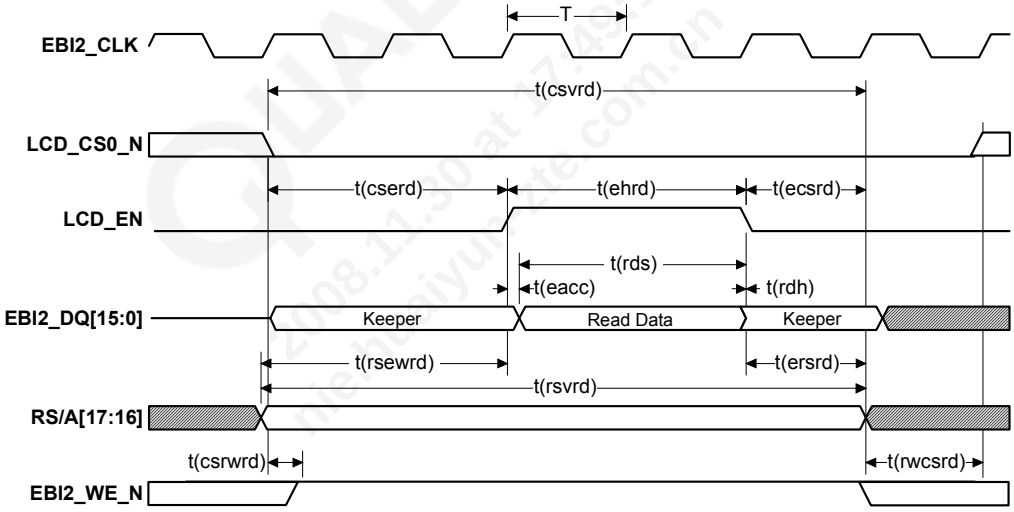


Figure 3-15 LCD interface read timing (with LCD_EN)

Table 3-17 LCD read timing (with LCD_EN)[1]

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(csvrd)	Chip-select active	(s+w+h)T-1	—	ns
t(rsvrd)	Address/RS valid	(c+r+s+w+h)T-5	—	ns
t(rds)	Read-data setup	20	—	ns
t(rdh)	Read-data hold	0	—	ns
t(cserd)	Chip-select active to LCD_E active	(e)T-5	—	ns
t(rserd)	RS/address valid to LCD_E active	(c+e)T-5	—	ns
t(ehrd)	LCD_E active	(p)T-1	—	ns

Table 3-17 LCD read timing (with LCD_EN)[1] (cont.)

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(ecsrd)	LCD_E inactive to chip-select inactive	-5	—	ns
t(ersrd)	LCD_E inactive to RS/address invalid	-5	—	ns
t(rwcsrd)	R/W high to chip-select active	-5	—	ns
t(csrwrd)	Chip-select inactive to R/W low	T-5	—	ns
t(eacc)	LCD_E access time	t(ehrd)-t(rds)-21	—	ns

1. T = EBI2_CLK = HCLK/2 cycle.
   c: ADDR_CS_SETUP = (EBI2_LCD_CFG0[29:25]+1) setup time from address to chip-select.
   s: CS_WR_RD_SETUP = (EBI2_LCD_CFG0[14:10]+1) chip-select to write/read setup time.
   w: RD_ACTIVE = (EBI2_LCD_CFG0[9:5]+1) write-enable signal assertion time.
   h: RD_CS_HOLD = (EBI2_LCD_CFG0[4:0]+1) write to chip-select hold time.
   p: RDENBL_ACTIVE = (EBI2_LCD_CFG1[21:16]+1) read enable assertion time.
   e: CS_RDENBL_SETUP = (EBI2_LCD_CFG1[15:11]+1) chip-select to the enable assertion during write.
   r: LCD_RECOV_CYCLES = (EBI2_LCD_CFG1[31:27]+1) LCD recovery cycles.

3.2.6.2.3 LCD interface write timing (without LCD_EN)

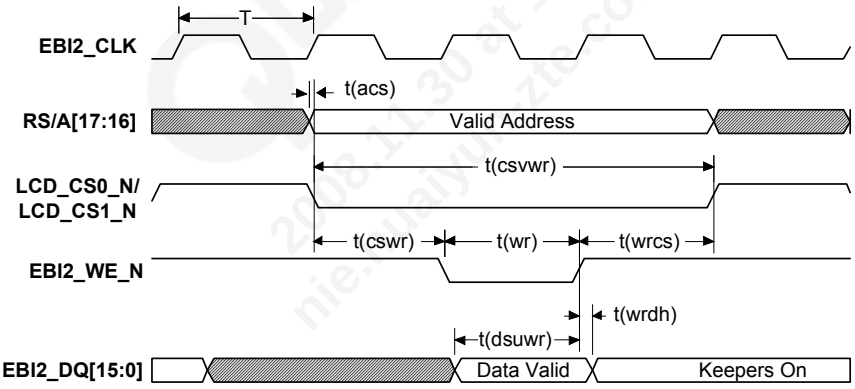


Figure 3-16 LCD interface write timing (without LCD_EN)

Table 3-18 LCD write (without LCD_EN)[1]

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(acs)	Address valid to chip-select active	(c+r)T-1	—	ns
t(csvwr)	Chip-select active	(s+w+h)T-1	—	ns
t(wrdh)	Write data hold	0	—	ns
t(cswr)	Chip-select active to write active	(s)T-5	—	ns
t(wr)	Write active	(w)T-1	—	ns
t(dsuwr)	Write data setup	(w)T-5	—	ns

Table 3-18 LCD write (without LCD_EN)[1] (cont.)

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(wrcs)	Write inactive to chip-select inactive	(h)T-5	—	ns

1. T = EBI2_CLK = HCLK/2 cycle.
   c: ADDR_CS_SETUP = (EBI2_LCD_CFG0[29:25]+1) setup time from address to chip-select.
   s: CS_WR_RD_SETUP = (EBI2_LCD_CFG0[14:10]+1) chip-select to write/read setup time.
   w: WR_ACTIVE = (EBI2_LCD_CFG0[24:20]+1) write-enable signal assertion time.
   h: WR_CS_HOLD = (EBI2_LCD_CFG0[19:15]+1) write to chip-select hold time.
   r: LCD_RECOV_CYCLES = (EBI2_LCD_CFG1[31:27]+1) LCD recovery cycles.

3.2.6.2.4 LCD interface read timing (without LCD_EN)

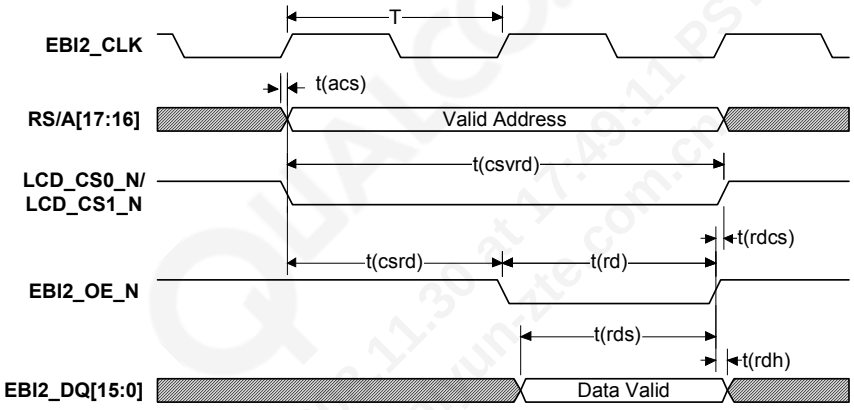


Figure 3-17 LCD interface read timing (without LCD_EN)

Table 3-19 LCD read (without LCD_EN)[1]

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(acs)	Address valid to chip-select active	(c+r)T-1	—	ns
t(csvrd)	Chip-select active	(s+w+h)T-1	—	ns
t(csrd)	Chip-select active to read active	(s)T-5	—	ns
t(rd)	Read active	(w)T-1	—	ns
t(rds)	Read-data setup	20	—	ns
t(rdh)	Read-data hold	0	—	ns

Table 3-19 LCD read (without LCD_EN)[1] (cont.)

Parameter	Description	VDD_P2 = 1.8/2.6 V		Unit
		Min	Max	
t(rdcs)	Read inactive to chip-select inactive	(h)T-2	—	ns

1. T = EBI2_CLK = HCLK/2 cycle.
   c: ADDR_CS_SETUP = (EBI2_LCD_CFG0[29:25]+1) setup time from address to chip-select.
   s: CS_WR_RD_SETUP = (EBI2_LCD_CFG0[14:10]+1) chip-select to write/read setup time.
   w: RD_ACTIVE = (EBI2_LCD_CFG0[9:5]+1) write-enable signal assertion time.
   h: RD_CS_HOLD = (EBI2_LCD_CFG0[4:0]+1) write to chip-select hold time.
   r: LCD_RECOV_CYCLES = (EBI2_LCD_CFG1[31:27]+1) LCD recovery cycles.

3.2.6.3 EBI2 NAND interface

The NAND flash memory is connected to EBI2_CS2_N (or EBI2_CS3_N for second NAND). The EBI2 arbiter for the MSM7x25 and later devices allow NAND memory access only when the sole request present is that of the NAND controller. In other words, the NAND controller has the lowest priority of all requests to EBI2, and it only gets the grant when all other requests are idle.

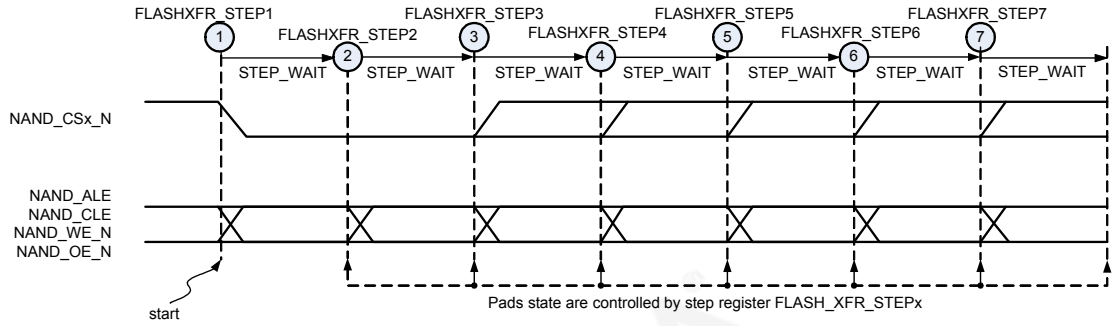
Each access to the NAND flash device involving the controller executes a sequence of signal assertion and de-assertion. The state-machine registers are designed to allow up to seven distinct configurations, including wait states.

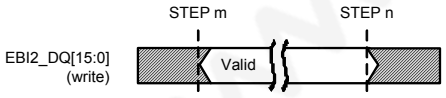
The register settings dictate the signal status once the state-machine is started. For example, CMD_CLE_EN (FLASH_XFR_STEPx[22]) values in the step controls the CLE pin state (1: high, 0: low). If the controller must send a multiple command sequence, it may not need to do all the steps. It can start from the beginning of the sequence and, after sending the command, it can loop back and send the next command without finishing the sequence.

FLASH_XFR_STEPx[31:30] – CMD_SEQ_STEP_NUMBER and FLASH_XFR_STEPx[15:14] – DATA_SEQ_STEP_NUMBER defines the step number in the command/data sequence:

00 => Simple step
01 => Loop start
10 => Loop end
11 => Last step

If a value of ‘11’ is programmed to the SEQ_STEP_NUMBER register, it indicates the step is the last step in the sequence and the controller will end the sequence after finishing the step. The timing parameters in Table 3-20 use 4-step configuration as an example. If the step configuration is changed, the timing parameters that mapped to the registers should be adjusted accordingly. In step configuration registers (FLASH_XFR_STEPx), the upper 16-bit [31:16] configures the NAND “Command” and “Address cycles,” whereas lower 16-bit [15:0] configures the “Data” read and write cycles behaviors.





FLASH_XFR_STEPx (x = 1 to 7)			
Command/Address		Data	
31:30	CMD_SEQ_SETP_NUM	15:14	DATA_SEQ_STEP_NUMBER
29:26	CMD_STEP1_WAIT	13:10	DATA_STEP1_WAIT
25	CMD_AOUT_EN*	9	DATA_AOUT_EN*
24	CMD_DATA_EN	8	DATA_DATA_EN
23	CMD_CE_EN	7	DATA_CE_EN
22	CMD_CLE_EN	6	DATA_CLE_EN
21	CMD_ALE_PIN	5	DATA_ALE_PIN
20	CMD_WE_EN	4	DATA_WE_EN
19	CMD_RE_EN	3	DATA_RE_EN
18	CMD_WIDE	2	DATA_WIDE
17:16	RESERVED*	1:0	EXTA_READ_WAIT

* Not used

Figure 3-18 NAND state machine registers

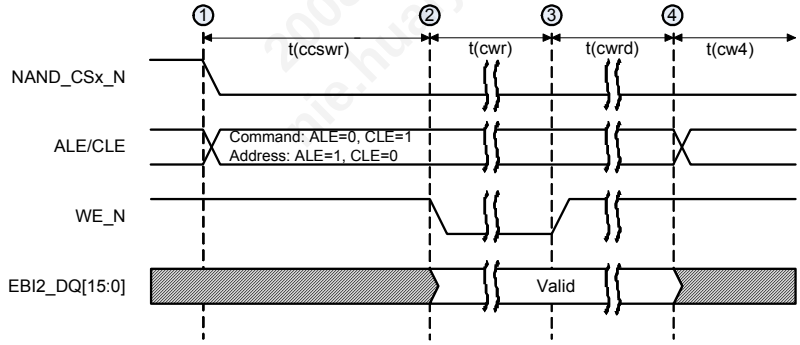


Figure 3-19 NAND command and address cycles

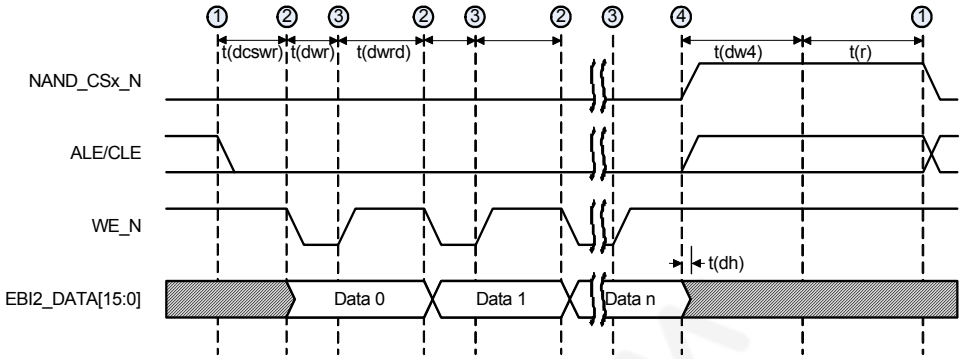


Figure 3-20 Data write

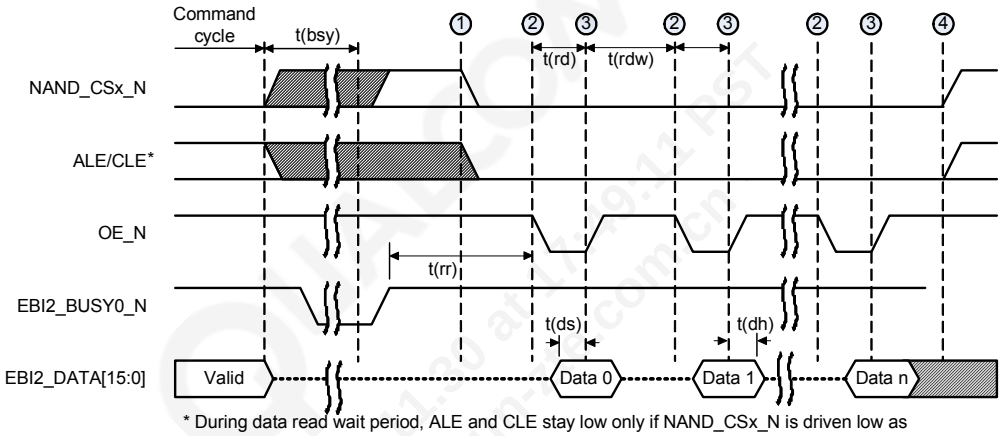


Figure 3-21 Data read

Table 3-20 NAND timing – AC characteristics

Symbol	Description	VDD=1.8/2.6 V		Unit
		Min	Max	
Command/address cycles				
t(ccswr)[1, 2]	Chip-select active to write active	(a)T-3	—	ns
t(cwr)[1, 2]	WE_N active time	(b)T-3	—	ns
t(cwrd)[1, 2]	Data hold time	(c)T-3	—	ns
t(cw4)[1, 2]	Wait cycle	(d)T-3	—	ns
Data cycles				
t(dcswr)[1, 2]	Chip-select active to write active	(e)T-3	—	ns
t(dwr)[1, 2]	WE_N active time	(f)T-3	—	ns
t(dwrd)[1, 2]	Write data hold time	(g)T-3	—	ns
t(dw4)[1, 2]	Wait cycle	(h)T-3	—	ns
t(r)[1, 2]	Recovery cycles	(i)T-3	—	ns
t(rr)[1, 2]	Busy to read delay	3T	—	ns

Table 3-20 NAND timing – AC characteristics (cont.)

Symbol	Description	VDD=1.8/2.6 V		Unit
		Min	Max	
t(rd)[1, 2]	OE_N active time	(k)T-3	—	ns
t(rdw)[1, 2]	Read wait cycle	(m)T-3	—	ns
t(bsy)[1, 2]	Busy detect delay	(n)T-3	—	ns
t(ds)	Read-data setup time	20	—	ns
t(dh)	Read-data hold time	0	—	ns

1. The following applies to all NAND timing parameters:
   T = Peripheral CLK cycle (20 to 66 MHz), timing parameters are based on a 4-step configurations, FLASH_XFR_STEP1 to FLASH_XFR_STEP4.
2. **a:** FLASH_XFR_STEP1[29:26]+1
   b: FLASH_XFR_STEP2[29:26]+1
   c: FLASH_XFR_STEP3[29:26]+1
   d: FLASH_XFR_STEP4[29:26]+1
   e: FLASH_XFR_STEP1[13:10]+1
   f/k: FLASH_XFR_STEP2[13:10]+1
   g: FLASH_XFR_STEP3[13:10]+1
   h: FLASH_XFR_STEP4[13:10]+1
   i: NAND_DEVn_CFG1[4:2]+1
   n: {NAND_DEVn_CFG[22:17]+1} x 2
   m: FLASH_XFR_STEP3[13:10]+FLASH_XFR_STEP3[1:0]+1

3.2.6.4 EBI2 OneNAND synchronous memory interface

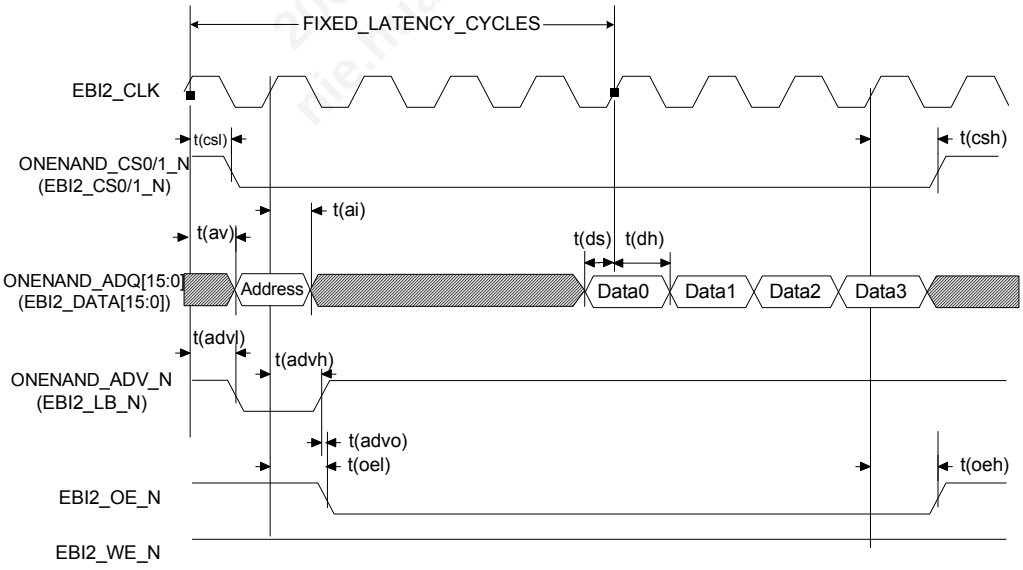


Figure 3-22 OneNAND synchronous memory read timing diagram, 16-bit

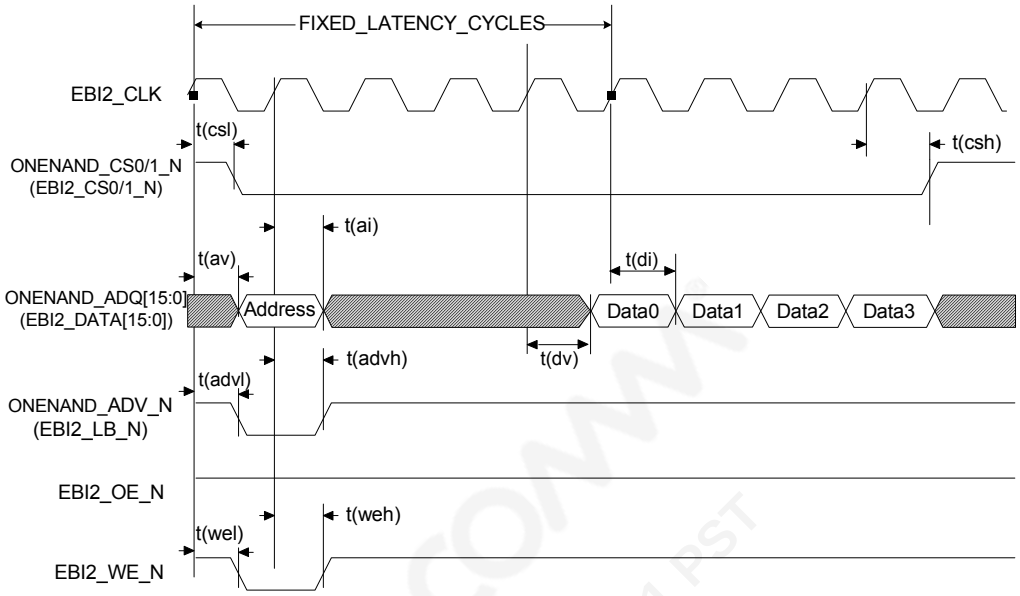


Figure 3-23 OneNAND synchronous memory write timing diagram, 16-bit

Table 3-21 OneNAND synchronous memory controller timing

Symbol	Description	Min	Max	Unit
t(av)[1, 2]	Clock to address valid	–	(T/4)+5.7	ns
t(ai)[1, 2]	Clock to address invalid	(T/4)-0.9	–	ns
t(csl)[1, 2]	Clock to chip-select low	–	(T/4)+5.7	ns
t(csh)[1, 2]	Clock to chip-select high	(T/4)-0.9	–	ns
t(advl)[1, 2]	Clock to ADV# low	–	(T/4)+5.7	ns
t(advh)[1, 2]	Clock to ADV# high	(T/4)-0.9	–	ns
Read cycle				
t(oel)[1]	Clock to OE# low	–	(T/4)+5.7	ns
t(oeh)[1]	Clock to OE# high	(T/4)-0.9	–	ns
t(ds)[3]	Read data setup time	3	–	ns
t(dh)[3]	Read data hold time	2.5	–	ns
t(advo)[1]	ADV high to OE low	0	–	ns
Write cycle				
t(dv)[1]	Clock to data valid	–	(T/4)+5.7	ns
t(di)[1]	Clock to data invalid	(T/4)-0.9	–	ns
t(wel)[1]	Clock to write enable low	–	(T/4)+5.7	ns
t(weh)[1]	Clock to write enable high	(T/4)-0.9	–	ns

1. This parameter is an MSM device output driving an external device input.
2. This parameter is common to both read and write.
3. This parameter is an external device output driving an MSM device input.

3.2.7 Auxiliary interfaces

3.2.7.1 CAMIF

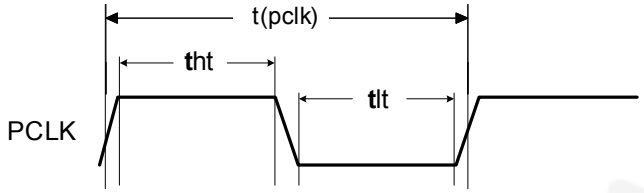


Figure 3-24 CAMIF CLK timing

Table 3-22 CAMIF CLK timing

Symbol	Description	Min	Max	Units
t(pclk)	CAMIF PCLK clock period	10.42		ns
tht	CAMIF PCLK minimum high time	3.65		ns
Tlt	CAMIF PCLK minimum low time	3.65		ns

Note: CAMIF PCLK maximum frequency is limited to 96 MHz.

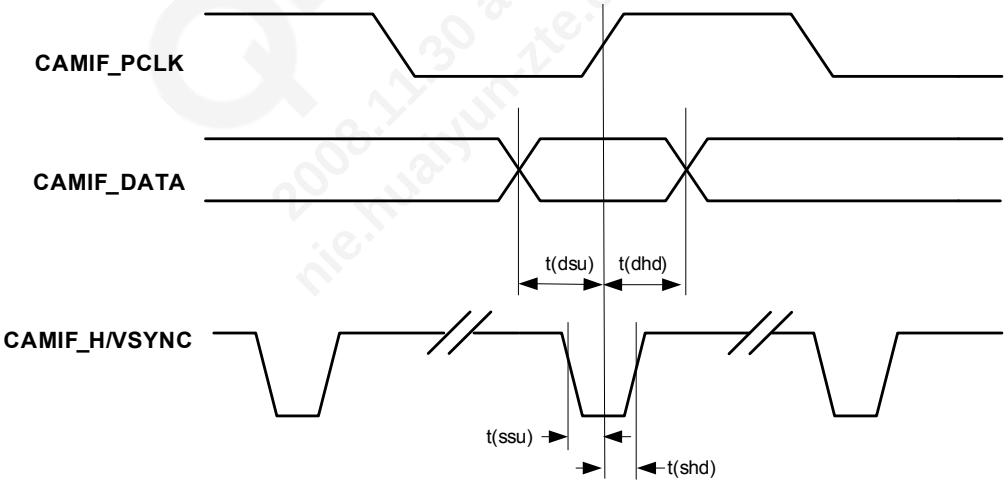


Figure 3-25 CAMIF signals

Table 3-23 CAMIF signals

Symbol	Description	Min	Max	Units
t(dsu)	CAMIF DATA signal setup time	2.5		ns
t(dhd)	CAMIF DATA signal hold time	2.5		ns
t(ssu)	CAMIF V/HSYNCH signal setup time	2.5		ns
t(shd)	CAMIF V/HSYNCH signal hold time	2.5		ns

3.2.7.2 JTAG

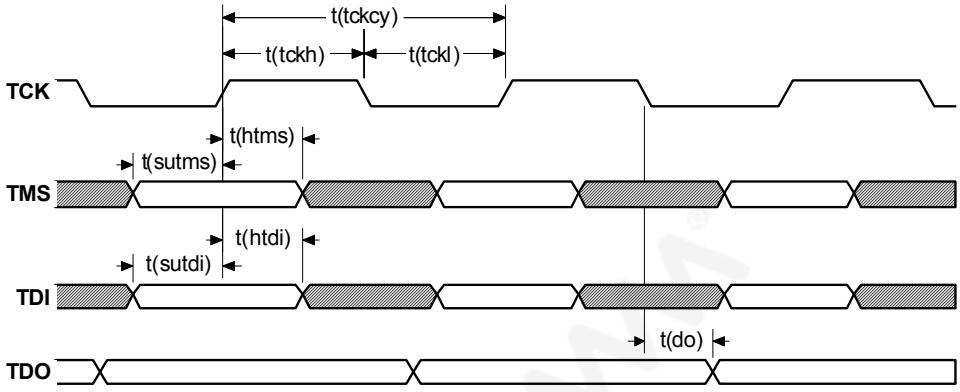


Figure 3-26 JTAG interface timing

Table 3-24 JTAG interface timing

Parameter	Description	Min	Typical	Max	Units
t(tckcy)	TCK period t	100			ns
t(tckh)	TCK pulse width high	40			ns
t(tckl)	TCK pulse width low	40			ns
t(sutms)	TMS input setup time	25			ns
t(htms)	TMS input hold time	25			ns
t(sutdi)	TDI input setup time	25			ns
t(htdi)	TDI input hold time	25			ns
t(do)	TDO data output delay			70	ns

3.2.7.3 Secure digital (SD) card interface

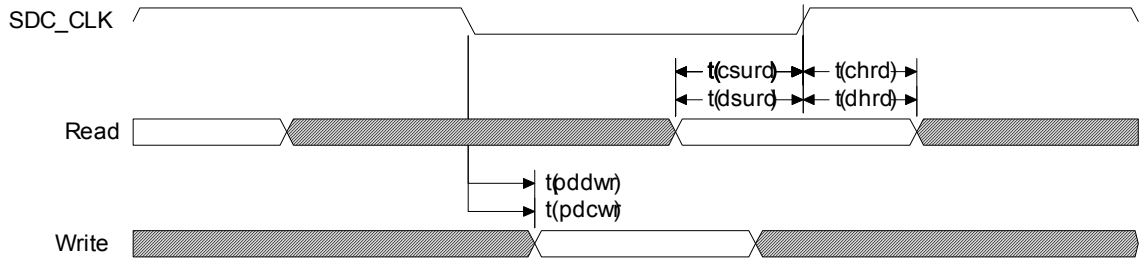


Figure 3-27 SD card interface timing

Table 3-25 SD card interface timing

Parameter	Description	Min	Max	Units
T(chrd)	Command hold	2.5		ns
T(csurd)	Command setup	4		ns
T(dhrd)	Data hold	2.5		ns
T(dsurd)	Data setup	4		ns
T(pddwr)	Propagation delay on data write	-2.5	2.5	ns
T(pdcwr)	Propagation delay on command write	-2.5	2.5	ns

3.2.7.4 LCD controller

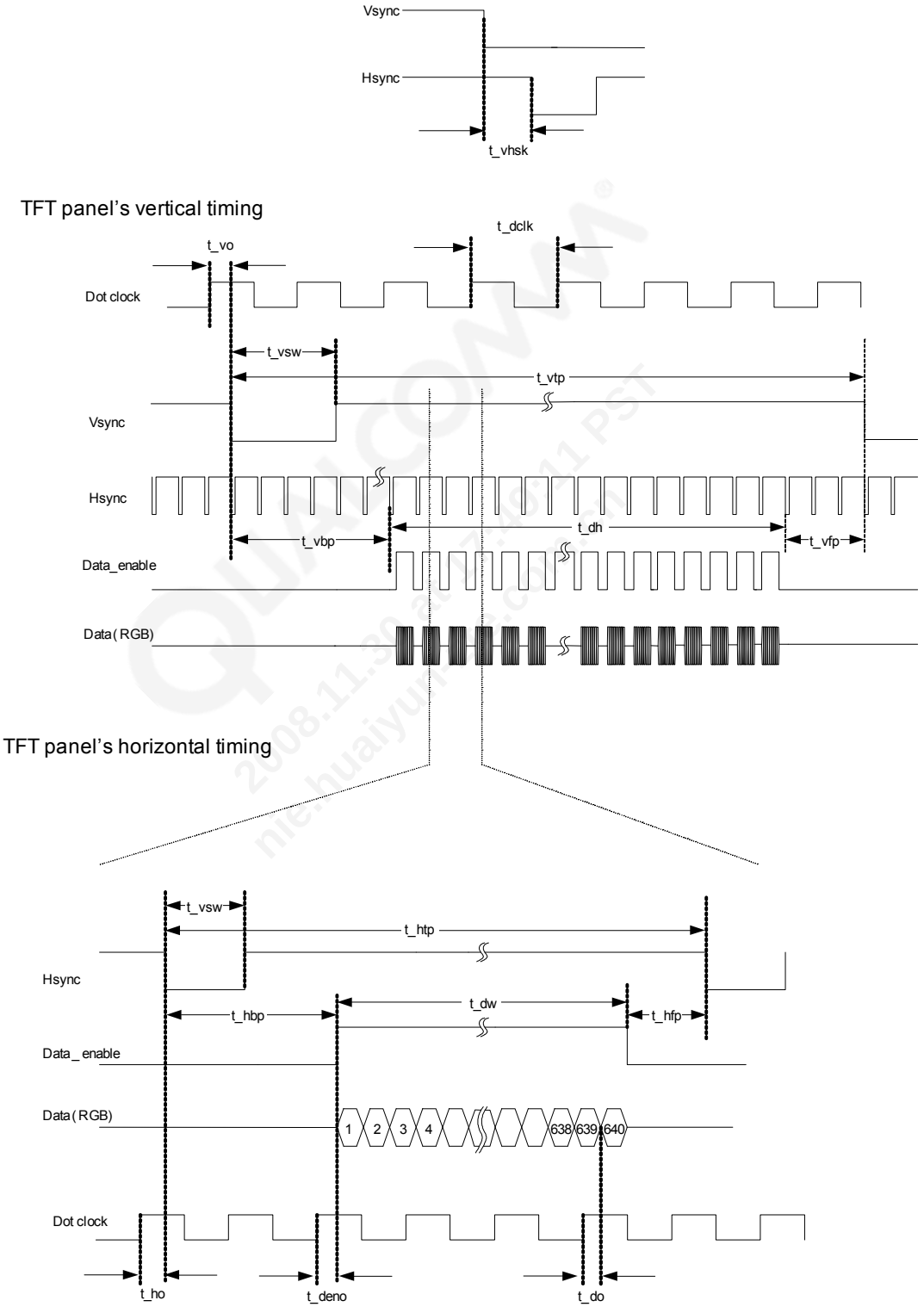


Figure 3-28 LCD controller timing

Table 3-26 LCD controller interface timing

Parameter	Description	Min	Typical	Max	Units	Notes
t(dclk)	Dot clock period	20.8		200	ns	
t(vsw)	Vertical sync pulse width	1		$2^{24}-1$	dclk	
t(vtp)	Vertical sync time period	1		$2^{24}-1$	dclk	
t(vbp)	Vertical back porch	1		$2^{24}-1$	dclk	
t(vfp)	Vertical front porch	1		$2^{24}-1$	dclk	
t(hsw)	Horizontal sync pulse width	1		4095	dclk	
t(htp)	Horizontal sync time period	1		4095	dclk	
t(hfp)	Horizontal sync front porch	1		4095	dclk	
t(hbp)	Horizontal sync back porch	1		4095	dclk	
t(adw)	Active display width	1		480	pixels	1
t(adh)	Active display height	1		480	lines	1
t(vo)	VSYNC output delay (relative to DCLK launching edge)	0.5		1.5	ns	4
t(ho)	HSYNC output delay (relative to DCLK launching edge)	0.5		1.5	ns	4
t(deno)	Date enable output delay (relative to DCLK launching edge)	0.2		1.1	ns	4
t(do)	DATA output delay (relative to DCLK launching edge)	1.1		3.0	ns	2, 4
t(vhsk)	Skew between active VSYNC and HSYNC edges	0		4095	dclk	3

Notes:

1. MSM7625 supports up to WQVGA (480 x 272) display resolution through its RGB interface. Both portrait and landscape mode can be accommodated.
2. The t(do) parameter also indicates when it is safe to sample data. Unless otherwise indicated, it should be assumed the valid window starts at this time and lasts until the next launching DCLK edge.
3. The t(vhsk) parameter shown in this table is basically the same as the HSYNC_SKEW setting programmed into the MDP_LCDC_HSYNC_SKEW register. A more accurate calculation of t(vhsk) will take into account the t(vo) and t(ho) parameters. More specifically, the following formula should be used: t(ho)-t(vo)+[(1/DCLK)*HSYNC_SKEW], where the resulting answer is in ns.
4. Setup/hold window target is a maximum of PCLK_CYCLE/2 - 2.5 ns.
5. While the timing data in the table reflects a certain polarity and DCLK launching edge, it is essentially representative of the reverse polarity and/or opposite launching edge as well.

3.3 Mixed-signal characteristics

3.3.1 HKADC specifications

Table 3-27 HKADC performance specifications

Specification	Min	Typ	Max	Units	Comments/conditions
Resolution		8		Bits	
Differential nonlinearity (DNL)	-0.75		+0.75	LSB	V_{DD_A} = ADC reference 300 kHz – 1.2 MHz sample rate
Integral nonlinearity (INL)	-1.5		+1.5	LSB	
Gain error	-2.5		+2.5	%	
Offset error	-3		+3	LSB	
Channel isolation		50			At DC
Full-scale input range	GND		V_{RT}		V_{RT} is variable 0 V to V_{DD_A}
3 dB input bandwidth		2500			Source resistance = 50 Ω
Input serial resistance			1	kΩ	Sample and hold switch resistance
Input capacitance		12		pF	
Power-down to wakeup			5	µs	
Throughput rate	40.98	67.56		kHz	

Notes:
1. For an acquisition time of three clock periods, the CLK period>2•τ, τ=2•(input resistance+source resistance)•input capacitance.
2. Values in this table are projected and are subject to change without notice.

3.3.2 Touchscreen ADC specifications

Table 3-28 Recommended ADC operating conditions

Parameter	Min	Nom	Max	Unit
Supply voltage V_{DD}	2.5	2.6	2.7	V
Touchscreen panel resistance	200		1000	Ω
Touchscreen panel capacitance	0.1		10	nF

Table 3-29 Touchscreen ADC performance specifications

Requirements	conditions	Min	Typ	Max	Unit
Resolution	1 LSB=2.6 V/4096=0.6 mV (typ)			12	LSB
Differential non-linearity (DNL)	Monotonic between ground and V_{DD} Throughput rate = 150 kHz	-2		+2	LSB
Integral non-linearity (INL)	Monotonic between ground and V_{DD} Throughput rate = 150 kHz	-9		+9	LSB
Gain error		-19		+19	LSB
Offset error		-13		+13	LSB
Channel Isolation			70		dB
Switch drivers: Sp1, Sp2, Sp3, Sn1, Sn2, Sn3	On-resistance		7		Ω

Notes:
1. These specifications are applicable to all five inputs (TS_UL, TS_UR, TS_LR, TS_LL, and wiper).
2. These specifications are applicable to both single-ended and differential modes.
3. Clock mode: div8 (clock = 19.2 MHz).

3.3.3 PCM interface

The MSM7625 PCM interface can be used in two modes:

- The default mode is its auxiliary PCM that runs at 128 kHz and uses a 62.5-µs sync pulse (half a time frame).
- The second mode is its primary PCM that runs at 2.048 MHz and uses 488 ns sync pulse (one 2.048-MHz clock tick).

The default PCM interface on power-up is the auxiliary PCM interface. Under PCM, the data is output on the rising edge of pcm_clk and sampled at the falling edge of pcm_clk. This is true, regardless of the clock source (MSM or external device) and regardless of the data source (MSM or external device).

Both the PCM interface modes, auxiliary and primary, use the same MSM pins. The PCM pin assignments are listed in Table 3-30.

Table 3-30 Pin assignments for the PCM interface

GPIO	Pin #	AUX_PCM functionality	Primary PCM interface functionality
GPIO_70	AD1	AUX_PCM_SYNC	PCM_SYNC
GPIO_71	AD2	AUX_PCM_CLK	PCM_CLK
GPIO_69	AA4	AUX_PCM_DIN	PCM_DIN
GPIO_68	AA5	AUX_PCM_DOUT	PCM_DOUT

3.3.3.1 Primary PCM interface

The aux codec port also supports 2.048-MHz PCM data and sync timing for linear, μ-law, and A-law codecs that match the sync timing — this is called the primary PCM interface (or PCM interface).

The primary PCM codec port operates with a 2.048-MHz clock. The PRIM_PCM_SYNC runs at 8 kHz with a 50% duty cycle.

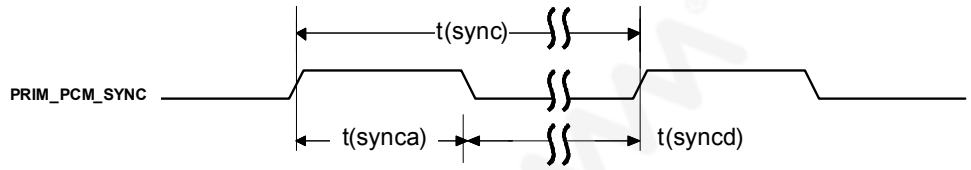


Figure 3-29 PRIM_PCM_SYNC timing

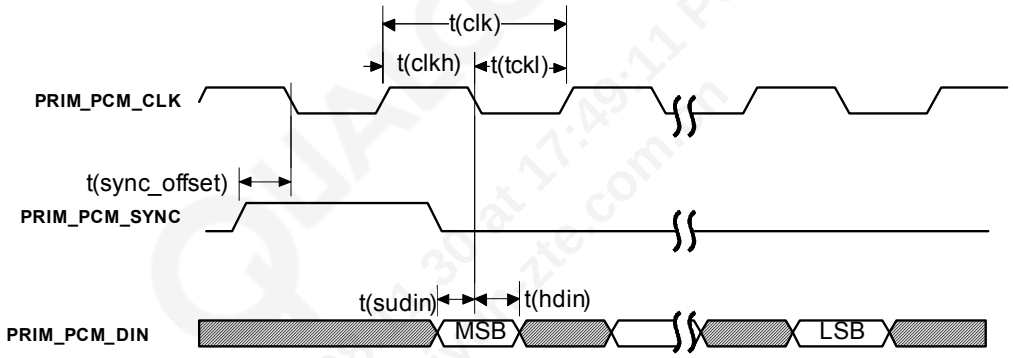


Figure 3-30 PRIM_PCM_CODEC to MSM7625 timing

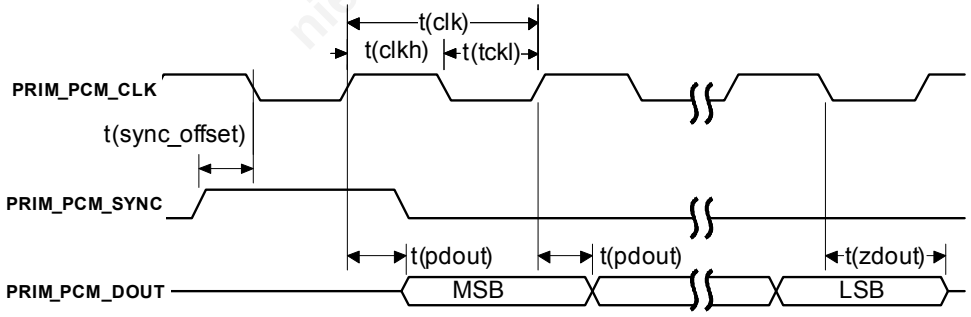


Figure 3-31 MSM7625 to PRIM_PCM_CODEC timing

Table 3-31 PRIM_PCM_CODEC timing parameters

Parameter	Description	Min	Typical	Max	Units	Notes
t(sync)	PCM_SYNC cycle time (PCM_SYNC_DIR = 1)		125		μs	
	PCM_SYNC cycle time (PCM_SYNC_DIR = 0)		125		μs	
t(synca)	PCM_SYNC asserted time (PCM_SYNC_DIR = 1)		488		ns	2
	PCM_SYNC asserted time (PCM_SYNC_DIR = 0)				ns	

Table 3-31 PRIM_PCM_CODEC timing parameters (cont.)

Parameter	Description	Min	Typical	Max	Units	Notes
t(syncd)	PCM_SYNC de-asserted time (PCM_SYNC_DIR =1)		124.5		µs	3
	PCM_SYNC de-asserted time (PCM_SYNC_DIR = 0)				µs	
t(clk)	PCM_CLK cycle time (PCM_CLK_DIR = 1)		488		ns	4
	PCM_CLK cycle time (PCM_CLK_DIR = 0)				ns	
t(clkh)	PCM_CLK high time (PCM_CLK_DIR = 1)		244		ns	1, 5
	PCM_CLK high time (PCM_CLK_DIR = 0)				ns	
t(clkl)	PCM_CLK low time (PCM_CLK_DIR = 1)		244		ns	1, 5
	PCM_CLK low time (PCM_CLK_DIR = 0)				ns	
t(sync_offset)	PCM_SYNC offset time to PCM_CLK falling		122		ns	6
	(PCM_SYNC_DIR = 1, PCM_CLK_DIR = 1)					
	PCM_SYNC offset time to PCM_CLK falling				ns	
	(PCM_SYNC_DIR = 0, PCM_CLK_DIR = 0)					
t(sudin)	PCM_DIN setup time to PCM_CLK falling	60			ns	
t(hdin)	PCM_DIN hold time after PCM_CLK falling	60			ns	
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid			60	ns	
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z	5		60	ns	

Notes:
1. t(clkh) and t(clkl) are independent of PCM_CLK_SENSE.
2. One t(clk) period.
3. PCM_SYNC cycle time minus one t(clk) period.
4. t(clk) = 1/(2.048 MHz).
5. PCM_CLK high or low time = t(clk)/2 ± 10 ns.
6. PCM_SYNC offset time = t(clk)/4.

3.3.3.2 Auxiliary PCM interface

The auxiliary PCM interface enables communication with an external codec to support hands-free applications. Linear, µ-law, and A-law codecs are supported by the auxiliary PCM interface.

The auxiliary codec port operates with standard long-sync timing and a 128-kHz clock. The AUX_PCM_SYNC runs at 8 kHz with a 50% duty cycle. Most µ-law and A-law codecs support the 128-kHz AUX_PCM_CLK bit clock.

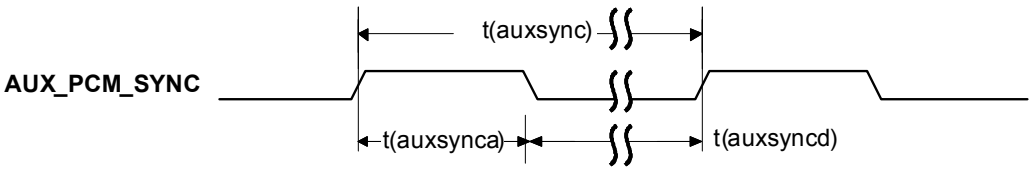


Figure 3-32 AUX_PCM_SYNC timing

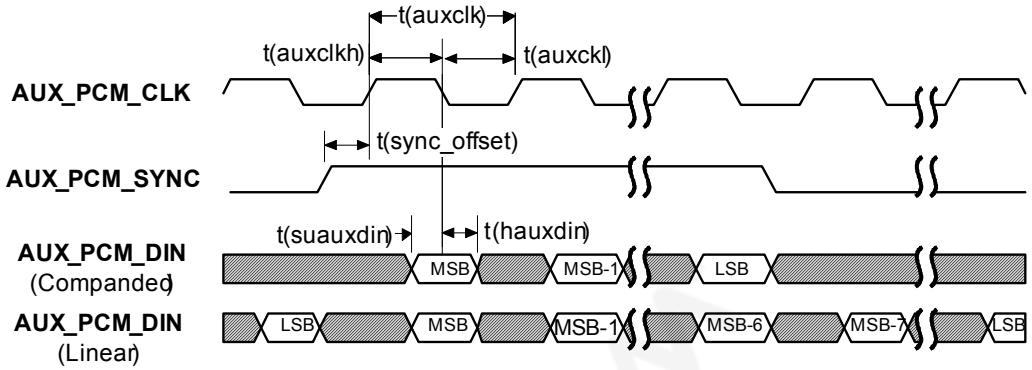


Figure 3-33 AUX_PCM_CODEC to MSM7625 timing

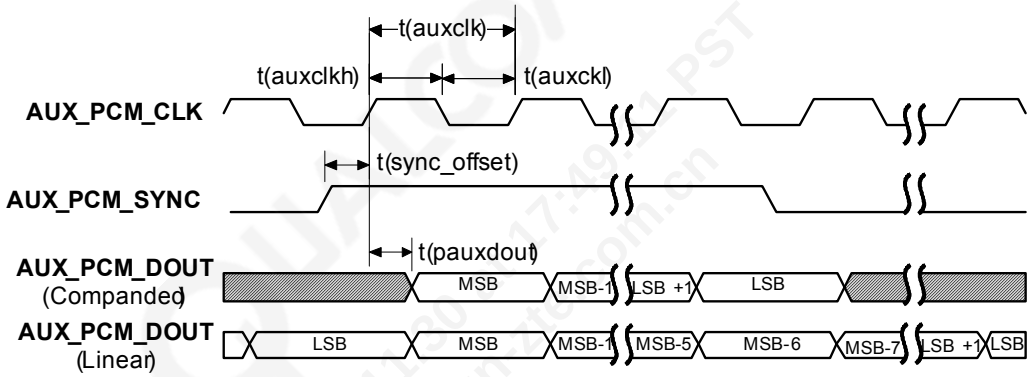


Figure 3-34 MSM7625 to AUX_PCM_CODEC timing

Table 3-32 AUX_CODEC timing parameters

Parameter	Description	Min	Typical	Max	Units	Notes
t(auxsync)	AUX_PCM_SYNC cycle time		125		µs	
t(auxsynca)	AUX_PCM_SYNC asserted time		62.5		µs	1
t(auxsyncd)	AUX_PCM_SYNC de-asserted time		62.5		µs	1
t(auxclk)	AUX_PCM_CLK cycle time		7.8		µs	2
t(auxclkh)	AUX_PCM_CLK high time		3.9		µs	3
t(auxclkl)	AUX_PCM_CLK low time		3.9		µs	3
t(sync_offset)	AUX_PCM _SYNC offset time to AUX_PCM_CLK rising		1.95		µs	4
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling	60			ns	
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling	60			ns	

Table 3-32 AUX_CODEC timing parameters (cont.)

Parameter	Description	Min	Typical	Max	Units	Notes
t(pauxdout)	Propagation delay from AUX_PCM_CLK AUX_PCM_DOUT valid			60	ns	

Notes:
1. t(auxsync)/2 ± 10 ns.
2. t(auxclk) = 1/(128 kHz).
3. t(auxclk)/2 ± 10 ns.
4. t(auxclk)/4 ± 10 ns.

3.3.4 I²S/stereo DAC interface specification

The I²S bus provides a serial link specifically for digital audio. The bus only handles audio data, while the other signals, such as subcoding and control, are transferred separately. Since the transmitter and the receiver have the same clock signal for data transmission, the transmitter, as the master, has to generate the bit clock, word select (L_R_N) signal, and data.

Table 3-33 Pin assignment for I²S interface

GPIO	Pin #	SDAC functionality	SADC functionality
GPIO_70	AD1	SDAC_L_R_N	SADC_L_R_N
GPIO_71	AD2	SDAC_CLK	SADC_CLK
GPIO_69	AA4	SDAC_MCLK	SADC_MCLK
GPIO_68	AA5	SDAC_DOUT	SADC_DIN

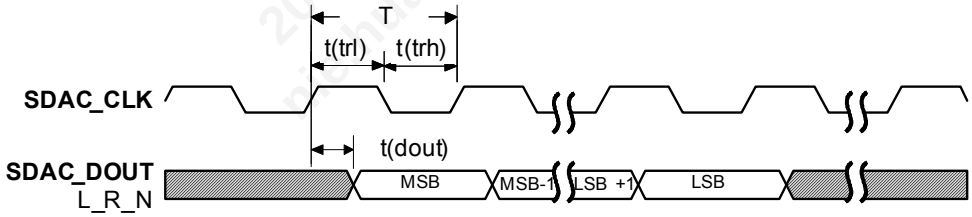


Figure 3-35 Clock timing for transmitter mode (stereo DAC)

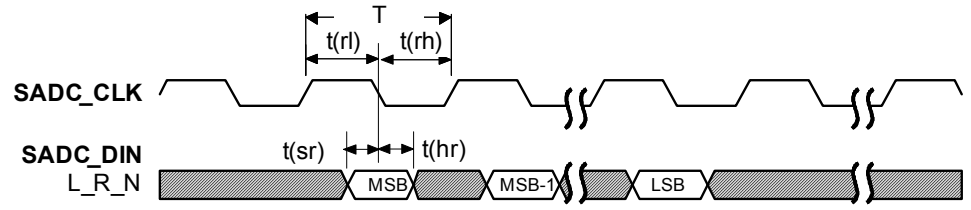


Figure 3-36 Clock timing for receiver mode (stereo ADC)

Table 3-34 I²S timing parameters

Symbol	Parameter	Min	Typ	Max	Units
Transmitter mode					
T	One clock period		1/(SDAC_CLK)		ns
t(trh)	SDAC_CLK logic high		((1/SDAC_CLK)/2)±10		ns
t(trl)	SDAC_CLK logic low		((1/SDAC_CLK)/2)±10		ns
t(dout)	Delay from SCLK rising to data valid			60	ns
Receiver mode					
t(rh)	SDAC_CLK logic high	35		65	%
t(rl)	SDAC_CLK logic low	35		65	%
t(sr)	DATA setup time to SCLK falling	60			ns
t(hr)	DATA hold time after SCLK falling	60			ns

Note: SDAC_CLK = 1.024 MHz, 1.4112 MHz, or 1.536 MHz.

3.3.5 Codec specifications

Table 3-35 Recommended operating conditions

Parameter	Min	Nom	Max	Unit
Supply voltage, AV_{DD}, DV_{DD}, $HPHV_{DD,}$ $EARV_{DD,}$	2.5	2.6	2.7	V
Load impedance between EAR1OP and EAR1ON	25.6	32		Ω
Load impedance between HPH_L and HPH_VREF/AVSS, HPH_R and HPH_VREF/AVSS	12	16		Ω
Load impedance between LINE_ON and LINE_OP (differential mode)		600		Ω
Load impedance between Line_Out_L and AV_{SS}, Line_Out_R and AV_{SS}		600		Ω
Load impedance between AUXOUT and AVss		600		Ω

Notes:
1. Voltages at analog inputs, outputs and V_{DD} are with respect to AV_{SS}.
2. Supply current is measured one channel at a time.

Table 3-36 Electrical characteristics versus supply voltage and free-air temperature

Parameter		Test conditions	Min	Typ	Max	Unit
I_{dd}	Supply current from V_{DD}	Operating, EAR1_AMP selected (13-bit mode), Tx enabled, 8 kHz			13	mA
I_{dd}	Supply current from V_{DD}	Operating, HPH_L AMP selected (13-bit mode), Tx enabled, 8 kHz			13.36	mA
I_{dd}	Supply current from V_{DD}	Operating, LINE_AMP selected, (13-bit mode), differential output, Tx enabled, 8 kHz			11.68	mA
I_{dd}	Supply current from V_{DD}	Operating, AUX_AMP selected, (13-bit mode), Tx enabled, 8 kHz			11.18	mA

Table 3-36 Electrical characteristics versus supply voltage and free-air temperature (cont.)

Parameter		Test conditions	Min	Typ	Max	Unit
I_{dd}	Supply current from V_{DD}	Operating, HPH_L AMP selected (16-bit mode), Tx enabled, 16 kHz			16.56	mA
I_{dd}	Supply current from V_{DD}	Operating, HPH_L AMP selected (16-bit mode), Tx enabled, 48 kHz			25.16	mA
I_{dd}	Supply current from V_{DD}	Operating, HPH_R AMP selected (16-bit mode), Tx enabled, 16 kHz			16.56	mA
I_{dd}	Supply current from V_{DD}	Operating, HPH_R AMP selected (16-bit mode), Tx enabled, 48 kHz			25.16	mA
I_{dd}	Supply current from V_{DD}	Operating, LINE_AMP selected, single-ended Line_Out_L, (16-bit mode), Tx enabled, 16 kHz			15.18	mA
I_{dd}	Supply current from V_{DD}	Operating, LINE_AMP selected, single-ended Line_Out_R, (16-bit mode), Tx enabled, 48 kHz			22.88	mA
I_{dd}	Supply current from V_{DD}	Operating, AUX_AMP selected (16-bit mode), Tx enabled, 16 kHz			15.18	mA
I_{dd}	Supply current from V_{DD}	Powerdown mode			10	μA
t_{pu}	Powerup time from powerdown	Turn on Rx and Tx paths, all outputs selected			60	ms

Notes:
1. PCMI = “0000000000000” for 13-bit mode, PCMI = “0000000000000000” for 16-bit mode and 0 Vrms analog input.
2. Supply current is measured one channel at a time.

Table 3-37 Microphone interface requirements

Parameter		Test conditions	Min	Typ	Max	Unit
V_{IO}	Input offset voltage at MIC1, MIC2, AUX and Line_in inputs	Over recommended ranges of supply voltage and free-air temperature	-5		+5	mV
C_I	Input capacitance at MIC1, MIC2, AUXI and Line_In inputs	At each pin of all inputs		5		pF
	Input DC common mode voltage		1.13	1.25	1.38	V
V_{mbias}	Microphone bias supply voltage	Open circuit DC voltage	1.69	1.8	1.91	V
	MBIAS output DC source current	1.69-kΩ 1% resistive load	1	1.07		mA
	MICMUTE attenuation	+3 dBm0 analog input level 1.02-kHz sine wave	80			dB
Z_{in1}	Input impedance, MIC1, MIC2, AUXI and Line_in inputs	Fully differential, A/D path	16	20	24	KΩ
THD_v	Total harmonic distortion + Noise (voice)	All inputs, AV_{DD}= 2.5 V, 13-bit mode, analog input at 229 mVpp, 498-Hz sine wave			1.78	%
THD_v	Total harmonic distortion + Noise (audio)	All inputs, AV_{DD}= 2.5 V, 16-bit mode, analog input at 229 mVpp, 498-Hz sine wave		0.05	0.1	%

Table 3-38 Speaker interface requirements

Parameter		Test conditions	Min	Typ	Max	Unit
P_{O1}	EAR1_AMP output power (rms)	Differential, 32-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave		70		mW
P_{O2}	HPH_L AMP output power (rms)	Single-ended, 16-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave		21.6		mW
P_{O3}	HPH_R AMP output power (rms)	Single-ended, 16-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave		21.6		mW
P_{O4}	LINE_AMP output power (rms)	Differential, 600-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave		2.30		mW
P_{O5}	LINE_AMP output power (rms)	Single-ended, 600-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave (Line_Out_L, Line_Out_R)		0.58		mW
P_{O6}	AUX_AMP output power (rms)	Single-ended, 600-Ω load, PCMI = +3 dBm0, 1.02-kHz sine wave		0.58		mW
	Output DC offset voltage between EAR1OP and EAR1ON, Line_op and Line_On	Fully differential	-20		20	mV
	Output common mode voltage, EAR1OP, EAR1ON, AUXO, HPH_L, HPH_R, HPH_VREF Line_Out_L and Line_Out_R	Measured at each output pin with respect to AVSS: Vdd = 2.5 V to 2.7 V	1.13	1.25	1.38	V
Z_{OUT1}	Differential output impedance	At 1.02 kHz, for outputs EAR1 and LINE_AMP			1	Ω
Z_{OUT2}	Single-ended output impedance	At 1.02 kHz, for output EAR2, EAR3 and LINE_AMP and AUX_AMP			0.5	Ω
Z_{OUT3}	Single-ended output impedance	At 1.02 kHz, for output HPH_VREF			0.2	Ω
C_{L1}	Load capacitance: EAR1_amp	For differential outputs of EAR1_amp (Figure 3-37)			500	pF
C_{L1}	Load capacitance: Line _amp	For differential outputs of Line_amp (Figure 3-37)			500	pF
C_{L2}	Load capacitance: Line_amp	For single-ended outputs between each pin of Line_amp and AV_{SS} (Figure 3-37)			1000	pF
C_{L3}	Load capacitance: HPH_L and HPH_R amps	For outputs HPH_L/HPH_R single-ended (Figure 3-38)			1000	pF
C_{L4}	Load capacitance: HPH_L/HPH_R amps	For outputs HPH_L/HPH_R, differential (Figure 3-39)			500	pF
C_{L5}	Load capacitance: AUX_amp	For single ended output of AUX_amp (Figure 3-40)			500	pF
THD_v	Total harmonic distortion + noise (voice)	AV_{DD}= 2.5 V, 13-bit mode, PCMI = +3 dBm0, 498-Hz sine wave, 32-Ω load for EAR1_amp, 16-Ω load for HPH_L and HPH_R amps, 600-Ω load for differential outputs of Line_amp and AUX_amp.			4	%

Table 3-38 Speaker interface requirements (cont.)

Parameter		Test conditions	Min	Typ	Max	Unit
THD_a	Total harmonic distortion + Noise (audio)	AV_{DD}= 2.5 V, 16-bit mode, PCMI = +3 dBm0, 1.02-kHz and 5-kHz sine waves, 16-Ω load for HPH_L and HPH_R amps, 600-Ω load for single-ended line outputs.		0.05	0.1	%
	Channel attenuation	PCMI = +3 dBm0, 1.02-kHz sine wave	70			dB

Notes:
1. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
2. CODECRXGAIN = 0 dB.

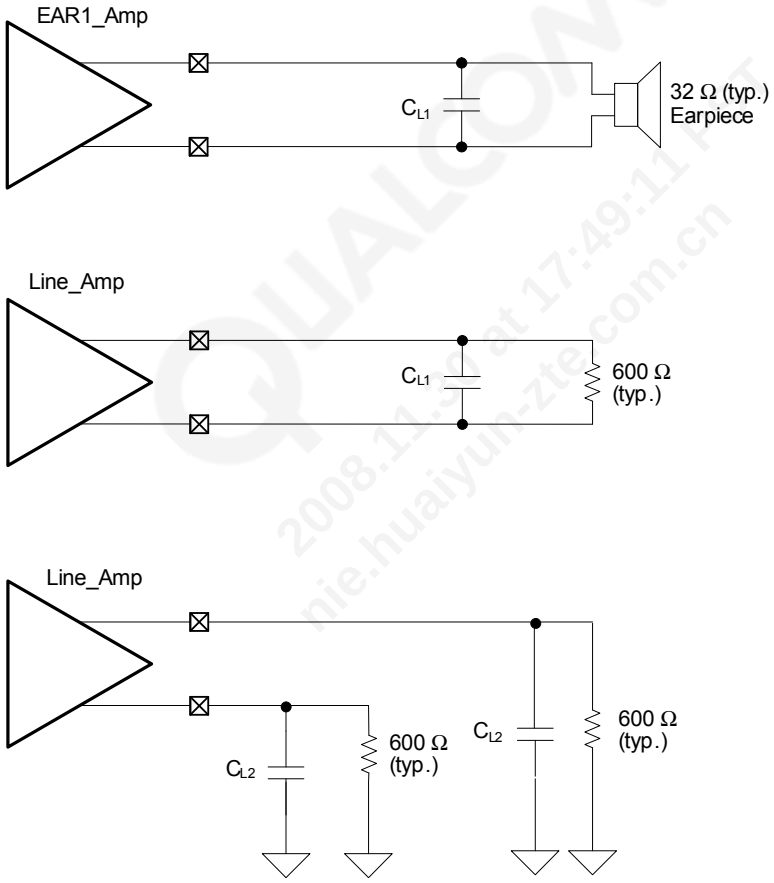


Figure 3-37 Load capacitance CL1 and CL2

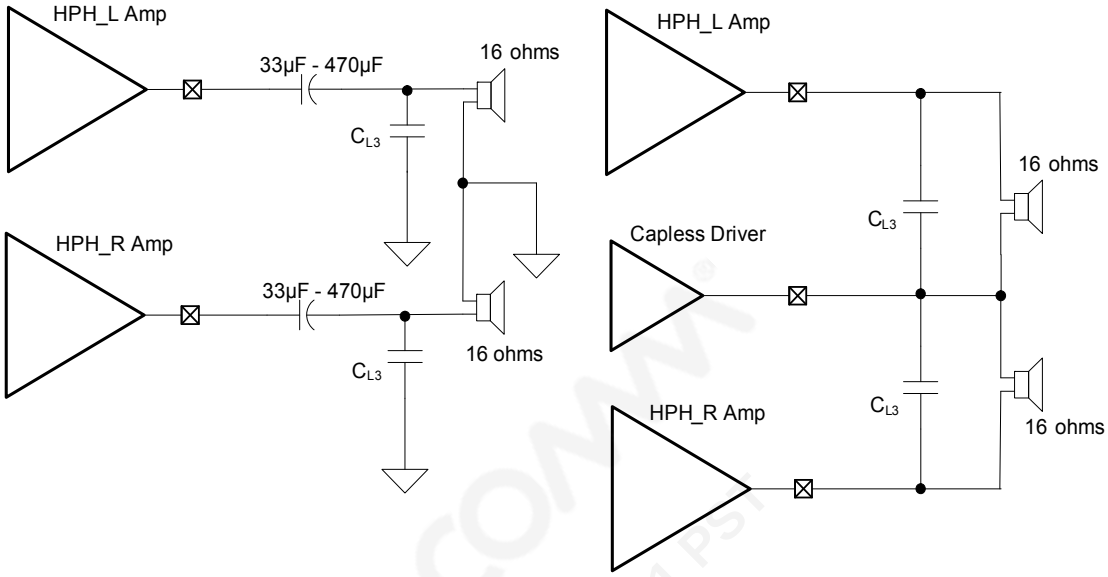


Figure 3-38 Load capacitance CL3, single-ended output

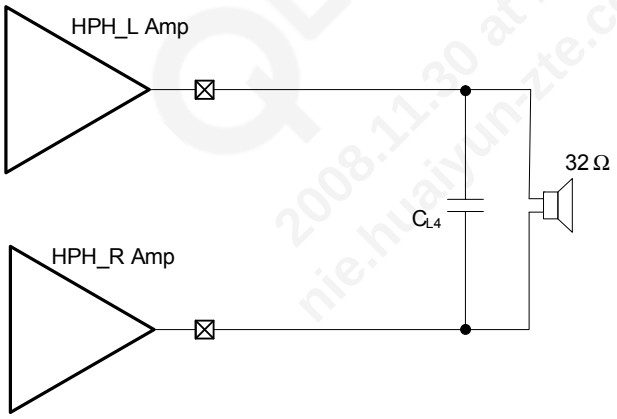


Figure 3-39 Load capacitance CL4, differential output

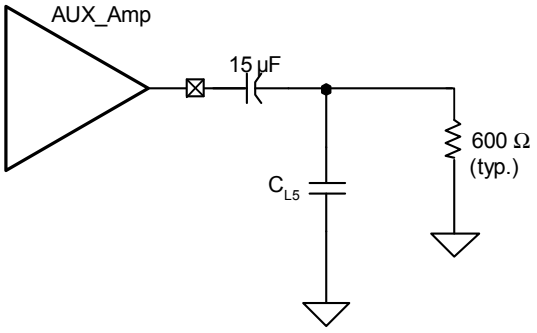


Figure 3-40 Load capacitance CL5

Table 3-39 Transmit voice path level translation and linearity, differential input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit reference-signal level (0 dBm0)	Differential analog input		57.3		mV_{rms}
Overload-signal level (+3 dBm0)	Differential analog input		229		mV_{pp}
Absolute gain error [1]	-10 dBm0 analog input level, 1.02-kHz sine wave	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from +3 dBm0 to -30 dBm0	-0.5		0.5	dB
Gain error relative to gain at -10 dBm0	Analog input level from -31 dBm0 to -45 dBm0	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from -46 dBm0 to -55 dBm0	-1.2		1.2	dB

Notes:
1. This specification must be applicable to all microphone amplifier gain settings (i.e., MIC_AMP1 is set to 0 dB and +24 dB; MIC_AMP2 is set to +25.5 dB to -6 dB with 1.5-dB steps).
2. These specifications apply to all inputs MIC1, MIC2, AUX and Line_In.
3. The total transmit channel gain in this default configuration is +24 dB (microphone amplifier 1 is set to +24 dB, and microphone amplifier 2 is set to 0 dB).
4. Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-40 Tx voice path response & image rejection, digital Tx slope filter disabled (8 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, digital Tx high pass filter disabled.	Frequency < 0.0125xFs Hz	-0.5		0.5	dB
	Frequency = 0.025xFs Hz	-0.5		0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0	dB
	Frequency = 0.4975xFs Hz			-14	dB
	Frequency = 0.575xFs Hz			-35	dB
	Frequency = 0.9975xFs Hz			-47	dB
Gain relative to input signal gain at 1.02 kHz, digital Tx high pass filter enabled.	Frequency < 0.0125xFs Hz			-15	dB
	Frequency = 0.025xFs Hz			-5	dB

Notes:
1. The Tx path input level is -10 dBm0.
2. Frequencies 0.575xFs Hz and 0.9975xFs Hz are used to determine image rejection performance.
3. Fs = sampling rate: 8 kHz.

Table 3-41 Transmit voice path anti-aliasing image rejection, differential input (8 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit image rejection at 2.048 MHz (256 x Fs)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 gain = 0 dB. Analog input level 229 mVpp at 2.047 MHz	30	60		dB

Notes:
1. Specifications must be met for left and right channels.
2. Select MIC1 differential input
3. 13-bit mode; Fs = sampling rate: 8 kHz.

Table 3-42 Tx voice path response & image rejection, digital Tx slope filter disabled (16 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz; digital Tx high-pass filter disabled.	Frequency < 0.0125xFs Hz	-0.5		0.5	dB
	Frequency = 0.025xFs Hz	-0.5		0.5	dB
	Frequency = 0.0375xFs Hz — 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0	dB
	Frequency = 0.4975xFs Hz			-25	dB
	Frequency = 0.575xFs Hz			-50	dB
	Frequency = 0.9975xFs Hz			-60	dB
Gain relative to input signal gain at 1.02 kHz; digital Tx high pass filter enabled.	Frequency < 0.00625xFs Hz			-15	dB
	Frequency = 0.0125xFs Hz			-3	dB

Notes:
1. The Tx path input level is -10 dBm0.
2. Frequencies 0.575xFs Hz and 0.9975xFs Hz are used to determine image rejection performance.
3. Fs = sampling rate: 16 kHz.

Table 3-43 Transmit voice path anti-aliasing image rejection, differential input (16 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit image rejection at 4.096 MHz (256 × Fs)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 gain = 0 dB. Analog input level 229 mVpp at 4.095 MHz	30	60		dB

Notes:
1. Specifications must be met for left and right channels.
2. Select MIC1 differential input.
3. 13-bit mode; Fs = sampling rate: 16 kHz.

Table 3-44 Tx voice path response & image rejection, digital Tx slope filter enabled

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, with slope filter selected; digital Tx high-pass filter enabled.	Frequency = 0.0125xFs Hz			-27	dB
	Frequency = 0.025xFs Hz			-8	dB
	Frequency = 0.03125xFs Hz			-4	dB
	Frequency = 0.0375xFs Hz		-1.80		dB
	Frequency = 0.05xFs Hz		-1.50		dB
	Frequency = 0.0625xFs Hz		-1.30		dB
	Frequency = 0.075xFs Hz		-1.1		dB
	Frequency = 0.0875xFs Hz		-0.8		dB
	Frequency = 0.1xFs Hz		-0.57		dB
	Frequency = 0.1125xFs Hz		-0.25		dB
	Frequency = 0.1275xFs Hz		0		dB
	Frequency = 0.1875xFs Hz		1.8		dB
	Frequency = 0.2475xFs Hz		4.0		dB
	Frequency = 0.3125xFs Hz		6.5		dB
	Frequency = 0.375xFs Hz		7.6		dB
	Frequency = 0.3875xFs Hz		7.7		dB
	Frequency = 0.4125xFs Hz		8.0		dB
	Frequency = 0.4375xFs Hz		6.48		dB
	Frequency = 0.4975xFs Hz			-13	dB
	Frequency = 0.5625xFs Hz			-35	dB
	Frequency = 0.625xFs Hz			-45	dB
	Frequency = 0.9975xFs Hz			-50	dB

Notes:
1. The passband tolerance is ± 0.25 dB from 300 Hz to 3500 Hz.
2. The Tx path input level is -10 dBm0.
3. Frequencies 0.5625xFs, 0.625xFs, and 0.9975xFs Hz are used to determine image rejection performance.
4. Fs = sampling rate: 8 kHz.

Table 3-45 Transmit voice path idle channel noise and distortion (8 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit noise (input refer noise)	CODECTXGAIN gain = 0 dB, MIC_AMP1 = +24 dB, MIC_AMP2 = 0 dB		10	15	μVrms
Transmit signal-to-THD+N ratio with 1020-Hz sine wave input	Analog input level at +3 dBm0	35			dB
	Analog input level at 0 dBm0	50			dB
	Analog input level at -5 dBm0	50			dB
	Analog input level at -10 dBm0	46			dB
	Analog input level at -20 dBm0	45			dB
	Analog input level at -30 dBm0	40			dB
	Analog input level at -40 dBm0	30			dB
	Analog input level at -45 dBm0	25			dB

Notes:
1. Specifications must be met with and without Tx slope filter enabled.
2. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
3. C-message weighted for 8-K sampling rate.
4. Fs = sampling rate: 8 kHz.
5. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-46 Transmit voice path idle channel noise and distortion (16 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit noise (input refer noise)	CODECTXGAIN gain = 0 dB, MIC_AMP1 = +24 dB, MIC_AMP2 = 0 dB			18	μVrms
Transmit signal-to-THD+N ratio with 1020-Hz sine wave input	Analog input level at +3 dBm0	35			dB
	Analog input level at 0 dBm0	50			dB
	Analog input level at -5 dBm0	50			dB
	Analog input level at -10 dBm0	46			dB
	Analog input level at -20 dBm0	45			dB
	Analog input level at -30 dBm0	40			dB
	Analog input level at -40 dBm0	30			dB
	Analog input level at -45 dBm0	25			dB

Notes:
1. Specifications must be met with Tx slope filter disabled.
2. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
3. A-weighted for 16 K sampling rate.
4. Fs = sampling rate: 16 kHz.
5. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-47 Transmit audio path level translation and linearity, differential input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit reference-signal level (0 dBm0)	Differential analog input		908		mV_{rms}
Overload-signal level (+3 dBm0)	Differential analog input		3.626		V_{pp}
Absolute gain error [1]	-10 dBm0 analog input level, 1.02-kHz sine wave	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from +3 dBm0 to -30 dBm0	-0.5		0.5	dB
Gain error relative to gain at -10 dBm0	Analog input level from -31 dBm0 to -45 dBm0	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from -46 dBm0 to -55 dBm0	-1.2		1.2	dB

Notes:
1. This spec must be applicable to all microphone amplifier gain settings (i.e., MIC_AMP1 is set to 0 dB and +24 dB; MIC_AMP2 is set to +25.5 dB to -6 dB with a 1.5 dB step).
2. These specifications apply to all inputs MIC1, MIC2, AUX, and Line_In.
3. These specifications are applicable to left and right channel selection.
4. The total transmit channel gain in this default configuration is 0 dB (microphone amplifier 1 and amplifier 2 are set to 0 dB).
5. 16-bit mode.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-48 Transmit audio path level translation and linearity, single-ended input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit reference-signal level (0 dBm0)	Single-ended analog input		540		mV_{rms}
Overload-signal level (+3 dBm0)	Single-ended analog input		2.155		V_{pp}
Absolute gain error [1]	0 dBm0 analog input level, 1.02-kHz sine wave	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from +3 dBm0 to -30 dBm0	-0.5		0.5	dB
Gain error relative to gain at -10 dBm0	Analog input level from -31 dBm0 to -45 dBm0	-1		1	dB
Gain error relative to gain at -10 dBm0	Analog input level from -46 dBm0 to -55 dBm0	-1.2		1.2	dB

Notes:
1. This specification must be applicable to all microphone amplifier gain settings (i.e., MIC_AMP1 is set to 0 dB and +24 dB; MIC_AMP2 is set to +25.5 dB to -6 dB with a 1.5 dB step).
2. These specifications apply to Aux_In and Line_In.
3. These specifications are applicable to left- and right-channel selection.
4. The total transmit channel gain in this default configuration is +4.5 dB (microphone amplifier 1 is set to 0 dB, and amplifier 2 is set to +4.5 dB).
5. 16-bit mode.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-49 Transmit audio path anti-aliasing image rejection, differential input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit image rejection at 12.288 MHz (256 x Fs)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 gain = 0 dB. Analog input level 3.626 Vpp at 12.2887 MHz.	96	100		dB
Transmit image rejection at 6.144 MHz (128 x Fs)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 gain = 0 dB. Analog input level 3.626 Vpp at 6.143 MHz.	69	76		dB
Transmit image rejection at 3.072 MHz (64 x Fs)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 gain = 0 dB. Analog input level 3.626 Vpp at 3.071 MHz.	48	55		dB

Notes:
1. Specifications must be met for left and right channels.
2. Select MIC1 differential input.
3. 16-bit mode; Fs = sampling rate: 48 kHz.

Table 3-50 Transmit audio path frequency response and image rejection

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz; digital Tx high-pass filter disabled.	Frequency < 0.0125xFs Hz	-0.5		0.5	dB
	Frequency = 0.025xFs Hz	-0.5		0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0	dB
	Frequency = 0.4975xFs Hz			-14	dB
	Frequency = 0.575xFs Hz			-35	dB
	Frequency = 0.9975xFs Hz			-47	dB

Notes:
1. The Tx path input level is -10 dBm0.
2. Frequencies 0.4975xFs, 0.575xFs Hz, and 0.9975xFs Hz are used to determine image rejection performance.
3. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-51 Transmit audio path idle channel noise & distortion, left channel selected, differential input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit input refer noise (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Analog in is gnd.		36	51	µVrms
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input +3 dBm0.		-66	-60	dB
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 24 dB. Input -57 dBm0.		-24	-21	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-31	-28	dB
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = bypassed, microphone amp 2 = 24 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = bypassed. Input -57 dBm0.		-28	-25	dB

Notes:
1. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
2. A-weighted; 16-bit mode.
3. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
4. Refer to Figure 3-41 for analog input ground connection.
5. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-52 Transmit audio path idle channel noise & distortion, left channel selected, single-ended input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit input refer noise (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Analog in is gnd.		36	51	µVrms
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = +4.5 dB. Input +3 dBm0.		-66	-60	dB
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 24 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-31	-28	dB

Table 3-52 notes:
1. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
2. A-weighted; 16-bit mode.
3. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
4. Refer to Figure 3-41 for analog input ground connection.

Table 3-53 Transmit audio path idle channel noise & distortion, right channel selected, differential input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit input refer noise (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Analog input is grounded.		36	51	μVrms
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input +3 dBm0.		-66	-60	dB
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 24 dB. Input -57 dBm0.		-24	-21	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-31	-28	dB
Total harmonic distortion + Noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = bypassed, microphone amp 2 = 24 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = bypassed. Input -57 dBm0.		-28	-25	dB

Notes:
1. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
2. A-weighted.
3. 16-bit mode.
4. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
5. Refer to Figure 3-41 for analog input ground connection.
6. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-54 Transmit audio path idle channel noise & distortion, right channel selected, single-ended input

Parameter	Test conditions	Min	Typ	Max	Unit
Transmit input refer noise (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Analog input is grounded.		36	51	μVrms
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = +4.5 dB. Input +3 dBm0.		-66	-60	dB
Total harmonic distortion + noise (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 24 dB. Input -57 dBm0.		-28	-25	dB

Table 3-54 Transmit audio path idle channel noise & distortion, right channel selected, single-ended input (cont.)

Parameter	Test conditions	Min	Typ	Max	Unit
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 24 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-28	-25	dB
Total harmonic distortion + (THD+N) with 1020-Hz sine wave input (A-weighted)	Microphone amplifier 1 gain = 0 dB, microphone amp 2 = 0 dB. Input -57 dBm0.		-31	-28	dB

Notes:
1. Specifications must be met for all inputs MIC1, MIC2, AUX, and Line_In.
2. A-weighted.
3. 16-bit mode.
4. Fs = sampling rate:11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
5. Refer to Figure 3-41 for analog input ground connection.

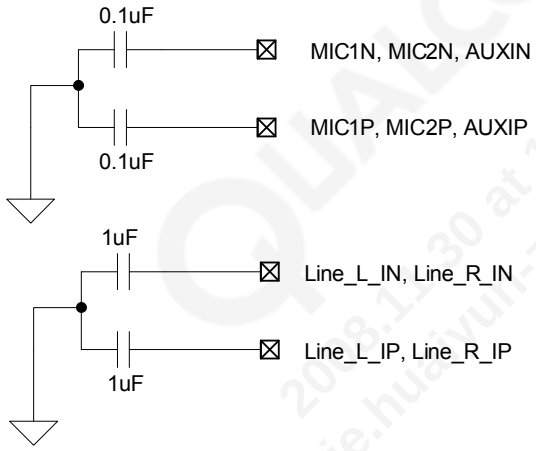


Figure 3-41 Tx analog input ground connection

Table 3-55 Receive voice path level translation and linearity, EAR1_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		1.06		V_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		4.24		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially between EAR1ON and EAR1OP.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Loaded condition (32 Ω).
5. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-56 Rx voice path level translation & linearity, HPH_L AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a 16-Ω load connected between HPH_R and HPH_REF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_L and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-57 Rx voice path level translation & linearity, HPH_R AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with 16-Ω load connected between HPH_R and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_R and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-58 Rx voice path level translation & linearity, HPH_L AMP & HPH_R AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		833		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		3.33		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB

Table 3-58 Rx voice path level translation & linearity, HPH_L AMP & HPH_R AMP selected, differential (cont.)

Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Table 3-58 notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially with a 32-Ω load connected between HPH_L and HPH_R.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-59 Rx voice path level translation & linearity, LINE_AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		833		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		3.33		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially between LINE_OP and LINE_ON.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave; loaded condition (600 Ω).
4. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-60 Receive voice path level translation and linearity, AUX_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended between AUXO and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave; loaded condition (600 Ω).
4. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.

Table 3-61 Receive voice path frequency response and image rejection (8 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz; digital Rx high-pass filter disabled.	Frequency < 0.0125xFs Hz	-0.5		0.5	dB
	Frequency = 0.025xFs Hz	-0.5		0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0	dB
	Frequency = 0.4975xFs Hz			-14	dB
	Frequency = 0.575xFs Hz			-40	dB
	Frequency = 0.9975xFs Hz			-50	dB
Gain relative to input signal gain at 1.02 kHz; digital Rx high-pass filter enabled.	Frequency < 0.0125xFs Hz			-15	dB
	Frequency = 0.025xFs Hz			-5	dB

Notes
1. CODECRXGAIN = 0 dB.
2. The Rx path input level is -10 dBm0.
3. This specification applies to EAR1_AMP, HPH_L AMP, HPH_R AMP, LINE_AMP, and AUX_AMP outputs.
4. Loaded condition.
5. Frequencies 0.4975xFs, 0.575xFs Hz, and 0.9975xFs Hz are used to determine image rejection performance.
6. 13-bit mode; Fs = sampling rate: 8 kHz.

Table 3-62 Receive voice path frequency response and image rejection (16 K)

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz; digital Rx high pass filter disabled.	Frequency < 0.0125xFs Hz	-0.5		0.5	dB
	Frequency = 0.025xFs Hz	-0.5		0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0.5	dB
	Frequency = 0.4975xFs Hz			-25	dB
	Frequency = 0.575xFs Hz			-50	dB
	Frequency = 0.875xFs Hz			-70	dB
Gain relative to input signal gain at 1.02 kHz; digital Rx high pass filter enabled.	Frequency < 0.00625xFs Hz			-15	dB
	Frequency = 0.0125xFs Hz			-3	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. The Rx path input level is -10 dBm0.
3. This specification applies to EAR1_AMP, HPH_L AMP, HPH_R AMP, LINE_AMP, and AUX_AMP outputs.
4. Loaded condition.
5. Frequencies 0.4975xFs Hz, 0.575xFs Hz, and 0.9975xFs Hz are used to determine image rejection performance.
6. 13-bit mode; Fs = sampling rate: 16 kHz.

Table 3-63 Receive voice path idle channel noise and distortion, EAR1_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMIN = “0000000000000”		124	150	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine wave input	PCMI = +3 dBm0	29			dB
	PCMI = 0 dBm0	50			dB
	PCMI = -5 dBm0	47			dB
	PCMI = -10 dBm0	46			dB
	PCMI = -20 dBm0	42			dB
	PCMI = -30 dBm0	40			dB
	PCMI = -40 dBm0	30			dB
	PCMI = -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to a 0-dBm0 sine wave	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially between EAR1ON and EAR1OP.
3. +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Loaded condition (32 Ω).
5. 13-bit mode.
6. A-weighted.
7. Fs = sampling rate: 8 kHz or 16 kHz.
8. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-64 Rx voice path idle channel noise & distortion, HPH_L AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000”			106	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine wave input	Output level at +3 dBm0	26			dB
	Output level at 0 dBm0	45			dB
	Output level at -5 dBm0	44			dB
	Output level at -10 dBm0	42			dB
	Output level at -20 dBm0	39			dB
	Output level at -30 dBm0	37			dB
	Output level at -40 dBm0	27			dB
	Output level at -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to a 0-dBm0 sine wave.	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with 16-Ω load connected between HPH_L and HPH_VREF.

3. Output also measured single-ended with a series combination of a (450 µF) DC-blocking capacitor and 16-Ω load connected between HPH_L and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.
6. A-weighted; measurement bandwidth = 100 Hz to 20 kHz.

Table 3-65 Receive voice path idle channel noise & distortion, HPH_R AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000”			106	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine-wave input	Output level at +3 dBm0	26			dB
	Output level at 0 dBm0	45			dB
	Output level at -5 dBm0	44			dB
	Output level at -10 dBm0	42			dB
	Output level at -20 dBm0	39			dB
	Output level at -30 dBm0	37			dB
	Output level at -40 dBm0	27			dB
	Output level at -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to a 0-dBm0 sine wave.	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with 16-Ω load connected between HPH_R and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and 16-Ω load connected between HPH_R and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 13-bit mode; Fs = sampling rate: 8 kHz or 16 kHz.
6. A-weighted; measurement bandwidth = 100 Hz to 20 kHz.

Table 3-66 Rx voice path idle channel noise & distortion, HPH_L AMP & HPH_R AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000”			150	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine wave input	Output level at +3 dBm0	29			dB
	Output level at 0 dBm0	50			dB
	Output level at -5 dBm0	47			dB
	Output level at -10 dBm0	46			dB
	Output level at -20 dBm0	42			dB
	Output level at -30 dBm0	40			dB
	Output level at -40 dBm0	30			dB
	Output level at -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to a 0-dBm0 sine wave	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially with 32-Ω load connected between HPH_L and HPH_R.
3. The +3-dBm0 level corresponds a 0-dB full-scale sine wave.
4. 13-bit mode.
5. A-weighted.
6. Fs = sampling rate: 8 kHz or 16 kHz.
7. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-67 Rx voice path idle channel noise & distortion, LINE_AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMIN = “0000000000000000”			150	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine-wave input	PCMI = +3 dBm0	29			dB
	PCMI = 0 dBm0	50			dB
	PCMI = -5 dBm0	47			dB
	PCMI = -10 dBm0	46			dB
	PCMI = -20 dBm0	42			dB
	PCMI = -30 dBm0	40			dB
	PCMI = -40 dBm0	30			dB
	PCMI = -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to a 0-dBm0 sine wave.	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially between LINE_OP and LINE_ON.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 13-bit mode.

6. A-weighted.
7. Fs = sampling rate: 8 kHz or 16 kHz.
8. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-68 Receive voice path idle channel noise and distortion, AUX_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMIN = “0000000000000000”			106	μV_{rms}
Receive signal-to-THD+N ratio with 1020-Hz sine wave input	PCMI = +3 dBm0	26			dB
	PCMI = 0 dBm0	45			dB
	PCMI = -5 dBm0	44			dB
	PCMI = -10 dBm0	42			dB
	PCMI = -20 dBm0	39			dB
	PCMI = -30 dBm0	37			dB
	PCMI = -40 dBm0	27			dB
	PCMI = -45 dBm0	25			dB
Intermodulation distortion (two-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones; composite peak level equivalent to 0-dBm0 sine wave.	50			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended between AUXOUT and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 13-bit mode.
6. A-weighted.
7. Fs = sampling rate: 8 kHz or 16 kHz.
8. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-69 Receive audio path level translation and linearity, HPH_L AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a 16-Ω load connected between HPH_L and HPH_VREF.
3. Output measured single-ended with a series combination of a (450 µF) DC blocking capacitor and 16-Ω load connected between HPH_L and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 16-bit mode.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-70 Receive audio path level translation and linearity, HPH_R AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a 16-Ω load connected between HPH_R and HPH_VREF.
3. Output measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_R and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 16-bit mode.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-71 Rx audio path level translation & linearity, HPH_L AMP & HPH_R AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		833		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		3.33		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially with a 32-Ω load connected between HPH_L and HPH_R.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. 16-bit mode.
5. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-72 Rx audio path level translation & linearity, LINE_AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		833		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		3.33		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-Hz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB

Table 3-72 Rx audio path level translation & linearity, LINE_AMP selected, differential (cont.)

Parameter	Test conditions	Min	Typ	Max	Unit
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB; 16-bit mode.
2. Output measured differentially with a 600-Ω load connected between LINE_OP and LINE_ON.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-73 Rx audio path level translation & linearity, LINE_AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB; 16-bit mode.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between LINE_OUT_L and AVSS, and between LINE_OUT_R and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-74 Receive audio path level translation and linearity, AUX_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02-kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02-kHz sine wave		1.664		V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02-kHz sine wave	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to -40 dBm0	-0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = -41 dBm0 to -50 dBm0	-1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = -51 dBm0 to -55 dBm0	-1.2		+1.2	dB

Notes:
1. CODECRXGAIN = 0 dB; 16-bit mode.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between AUXOUT and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-75 Receive path audio frequency response and image rejection

Parameter	Test conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz	Frequency (F) < 0.0125xFs; F = 0.025xFs; and F = 0.0375xFs to 0.375xFs Hz	-0.5		0.5	dB
	Frequency = 0.425xFs Hz	-1.5		0	dB
	Frequency = 0.4975xFs Hz			-14	dB
	Frequency = 0.575xFs Hz			-35	dB
	Frequency = 0.9975xFs Hz			-47	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. The Rx path input level is -10 dBm0.
3. This specification applies to EAR1_AMP, HPH_L AMP, HPH_R AMP, LINE_AMP, AUX_AMP outputs.
4. Loaded condition.
5. Frequencies 0.4975xFs, 0.575xFs Hz, and 0.9975xFs Hz characterize image rejection performance.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

Table 3-76 Receive audio path idle channel noise and distortion, HPH_L AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”		16.6	20.9	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a 16-Ω load connected between HPH_L and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_L and AVSS.
4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 16-bit mode; A-weighted.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-77 Receive audio path idle channel noise and distortion, HPH_R AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”		16.6	20.9	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with 16-Ω load connected between HPH_R and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_R and AVSS.

4. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
5. 16-bit mode; A-weighted.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-78 Rx audio path idle channel noise & distortion, HPH_L & HPH_R selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”		33.2	41.8	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially with 32-Ω load connected between HPH_L and HPH_R.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. 16-bit mode.
5. A-weighted.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-79 Rx audio path idle channel noise & distortion, LINE_AMP selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”		16.6	20.9	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured differentially between LINE_OP and LINE_ON.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave. Loaded condition (600 Ω).
4. 16-bit mode.
5. A-weighted.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-80 Rx audio path idle channel noise & distortion, LINE_AMP selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”		16.6	20.9	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Table 3-80 notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between LINE_OUT_L and AVSS, and between LINE_OUT_R and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. 16-bit mode.
5. A-weighted.
6. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
7. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-81 Receive audio path idle channel noise and distortion, AUX_AMP selected

Parameter	Test conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000000"		16.6	20.9	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-66	-60	dB
Total harmonic distortion + noise (THD+N)	Output level at -57 dBm0, 1.02 kHz and 5 kHz, Vdd = 2.5 V		-31	-29	dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between AUXO and AVSS.
3. The +3 dBm0 level corresponds to a 0-dB full-scale sine wave.
4. 16-bit mode; A-weighted.
5. Fs = sampling rate: 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.
6. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-82 Line_L_IP & Line_L_IN input to MIC_AMP1, AUX_PGA and EAR1_AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		4.24		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 V_{pp}, line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd=2.5 V			-29	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3-dB steps	-1.0		+1.0	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB, 3-dB steps	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured differentially between EARN and EARP, loaded condition (32 Ω). Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.
4. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to EAR1_AMP output.

Table 3-83 Line_L_IP and Line_L_IN input to AUX_PGA and EAR1_AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		4.24		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured differentially between EARN and EARP, loaded condition (32 Ω).
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-84 Line_L_IP & Line_L_IN input to MIC_AMP1, AUX_PGA and HPH_L AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V			-29	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3 dB steps	-1.0		+1.0	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured single-ended with 16-Ω load connected between HPH_L and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC-blocking capacitor and 16-Ω load connected between HPH_L and AV_{SS}.
4. Left and right DAC channels are in mute condition.
5. Measurement bandwidth = 20 Hz to 20 kHz.
6. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to HPH_L Amp output.

Table 3-85 Line_L_IP and Line_L_IN input to AUX_PGA and HPH_L AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Table 3-85 notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with 16-Ω load connected between HPH_L and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC-blocking capacitor and 16-Ω load connected between HPH_L and AV_{SS}.
4. Left and right DAC channels are in mute condition.
5. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-86 Line_L_IP & Line_L_IN in to MIC_AMP1, AUX_PGA & LINE_AMP output selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		3.32		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3-dB steps	-1.0		+1.0	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB, 3 dB steps	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured differentially between LINE_OP and LINE_ON.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.
5. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to Line_Amp output.

Table 3-87 Line_L_IP & Line_L_IN input to AUX_PGA and LINE_AMP output selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		3.32		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured differentially between LINE_OP and LINE_ON.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-88 Line_L_IP & Line_L_IN in to MIC_AMP1, AUX_PGA & LINE_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3-dB steps	-1.0		+1.0	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between Line_Out_L and AV_{SS}.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.
5. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to Line_Amp output.

Table 3-89 Line_L_IP & Line_L_IN input to AUX_PGA and LINE_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 $V_{pp,}$ line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC-blocking capacitor and 600-Ω load connected between connected between Line_Out_L and AV_{SS}.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-90 Line_L_IP & Line_L_IN in to MIC_AMP1, AUX_PGA & AUX_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 V_{pp}, line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB in 3-dB steps	-1.0		+1.0	dB
Absolute gain error	Line_L_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to-24.5 dB	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between AUXO and AV_{SS}.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.
5. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to AUX_AMP output.

Table 3-91 Line_L_IP & Line_L_IN input to AUX_PGA and AUX_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_L_IP = 0 V_{pp}, line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_L_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and a 600-Ω load connected between AUXO and AV_{SS}.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-92 Line_R_IP & Line_R_IN input to MIC_AMP1, AUX_PGA and HPH_R AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 $V_{pp,}$ line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-Hz sine wave, line PGA = +11.5 dB to +2.5 dB, 3-dB steps	-1.0		+1.0	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with 16-Ω load connected between HPH_R and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and a 16-Ω load connected between HPH_R and AV_{SS}.
4. Left and right DAC channels are in mute condition.
5. Measurement bandwidth = 20 Hz to 20 kHz.
6. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to HPH_R AMP output.

Table 3-93 Line_R_IP & Line_R_IN input to AUX_PGA & HPH_R AMP output selected

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 $V_{pp,}$ line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB in 3-dB steps.
2. Output measured single-ended with 16-Ω load connected between HPH_R and HPH_VREF.
3. Output also measured single-ended with a series combination of a (450 µF) DC blocking capacitor and 16-Ω load connected between HPH_R and AVSS.
4. Left and right DAC channels are in mute condition.
5. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-94 Line_R_IP & Line_R_IN in to MIC_AMP1, AUX_PGA & LINE_AMP output selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		3.32		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 V_{pp}, line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3 dB steps	-1.0		+1.0	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB, 3-dB steps	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3 dB steps.
2. Output measured differentially between LINE_OP and LINE_ON.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.
5. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to LINE_AMP output.

Table 3-95 Line_R_IP and Line_R_IN input to AUX_PGA and LINE_AMP output selected, differential

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		3.32		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 V_{pp}, line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured differentially between LINE_OP and LINE_ON.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-96 Line_R_IP & Line_R_IN in to MIC_AMP1, AUX_PGA & LINE_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 V_{pp}, line PGA = +11.5 dB			60	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB, Vdd = 2.5 V		-66	-60	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = +11.5 dB to +2.5 dB, 3 dB steps	-1.0		+1.0	dB
Absolute gain error	Line_R_IP = 752 mV_{pp}, 1.02-kHz sine wave, line PGA = -0.5 dB to -24.5 dB	-1.5		+1.0	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between Line_Out_R and AVSS.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.
5. The specifications above must be applicable to the line input routed through MIC_AMP1 (set to 0 dB), AUX_PGA path, and to LINE_AMP output.

Table 3-97 Line_R_IP & Line_R_IN input to AUX_PGA and LINE_AMP output selected, single-ended

Parameter	Test conditions	Min	Typ	Max	Unit
Overload-signal level [1]	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB		1.664		V_{pp}
Output referred noise [1] (A-weighted)	Line_R_IP = 0 V_{pp}, line PGA = +5.5 dB			40	μV_{rms}
Total harmonic distortion + noise (THD+N) [1] (A-weighted)	Line_R_IP = 1.5 V_{pp}, 1.02-kHz sine wave, line PGA = +5.5 dB, Vdd = 2.5 V		-66	-60	dB

Notes:
1. Levels should scale for AUX_PGA gains = +8.5 dB to -24.5 dB, 3-dB steps.
2. Output measured single-ended with a series combination of a (15 µF) DC blocking capacitor and 600-Ω load connected between Line_Out_R and AVSS.
3. Left and right DAC channels are in mute condition.
4. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-98 Power supply rejection and crosstalk attenuation

Parameter	Test conditions	Min	Typ	Max	Unit
Power supply rejection ratio (PSRR), transmit channel	Analog input level = 0 Vpp AV_{DD} = 2.5 V_{dc} + 100 mV_{pp}, Frequency = 0 Hz – 20 kHz	65			dB
Power supply rejection ratio (PSRR), receive channel	PCMIN = “0000000000000” AV_{DD} = 2.5 V_{dc} + 100 mV_{pp} Frequency = 0 Hz – 20 kHz	65			dB
Crosstalk attenuation, transmit-to-receive (differential outputs) with sidetone disabled	0 dBm0 analog input level Frequency = 0.0375xFs – 0.425xFs Hz Measured differentially at Rx path output	70			dB
Crosstalk attenuation, receive-to-transmit	PCMI = 0 dBm0 Frequency = 0.0375xFs -0.425xFs Hz Measured at PCMO EAR/HPH_L/HPH_R/Line_Out_L/Line_Out_R/ AUXO unloaded	70			dB
Interchannel Rx isolation, left to right channels	Left channel input = 0 dBm0 Right channel = all zeros input Frequency = 20 Hz – 20 kHz Measured HPH_R output	70			dB
Interchannel Rx isolation, right to left channels	Right channel input = 0 dBm0 Left channel = all zeros input Frequency = 20 Hz – 20 kHz Measured HPH_L output	70			dB
Interchannel Rx isolation, left to right channels	Left channel input = 0 dBm0 Right channel = all zeros input Frequency = 20 Hz – 20 kHz Measured Line_Out_R output	66			dB
Interchannel Rx isolation, right to left channels	Right channel input = 0 dBm0 Left channel = all zeros input Frequency = 20 – 20 kHz Measured Line_Out_L output	66			dB
Interchannel Tx input isolation, left to right channels	Line_In_L set at 0 dBm0 Line_In_R = AC ground Frequency = 20 Hz – 20 kHz Measured right channel input	70			dB
Interchannel Tx input isolation, right to left channels	Line_In_R set at 0 dBm0 Line_In_L = AC ground Frequency = 20 – 20 kHz Measured left channel input	70			dB
Input isolation, one input to another (MIC1, MIC2, AUXIN, Line_in)	One unselected input (1.02-kHz sine wave) = 0 dBm0 The other selected input = AC grounded Frequency = 20 Hz – 20 kHz Measure selected input	70			dB

Notes:
1. CODECRXGAIN = 0 dB.
2. Applies to all four Tx path inputs and all five Rx path outputs.
3. Fs = sampling rate: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz.

4 Device Marking and Ordering Information

4.1 Part marking

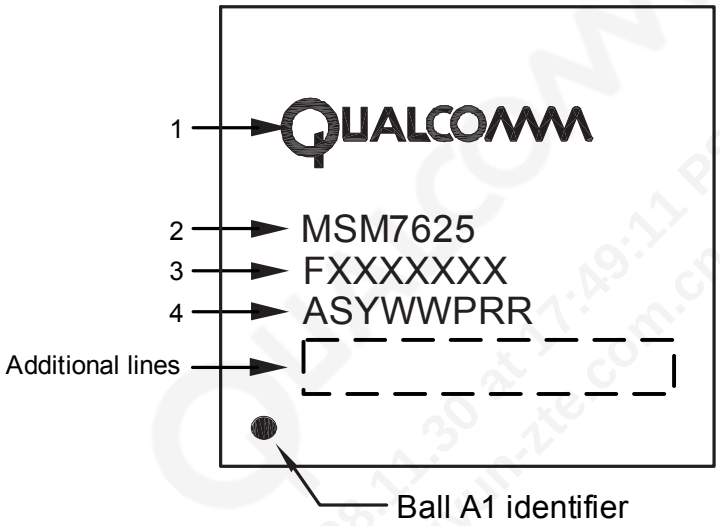


Figure 4-1 MSM7625 part marking (top view – not to scale)

Table 4-1 Part marking line descriptions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	MSM7625	Qualcomm product name
3	FXXXXXXX	F = supply source code ■ F = A [TSMC (digital die) + Chartered (analog die)] ■ F = B [TSMC (digital die) + IBM (analog die)] XXXXXXX = traceability number

Table 4-1 Part marking line descriptions (cont.)

<table>
<tr><th>Line</th><th>Marking</th><th>Description</th></tr>
<tr><td>4</td><td>AXYWWPRR</td><td>A = assembly site code
■ A = H (STATSChipPAC, South Korea)
■ A = C (Amkor, K4, South Korea)
X = traceability number
Y = single-digit year
WW = workweek (based on calendar year)
P = configuration code
■ P = 0
RR = product revision
<table><tr><th>RR</th><th>Revision description</th></tr><tr><td></td><td>Engineering sample; hardware ID = 0x901E00E1</td></tr><tr><td>01</td><td>TSMC (digital die) + Chartered (analog die)</td></tr><tr><td>02</td><td>TSMC (digital die) + IBM (analog die)</td></tr><tr><td></td><td>Commercial sample; hardware ID = 0xB01E00E1</td></tr><tr><td>03</td><td>TSMC (digital die) + Chartered (analog die)</td></tr><tr><td>04</td><td>TSMC (digital die) + IBM (analog die)</td></tr></table></td></tr>
<tr><td colspan="3">Note:
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm’s suppliers.</td></tr>
</table>

NOTE For complete marking definitions of all MSM7625 device revisions, refer to the *MSM7625 Mobile Station Modem Device Revision Guide* (80-VJ153-4).

4.2 Device ordering information

To order this device, customers should provide an identification code as shown in Figure 4-2.

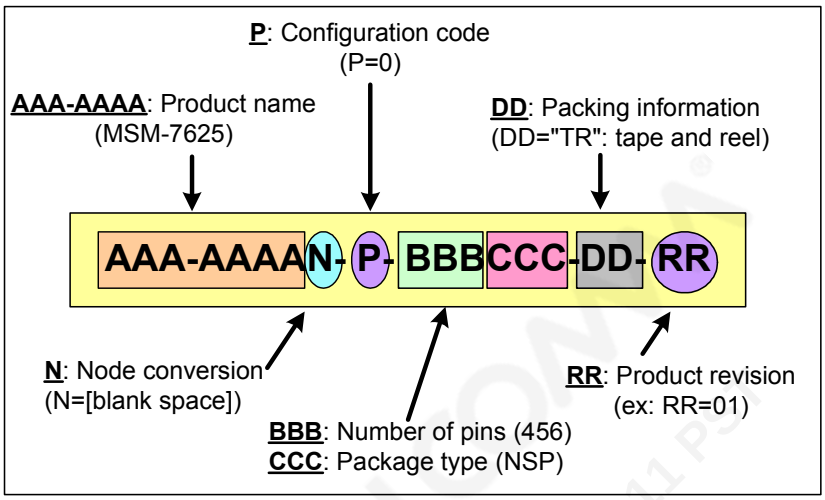


Figure 4-2 Example device identification code

An example for the MSM7625 device can be as follows: MSM-7625-0-456NSP-TR-01.

The P and RR values are defined in Section 4.1.

5 Package and Carrier Information

Details about the package information, tape and reel carrier, the method of packing for shipment, and the materials used for packing are described in this chapter. Additional details are available in the *BGA Package User Guide* (80-V2560-1), which can be downloaded from the CDMA Tech Support website (https://support.cdmatech.com).

5.1 Device physical dimensions

The MSM7625 IC is available in the 456-pin nano-scale package (456 NSP) that includes many dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 456 NSP package has an 11 mm × 11 mm body with a maximum height of 1.05 mm. Pin A1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below. The 456 NSP outline drawing is shown in Figure 5-1.

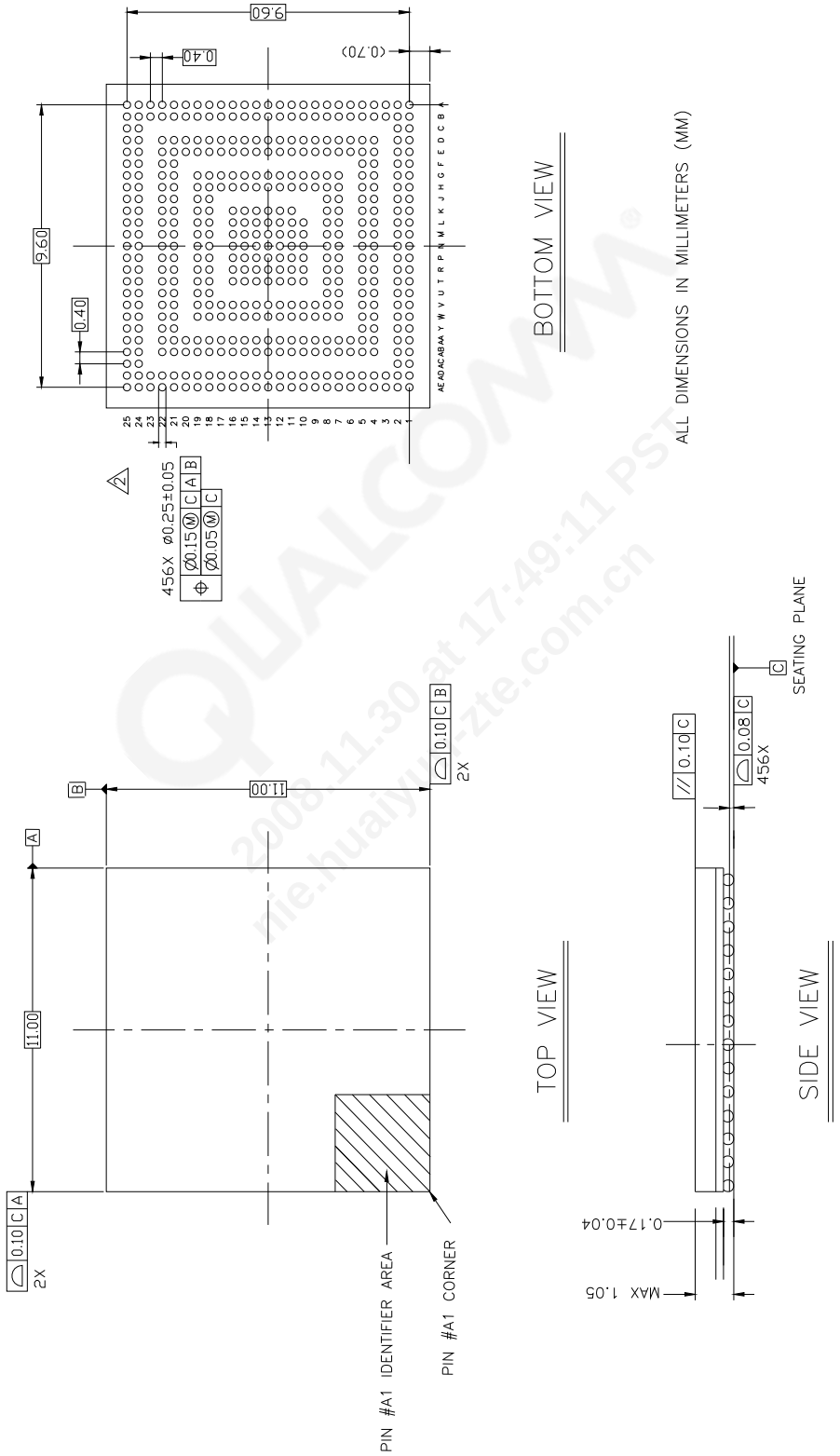


Figure 5-1 456 NSP (11 × 11 × 1.05 mm) outline drawing

5.2 Tape and reel information

Figure 5-2 shows the single-feed tape carrier for the MSM7625 device, including its proper part orientation. The tape width is 24 mm and the parts are placed on the tape with a 24 mm pitch. The reels are 330 mm (13 inches) in diameter with 102 mm (4-inch) hubs. Each reel can contain up to 1000 devices.

5.2.1 Package orientation in carrier tape

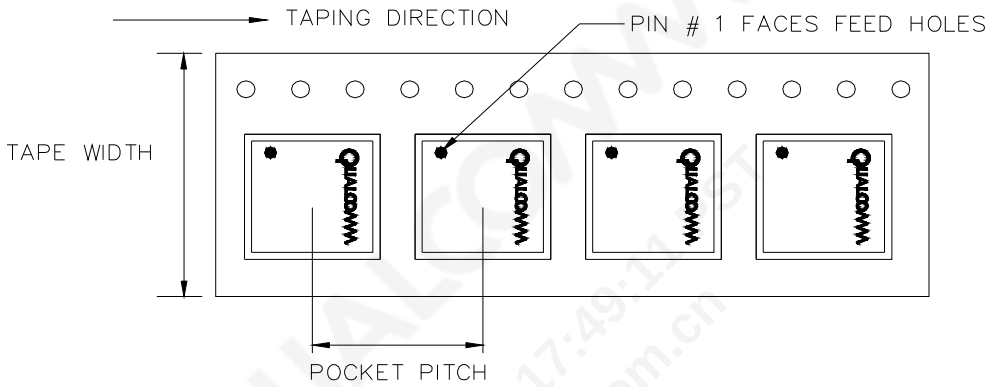


Figure 5-2 Carrier tape drawing with part orientation

5.2.2 Tape and reel features

The carrier tape and reel features conform to the EIA-481 standard:

- 8 mm through 200 mm embossed carrier taping
- 8 mm or 12 mm punched carrier taping of the surface mount components for automatic handling

5.2.3 Tape handling

Tape-handling recommendations are shown in Figure 5-3.

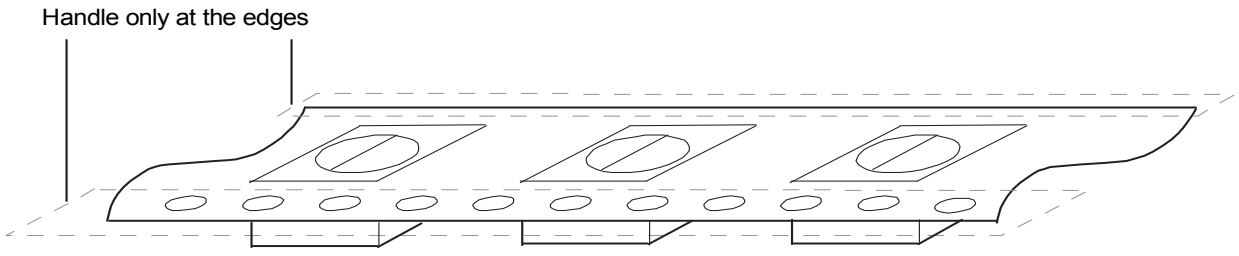


Figure 5-3 Tape handling

5.3 Barcode label and packing for shipment

For all barcode label and packing related information, refer to the *IC Packing Methods and Materials Specification* (80-VK055-1).

6 PCB Mounting Guidelines

This chapter presents guidelines for mounting the MSM7625 IC onto a printed circuit board (PCB), including storage recommendations after the devices are removed from their shipping packages, land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification. Additional details are available in the *BGA Package User Guide* (80-V2560-1), which can be downloaded from the CDMA Tech Support website (https://support.cdmatech.com).

The MSM7625 IC is lead-free externally, but not internally (internal SnPb solder bumps). It is RoHS-compliant. Its SnAgCu solder balls use SAC105 composition.

NOTE Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. See the *IC Package Environmental Roadmap* (80-V6921-1) for discussion of the Qualcomm package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm IC products.

6.1 Storage conditions, unpacking, and handling

The following sections present high-level instructions for storing, unpacking, and handling MSM7625 devices.

6.1.1 Storage conditions

The MSM7625 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier, anti-static bags. The Qualcomm-calculated shelf life in a sealed moisture bag is 60 months; this value requires an ambient temperature lower than 40 °C and relative humidity less than 90%.

6.1.2 Device moisture sensitivity level (MSL)

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. The MSM7625 IC is classified as MSL3 @ 250 °C. This temperature is referred to as the MSL classification temperature. It is defined as the minimum temperature of moisture-sensitivity testing during device qualification.

6.1.3 Out-of-bag duration

The MSM7625 IC must be soldered to a PCB within its factory floor life of ***one week*** after opening the moisture barrier bag (MBB).

NOTE The factory must provide an ambient temperature lower than 30 °C and relative humidity less than 60%, as specified in the IPC/JEDEC J-STD-033 standard.

6.1.4 Baking

It **is not necessary** to bake the MSM7625 devices if the conditions specified in Section 6.1.1 and Section 6.1.3 have **not been exceeded**.

It **is necessary** to bake the MSM7625 devices if any condition specified in Section 6.1.1 or Section 6.1.3 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125 °C. Devices should not be baked in tape and reel carriers at any temperature.

6.1.5 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the MSM7625 device ESD ratings.

6.2 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on Qualcomm internal characterizations for SnPb and lead-free solder pastes on a four-layer test PCB and a 100 micron-thick stencil. The PCB land pattern and stencil design for the 456 NSP package are the same whether SnPb or lead-free solder is used. Figure 6-1 shows the land pattern drawing, and Figure 6-2 shows the stencil design.

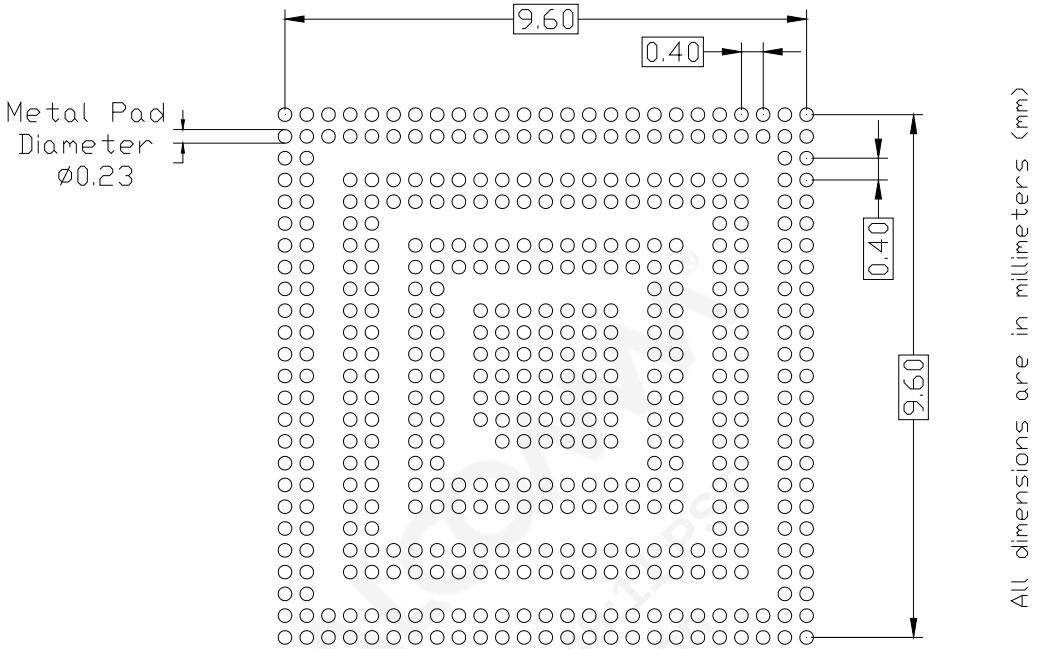


Figure 6-1 456 NSP land pattern drawing

The 456 NSP solder stencil pattern can use a square aperture (Figure 6-2).

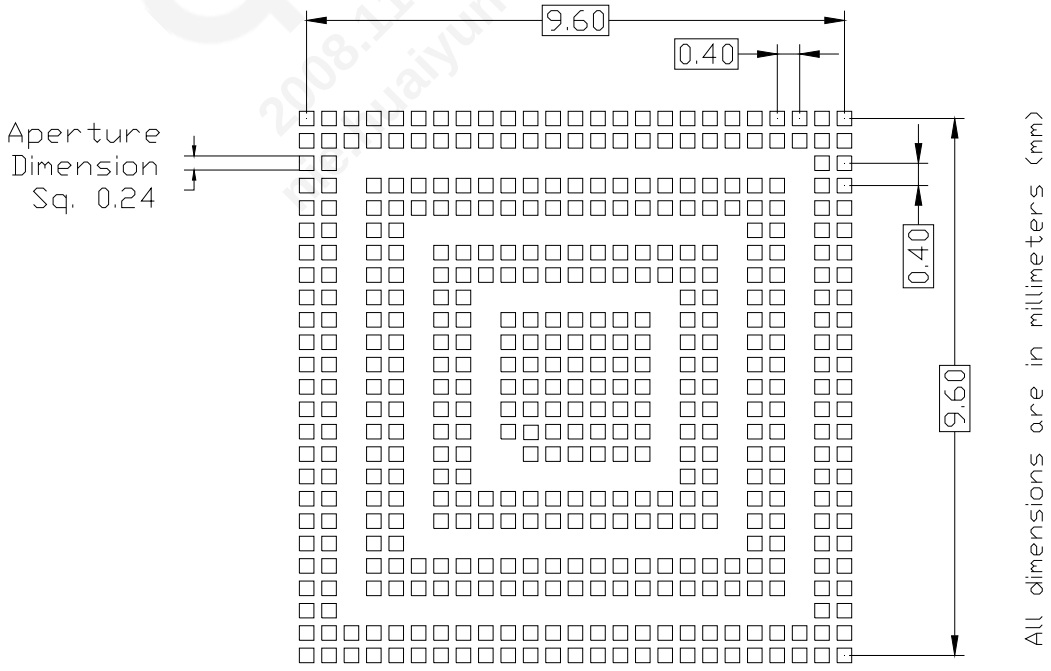


Figure 6-2 456 NSP solder stencil design

6.3 SMT development and characterization

This section describes Qualcomm board-level characterization process parameters. It is included to assist customers when starting their SMT process development; however, it is not intended to be a specification for customer SMT processes.

NOTE Qualcomm recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Qualcomm characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Peel test
- Bend-to-failure
- Bend cycle
- Tensile pull
- Drop shock
- Temperature cycling

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile ***prior to PCB production***. Review the land pattern and stencil pattern design recommendations in Section 6.2 as a guide for characterization.

Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, to decrease voiding, and to increase board-level reliability.

Daisy-chain packages are suitable and available for SMT characterization; ordering information is included in the *BGA Package User Guide* (80-V2560-1).

Reflow profile conditions typically used by Qualcomm for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 Qualcomm typical SMT reflow profile conditions (for reference only)

Profile stage	Description	SnPb (standard) condition limits	Lead-free (high-temp) condition limits
Preheat	Initial ramp	3 °C/sec max	3 °C/sec max
Soak	Dry out and flux activation	135 to 165 °C 60 to 120 sec	135 to 175 °C 60 to 120 sec
Reflow	Time above solder paste melting point	30 to 90 sec	40 to 90 sec
	SMT peak package body temperature	230 °C	245 °C
Cool down	Cool rate – ramp to ambient	6 °C/sec max	6 °C/sec max

6.4 SMT peak package body temperature

Qualcomm recommends the following limits during the SMT board-level solder attach process:

- SMT peak package body temperature of 250 °C – the temperature that should not be exceeded as measured on the package body's top surface
- Maximum duration of 40 seconds at this temperature

Although the solder paste manufacturer's recommendations for optimum temperature and duration for solder reflow should be followed, the Qualcomm-recommended limits must not be exceeded.

6.5 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

7 Part Reliability Test Specification

7.1 Reliability qualifications summary

Table 7-1 Stress tests for the MSM7625 device

Tests, standards, and conditions	Sample size	Result
Average failure rate (AFR) – HTOL: JESD22-A108-A Temperature: 140 °C, time: 36 hours	3191	40 failures in time (FIT)
Mean time to failure (MTTF) t = 1/λ in million hours	3191	2.5×10^7 hours
ESD – human body model (HBM) JESD22-A114-C	3	2000 V
ESD – charge device model (CDM) JESD22-C101-C	3	500 V
Latchup (I-test): EIA/JESD78 Trigger current: ±100 mA, temperature: 85 °C	6	Pass
Latchup (Vsupply overvoltage): EIA/JESD78 Trigger voltage: 1.5 x VDD nominal, temperature: 85 °C	6	Pass
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5 °C (MSL = moisture sensitivity level)	231	MSL3
Temperature cycle: JESD22-A104-B Temperature: -55 to 125 °C, number of cycles: 1000 Soak time at min/max temperature: 10 minutes Cycle rate: 2-3 cycles per hour (cph) Preconditioning: JESD22-A113-C MSL3 reflow temperature: 260 +5/-0 °C	231	Pass
Highly accelerated stress test (HAST) JESD22-A110-B Preconditioning: JESD22-A113-C MSL3 reflow temperature: 260 +0/-5 °C	231	Pass
High temperature storage life: JESD22-A103-B Temperature: 150 °C, time: 1000 hours	78	Pass
Flammability UL-STD-94	Certificate	Certificate
Physical dimensions: JESD22-B100-A	5x1	Pass

7.2 Qualification sample description

Device characteristics

Device name:	MSM7625
Package type:	456 NSP
Package body size:	11 mm × 11 mm × 1.05 mm
Ball count:	456
Ball composition:	Sn/1.0 Ag/0.5 Cu % by weight
Process:	65 nm
Fab site:	TSMC
Assembly site:	Amkor, STATSChipPAC
Ball pitch:	0.4 mm