White-Box Op-Amp Design via Human-Mimicking Reasoning

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Abstract—This brief proposes *White-Op*, an interpretable operational amplifier (op-amp) parameter design framework based on the human-mimicking reasoning of large-language-model agents. We formalize the implicit human reasoning mechanism into explicit steps of *introducing hypothetical constraints*, and develop an iterative, human-like *hypothesis-verification-decision* workflow. Specifically, the agent is guided to introduce hypothetical constraints to derive and properly regulate positions of symbolically tractable poles and zeros, thus formulating a closed-form mathematical optimization problem, which is then solved programmatically and verified via simulation. Theory-simulation result analysis guides the decision-making for refinement. Experiments on 9 op-amp topologies show that, unlike the uninterpretable black-box baseline which finally fails in 5 topologies, White-Op achieves reliable, interpretable behavioral-level designs with only 8.52% theoretical prediction error and the design functionality retains after transistor-level mapping for all topologies. White-Op is open-sourced at https://github.com/zhchenfdu/whiteop.

Index Terms—analog circuit, operational amplifier, parameter design, large language model, mathematical reasoning

I. INTRODUCTION

Operational amplifiers (op-amps) are fundamental building blocks in analog circuits. Their parameter design directly determines the circuit performance. Given the diverse application scenarios and stringent specifications (specs), op-amps often require labor-intensive manual parameter customization.

Automated black-box optimizers like Bayesian optimization (BO) [1]–[3] can discover high-score parameter combinations, but the pure score-driven search without physical grounding, presents key limitations on their *non-interpretability*, which (i) often harbors severe latent design defects and even failures manifesting in downstream implementation, and (ii) hinders human designers from understanding, adopting, or refining the solution. Therefore, interpretable, or so-called *white-box* op-amp design tools remain desirable.

Symbolic derivation is crucial for white-box op-amp design. Rule-based symbolic circuit derivation tools like GPDD [4] yield unbiased but lengthy transfer functions (TFs), rendering pole-zero (PZ) extraction hard. In practice, experts typically rely on their mathematical-physical intuition to simplify TFs and solve PZs, where experience-driven human reasoning are opaque and implicit, and thereby, is hard to encode in software. Follow-up works [5], [6] hard-code some TF simplification rules to bridge this gap, yet the transparency of PZ extraction and the adaptability of the fixed rules remain open challenges.

Beyond TF and PZ derivation, the flexible, reliable regulation of PZ positions ensures both functionality and performance, which is more nuanced, remaining largely unsolved by developing rule-based symbolic derivation tools.

Large language models (LLMs), with human-like learning and task execution capacity, have shown potential for white-box op-amp design. Existing efforts focus on two methods: (i) equipping LLMs with carefully curated knowledge bases of ready-made parameter calculation recipes for specific topologies [7], [8], to enable the reproduction of typical designs [9], while the LLM itself functions primarily as a procedural executor; (ii) integrating LLMs as parameter predictors within conventional sizing loops [10]–[12], where sizing experience accumulates but the real rationale remains opaque. These methods do not fully enable human-like op-amp design, partly constrained by limited reasoning capabilities of earlier LLMs.

Recent advances in reasoning LLMs [13], [14], achieving or exceeding human parity in mathematics, suggest that LLM-assisted symbolic derivation is within reach.

However, human-like op-amp design presents harder challenges than derivation: it relies heavily on the ***implicit reasoning mechanism*** that experts apply but rarely articulate. For example, (i) *TF simplification* requires discarding negligible terms, but which terms qualify is usually judged informally; (ii) *PZ extraction* often needs approximate solving techniques like root separation, but their suitablitity conditions are usually unspoken in literature; (iii) *PZ positioning* often follows unstated insights like how far poles separates, why this separation, and so on. Such implicit reasoning processes resist formalization into explicit, LLM-executable reasoning tasks.

To this end, this brief proposes ***White-Op***, an op-amp design framework via human-mimicking reasoning of agents. The key idea is that the above reasoning mechanism is distilled as explicit reasoning steps of ***introducing hypothetical constraints*** (e.g., ...≫...), enabling tractable TF simplification, reasonable PZ extraction, and deliberate positioning of PZs.

Since such hypotheses may not always correct, we devevlop an iterative ***hypothesis-verification-decision*** workflow to validate and adjust the constraints, where the agent: (i) proposes hypothetical constraints to extract and position PZs, thus formulating a closed-form optimization problem; (ii) solves it programmatically and validates the solution via simulation; (iii) analyzes theory-simulation results and makes refinements.

White-Op offers op-amp designs with interpretability and reliability through LLM reasoning, without referring to predefined parameter calculation recipes for specific topologies, black-box sizers or rule-based symbolic derivation tools.

Experiments across 9 op-amp topologies show that, unlike the uninterpretable black-box baseline which fails in 5 topologies after transistor-level mapping, White-Op achieves reliable, interpretable behavioral-level designs with only 8.52% theoretical prediction error, and retains circuit functionality in transistor-level for all topologies. White-Op is open-sourced at https://github.com/zhchenfdu/whiteop.
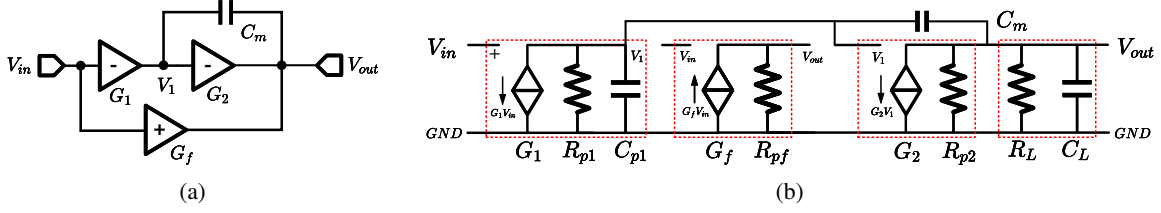
Fig. 1: Behavioral-level modeling. Fig. 1a is an MZC topology example (loads omitted). Fig. 1b shows the small-signal model.

II. PRELIMINARIES

A. Op-amp Behavioral-Level Modeling

In this work, behavioral-level design is conducted and then mapped to transistor-level (180-nm) via g_m/I_d method [15].

Fig. 1a shows an MZC (multipath zero cancellation) topology [16] example. Each stage is a transconductance G_i with a pair of parasitic resistance $R_{p,i}$ and capacitance $C_{p,i}$ in Fig. 1b.

The transconductance G_i serves as an independent design variable ($10\,\mu$S to 1 mS), whose sign indicates the phase shift. $R_{p,i}$ can be derived from the stage gain A_i (40 to 80) and G_i:

$$R_{p,i} = A_i/G_i. \tag{1}$$

$C_{p,i}$ is actually the input parasitic capacitance of the subsequent stage (null for the final stages connected to the load):

$$C_{p,i} = G_{i+1}/\omega_t, \tag{2}$$

where $\omega_t \approx 2\pi \cdot 200$ MHz is the empirical transition frequency.

Other design variables include independent resistors ($10\,\Omega$ to $1\,$MΩ) and capacitors ($10\,$fF to $10\,$pF).

B. Problem Formulation

Op-amp parameter design is defined as tuning independent design variables $\mathbf{x}$ to optimize a set of metrics $\mathbf{y}$. The objective function $f(\cdot)$ is set as the figure of merit (FoM) in Eq. (3):

$$\text{FoM} = \text{GBW[MHz]} \times C_L\text{[pF]} \ / \ \text{Power[mW]}. \tag{3}$$

We considers gain, gain-bandwidth product (GBW), phase margin (PM), and power as metrics in the work. Note that we estimate power in behavioral-level design via Eq. (4), where $(g_m/I_D)_i$ for each stage is empirically set to 20:

$$\text{Power} = \sum_i [G_i/(g_m/I_D)_i] \cdot V_{DD}. \tag{4}$$

III. PROPOSED APPROACHES

The core challenge is to distill the reasoning mechanism, particularly during PZ solving and positioning, into explicit, LLM-executable reasoning steps. The agent is guided to introduce hypothetical constraints, explicit inequalities that encode reasonable, physical-grounded assumptions. These transform informal human reasoning into tractable mathematical problems which can be verified via programming and simulation. The workflow is shown in Fig. 2, which is detailed in subsections below, using the MZC topology as a running example.

A. Proposal of Theoretical Hypothetical Design

In this phase, the agent performs symbolic derivation and simplification, and formulates a hypothetical op-amp design.

1) Preparing unbiased TF from circuit equations: Like humans, the agent begins by listing circuit equations.

• *Topology interpretation:* This preparatory step helps the agent identify signal paths and phase signs of each stage, thereby mitigating careless sign errors in equation formulation.
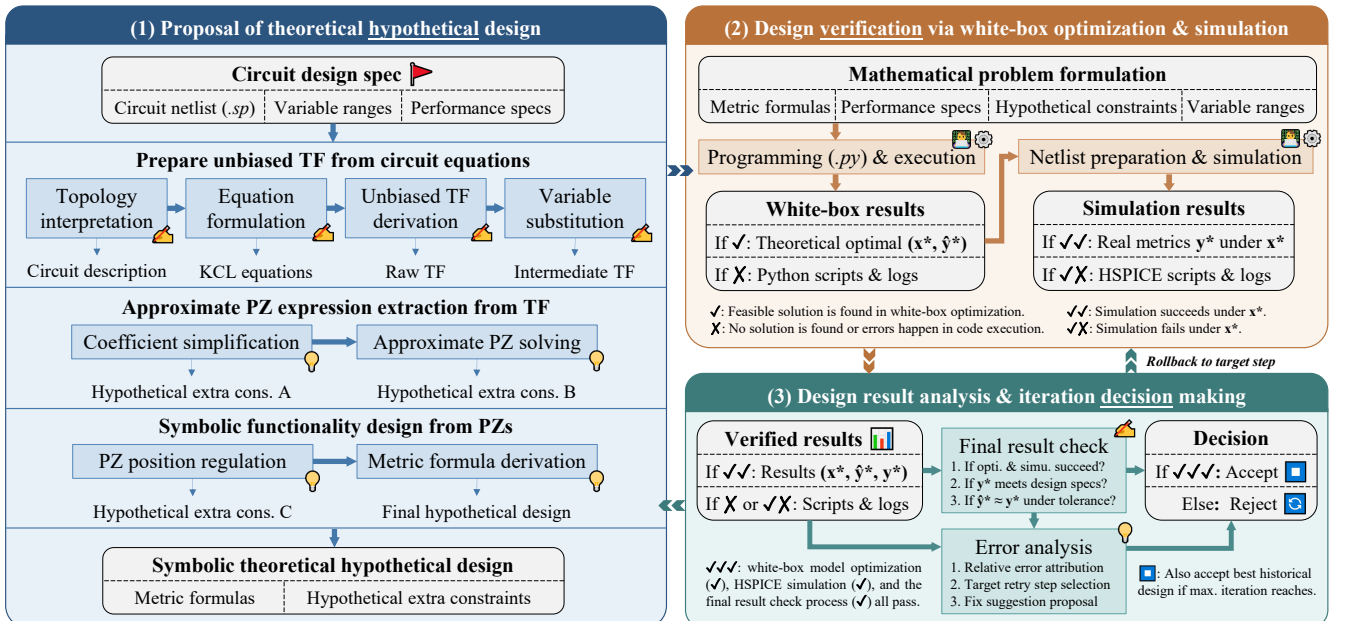

Fig. 2: The overall workflow of White-Op.

- **Equation formulation:** The agent then formulates equations using Kirchhoff's Current Law (KCL). In the MZC design example, the key response for this step is shown below:

> **Key response 1, iteration 1 —— KCL equations:**
> Based on the topology analysis and KCL, here are the s-domain circuit equations...
> $$\begin{cases} G_1V_{in}+V_1(1/R_{p1}+sC_{p1}+sC_m)-V_{out}sC_m=0 \\ -G_fV_{in}+V_1(G_2-sC_m)+V_{out}(1/R_{p2}+1/R_{pf}+1/R_L+sC_L+sC_m)=0 \end{cases}$$

- **Unbiased TF derivation:** The agent then solves the KCL equations using Cramer's rule to obtain the standard-form TF, termed the *raw TF*, where every coefficient in the numerator and denominator polynomials is detailed and precise.

- **Variable substitution:** Following Section II-A, we use transconductances G, stage gains A, independent resistances R and capacitances C as design variables. Parasitic terms are substituted per Eqs. (1) and (2), yielding the *intermediate TF*:

> **Key response 2, iteration 1 —— Intermediate TF:**
> Solving the KCL equations using Cramer's rule yields the standard-form TF:
> $$H(s)=(a_1s+a_0)/(b_2s^2+b_1s+b_0).$$
> After substitution ($R_{p1}=A_1/G_1$, $C_{p1}=G_2/\omega_t$, $R_{p2}=A_2/G_2$, $R_{pf}=A_f/G_f$), we get the intermediate TF coefficients as follows:
> $$a_1=G_f(C_{p1}+C_m)-G_1C_m=G_fG_2/\omega_t+C_m(G_f-G_1),$$
> $$a_0=G_1G_2+G_f/R_{p1}=G_1G_2+G_1G_f/A_1,$$
> $$b_2=C_LC_{p1}+C_LC_m+C_mC_{p1}=(G_2/\omega_t)(C_L+C_m)+C_LC_m...$$

2) Approximate PZ extraction from TF:

The intermediate TF above is overly complex to analyze directly. The agent usually simplifies the TF to extract approximate yet traceable PZs. This step specifically exemplifies human-like reasoning. To ensure the validity of simplifications, the agent often introduces **extra constraints (cons.)**, except for reductions that can be safely performed based on variable bounds alone.

- **Coefficient simplification:** The agent performs necessary simplifications on polynomial coefficients based on variable bounds to facilitate subsequent root-finding. Specifically, the agent is required to estimate coefficient ranges based on variable bounds. If extra constraints are needed to justify a simplification, they are recorded as **extra constraints A**.

Especially, since parasitic capacitances could be comparable to or even larger than compensation capacitances, the agent are encouraged by prompts to carefully consider them (e.g., explicitly using equivalent total node capacitance in derivation). Besides, inequality constraints are more encouraged over equality constraints, as the latter may be physically fragile and significantly reduce the feasible solution space. In the MZC design example, the agent's coefficient simplification strategies are summaried as below, which is basically reasonable:

> **Key response 3, iteration 1 —— Coefficient simplification:**
> We define auxiliary variables: $g_{o1}=G_1/A_1$, $g_{o2}=G_2/A_2+G_f/A_f+1/R_L$, and $C_{p1}=G_2/\omega_t$ to represent physical conductances and capacitances...
> **Cons. A1:** for $a_0=G_1G_2+G_1G_f/A_1$, comparing G_1G_2 vs G_1G_f/A_1: since $A_1\geq40$, the second term is $<2.5\%$ of the first term. To justify this simplification, we introduce Cons. A1: $A_1\gg1$ (naturally satisfied), enabling $a_0\approx G_1G_2$...
> **Cons. A2:** for $b_1=G_2C_m+g_{o2}(C_{p1}+C_m)+g_{o1}(C_L+C_m)$, the Miller term G_2C_m should dominate, but $g_{o1}C_L$ can be significant if C_m is very small. Therefore, we introduce Cons. A2: $C_m>G_1C_L/(G_2A_1)$, enabling $b_1\approx G_2C_m$...
> **Cons. A3:** for $b_2=C_LC_{p1}+C_LC_m+C_mC_{p1}$, comparing magnitudes: $C_L=10$ pF $\gg C_{p1}\approx0.1-0.8$ pF. We introduce Cons. A3: $C_L\gg C_{p1}$ (satisfied by design), enabling $b_2\approx C_L(C_m+C_{p1})$, where we retain C_{p1} as it becomes significant when...

- **Approximate PZ solving:** The agent extracts PZs from simplified polynomials by first attempting natural factorization. Since most polynomials cannot be factorized without bias, the agent should introduce **extra constraints B** to approximate PZ expressions. A strategy favored by both humans

and LLMs is *root separation*, which does not always hold in op-amps with complex compensation. Thus, the agent usually introduces extra constraints to ensure widely separated roots.

Especially, we set several useful reminders in the prompt. First, the agent is encouraged to avoid blind, default reduction (e.g., higher-order terms should not be discarded based on habit, as their impact on PZ locations may be non-negligible). Second, discriminant checking is mandatory when facing the quadratic formula. In op-amps with complex compensation, complex conjugate poles are common and should be expressed using natural frequency ω_n and damping ratio ζ rather than assuming all poles are real. The following example shows a classical approach to handle second-order real poles:

> **Key response 4, iteration 1 —— Approximate PZ solving:**
> From $N(s)=a_1s+a_0=0$ we yield $z_1=-a_0/a_1=-G_1G_2/[G_fC_{p1}+C_m(G_f-G_1)]$. If $G_f=0$, $z_1=G_2/C_m$ (RHP zero, degrades phase margin). If G_f is large enough such that the denominator becomes positive, the zero moves to the LHP...
> **Cons. B1:** For $D(s)=b_2s^2+b_1s+b_0$, we assess the discriminant: $\Delta=b_1^2-4b_0b_2$. With Miller compensation, the Miller term G_2C_m creates a massive term in b_1, making b_1^2 extremely large compared to $4b_0b_2$. Therefore, $\Delta>0$ and roots are real and widely separated. We introduce Cons. B1: $b_1^2\gg4b_0b_2$, i.e., $(G_2C_m)^2\gg4(g_{o1}g_{o2})C_L(C_m+C_{p1})$. This enables approximate factorization:
> $$D(s)\approx b_2(s-p_1)(s-p_2)\approx b_2(s+b_0/b_1)(s+b_1/b_2),$$
> where dominant pole $p_1\approx-b_0/b_1=-g_{o1}g_{o2}/(G_2C_m)...$ and non-dominant pole $p_2\approx-b_1/b_2=-G_2C_m/[C_L(C_m+C_{p1})]$. Note: As $C_m\to\infty$, $p_2\to-G_2/C_L$; as $C_m\to0$, p_2 is limited by C_{p1}, preventing the *infinite bandwidth* error...

3) Symbolic functionality design from PZs:

According to the control theory, PZ positions must be carefully regulated to control system stability and performance bounds.

- **PZ positioning:** To ensure reasonable values of metrics like PM, we introduce **extra constraints C** to regulate the mathematical properties of PZs. Advanced LLMs with the knowledge of control theory can autonomously formulate appropriate extra constraints such as pole splitting, zero-pole cancellation, half-plane regulation, and so on.

Also, the agent is reminded in the prompt that default ideas like dominant pole assumption should not be ignored. Besides, extremely loose or strict constraints (especially for $\gg$) should be carefully considered. Interestingly, in this MZC example (iteration 1), the agent carefulessly overlooks the dominant-pole assumption (though its zero-positioning strategy below is correct), reminding us that LLMs remain imperfect:

> **Key response 5, iteration 1 —— PZ position regulation:**
> **Cons. C1:** The MZC system is a second-order system with one zero z_1 and two poles p_1, p_2. The zero position depends critically on the sign of (G_f-G_1): if $G_f<G_1$, the denominator can be negative, leading to an RHP zero, which degrades phase margin; if $G_f>G_1$, the denominator is positive, yielding an LHP zero that provides phase lead. To ensure an LHP zero, Cons. C1: $G_f\geq1.1G_1$...

- **Metric formula derivation:** After introducing all extra constraints A, B, and C, The agent derives formulas based on the cooked TF and regulated PZs, including Gain, GBW, PM, and Power (per Eq. (4)). The cooked formulas in this MZC design example (iteration 1) are shown as follows:

> **Key response 6, iteration 1 —— Metric formula derivation:**
> We succeed auxiliary variables: $g_{o1}=G_1/A_1$, $g_{o2}=G_2/A_2+G_f/A_f+1/R_L$, and $C_{p1}=G_2/\omega_t$ (where $\omega_t=2\pi\times200$ MHz) and get the following formulas:
> PZs (rad/s):
> $$z_1=\frac{G_1G_2}{G_fC_{p1}+C_m(G_f-G_1)}, \quad p_2=\frac{G_2C_m}{C_L(C_m+C_{p1})}, \quad p_1=\frac{g_{o1}g_{o2}}{C_mG_2}$$
> PM (degrees):
> $$PM=90°-\frac{180°}{\pi}\arctan\left(\frac{GBW}{|p_2|}\right)+\frac{180°}{\pi}\arctan\left(\frac{GBW}{|z_1|}\right)$$
> Gain (dB): $Gain_{dB}=20\cdot\log_{10}(Gain)=20\cdot\log_{10}[G_1G_2/(g_{o1}g_{o2})]$
> GBW (Hz): $GBW=Gain\cdot|p_1|/(2\pi)=G_1/(2\pi C_m)$
> Power (W): $Power=0.05V_{DD}(G_1+G_2+G_f)=0.09(G_1+G_2+G_f)$

B. Verification via White-Box Optimization and Simulation

1) Programming and execution: The former phase outputs a set of hypothetical constraints, and analytical metric formulas under these hypotheses. The agent then yields a white-box, differentiable optimization problem and translates the it into `Python` code using `gekko` optimization suite. Executing this scripts yields a solution $(\mathbf{x}^*, \hat{\mathbf{y}}^*)$, which represents a theoretical local optimum rather than true simulation results.

2) Behavioral-level simulation: We then substitute $\mathbf{x}^*$ into the behavioral-level netlist and invoke HSPICE simulator to obtain the corresponding actual performance metrics $\mathbf{y}^*$. This step validates if the theoretical design holds in simulation.

C. Design Result Analysis and Iteration Decision-making

1) Result check: A solution is *accepted* only when three criteria are jointly satisfied: (i) the above white-box optimization yields a feasible solution; (ii) the simulated metrics $\mathbf{y}^*$ meet the design specifications, and (iii) the theoretical predictions $\hat{\mathbf{y}}^*$ exhibit sufficient agreement with $\mathbf{y}^*$. Upon acceptance, the workflow terminates with the current design.

2) Error analysis: In practice, various issues may arise: `python` optimization infeasibility, simulation failures, spec violations, or significant theory-simulation discrepancies. As shown in Fig. 2, under such cases, the agent examines the design trajectories, results, scripts, and debugging logs to perform three steps: (i) *error attribution* to identify the cause, (ii) *target identification* to determine the target rollback step, and (iii) *fix proposal* to suggest modifications. The agent then runs a rejection and retry cycle with the proposed corrections.

The following two examples of key responses respectively demonstrate: (i) in iteration 1, the error caused by the oversight of dominant-pole assumption mentioned in Section III-A2 is revealed; (ii) in the iteration 2, the design succeeds according to the reasonable fix suggestion and the framework completes.

Key response 7, iteration 1 —— Error analysis:

	Gain (dB)	GBW (MHz)	PM (°)	z_1 (MHz)	p_2 (kHz)	p_1 (kHz)
Theo.	69.26	377.6	64.4	181.03	191.8	∼120
Simu.	69.27	8.5	6.1	181.23	459.0	54.3
Error	0.01%	4337%	90.5%	0.11%	58.2%	∼120%

Error Attribution: The optimizer exploited a model loophole by minimizing C_m to its lower bound (10 fF) to maximize GBW=$G_1/(2\pi C_m)$, predicting 377.6 MHz. However, this caused $|p_2|{\approx}459$ kHz to fall far below the predicted GBW, violating the implicit assumption of single-pole roll-off (-20 dB/dec) up to unity gain. With $|p_2|{\ll}$GBW, early gain collapse occurs (-40 dB/dec slope), causing actual GBW to collapse to 8.5 MHz and PM to degrade to instability (6.1°).
Target and Fix: missing p_2–GBW coupling in the PZ positioning step. Solution: introduce $|p_2|{\geq}2{\times}$GBW to explicitly enforce the GBW formula's validity condition.

Key response 8, iteration 2 —— Result check:

	Gain (dB)	GBW (MHz)	PM (°)	z_1 (MHz)	p_2 (kHz)	p_1 (kHz)
Theo.	67.23	1.06	65.0	38.8	2119.7	≈2.89
Simu.	67.24	0.94	67.0	152	2180	2.79
Error	0.01%	12.7%	3.0%	74.5%	2.9%	3.6%

ACCEPT... Poles are predicted within 4% error; the large zero deviation is benign because the zero remains non-dominant (both $\gg$ GBW)...

IV. EXPERIMENTS

A. Experimental Setup

1) Environment: `gemini-3-pro-preview` is used as the backbone LLM. HSPICE performs behavioral-level simulation in the loops, while the g_m/I_D-based tool [17] maps the final solutions to transistor-level without further sizing.

2) Baseline and benchmark: BO is used as the baseline with 30 initial samples and 170 iterations. We set maximum iterations for White-Op to 3. The specs are: Gain > 60 dB, GBW > 0.5 MHz, PM $\in [45°, 90°]$, and Power $< 250\,\mu$W. Load capacitance C_L is fixed at 10 pF and load resistance R_L is fixed at 10 MΩ. To ensure sufficient margin for transistor-level mapping, PM target is tightened to $[55°, 65°]$ during optimization process. Experiments are conducted on 9 op-amp topologies from [9] with 10 trials per method.

TABLE I: Performance comparison among Theory, behavioral-level (BL), and transistor-level (TL) results using White-Op

Topo.	Gain (dB)			GBW (MHz)			PM (°)			Power (μW)		Rel. Err.		FoM			Time
	Th.	BL	TL	Th.	BL	TL	Th.	BL	TL	Th./BL	TL	Th.→BL	BL→TL	Th.	BL	TL	(min)
SMC	63.83	63.75	79.90	3.42	3.08	1.24	58.51	62.38	65.93	16.94	48.29	6.08%	74.27%	1135.82	1012.37	176.54	7.66
SMCNR	67.81	67.66	83.15	1.54	1.20	0.71	61.66	64.05	62.95	13.72	43.93	7.82%	80.43%	1320.59	973.66	158.08	10.83
MZC	66.33	66.35	83.41	1.22	1.04	0.61	59.79	63.73	62.12	37.39	43.71	7.09%	68.70%	794.55	679.65	138.76	10.83
NMC	98.71	98.59	116.53	2.65	3.28	1.67	59.58	63.63	69.93	51.67	125.52	13.03%	67.83%	491.26	569.96	116.30	15.39
NMCNR	99.36	99.25	118.42	1.66	1.82	1.00	60.56	63.15	74.74	35.94	89.80	7.45%	61.98%	537.70	594.63	123.93	16.90
MNMC	96.76	96.00	118.88	2.79	3.30	1.80	62.76	61.15	74.04	66.55	155.86	9.22%	54.87%	462.66	556.40	124.18	16.35
NGCC	103.49	103.40	116.04	1.80	1.79	1.06	62.69	58.35	71.44	41.43	103.83	5.93%	62.36%	503.77	531.60	113.57	13.01
NMCF	93.16	92.84	112.37	1.90	2.15	1.14	63.30	61.73	76.52	47.01	117.59	6.67%	75.11%	788.54	882.88	131.49	16.05
DFCFC	97.04	96.81	117.37	6.60	5.50	3.46	57.06	42.50	56.12	20.88	74.28	13.36%	93.68%	3090.23	2547.03	439.92	17.63

TABLE II: Performance comparison between behavioral-level (BL) and transistor-level (TL) results using BO

Topo.	Gain (dB)		GBW (MHz)		PM (°)		Power (μW)		Rel. Err.	FoM		Time
	BL	TL	BL	TL	BL	TL	BL	TL	BL→TL	BL	TL	(min)
SMC	70.20	76.28	3.58	2.02	57.66	57.91	50.00	117.03	62.17%	969.01	190.64	12.02
SMCNR	68.80	64.72	15.59	6.86	57.82	85.02	20.13	53.84	87.99%	9470.06	1083.13	11.82
MZC	63.56	58.91	13.42	6.81	58.25	53.44	145.78	279.60	43.34%	952.28	238.31	11.89
NMC	103.36	97.50	34.05	29.71	59.79	-108.35	123.53	320.46	116.73%	2804.09	fail	13.57
NMCNR	105.07	98.24	49.49	31.25	59.62	-167.76	143.07	347.34	141.95%	3548.60	fail	13.34
MNMC	101.62	95.65	27.51	21.78	59.74	-113.28	129.35	348.28	125.06%	2107.47	fail	13.21
NGCC	99.88	95.34	27.76	23.60	58.78	-111.64	182.47	481.02	120.29%	1536.34	fail	13.37
NMCF	101.81	96.64	32.48	25.73	59.76	-105.75	171.93	464.98	118.31%	1910.40	fail	13.58
DFCFC	100.36	97.55	12.17	5.99	57.92	67.97	180.45	465.37	57.70%	678.70	127.53	14.88

B. Results and Analysis

Table I shows White-Op's results across theoretical (Th.), behavioral-level (BL), and transistor-level (TL) with each row averaging 10 trials. Table II shows BO's results. Both methods take ∼13 minutes on average (BO mainly on Gaussian process model training, while White-Op mainly on LLM reasoning). White-Op's characteristics are analyzed as follows.

1) Effectiveness on Th.→BL: For White-Op, the Th.→BL metric discrepancy averages only 8.52% error, confirming the consistency between theoretical predictions and BL simulations. Note that power is excluded from this comparison since both Th. and BL designs employ Eq. (4).

2) Interpretability on BL: As shown in the design example across Section III, White-Op provides fully interpretable design rationale for human understanding and refinement.

Conversely, BO lacks interpretability. It seems to find BL designs with $2.87\times$ average FoM compared to White-Op (put aside the reversed situation after mapping to TL). This is expected since White-Op largely prunes the design space via introducing physically meaningful constraints, while BO explores the full design space as a black-box.

3) Reliability on BL→TL: The BL→TL metric discrepancy for both methods is inevitable and should not be attributed to White-Op itself. Instead, it arises from limitations in BL modeling (Section II-A), which captures dominant parasitics C_{gs} but neglects more complex parasitics C_{gd} and C_{db}. Furthermore, Eq. (4) just offers a power estimation with a uniform g_m/I_D across all stages, causing additional deviation.

White-Op's designs, despite these modeling imperfections, remain valid for all topologies after TL mapping. This reliability stems from our key idea: the clear constraints introduction reasoning steps in Sections III-A2 and III-A3 inherently enforce design redundancies (e.g., PZ relative positions), ensuring that designs validity (PM in reasonable range from $55°$ to $75°$) even when subjected to complex parasitic effects.

BO's seemingly better BL results, however, suffer severe degradation after TL mapping. In 5 out of 9 op-amp topologies, PM consistently falls outside reasonable ranges (averaging $-37.95°$), rendering these circuits invalid.

This contrast outcome lies in their mechanisms: BO's larger design space and naive higher-FoM-goal leads to BL solutions with highly entangled, unsafe PZ locations, which are acutely fragile in TL mapping. White-Op's interpretability, by contrast, maintain intrinsic safety margins, ensuring design resilience. BO does yield valid TL results for 4 topologies but such narrow success could be largely attributed to the inherent, parasitic tolerance of PZ positions in these circuit topologies.

V. Conclusions

This brief presents White-Op, an open-source op-amp design framework via agentic human-mimicking reasoning. The agent introduces extra constraints to derive and position PZs, formulating a mathematical problem solved programmatically and verified via simulation. White-Op offers interpretable, reliable BL designs retaining circuit functionality after TL mapping. White-Op supports flexible symbolic design for various topologies and specs, with potential extensions to similar analog circuit design problems.

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