

Maestro: A 302 GFLOPS/W and 19.8GFLOPS RISC-V Vector-Tensor Architecture for Wearable Ultrasound Edge Computing

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Abstract—Most Wearable Ultrasound (WUS) devices lack the computational power to process signals at the edge, instead relying on remote offload, which introduces latency, high power consumption, and privacy concerns. We present Maestro, a RISC-V SoC with unified Vector-Tensor Unit (VTU) and memory-coupled Fast Fourier Transform (FFT) accelerators targeting edge processing for wearable ultrasound devices, fabricated using low-cost TSMC 65nm CMOS technology. The VTU achieves peak 302GFLOPS/W and 19.8GFLOPS at FP16, while the multi-precision 16/32-bit floating-point FFT accelerator delivers peak 60.6GFLOPS/W and 3.6GFLOPS at FP16. We evaluate Maestro on a US-based gesture recognition task, achieving 1.62GFLOPS in signal processing at 26.68GFLOPS/W, and 19.52GFLOPS in Convolutional Neural Network (CNN) workloads at 298.03GFLOPS/W. Compared to a state-of-the-art SoC with a similar mission profile, Maestro achieves a 5 \times speedup while consuming only 12mW, with an energy consumption of 2.5mJ in a wearable US channel preprocessing and ML-based postprocessing pipeline.

Index Terms—Heterogeneous, RISC-V, Vector, Tensor, FFT, Low-Power, embedded, ultrasound SoC, WUS SoC, frequency-domain SoC

I. INTRODUCTION

THE recent advancements in Ultrasound (US) [1] transceiver technology are enabling the development of Wearable Ultrasound (WUS) systems [2] for the next-generation Human-Machine Interfaces (HMIs), with applications such as movement tracking [3] and gesture recognition [2], [4], benefitting from an increase in the miniaturization

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and energy efficiency of US probes: correspondingly, a fundamental requirement for all wearable systems is that they must be unobtrusive, compact and cost effective. Next-generation WUS systems also need to reduce the physical footprint of batteries that support onboard processing and ensure low operating temperature without active cooling. This translates in very strict <50mW power constraints, which in turn require an extremely energy-efficient edge processing platform.

For wearable processing systems focusing on biopotential signals (e.g., Electroencephalography (EEG), Electromiography (EMG)), several energy-efficient SoCs have been proposed for [5]–[7]. For this class of signals, input bandwidth is in the low-KHz range, preprocessing and conditioning effort is relatively low. On the other hand, US signals have orders of magnitude larger input bandwidth, and require more complex conditioning to convert A-mode data—i.e., the echo signals from muscle deformations—into meaningful features for downstream tasks (e.g., gesture classification) [8]–[12]. This is partly done by analog circuitry that excites the transducers, acquires the echoes, and amplifies the signal; and in part in the digital domain, where signals are usually filtered with classical Digital Signal Processing (DSP) algorithms such as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters, Hilbert Transform (HT), and Fast Fourier Transform (FFT) before being fed (often in the frequency domain) to into one of a large variety of Machine Learning (ML) models [10] (both conventional [9]—e.g., Support Vector Machines (SVM), Linear Discriminant Analysis (LDA)—and based on deep learning [4]). The large diversity of workloads involved in WUS processing calls for dedicated architectural solutions that couple flexibility with energy efficiency.

State-of-the-Art Ultra-Low Power (ULP) Microcontroller Units (MCUs) [5], [13], [14], commonly used in wearable scenarios, prioritize minimal power consumption with respect to performance and are unsuited to the complexity of WUS workloads. On the other hand, modern Artificial Intelligence (AI)-accelerated MCUs provide advanced AI capabilities but generally lack high-performance DSP features, particularly for frequency-domain processing [6], [15]–[17]. Whenever a given workload is not directly accelerated, these systems rely on software execution on simple, low-performance RISC processors,

which severely hinders end-to-end performance in the case of WUS. Embedded vector processors [18] provide an attractive alternative to couple performance and efficiency on a wide variety of DSP tasks with the flexibility of a programmable architecture. However, when targeting workloads that include modern AI algorithms such as Convolutional Neural Networks (CNNs) or Transformers, vector processors may still require an additional performance boost from an external tensor unit to achieve the target performance, with significant area and power overhead.

In this work, we propose to go one step further in integration, with a WUS processing architecture based on a unified vector/tensor unit to boost efficiency on AI and linear-algebra-centric workloads. By merging the tensor unit into the vector processor, we are able to share part of their microarchitectural resources, minimizing the overhead of the tensor unit while still retaining its performance. Additionally, to enable fast and efficient frequency-domain processing in the WUS scenario, we couple our processor with a companion multi-precision floating-point FFT engine. As an embodiment of this architectural approach, we present *Maestro*, a unified Vector-Tensor WUS System-on-a-Chip (SoC) prototyped in 65nm CMOS technology. In detail, the key contributions of this work are the following:

- a multi-precision unified Vector Unit (VU), based on the Spatz architecture [19], supporting the RISC-V Vector (RVV) Instruction-Set Architecture (ISA) with FP16–FP64 data, and high-performance General Matrix-Matrix Multiplication (GEMM) operations in FP8–FP16 precision in a fully integrated Vector-Tensor Unit (VTU);
- a multi-precision FP16–FP32 radix-2 Decimation In Time (DIT) FFT engine employing novel fused-arithmetic dual-output sum-of-dot-products modules for high-precision, low-energy operation;
- a heterogeneous compute cluster including the VU and FFT engine in a memory-coupled configuration with 128 KiB of low-latency L1 memory;
- the implementation and characterization of the proposed architecture on a commercial 65nm CMOS technology;
- the comparative analysis of the proposed architecture on an end-to-end ultrasound-based gesture recognition application versus GAP9 [7], a high performance & energy-efficiency commercial SoC.

Maestro delivers 1.62GFLOPS and 19.52GFLOPS in frequency domain and CNN tasks, respectively, outperforming GAP9 by $2.63\times$ and $6.53\times$. It delivers its highest energy efficiency in CNN processing at 298GFLOPS/W, $2.19\times$ higher than GAP9. Overall, our results show that Maestro’s unified Vector/Tensor processor + FFT companion architecture is highly competitive with GAP9 on WUS applications, achieving $5\times$ better end-to-end latency on our target WUS workload despite GAP9’s much more aggressive technology node (22nm). Furthermore, when employed in a Maestro-based ultrasound system, which acquires and processes data at the edge, the entire system operates with an ultra-low power consumption of just 12mW, achieving an energy cost of only 2.5mJ and operating up to 94 hours.

The manuscript is structured as follows: Section II reviews vector processors, hardware accelerators for AI and FFT, and state-of-the-art WUS applications and systems. Sections III, IV, and V detail Maestro’s architecture and accelerators. Section VI presents the silicon prototype implementation and measurements. Section VII evaluates the performance, energy efficiency, and latency of an A-Mode WUS application. Section VIII compares Maestro with similar prototypes, and Section IX concludes with key findings and future research directions.

II. RELATED WORK

This section analyzes the design principles and architectural components that define the proposed SoC, including vector cores, tensor cores, and FFT accelerators. Finally, we review the state of the art in WUS applications and systems shown in Table I.

A. Vector Cores

Vector processing presents an effective solution to the growing need for programming flexibility coupled with performance and energy efficiency. By leveraging Single-Instruction-Multiple-Data (SIMD) paradigm, a single vector instruction can process multiple data elements, significantly reducing the energy overhead associated with instruction fetch and dispatch [33].

Both ARM and RISC-V instruction sets support advanced vector processing capabilities with dedicated extensions. ARM introduced the Scalable Vector Extension (SVE) [34] and its successor, SVE2, while the RISC-V community developed the RISC-V Vector (RVV) ISA [35], known for its open and extensible design. The RVV specification reached its frozen 1.0 version in 2021, marking a significant milestone in RISC-V’s vector processing capabilities. Since then, both industry and academia have actively contributed to a wide range of vector processor implementations. These include High-Performance Computing (HPC) designed for large-scale processing and complex dataset analysis leveraging scalability, efficiency, and parallelism [20], [36], [37], Deep Neural Network (DNN) [22], [38], [39] and embedded applications [18], [19], [40].

Ara [20] is the first open-source RVV processor, operating at more than 1GHz in 22FDS Global Foundries technology. It integrates the Linux-capable CVA6 core [41] with a vector accelerator featuring 16 double-precision lanes, each accessing 16×64 -bit elements of the Vector Register File (VRF). This design delivers 33GFLOPS and 41GFLOPS/W for double-precision matrix multiplication, making it a power-efficient HPC solution with a peak power consumption of 763mW. Yun [21] is the first silicon prototype based on the smallest Ara configuration, featuring 4×64 -bit lanes and a Vector Length (VLEN) of 4096-bits. It operates up to 280MHz in 65nm TSMC technology and achieves 2.83GFLOPS and 10.8GFLOPS/W for double-precision matrix multiplication, with power consumption ranging from 57mW to 330mW.

Speed [22], aims to enable efficient quantized DNN inference operating at a frequency of 1.05GHz in TSMC 28nm

TABLE I
ARCHITECTURES FOR VECTOR, TENSOR, FFT ACCELERATION AND ULTRASOUND SYSTEMS

| Architecture | Technology | CPU | Max Frequency | Vector Accelerator | Tensor Accelerator | FFT Accelerator | Power Envelope |
|--|-------------|----------------------------------|---------------|--------------------|--------------------|-----------------|----------------|
| <i>Ara</i> [20] | GF22 FDX | CVA6 RV64GC | 1 GHz | ✓ | - | - | 763 mW |
| <i>YUN</i> [21] | TSMC 65 | CVA6 RV64GC | 280 MHz | ✓ | - | - | 330 mW |
| <i>Speed</i> [22] | TSMC 28 | CVA6 RV64GC | 1.05 GHz | ✓ | ✓ | - | 533 mW |
| <i>Spatz</i> [19] | GF 12LPP | Snitch RV32IMC | 1 GHz | ✓ | - | - | 164 mW |
| <i>Gemmni</i> [23] | GF22 FDX | Rocket RV64GC | 961 MHz | - | ✓ | - | - |
| <i>Tsunami</i> [24] | 65nm CMOS | - | 200 MHz | - | ✓ | - | 419 mW |
| <i>DARKSIDE</i> [25] | TSMC 65 | 8xRISCY-NN RVC32IMFXpulpNN2 | 290 MHz | - | ✓ | - | 213 mW |
| <i>ECHOES</i> [26] | TSMC 65 | CV32e40p | 350 MHz | - | - | ✓ | 134 mW |
| [27] | 16nm FinFET | Rocket-Chip | 940 MHz | - | - | ✓ | 22.6 mW |
| [28] | 65nm CMOS | - | 100 MHz | - | - | ✓ | 59.11 mW |
| [29] | TSMC 28 | - | 270 MHz | - | - | ✓ | 126 mW |
| <i>STM32F7</i> [30] (product) | 90nm CMOS | Cortex-M7 + DSP | 216 MHz | - | - | - | 900 mW |
| <i>TMS320F28379D</i> [31] (product) | - | 2xTMS320C28x + TMU + VCU-II | 200 MHz | - | - | ✓ | 576 mW |
| <i>dsPIC33EP512MU814</i> [32] (product) | - | 16-bit DSP | 70 MHz | - | - | - | 350 mW |
| <i>GAP9</i> / <i>VEGA</i> [7] | GF22 FDX | 10 × RI5CY RVC32IMFXpulp + SF | 370 MHz | - | ✓ | - | 50 mW |
| <i>This work</i> | TSMC 65 | Snitch RV32IMC | 210 MHz | ✓ | ✓ | ✓ | 212 mW |

technology. It supports processing precision ranging from 4-bit to 16-bit and integrates within each of the 4×16 -bit lanes an integer-multi-precision (4-8b) tensor unit. Experimental results show that SPEED achieves a peak throughput of 7.37TOPS and an energy efficiency of 1.38TOPS/W for 4-bit operations consuming up to 533mW.

These architectures are designed for large-scale HPC clusters, where their large VRF enables efficient compute-intensive edge and cloud systems processing of long vectors across multiple cores. Despite their relatively low per-core power consumption (<1W), their efficiency depends on sustaining high utilization through large-scale parallelism. This makes them well-suited for massively parallel workloads but inefficient for smaller, fragmented tasks, where their computational resources remain underutilized. Moreover, they are designed for application targets with much more relaxed power constraints than WUS.

The Spatz architecture [19] operates at over 1GHz in 12LPP technology. It implements an open-source dual-core vector processor based on a cluster that shares 128KB of memory. Each vector core is equipped with a 512-bit VRF divided across four 64-bit lanes. This smaller VRF design enhances utilization, ensuring more efficient use of functional units, particularly on small workloads, making it well-suited for embedded processing domains. The Spatz cluster achieves a peak performance of 15.7GFLOPS and a peak energy effi-

ciency of 95.7GFLOPS/W when executing a double-precision matrix multiplication workload, consuming up to 164mW.

The cluster proposed in Maestro, built on the Spatz cluster template, extends the vector DSP capabilities with frequency domain acceleration by integrating a memory-coupled FFT engine and a tightly coupled tensor unit accelerating ML and general matrix-matrix operations, offering increased performance and energy efficiency.

B. Tensor Cores

AI workloads are dominated by linear operations, such as matrix multiplication, making Tensor Core architectures the preferred solution for accelerating these computations. State-of-the-art implementations explore various architectural approaches to optimize performance, power efficiency, and area utilization. We focus the following survey on tensor engines designed for low-power edge applications.

Gemmni [23] is an open-source systolic array of 256 Computing Elements (CEs) of 8-bit Integer multiply-accumulate designed for inference of DNN that support runtime-programmable stationary weight and output data flows. It has been implemented in Intel 22FFL technology operating at over 961MHz achieving a peak energy efficiency of 73.3GOPS/W.

Tsunami [24], manufactured in 65nm CMOS technology, targets high energy efficiency in DNN training with

1024×16 -bit floating-point CEs at 200MHz. Relying on pruning to eliminate unnecessary computations, Tsunami delivers 310GFLOPS and 1.71TFLOPS/W on 16-bit floating-point operations with a maximum power consumption of 419mW.

DARKSIDE [25] is a heterogeneous RISC-V compute cluster for TinyML at the extreme edge. It features 8 DSP-enhanced RISC-V cores, a Depth-Wise Convolution Engine, a DataMover, and a 16-bit floating-point tensor core for matrix operations consisting of 32 FP16 Fused Multiply-Accumulate (FMA) units. Fabricated in TSMC 65nm, it runs at 290MHz and delivers 18.2GFLOPS at 300GFLOPS/W, with a peak power consumption of 213mW.

Our work, Maestro, introduces a unified vector-tensor processing framework, integrating a tensor unit within the vector core to enable tightly coupled cooperation with the VRF. Unlike previous designs [22], [23], Maestro's tensor unit, an area-improved design of the open-source RedMulE architecture [42], supports mixed-precision 8/16-bit floating-point arithmetic (FP8/FP16) and offers up to 48 CEs, enabling efficient embedded processing across diverse workload types by coordinating its execution among other functional units. The inclusion of FP8 and FP16 support balances precision and efficiency for edge WUS applications scenarios with AI and DSP workloads.

C. FFT Accelerators

As frequency-domain workloads grow in complexity, software-based FFT solutions struggle to achieve real-time performance and energy efficiency, highlighting the need for specialized hardware accelerators. Wang et al. [27] introduced an FFT accelerator capable of handling 24-bit precision fixed-point data, while Sinigaglia et al. [26] supports 8/16/32-bit fixed-point precision on the TSMC 65nm implementation of a frequency domain Echoes SoC delivering up to 200GOPS/W and running up to 350MHz with a power envelope of 134mW.

Wang et al. [27] present a 16nm FinFET runtime-reconfigurable $2^n3^m5^k$ FFT fixed-point accelerator designed for multi-standard wireless communication systems such as LTE and Wi-Fi. The accelerator is built using a memory-based architecture optimized for high area efficiency and is integrated with a RISC-V core to demonstrate a complete software-defined radio (SDR) system operating up to 940MHz, and consuming up to 22.6mW depending on the FFT workload. The use of fused floating-point operations tailored for FFT processors is explored in studies such as [43], [44].

Hitesh et al. [28] investigate the implementation of a high-precision frequency measurement system for MEMS gyroscopes, employing a low-precision (11-bit) floating-point approach for radix-2 FFT computation. The system enhances computational efficiency by optimizing memory access patterns through the matrix transposition technique (CTMT), which is applied alongside the Cooley-Tukey FFT algorithm, a standard approach for FFT computation. The design is capable of performing a 256-point FFT while maintaining scalability to variable-length FFTs. Implemented in 65nm CMOS technology, it operates at 100MHz, while delivering a power consumption of approximately 59.1mW at a 1.2V power supply voltage.

The work by Larry et al. [29] introduces a hardware accelerator specifically designed to enhance the performance of FFTW software library for scientific computing. Fabricated in TSMC 28nm technology, the accelerator adopts a fully unrolled radix-8 FFT architecture. It employs single-precision floating-point arithmetic. Operating at 270MHz with a 0.9V power supply, the accelerator has a power consumption of 126 mW, making it a highly efficient solution for embedded signal processing delivering 16.5GFLOPS/W @ 270MHz.

Most existing hardware FFT implementations either rely on fixed-point arithmetic [45], which is unsuitable for frequency-domain processing in WUS applications; or they do not target embedded applications. In this work, a memory-coupled multi-precision 16/32-bit floating-point radix-2 FFT accelerator design is proposed. It is integrated as a Cluster-coupled Hardware Processing Engine (HWPE), where both the vector core and the accelerator share memory directly through the same interconnect. Unlike traditional FFT accelerators, it does not require large internal buffers and instead relies entirely on the memory interconnect for data access. This approach improves the efficiency of the accelerators, reducing area usage while maintaining strong computing performance. The accelerator supports up to 512 FFT points for FP32 precision and 1024 FFT points for FP16 precision, where both the real and imaginary components are represented in FP32 or FP16, respectively.

D. Wearable Ultrasound Applications and Systems

State-of-the-art embedded systems for WUS applications often rely on MCUs that do not play a central role in processing steps. Instead, they are used mainly to acquire echo data from the US probes and transmit them to an external computer for further processing.

In [9], a prosthetic hand control system employs four A-mode transducers and a STM32F7 [30] MCU to acquire echoes, perform basic filtering, and transmit data to a Personal Computer (PC) for further feature extraction and classification. Although the MCU features a 32-bit Cortex-M7 running at 216MHz with a DSP unit, it mainly serves for data acquisition, offloading signal processing—i.e., envelope extraction via HT, Principal Component Analysis (PCA) for dimensionality reduction, and ML-based classification—to an external computer. Similarly, the wearable system in [10] uses a TMS320F28379D [31] MCU (dual-core, 200MHz) to digitize analog US signals, apply a 1024-point FFT, and transmit results to a PC, where the LDA model is applied for classification.

Xia et al. [8] propose a portable hybrid surface Electromyography (sEMG)/A-mode US system for Human-Machine Interface (HMI), integrating a composite sensor armband, signal acquisition modules, a DSP, and a communication module. The US acquisition module consists of two main components: the Signal Excitation Part (SEP), responsible for generating and firing ultrasound waves via a beamformer, and the Signal Conditioning Part (SCP), which amplifies, filters, and optimizes the received echoes. The processed analog signals are digitized and further refined by a dsPIC33EP512MU814

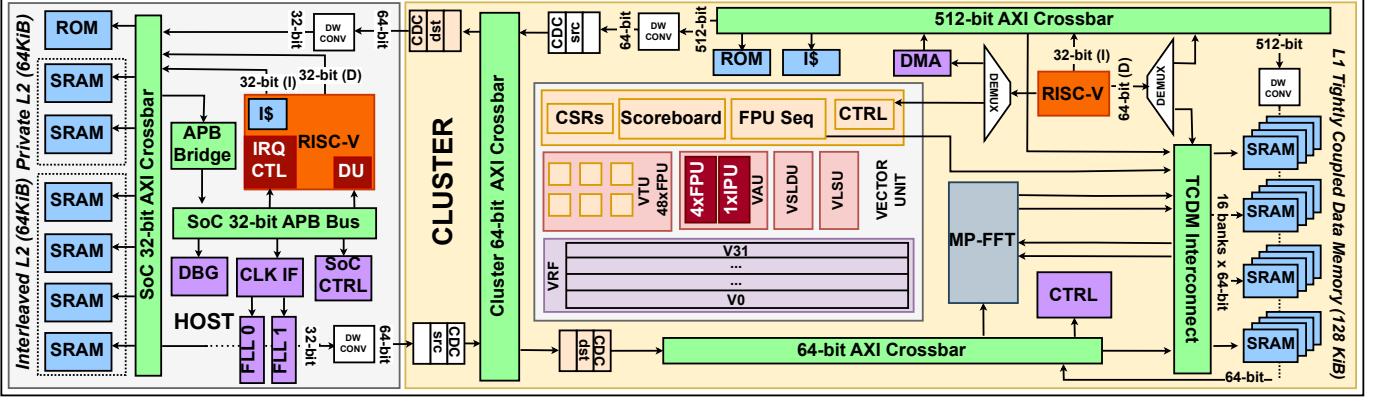


Fig. 1. Maestro architecture with Host and Cluster domains. The Host domain includes a 32-bit RISC-V core, 64 KiB L2 memory, and two FLLs. The Cluster domain features a 32-bit RISC-V core, 128 KiB L1 memory, DMA, Vector Unit (VTU, VAU, VSLDU, VLSU, VRF), and MP-FFT accelerator, all sharing the L1 memory.

DSP [32], which applies filtering, amplification, and scaling to optimize signal quality for subsequent analysis. This system has also been used by Zeng et al. [4]: in this work, the authors propose an adaptive CNN based on A-mode US for gesture recognition tasks. The raw A-mode US data undergoes a series of preprocessing steps—Time Gain Compensation (TGC), filtering, envelope detection via HT, and log compression—before being fed into the CNN. Then, at test time, the feature extractor part is updated via backpropagation based on a pseudo-label. However, the test-time adaptation is still not performed locally but on an external PC.

Frey et al. proposed an sEMG-triggered Ultrasound System platform [46], which integrates sEMG and US for the long-term monitoring of muscle activity. This system integrates two state-of-the-art wearable devices: BioGAP [47] for biosignal acquisition and WULPUS [48] for ultrasound data acquisition. It operates at 7.8mW when only BioGAP performs single-channel sEMG measurement, with WULPUS in sleep mode, and consumes 29.8 mW when both sEMG and US systems are continuously active. BioGAP is powered by GAP9, a commercial version of VEGA [7] along with an nRF52811 [49] that provides data communication capability through a flexible Bluetooth Low Energy (BLE) communication. GAP9 is an ultra-low-power processor designed for hearable and battery-powered smart devices. It delivers 32.2 GMACs for ML tasks and 15.6 GOPs for DSP workloads, operating within a power envelope of up to 50mW. WULPUS is built around an MSP430 [50] MCU that manages communication with the US transducers and forwards the incoming data to an nRF52832 [51] MCU that streams them via BLE to an external PC that receives both sEMG and US data from BioGAP and WULPUS, respectively.

In contrast to these designs—which rely heavily on external computing or only feature limited DSP capabilities—Maestro’s SoC integrates a programmable vector unit, a hardware FFT accelerator, and a tensor engine in a compact cluster, enabling high-performance frequency-domain analysis and ML-based inference at the edge within a low power envelope. This unified and heterogeneous approach eliminates the need to transfer data across multiple components, allowing

efficient, integrated embedded processing of WUS signals.

III. MAESTRO ARCHITECTURE

The Maestro SoC, comprises two distinct clock domains, as depicted in Fig. 1: (i) the Host, featuring the main 32-bit core of the SoC, and (ii) the Cluster, equipped with an advanced VU extended with a Tensor Unit (TU) and a 16/32-bit multi-precision FFT processing engine.

A. Host Domain

The Host domain features a compact, 2-stage, 32-bit RISC-V RV32IMC core [52], optimized for low-cost and energy-efficient operation. This core is supported by a memory subsystem consisting of 64KiB of shared L2 Tightly-Coupled Data Memory (TCDM) organized into 4 interleaved SRAM banks, four additional 16KiB interleaved SRAM banks designated as private memory, and a boot ROM. All components are interconnected through a 32-bit Advanced eXtensible Interface (AXI)-4 crossbar, ensuring efficient access and integration. Additionally, an Advanced Peripheral Bus (APB) interconnect provides access to SoC control registers and a debug interface, enabling system management and debugging capabilities. To ensure robust clocking for both the Host and Cluster domains, the architecture incorporates two dedicated Frequency-Locked Loops (FLLs). This setup showcases the adaptability of the Cluster, which can be incorporated with alternative Host subsystems to meet the needs of diverse applications or architectural requirements.

B. Cluster Domain

The Cluster domain hosts the core contribution of this work, featuring a single-stage RISC-V RV32IMAFD Snitch scalar core [53], augmented with an RVV1.0 Zve64d-compliant Spatz VU [19]. This architecture enhances the VU with a fully programmable TU based on RedMule architecture [42], forming a unified and versatile area-optimized VTU for high-performance and energy efficiency vector-tensor operations. Moreover, the Cluster includes a floating-point multi-precision

16/32-bit FFT accelerator, integrated as HWPE sharing the memory with the Cluster through a low-latency L1 TCDM interconnect.

The memory subsystem features a shared 128KiB L1 TCDM organized into 16 interleaved SRAM banks to optimize parallel access and minimize contention. Additionally, a 512-bit/cycle read and 512-bit/cycle write Direct Memory Access (DMA) controller [54] facilitates data movement between L2 and L1. The interconnect of the Cluster is designed to ensure efficient communication both within its internal components and with external systems. A 64-bit AXI-4 crossbar serves as the primary interface between the Cluster and the Host, enabling bidirectional data transfer. At the Cluster boundary, Clock Domain Crossing (CDC) First-In First-Out (FIFO) queues to ensure communication with the host domain enabling the two blocks to work at different frequencies. The Cluster features a hierarchical interconnect designed to handle efficient data and instruction transfers. At the top level, a high-throughput 512-bit wide AXI-4 crossbar enables data transfers, reducing the number of cycles required for large transactions. This interconnect links the instruction cache and the boot ROM to the scalar core, while the DMA controller facilitates data movement between L1 and L2 memory. A smaller 64-bit AXI-4 interconnect provides access to the Cluster's control registers and enables communication with the FFT accelerator.

The scalar core pre-decodes and dispatches vector instructions via a generic accelerator interface, which also facilitates communication with the DMA, allowing parallel execution with the VU. The VU features 32×512 -bit latch-based vector registers coupled with four Functional Units (FUs), featuring a VLEN of 512-bit and maintaining a throughput of 64-bit/cycle. The Vector Arithmetic Unit (VAU) consists of four mixed-precision Floating Point Units (FPUs) that support FP64, FP32, FP16, BF16, and FP8 (E4M3, E5M2), along with dot product operations featuring higher-precision accumulation, where 8-bit and 16-bit inputs are accumulated into 16-bit and 32-bit results (G16-32/G8-16). Additionally, it includes an Integer Processing Unit (IPU) that supports 8-bit, 16-bit, and 32-bit integer operations. The Vector Slide Unit (VSLDU) handles vector permutation operations, including vector slide up/down and vector move instructions. The Vector Load Store Unit (VLSU) manages the memory-to-register and register-to-memory transfer, supporting indexed, non-unit-strided, and unit-strided memory accesses. Along these three FUs the VTU described in the following Section enhances tensor operations.

IV. UNIFIED VECTOR-TENSOR UNIT

In this Section, we focus specifically on the combination of the VU and the VTU, which is depicted in detail in Fig. 2. To realize the VTU, we augmented the Spatz's FUs with a tightly integrated TU [42] for GEMM and General Matrix-Matrix Operations (GEMM-Ops) execution consisting of two-dimensional array of 12×4 CEs, resulting in a peak performance rate of 48 FMA/cycle.

A. Vector-Tensor Unit Architecture

A Transfer Unit handles data transfers to and from the VRF, providing an input and output bandwidth of 256-bits/cycle. It

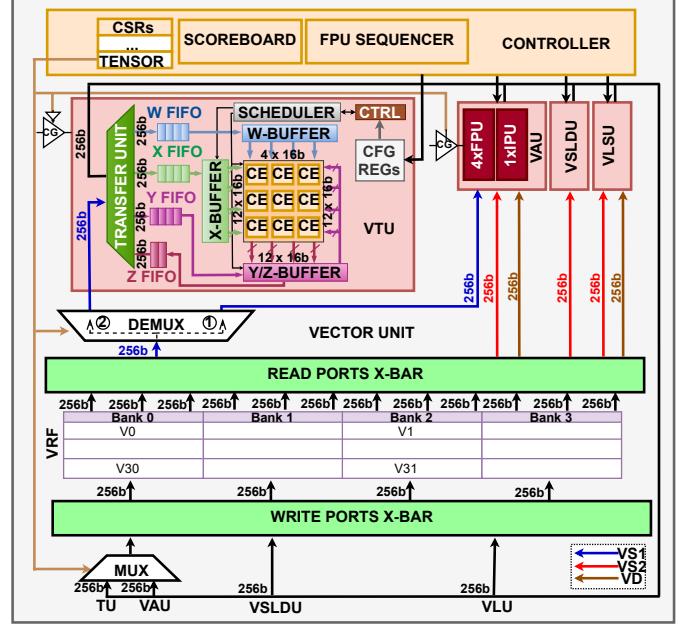


Fig. 2. Vector-Tensor Unit (VTU) architecture and Vector Register File (VRF) interconnect with Vector Functional Units (VFU). The VTU features the transfer unit and X, W, and Z/W buffers filling the 4×12 Computing Elements (CEs) datapath. The Tensor Control Status Register (TCSR) manages Vector-Tensor capabilities.

is equipped with three dedicated buffers: the X-Buffer, which updates the 12-column inputs of the X matrix; the W-Buffer, composed of 4 shift registers, which efficiently distributes new 64-bit/cycle inputs of the W matrix to the CEs; and the Z-Buffer, which simultaneously stores and forwards computed outputs while pre-loading elements from the Y input matrix, functioning as both an output buffer and a pre-load buffer.

The VRF is equipped with 6×256 -bit-wide read ports and 3×256 -bit-wide write ports to support high-bandwidth vector operations efficiently. Of the six read ports, three are dedicated to the VAU, providing the 3×256 -bits/cycle input bandwidth required for operations such as Vector Fused Multiply-Accumulate (VFMACC), which processes three vector inputs. The VAU also utilizes one write port to handle its 256-bits/cycle output. Two additional read ports are allocated to the VLSU for accessing vector data, while the remaining read port is assigned to the VSLDU, supporting sliding operation. The VRF, organized into four banks, features a multi-ported architecture with 3×256 -bit wide read ports and 1×256 -bit wide write port per bank.

To efficiently arbitrate accesses among competing functional units, a priority-based scheme is applied both for read and write operations on each bank. For read operations, port 0 is primarily dedicated to the VAU, granting it the highest priority for accessing the VS2 operand. If the VAU does not utilize the port in a given cycle, the VLSU is granted access to retrieve the VS2 operand. Similarly, port 1 follows a hierarchical priority scheme, with the VAU having precedence for accessing the VS1 operand. When the VAU does not require the port, the VSLDU gains access to fetch its VS2 operand. Finally, port 2 prioritizes the VAU for reading the VD operand. In the absence

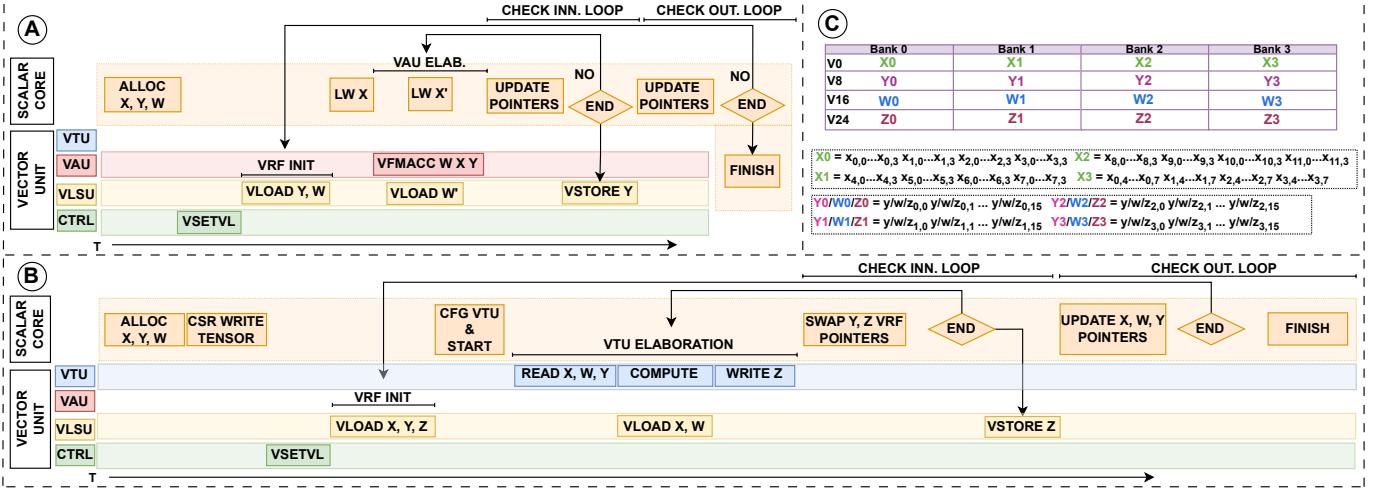


Fig. 3. Vector Arithmetic Unit (VAU) and Vector-Tensor Unit (VTU) temporal execution flow of a general matrix-matrix multiplication (A-B). Vector Register File (VRF) data organization when executing on VTU (C).

of VAU activity, the VLSU is permitted to use the port for VD operand handling.

The write priority scheme for the single write port of each VRF bank ensures efficient operation by giving the highest priority to the VAU for writing arithmetic results. If unused by the VAU, the VLSU gains access for memory operations, followed by the VSLDU, which writes only when neither the VAU nor VLSU requires the port.

A Tensor Control Status Register (TCSR) manages the clock-gating mechanism to disable the unused FUs, optimizing power efficiency while enabling tensor capabilities by multiplexing the VAU's VS1 read port to the TU. Additionally, the TU and the VAU share the same write port to the VRF.

B. Buffer Reduction

A key aspect of this integration is the VTU's buffer size reduction, which is made possible by leveraging the VRF as a shared resource between vector and tensor operations. Using a single 256-bit read port from the VRF, the design supplies data for all 48 CEs over three clock cycles. Each Computing Element (CE) uses its X value for 16 clock cycles, eliminating the need for repeated reads. However, due to the staggered timing of computations across columns—immediate for the first column and delayed by 4, 8, and 12 clock cycles for the subsequent columns—an additional register is introduced for each CE to hold the new X value until it becomes valid for the respective column. This dual-register approach keeps operations synchronized and ensures they run correctly within the required timing. The result is a more efficient X-buffer design that maintains performance with significantly reduced memory overhead.

In the original TU, each CE has a queue of 4x16-bit elements, along with two additional queue slots to synchronize data usage across the processing array, leading to a total buffer size of 576 bytes, calculated as (1):

$$(2 + 4)queue * 48CEs * 16bits = 576B \quad (1)$$

In the integrated VTU design, both queue sizes have been halved per each CE, requiring only 288 Bytes (2).

$$(1 + 2)queue * 48CEs * 16bits = 288B \quad (2)$$

Table II and III provide a detailed comparison of the original TU and the integrated VTU, demonstrating that this optimization results in a 26.5% reduction of the whole buffer capacity with consequent 19.8% buffer area saving. Given that buffers account for 25.6% of the total RedMule area [42], this optimization reduces the TU area by 6%.

TABLE II
TENSOR UNIT BUFFERS CAPACITY

| | RedMule [42] | This work | Reduction |
|----------|--------------|-----------|-----------|
| X buffer | 576 B | 288 B | -50% |
| Y buffer | 384 B | 384 B | 0% |
| W buffer | 128 B | 128 B | 0% |
| Total | 1088 B | 800 B | -26.5% |

TABLE III
TENSOR UNIT AREA BREAKDOWN TSMC65 TECHNOLOGY

| | RedMule [42] [mm ²] | This work [mm ²] | Area Change [%] |
|---------------|---------------------------------|------------------------------|-----------------|
| Engine | 0.572 | 0.567 | -0.9 |
| Buffers | 0.241 | 0.194 | -19.8 |
| Transfer Unit | 0.077 | 0.074 | -3.1 |
| Scheduler | 0.026 | 0.026 | -1.8 |
| Control | 0.025 | 0.025 | -1.7 |
| Total Area | 0.942 | 0.886 | -6.0 |

C. VAU and VTU Execution Flow

Fig. 3 depicts the execution flow of a GEMM, emphasizing how the two computational units—the VAU (A) and the VTU (B)—are engaged to perform the operation. When executing on the VAU Fig. 3a, the scalar core allocates input and output matrices, then fetches and pre-decodes the vector instructions,

delegating their execution to the Vector Functional Units (VFUs). At the inner computation loop setup, the VU dynamically sets the vector length and loads the W and X data into the VRF. We adopt an outer product algorithm to maximize parallelism: a scalar from the input tensor is multiplied by a vector from the weight tensor while the Snitch and the VLSU pre-load, respectively, scalar and vector inputs for the next round. At the end of each iteration, the partial results are stored back in the memory, and the scalar core reassesses the computation's status, updating the pointers as needed. This execution flow relies on tight cooperation between the scalar core and the VU, as the scalar core handles the continuous pre-decoding, fetching, and dispatching of vector instructions.

When performing elaboration on the VTU Fig. 3b, the scalar core handles the initialization phase, which involves allocating the matrices and enabling tensor capabilities by configuring the TCSR, as described in Subsection IV-A. Following this, the scalar core delegates the task of loading X, W, and Y data from the L1 memory into the VRF, leveraging a Length Multiplier (LMUL)=8 configuration. This approach combines eight vector registers into a larger logical register, optimizing data locality and access efficiency.

Fig. 3c depicts how data are organized into the VRF during this process. Specifically, the V0 register is used for managing X-data, with its content distributed across four memory banks. Each bank holds 16×16 -bit elements, sufficient to populate four rows of $4 \times$ CEs progressively. For example, X0 stores elements for CE0,0 to CE3,3, X1 stores elements for CE4,0 to CE7,3, and so on, ensuring efficient data alignment and distribution across the computation elements. The V8 and V16 registers are designated for managing Y and W data, respectively. As illustrated in the legend, these registers follow a consistent loading pattern, with each memory bank handling 16×16 -bit elements required to refill the Y and W buffers efficiently. The VTU uses the V24 register to store Z elements.

When the VRF initialization is complete, the scalar core configures and triggers the VTU execution, while the VLSU simultaneously loads new X and W values. Upon completion, the VTU streams the computed Z back to the VRF. The scalar core then applies double-buffering, swapping the Y and Z pointers used by the VTU while relaunching the inner loop computation. Once this process concludes, the VLSU stores the final Z output, and the outer loop check is performed by updating pointers and reinitializing the VRF for the next iteration.

V. MIXED PRECISION FFT ACCELERATOR

The MP-FFT accelerator shown in Fig. 4 implements a configurable mixed-precision floating-point FP16 and FP32 radix-2 Cooley-Tukey FFT [55] following the template of the fixed-precision accelerator in [56]. In this Section, we describe in detail the architecture of the MP-FFT, as well as the novel floating-point butterfly implementation that we propose and the integration in the Maestro system.

A. MP-FFT Architecture

The accelerator targets IEEE-754 single- and half-precision floating-point arithmetic [57] and supports up to 1024-point

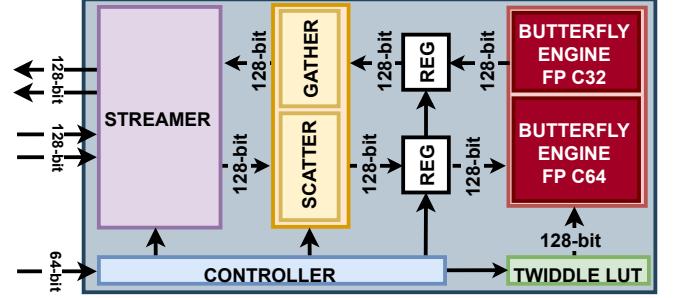


Fig. 4. Multi-Precision FFT Accelerator featuring the Streamer, Controller, Gather and Scatter units, along with two Butterfly Engines: one C32 and one C64.

and 512-point FFT computations for complex data with 16-bit and 32-bit real and imaginary parts, respectively, defined as C32 and C64 formats. Its design implementation consists of several submodules organized in a pipelined architecture described as follows.

The Streamer serves as a specialized DMA unit, efficiently managing data transfers between L1 memory and the accelerator. The MP-FFT accelerator includes four 64-bit memory ports, divided into two input and two output ports. The Controller is responsible for managing the status of various accelerator modules, coordinating their operations, handling the register file used for programming, and controlling the peripheral interconnect. The Gather-Scatter Unit reorganizes the samples. The Scatter module inserts new data from the Streamer into the butterfly registers, while the Gather module extracts processed data and returns it to the Streamer to store it in memory. The Butterfly Registers, comprising a pair of four 64-bit registers, act as temporary storage positioned in front of the Butterfly Unit, which is the main computation engine of the MP-FFT. For coefficient management, the Twiddle Factor Look-Up Tables (LUTs) store precomputed twiddle factors corresponding to the maximum FFT points. The architecture integrates a C64 LUT with 65 elements and two C32 LUTs, each containing 129 elements, ensuring efficient multi-precision support.

At the core of the accelerator, the Floating-Point Butterfly Unit performs the radix-2 FFT computation. It consists of two Butterfly Engines, one FP16 for C32 precision and one FP32 for C64 precision. Each Butterfly Engine incorporates two fused-arithmetic Dual-Output Sum of Dot Product (SDOTP) modules, which are discussed in detail in Sec. V-B. Since the accelerator reuses larger engines to compute lower-precision butterflies, the accelerator can compute either one C64 or two C32 butterflies at each cycle. In case an FFT C32 is performed, the inputs are rearranged to words with the right data size and are scattered to both butterfly engines reusing the C64 Butterfly for C32 computation. At the output, the results of the butterflies are concatenated to come back to two 32-bit complex words.

B. Floating-Point Butterfly Engine Implementation

Each MP-FFT's Butterfly Engine implements the radix-2 DIT butterfly operation.

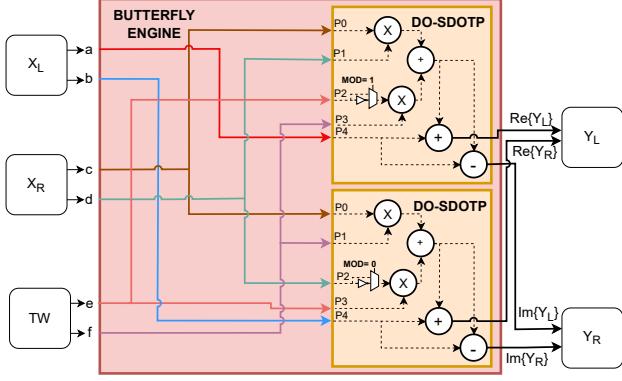


Fig. 5. Floating-Point Radix-2 Butterfly Engine.

By exploiting its symmetry, the butterfly can be rewritten so that the real and imaginary parts of both the left and right-sided can be expressed in the form:

$$E \pm (A \cdot B \pm C \cdot D) \quad (3)$$

This operation can be conveniently implemented as a high-accuracy fused-arithmetic floating-point instruction.

Exploiting this observation, we designed each Butterfly Engine with two fused-arithmetic Dual-Output Sum of Dot Products (DO-SDOTP) units. DO-SDOTP handles subnormal numbers consistently with other IEEE-754 operations, and consists of a five-operand module: four inputs and an accumulator input/output.

We designed the DO-SDOTP module as a parametric design that can be configured to support multiple precision formats ranging from FP8 to FP64; we employed the FP16 and FP32 versions in Maestro. It includes a special input signal, MOD, which inverts the sign of the third operand. As a result, the implemented hardware module is illustrated in Fig. 5.

Compared to a conventional Radix-2 FP datapath, the fused DO-SDOTP datapath avoids precision loss in low-bitwidth FP formats by reducing rounding errors. Each unit instance operates within the largest exponent and mantissa widths defined by the format parameterization, allowing lower-precision computations to be mapped onto the same datapath by assigning narrower exponent and mantissa fields to specific bit positions. The computation starts with mantissa multiplication, producing values at double precision. These are sorted, zero-padded, and aligned by right-shifting based on the exponent difference. A second sorting stage incorporates a fifth operand, ensuring precision consistency. Two adders then perform addition and subtraction, with the sign bit inverted in the exponent datapath. Finally, results undergo normalization and rounding, restoring the original precision.

C. FFT Accelerator Integration

The FFT accelerator is integrated into Maestro's cluster as an HWPE engine, tightly coupled with the 128KiB L1 memory through a low-latency interconnect. The programmability of the accelerator is ensured by connecting the HWPE's control

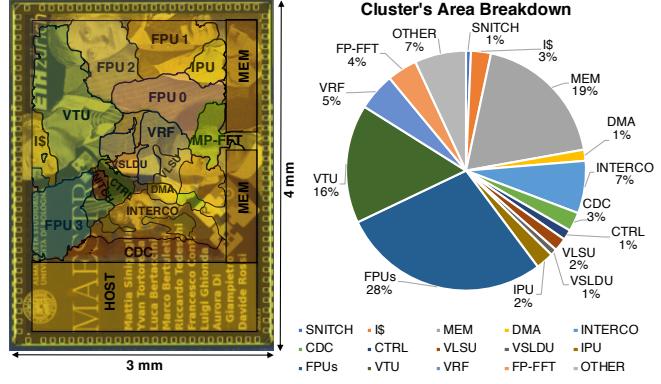


Fig. 6. Chip micrograph and Cluster's area breakdown.

port to the 64-bit AXI-4 crossbar. When an FFT computation needs to be accelerated, the Scalar core in the system configures the accelerator through its memory-mapped control registers and triggers the execution of a job.

The accelerator begins by loading a set of left-wing samples from consecutive memory addresses through the Streamer. In the subsequent cycle, it recovers the corresponding right-wing samples for the same butterflies. The Scatter Unit then reorganizes these samples into two of the four 64-bit registers positioned in front of the Butterfly Unit. Once both the left and right wings of the butterflies are stored in the registers, the Butterfly Unit processes them. After computation, the processed partial results are sampled back into the registers. As the computation progresses, the Scatter Unit continues to insert new inputs into the registers, overwriting samples that the Butterfly Unit has already processed. Meanwhile, the Gather Unit works in tandem with the Scatter Unit, extracting outputs from the butterfly engines and passing them to the Streamer, which sends the processed samples back to memory.

The accelerator outputs data in bit-reversed order, requiring special care during the final FFT stage to avoid banking conflicts when reordering. As a result, only two bit-reversed samples can be written per cycle, temporarily stalling the pipeline to prevent overwriting meaningful data in the accelerator registers. This limitation allows the full output bandwidth to be utilized only in C64 FFTs, while in C32 FFTs, only half of the bandwidth can be exploited.

To optimize power consumption, a two-level clock-gating mechanism has been implemented. At the cluster level, a clock-gating cell completely disables the accelerator when not in use, controlled via a dedicated software-configurable register. At the accelerator level, the accelerator remains inactive, except for the control unit responsible for programming, until execution is triggered. Once the job is completed, the accelerator automatically clock-gates its functional units.

VI. PHYSICAL IMPLEMENTATION AND MEASUREMENTS

Fig. 6 shows the chip micrograph and the area breakdown of the Cluster in the Maestro SoC, highlighting the main building blocks described in Section III. The SoC is implemented in TSMC 65nm CMOS technology and occupies 12mm² (3mm × 4mm) of die area, of which the Cluster domain occupies

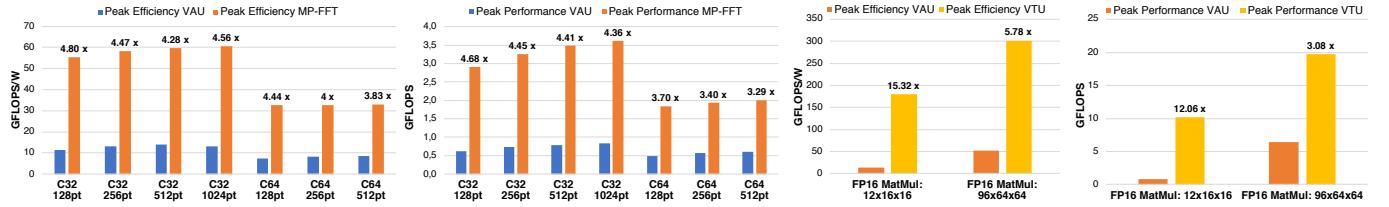


Fig. 7. Peak Performance and Energy Efficiency for FFT and MatMul Kernels over VAU, VTU, and MP-FFT accelerator.

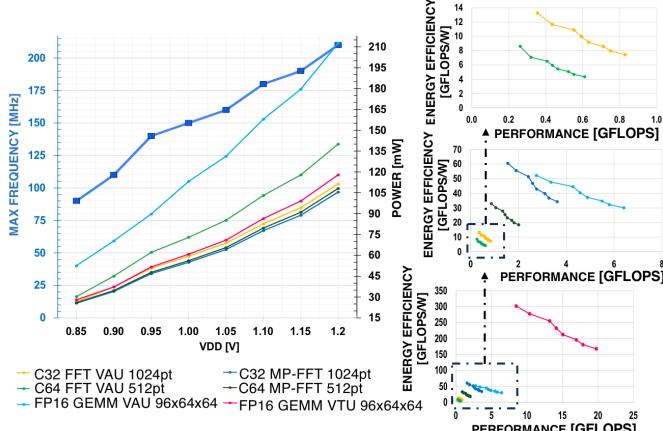


Fig. 8. Power - Frequency and Energy- Performance sweeps for FFT and MatMul Kernels.

7.28mm² (2.8mm × 2.6mm). It has been synthesized with Synopsys Design Compiler 2022.03, while Place & Route has been performed with Cadence Innovus 21.17, and chip finishing with Calibre 2022.3. The chip has been tested and characterized using an Advantest SoC hp9300 integrated circuit testing device.

Fig. 8 illustrates the maximum operating frequency and power consumption across a voltage range of 0.85V to 1.2V for representative computational workloads operating on low data precision FP16-FP32. These workloads include key tasks for embedded machine learning and frequency domain applications, executed on the VAU, VTU, and the MP-FFT accelerator. The Cluster operates within a frequency spectrum from 90MHz at 0.85V to 210MHz at 1.2V, with range power consumption varying from 25mW to 212mW.

An additional overview of the kernels' performance and energy efficiency across all operating points is provided in Fig. 8. Fig. 7 presents a more detailed analysis, focusing on peak performance and energy efficiency for each kernel configuration across different workload sizes for tensor and FFT operations. For MatMul, it evaluates a smaller 12×16 matrix multiplication, while for FFT, it examines different data precisions across various point sizes.

The VTU achieves 98% utilization of its internal FMAs, delivering near-to-ideal performance of 47 actual FMA/cycle on a 96×64 FP16 MatMul (out of 48 ideal FMA/cycle). This represents a 3× and 5.78× improvement over the Vector FPUs, achieving, respectively, a peak performance of 19.8GFLOPS and an energy efficiency of 301.7GFLOPS/W. Even with 50%

utilization on a 12×16 FP16 MatMul, the VTU enhances performance by up to 15× and energy efficiency by up to 12× for MatMul kernels with the same precision compared to VAU.

Similarly, the FFT processor outperforms the VU in both performance and efficiency across various FFT workloads by up to 4.80× and 4.68×, respectively on C32 128-point. Notably, the C32 FFT 1024-point configuration achieves a peak performance of 3.6GFLOPS and a peak efficiency of 60.6GFLOPS/W.

VII. END-TO-END ULTRASOUND APPLICATION

In this section, we present the hardware mapping of the WUS application pipeline to demonstrate the efficiency of the proposed SoC. The application is inspired by the work by Zeng et al. [4] and consists of a preprocessing chain followed by a CNN for gesture classification. Our implementation is designed to process and recognize hand gestures using 8 US transducers, each producing 512 echo samples.

A. Wearable Ultrasound Preprocessing

The preprocessing in Fig. 9 utilizes DSP algorithms to perform amplification, filtering, and envelope detection on A-mode US signal acquisition. Incoming US signals are first amplified using TGC and filtered with Gaussian Filtering (GF) to eliminate noise and enhance relevant information. By leveraging vector operations, the TGC computation processes 512 data samples simultaneously, significantly improving throughput. Implementing the Gaussian filter involves applying a Fourier transform of the US signal using the FFT accelerator and then multiplying transformed data by a Gaussian kernel through the VU, leveraging parallel processing. Finally, the filtered signals are reconstructed via an Inverse Fast Fourier Transform (iFFT), efficiently executed on the FFT accelerator. Envelope detection leverages the HT, with computations distributed between the VU and the FFT accelerator. The process begins with the VU applying a phase shift to the filtered output. Next, the FFT accelerator performs iFFT to reconstruct the signal. Finally, the VU calculates the magnitude to extract the envelope, completing the detection phase. Lastly, the VU performs logarithmic compression on the envelope derived from the HT process, reducing the dynamic range and enhancing the visibility of key signal features.

B. Wearable Ultrasound Machine Learning Model

The CNN model derived from [4] is illustrated in Fig. 9. It comprises three 2D convolutional layers, each followed

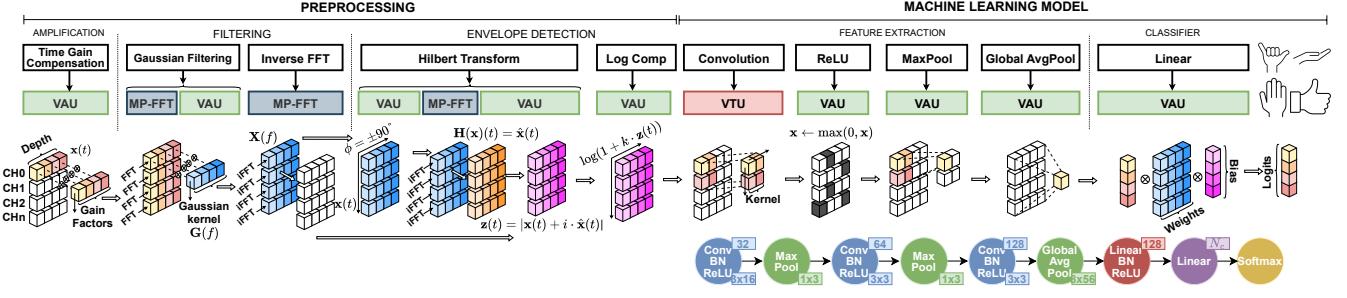


Fig. 9. Wearable Ultrasound A-Mode gesture recognition pipeline on Maestro SoC.

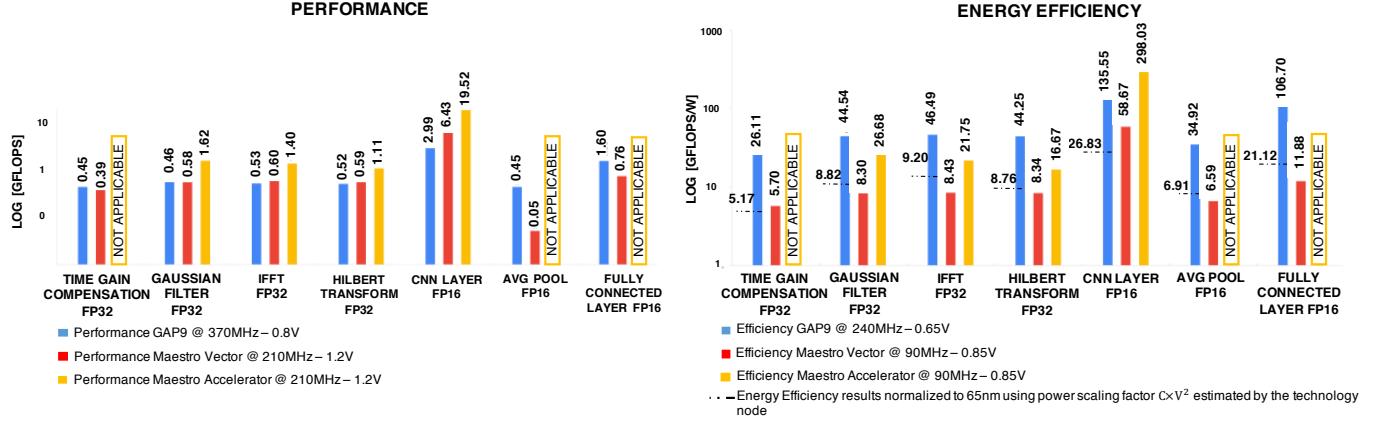


Fig. 10. Wearable Ultrasound A-Mode performance and energy efficiency comparison, showing Maestro executing on the VAU (red), VAU + MP-FFT or VTU (yellow), and GAP9 (blue).

by Batch Normalization (BN), ReLU activation, and Max Pooling (MP), progressively compressing data along the echo dimension while increasing the number of feature maps to 128. In particular, convolutional and BN layers are fused together and executed on the VTU, whereas MP are mapped to the VU. Then, global average pooling is applied, resulting in a 128-dimensional vector, which is passed through a Fully Connected (FC) layer—also followed by BN and ReLU. Likewise, the FC and BN layers are fused together and executed on the VU. Finally, an additional linear layer followed by a softmax activation function produces the probability distribution over the gesture categories.

C. Wearable Ultrasound Mapping and Performance Results

The capabilities of Maestro have been evaluated by running the WUS application on the VAU alone and, where applicable, leveraging the combined execution of the Vector-Tensor-FFT engines. The evaluation focuses on latency, performance, and energy efficiency, comparing results against GAP9, a commercial version of the VEGA SoC [7], developed by GreenWaves Technologies and fabricated in GlobalFoundries 22nm FDX technology, with operating ranges from 0.65 V @ 240 MHz to 0.8 V @ 370 MHz.

The preprocessing phase is evaluated using FP32 precision on both Maestro and GAP9, analyzing the execution time and performance of each individual preprocessing step for a single US channel. This approach enables a precise

comparison of Gaussian Filtering, inverse FFT, and Hilbert Transform on both platforms. The results, shown in Fig. 10, highlight how Maestro outperforms GAP9 in these accelerated tasks, particularly when utilizing the FFT accelerator, which significantly enhances preprocessing efficiency in terms of normalized energy metrics.

The ML model evaluation is performed using FP16 precision on the entire gesture recognition pipeline, where the eight US channels are preprocessed before feature extraction. The VTU demonstrates higher performance in CNN-based feature extraction. Despite the technology scaling difference (TSMC 65nm CMOS vs. GlobalFoundries 22nm FDX), which impacts energy efficiency, the VTU remains 2× more efficient in CNN tasks, achieving 298.03GFLOPS/W.

Fig. 11 presents the execution latency of the WUS application. While Maestro runs at 1.76× slower frequency than GAP9, its VU and the high-performance FFT accelerator enable the preprocessing phase to be completed 2.4× faster than GAP9, demonstrating the efficiency of the architecture in handling frequency-domain and signal processing tasks.

The majority of the ML execution time is consumed by CNN computations, whereas average pooling and fully connected layers account for less than 1% of the total execution time considering GAP9 execution. The primary reason for the suboptimal performance of the average pooling layer on the VU is its reliance on reduction operations, which are not well-suited to leverage the VU's capabilities. Additionally, the

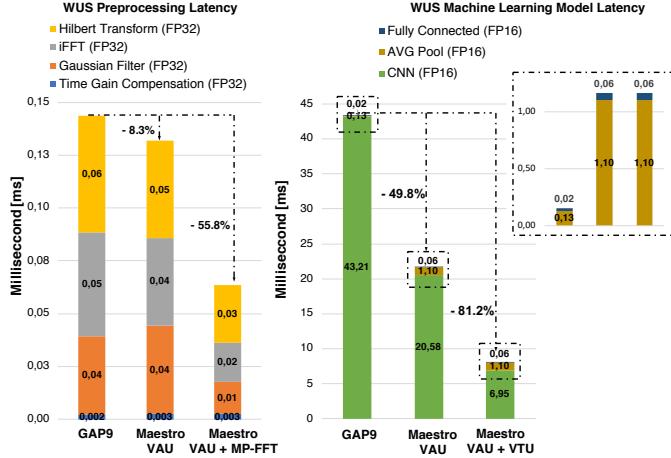


Fig. 11. Wearable Ultrasound A-Mode execution latency on GAP9, Maestro VAU only and Maestro VAU + MP-FFT or VTU.

vector-matrix multiplication used in fully connected layers reduces the parallelism of the VU, limiting its ability to achieve maximum throughput. However, since these two layers contribute only 1% to the total computation time, the overall performance impact remains minimal. The computational power of the VTU effectively compensates for the performance limitations of the average pooling and fully connected layers. While the VU achieves a $2\times$ speedup compared to GAP9, the VTU accelerates CNN-based feature extraction by up to $6.2\times$, reducing the ML execution time by 81%. Overall, the entire WUS application is executed $5\times$ faster on the highly specialized architecture of Maestro.

D. Wearable Ultrasound Maestro Platform: Power and Lifetime Analysis

We conceptualized the Maestro WUS platform, inspired by Frey et al. [48], to enable efficient on-device US processing. The analytical study in Fig. 12 considers a 320mAh, 3.7V LiPo battery powering a system composed of eight US transducers, a transducer controller for managing data acquisition, and the Maestro SoC, which receives input samples via SPI. The platform is configured to acquire 512 echo samples per frame at a frame rate of 39Hz.

By pipelining the acquisition phase with the preprocessing and ML model, described in Section VII-A and Section VII-B, respectively, this system fully supports energy-efficient WUS edge processing. The platform achieves up to 94 hours of battery life at Maestro’s highest energy efficiency point, consuming 12mW and 2.5mJ, while at peak performance conditions, it operates for 82 hours, consuming 14mW and 2.9mJ.

VIII. SOA COMPARISON

Table IV compares the Cluster of Maestro against a selection of state-of-the-art SoC with vector, tensor, and FFT processors. Compared to YUN [21], Maestro meets the requirement of low power consumption (21mW - 212mW) for a wearable device, while YUN relies on a less efficient

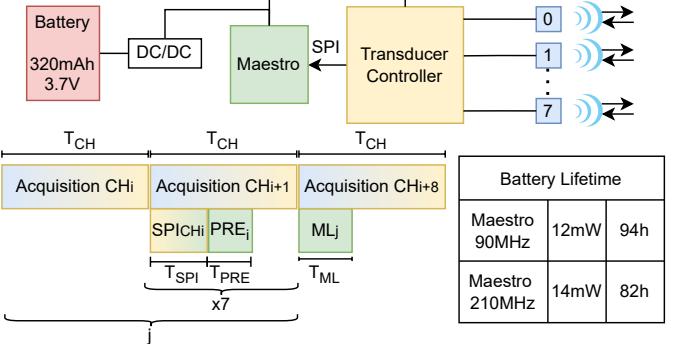


Fig. 12. Power and Lifetime Analysis of Maestro-based WUS processing platform.

architecture tuned for HPC, resulting in lower efficiency (-28% compared to FP32 execution in Maestro’s vector unit and $2.57\times$ compared to FP16). The FFT accelerators in [26], [27] are limited to fixed-point precision, making them less suitable for WUS applications with wide data ranges. Maestro’s FFT accelerator supports floating-point data, with only 50% lower efficiency than ECHOES [26] in C32int and $6.3\times$ lower than [27], which targets a more aggressive technology node (16nm). Maestro’s tensor unit achieves 301.7GFLOPS/W, 19.8GFLOPS@FP16 outperforming YUN [21] in terms of peak performance and [7], [21] in energy efficiency on GEMM kernels. Compared to Darkside [25], Maestro provides similar energy efficiency and slightly better performance with significantly improved flexibility due to the tight Vector-Tensor integration and FFT processor tuned for frequency domain processing. Maestro achieves a notable $2.33\times$ improvement in energy efficiency over VEGA [7] for FP16 tensor operations. While VEGA provides balanced performance across FP16 and FP32, Maestro’s architecture enhances FP16 performance by up to $6\times$ on the tensor unit and $2\times$ on the vector unit, with a $0.9\times$ factor in FP32. Furthermore, in an end-to-end WUS application, Maestro’s VAU achieves a $2\times$ speedup. In contrast, its VTU accelerates CNN-based feature extraction by up to $6.2\times$ compared to VEGA, resulting in an overall $5\times$ faster WUS execution on Maestro. Thus, Maestro paves the way for entirely shifting US processing to the edge, reducing reliance on external computation while enhancing latency, power efficiency, and system autonomy for WUS applications.

IX. CONCLUSION

We presented Maestro, a specialized SoC designed to bring WUS processing to the edge, eliminating the need to offload computation to remote PCs. By integrating frequency-domain and tensor acceleration within a compact and efficient embedded vector architecture, Maestro minimizes latency, power consumption, and privacy concerns, making it well-suited for wearable applications. Fabricated in low-cost TSMC 65nm CMOS technology, Maestro features an RV32-based Cluster featuring compact Vector-Tensor accelerators and a versatile multi-precision FFT engine enabling efficient execution of embedded workloads across diverse computational domains within a 212mW power envelope. The WUS application eval-

TABLE IV
COMPARISON WITH SOA SOCS.

| | [21] <i>YUN</i> | [26] <i>ECHOES</i> | [27] <i>LTE/Wi-Fi FFT SoC</i> | [25] <i>DARKSIDE</i> | [7] <i>VEGA</i> | <i>MAESTRO</i> (this work) |
|--|--|---|----------------------------------|--|---|--|
| <i>Technology</i> | 65-nm TSMC | 65-nm TSMC | 16-nm FinFET | 65-nm TSMC | 22-nm CMOS FDSOI | 65-nm TSMC |
| <i>Die size [mm²]</i> | 6 | 4 | 1.28 | 12 | 12 | 12 |
| <i>Application</i> | Vector | IoT+FFT | IoT+FFT | IoT+NSAA+DNN+QNNs | IoT+NSAA+DNN | IoT+Radar+FFT |
| <i>Cores</i> | RV64GCV0.9 | 1xRV32FXpulp+FFT | Rocket-Chip | 8xRISCY-NN RVC32IMFxPulpNN2 | 10xR15CY RVC32IMFxPulp | 1xRV32IMC + 1xRVV 1.0 ZVE64d |
| <i>Supply Voltage [V]</i> | 0.85–1.2 | 0.9–1.2 | 0.57–0.9 | 0.75–1.2 | 0.5–0.8 | 0.85–1.2 |
| <i>Frequency [MHz]</i> | 100–280 | 150–350 | 40–320 | 40–290 | 32e-3–450 | 90–210 |
| <i>Power range [mW]</i> | 57–330 | 8–133.5 | 0.46–22 | 12–213 | 1.7e-3–49.4 | 21–218 |
| <i>FP precision</i> | FP64, FP32 | FP32 | FP16, FP32, FP64 | FP16, FP32 | bfloat16, FP16, FP32 | FP64, FP32, FP16, BF16 FP8 (4,3), FP8 (5,2) |
| <i>FPU</i> | 4 × FP64 | 1 × FP32 | 1 × FP64 | 4 × FP32 + 32 × FP16 | bfloat16, 4 × FP32 | 4 × FP64 + 48 × FP16 |
| <i>FFT Accelerator Peak Perf</i> | - | 10.16 GOPS ^{A,4} 5.8 GOPS ^{B,3} 3.2 GOPS ^{D,1} | 8.60 GOPS ^{C,2} | - | - | 3.6 GFLOPS^{B,3} 2 GFLOPS^{D,1} |
| <i>FFT Accelerator Peak Efficiency</i> | - | 200 GOPS/W ^{A,4} 89.5 GOPS/W ^{B,3} 41.6 GOPS/W ^{D,1} | 380.55 GOPS/W ^{C,2} | - | - | 60.6 GFLOPS/W^{B,3} 33 GFLOPS/W^{D,1} |
| <i>Tensor Peak Perf [GFLOPS]</i> | - | - | - | 18.2 ^b | - | 19.8^b |
| <i>Tensor Peak Eff [GFLOPS/W]</i> | - | - | - | 300 ^b | - | 301.7^b |
| <i>FP Peak Perf [GFLOPS]</i> | 2.83 ^d 5.70^c | 0.16 ^c | 320 MFLOPS ^{*b} | 1.02 ^b 1.02 ^c | 3.3 ^b 2 ^c | 12.6 ^a 6.6^b 3.28 ^c |
| <i>FP Peak Eff [GFLOPS/W]</i> | 10.8 ^d 23.4 ^c | 9.68 ^c | - | 6.2 ^b 5 ^c | 129^b 79^c | 114.10^a 60.23 ^b 29.85 ^c |

FP Precision: a) FP8 - b) FP16 - c) FP32 - d) FP64 **FFT format:** A) C16 - B) C32 - C) C48 - D) C64

FFT points: 1) 512 - 2) 972 - 3) 1024 - 4) 2048 **Notes:** (*) Estimated from the paper

suation demonstrates that this WUS-optimized architecture significantly accelerates processing while maintaining ultra-low power consumption of 12mW, with an energy consumption of 2.5mJ. Maestro balances general-purpose vector acceleration (60.2 GFLOPS/W, 6.6 GFLOPS @ FP16) with the efficiency of the Tensor Unit (301.7 GFLOPS/W, 19.8 GFLOPS @ FP16) and the FFT accelerator (60.6 GFLOPS/W, 3.6 GFLOPS @ C32).

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