For memory map details check in the reference manual:

A memory map with text and images

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A close-up of a table

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Bus domains:

* There are 4 peripheral busses: APB1, APB2, AHB1, AHB2. They have their own base addresses
* AHB is used for peripherals that need high speed data communication
* APB is used for peripherals that need low speed communication

To reset all the peripheral registers in one shot, use the following register:

A computer error message

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**GPIO Pin interrupt Configuration:**

1. Pin must be in input mode
2. Configure the edge trigger (RE, FE, RFE)
3. Enable interrupt delivery from peripheral to the processor
4. Identify the IRQ number
5. Configure IRQ priority for the identified IRQ number
6. Enable interrupt reception on that IRQ number
7. Implement the ISR handler

Not: The ISR handlers should be implemented in the application layer of the program by overriding the default handler. The ISR handler then should call the driver supported function to process the request

**STM32 GPIO Pin Specifications**

* Vdd is the main power supply of the microcontroller, provided externally
* Standard operating voltage of Vdd: 1.8<=Vdd<=3.6V. Max voltage on Vdd pin: 4 V
* Vss is ground reference of the microcontroller and should be 0V
* Minimum Vss = -0.3V

A screenshot of a computer

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STM32 pins:

1. Three-volt tolerant (TT)
2. Five volt tolerant (FT)
3. Three-volt tolerant directly connect to the ADC (TTa)

General operating condition for TT & TTa pin: 0.3 V <= Vin <= Vdd + 0.3 V

FT pin:

* 0.3 V <= Vin <= 5.5 V
* GPIO is FT in input mode (not applicable when GPIO is in output or analog mode)
* FT GPio, max Vin is Vdd + 0.4 V

A screenshot of a table

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A screenshot of a computer

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Vil: maximum voltage level that is interpreted as a logical 0 by a digital input

ViH: minimum voltage level that is interpreted as as a logical 1 by a digital input

VoL: maximum output voltage low level voltage which can be interpreted as logic low

VoH: the minimum output high level voltage which can be interpreted as logic high

**SPI Details**

* Allows communication between one master and one or more slave devices
* 4 I/O pins for communication with external device
* MISO: Master In/Slave out data – pin used to transmit data in slave mode and receive data in master mode
* MOSI: Master Out/ Slave in data – pin used to transmit data in master mode and receive date in slave mode
* SCK: serial clock output pin for SPI master and input pin for SPI slaves
* NSS: slave select pin – depending on SPI and NSS settings, this pin can be used to select an individual slave device for communication
* Slave’s data comm lines (MISO, MOSI) will be in high impedance state until SS line is pulled to ground.

Slave management:

1. Software slave management

* Set SSM bit in the SPIx\_CR1 reg as 1
* Pin is grounded internally

1. Hardware slave management

* Set SSM bit in the SPI\_CR1 reg as 0
* The NSS pin must be grounded manually

SPI Communication Format:

* Format depends on the clock phase, clock polarity, and data frame format
* CPOL (clock polarity) – controls the idle state value of the clock when noi data is being transferred
* CPOL is reset, the SCLK pin has low-level idle state. If set to high, SCLK pin has high-level idle state
* CPHA controls at which clock edge of the SCLK the data should be sampled by the slave
* Combination of CPOL (clock polarity) and CPHA (clock phase) bits selects the data capture clock edge

**A close-up of a data register

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A black and white diagram

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