ECE 459: Project Design Review

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Project Choice

Opted for the logic obfuscation project

Steps involved in this project include:

- Determining testability of each node ✅
- Ranking nodes based on efficiency ⬛
- Determining the number of key gates and placing them ⬛
  - Hamming Distance

HOPE Fault Simulator

Chose to use HOPE for fault analysis portion of the project

- Allows for the calculation of the testability of each node
- Proven to reduce fault simulation time for circuits (good for the required large circuit)
- Need to rank results of analysis

Currently able to run HOPE. Results appear later in slideshow

- ./hope -r 32 -F s27.fault -D s27.test
  - S7.fault is shows faults detected after each test
  - -D ensures that we are shown the outputs resulting from the fault
  - * denotes the output is incorrect as a result of fault

Fault Impact: HOPE Output

- Test runs generate fault file
  - Exemplifies faults
  - Stuck at 1 or 0
- Flags only faults that affect output
- Filter through data to find number of faults

425 lines (425 sloc) | 5.68 KB

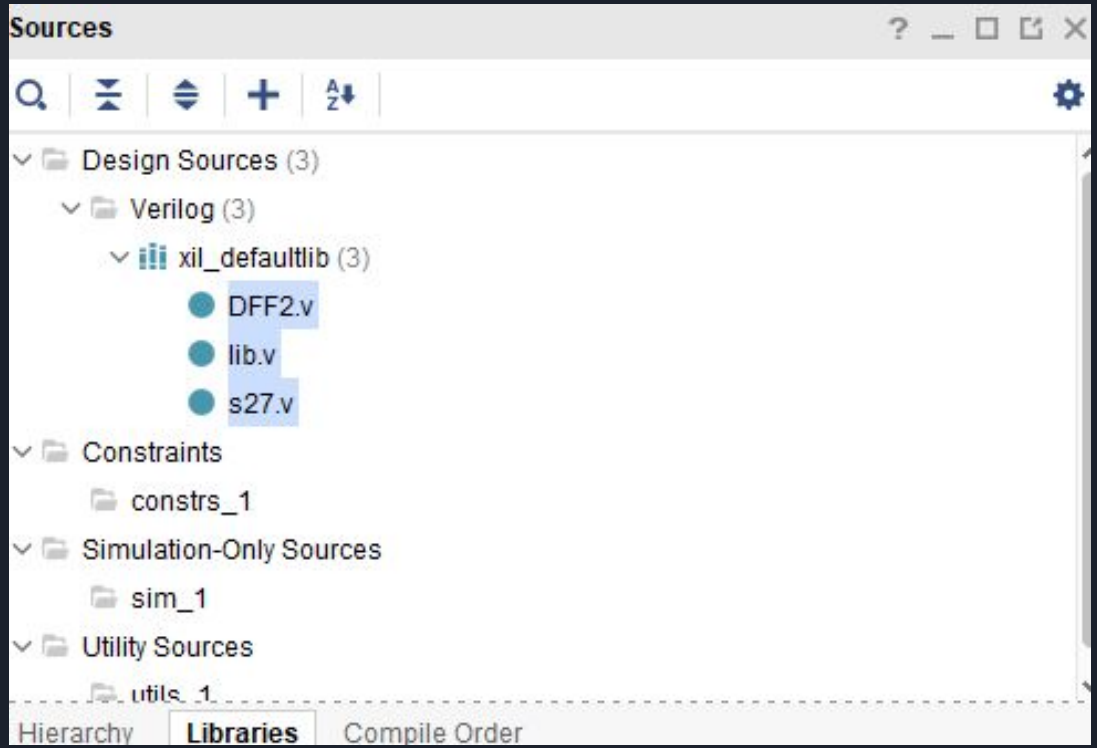
```
test    1: 0100 x
  G17 /1: 1
  G17 /0: 0
  G11 /1: 0
  G12->G15 /0: x
  G8->G15 /0: 1
  G8->G16 /0: 1
  G3 /0: x
  G5 /0: x
  G11 /0: 1
  G9 /0: x
  G15 /1: x
  G16 /1: x
  G10 /0: x
  G10 /1: x
  G14->G10 /0: x
  G11->G10 /0: x
  G14 /1: x
  G14 /0: 1
  G8 /1: x
  G14->G8 /1: x
  G11->G6 /0: x
  G8 /0: 1
  G6 /1: x
  G11->G6 /1: x
  G12 /1: x
  G7 /0: x
```

Fault Impact: Calculation

$$\text{Fault Impact} = (\text{NoP}_0 \cdot \text{NoO}_0 + \text{NoP}_1 \cdot \text{NoO}_1).$$

	A	B	C	D	E	F	G
1	S27.bench						
2	node	s-a-0 faults	s-a-1 faults	outputs effected by sa0	outputs affected by sa1	FAULT IMPACT	
3	G0	0	0	0	0	0	
4	G1	1	0	1	0	1	
5	G2	1	0	1	0	1	
6	G3	1	0	1	0	1	
7	G4	0	0	0	0	0	
8	G5	1	0	1	0	1	
9	G6	0	1	0	1	1	
10	G7	1	0	1	0	1	
11	G8	1	1	1	1	2	
12	G8->G15	1	0	1	0	1	
13	G8->G16	1	0	1	0	1	
14	G9	1	0	1	0	1	
15	G10	1	1	1	1	2	
16	G11	1	1	1	1	2	
17	G11->G6	1	1	1	1	2	
18	G11->G10	1	0	1	0	1	
19	G12	1	1	1	1	2	
20	G12->G15	1	1	1	1	2	
21	G12->G13	1	0	1	0	1	
22	G13	1	1	1	1	2	
23	G14	1	1	1	1	2	
24	G14->G10	1	0	1	0	1	
25	G14->G8	0	1	0	1	1	
26	G15	0	1	0	1	1	
27	G16	0	1	0	1	1	
28	G17	1	1	1	1	2	
29							

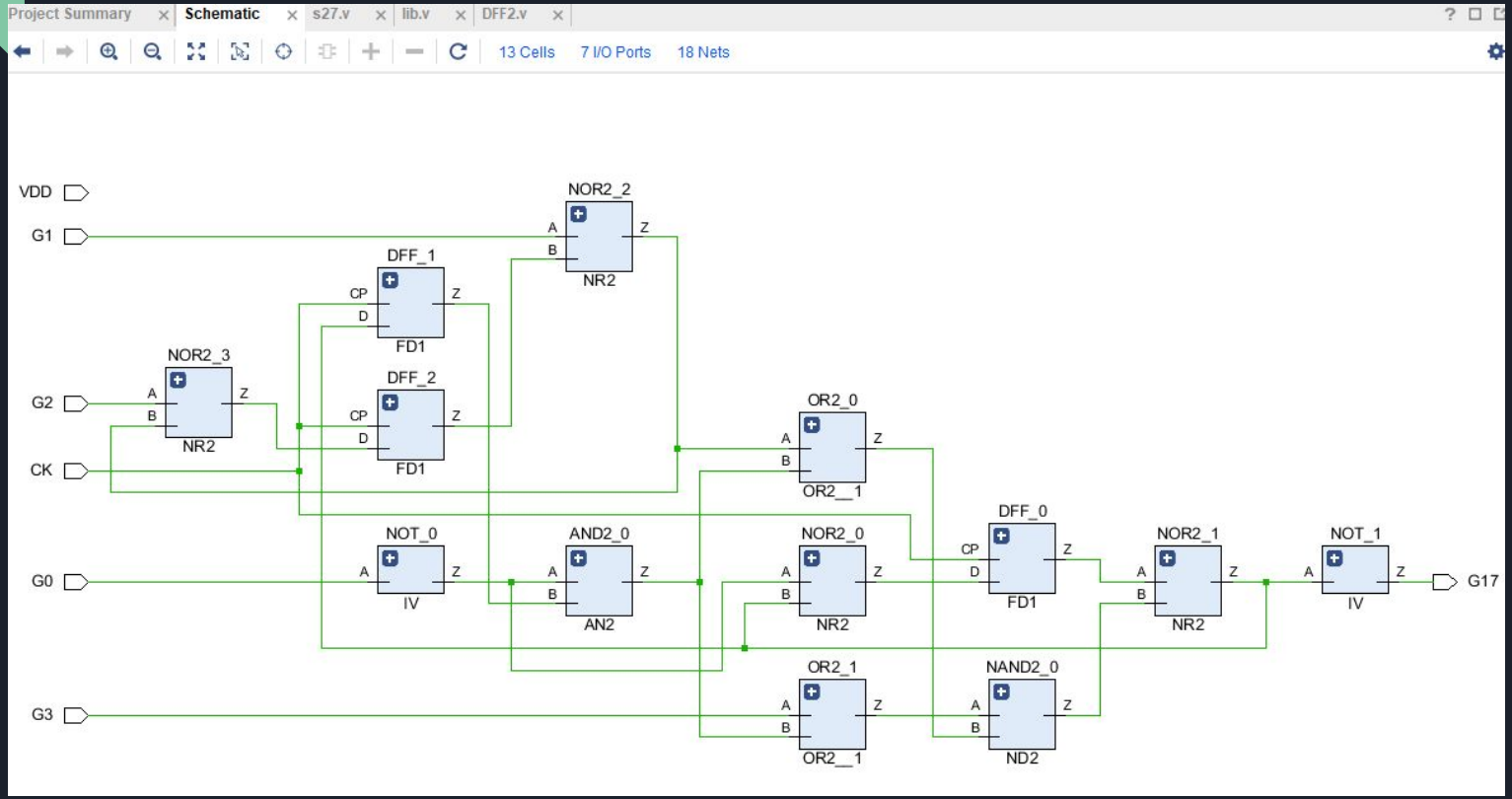
Viewing the ISC Files in Vivado



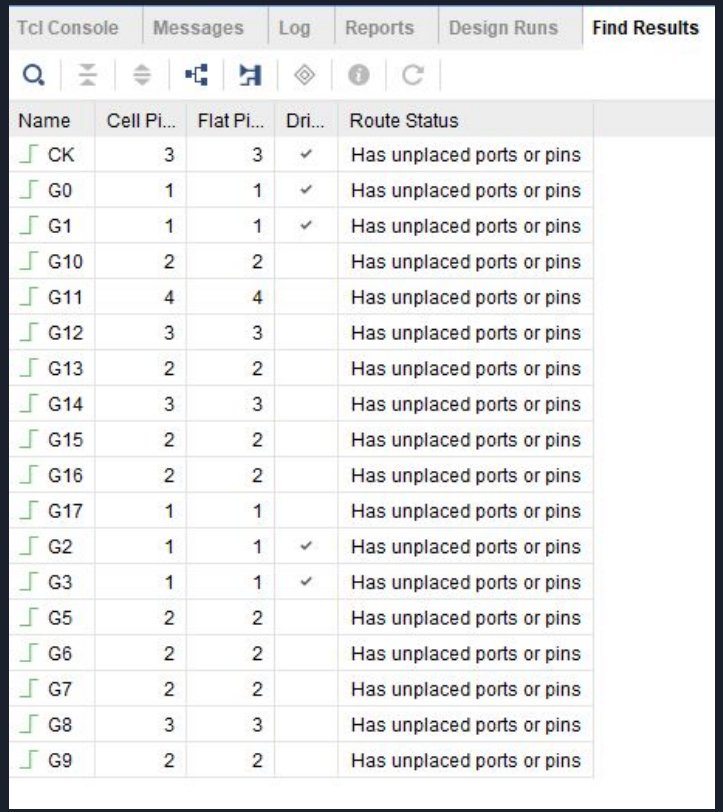
Verilog s27.v

```
module s27(VDD,CK,G0,G1,G17,G2,G3);
input VDD,CK,G0,G1,G2,G3;
output G17;

  wire G5,G10,G6,G11,G7,G13,G14,G8,G15,G12,G16,G9;

  FD1 DFF_0(CK,G5,G10);
  FD1 DFF_1(CK,G6,G11);
  FD1 DFF_2(CK,G7,G13);
  IV  NOT_0(G14,G0);
  IV  NOT_1(G17,G11);
 AN2 AND2_0(G8,G14,G6);
  OR2 OR2_0(G15,G12,G8);
  OR2 OR2_1(G16,G3,G8);
  ND2 NAND2_0(G9,G16,G15);
  NR2 NOR2_0(G10,G14,G11);
  NR2 NOR2_1(G11,G5,G9);
  NR2 NOR2_2(G12,G1,G7);
  NR2 NOR2_3(G13,G2,G12);

endmodule
```

Vivado - Elaborated Design



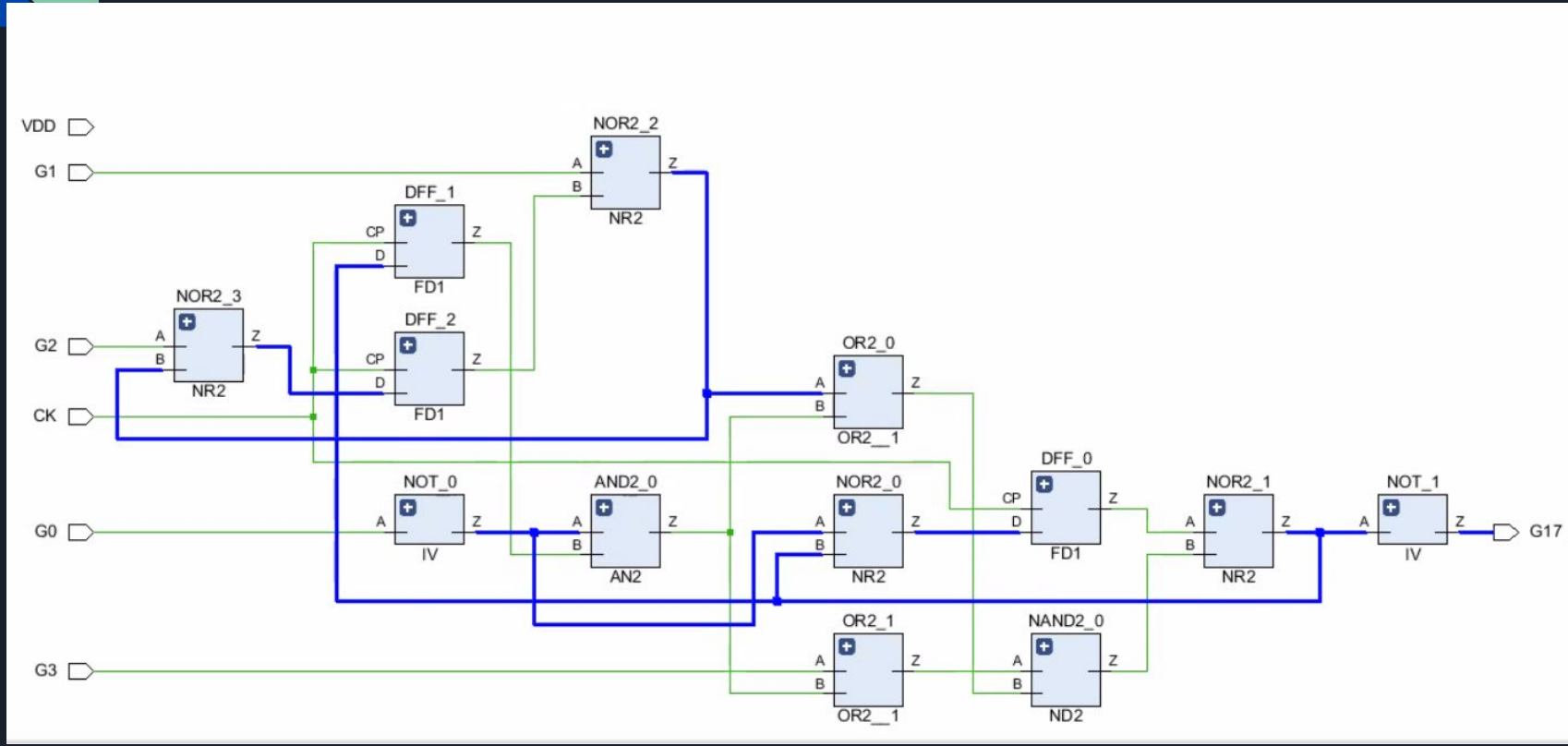
Vivado - Nets/Nodes



Tcl Console | Messages | Log | Reports | Design Runs | **Find Results**

Name	Cell Pi...	Flat Pi...	Dri...	Route Status
CK	3	3	✓	Has unplaced ports or pins
G0	1	1	✓	Has unplaced ports or pins
G1	1	1	✓	Has unplaced ports or pins
G10	2	2		Has unplaced ports or pins
G11	4	4		Has unplaced ports or pins
G12	3	3		Has unplaced ports or pins
G13	2	2		Has unplaced ports or pins
G14	3	3		Has unplaced ports or pins
G15	2	2		Has unplaced ports or pins
G16	2	2		Has unplaced ports or pins
G17	1	1		Has unplaced ports or pins
G2	1	1	✓	Has unplaced ports or pins
G3	1	1	✓	Has unplaced ports or pins
G5	2	2		Has unplaced ports or pins
G6	2	2		Has unplaced ports or pins
G7	2	2		Has unplaced ports or pins
G8	3	3		Has unplaced ports or pins
G9	2	2		Has unplaced ports or pins

Vivado - Nodes with high fault impact



Moving Forward

- Using Fault Results
  - Calculating testability
  - Hamming Distance
  - Observability
- Further Circuit Implementation
- Final Considerations