



STM32 CubeMX

1. Description

1.1. Project

Project Name	nucleo_G0B1RE_driver4
Board Name	NUCLEO-G0B1RE
Generated with:	STM32CubeMX 6.10.0
Date	07/22/2024

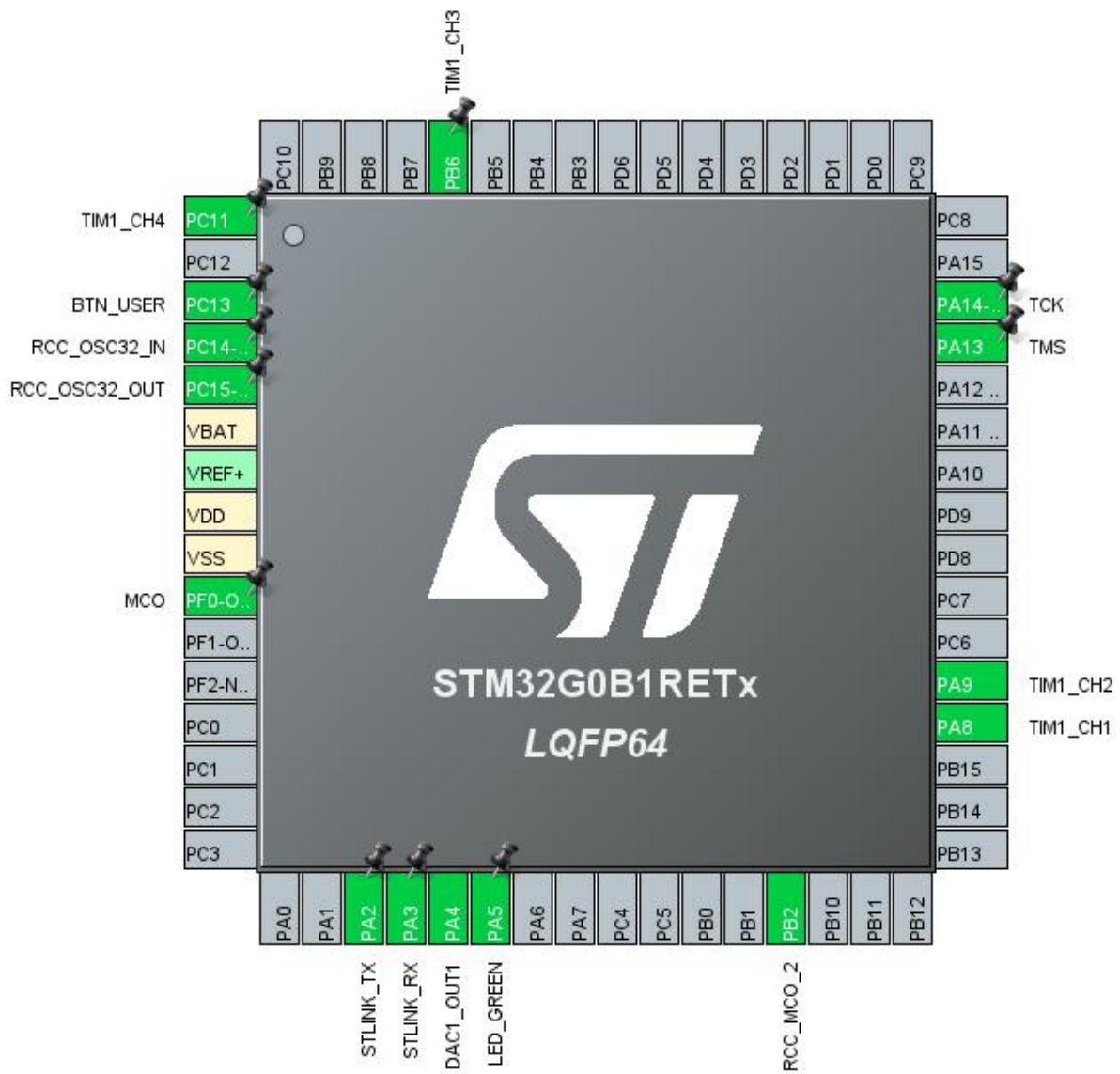
1.2. MCU

MCU Series	STM32G0
MCU Line	STM32G0x1
MCU name	STM32G0B1RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M0+
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2. Pinout Configuration

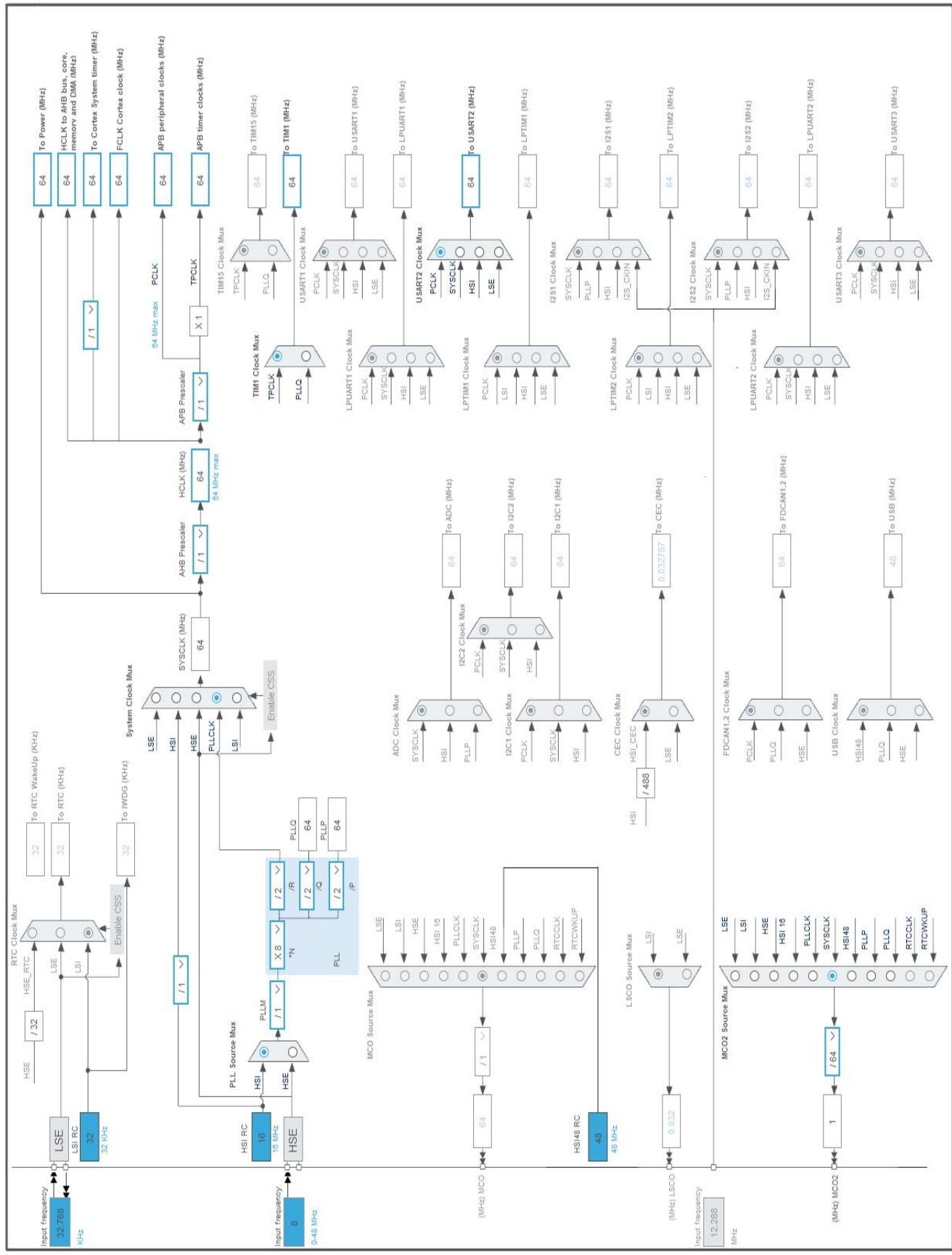


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PC11	I/O	TIM1_CH4	
3	PC13 *	I/O	GPIO_Input	BTN_USER
4	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
5	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
6	VBAT	Power		
8	VDD	Power		
9	VSS	Power		
10	PF0-OSC_IN (PF0)	I/O	RCC_OSC_IN	MCO
19	PA2	I/O	USART2_TX	STLINK_TX
20	PA3	I/O	USART2_RX	STLINK_RX
21	PA4	I/O	DAC1_OUT1	
22	PA5 *	I/O	GPIO_Output	LED_GREEN
29	PB2	I/O	RCC_MCO_2	
36	PA8	I/O	TIM1_CH1	
37	PA9	I/O	TIM1_CH2	
45	PA13	I/O	SYS_SWDIO	TMS
46	PA14-BOOT0	I/O	SYS_SWCLK	TCK
60	PB6	I/O	TIM1_CH3	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	nucleo_G0B1RE_driver4
Project Folder	C:\Users\John\code\STM32CubeIDE\PBM_Device_Code\nucleo_G0B1RE_driver
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G0 V1.6.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART2_UART_Init	USART2
4	MX_TIM1_Init	TIM1
5	MX_DAC1_Init	DAC1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32G0
Line	STM32G0x1
MCU	STM32G0B1RETx
Datasheet	DS13560_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

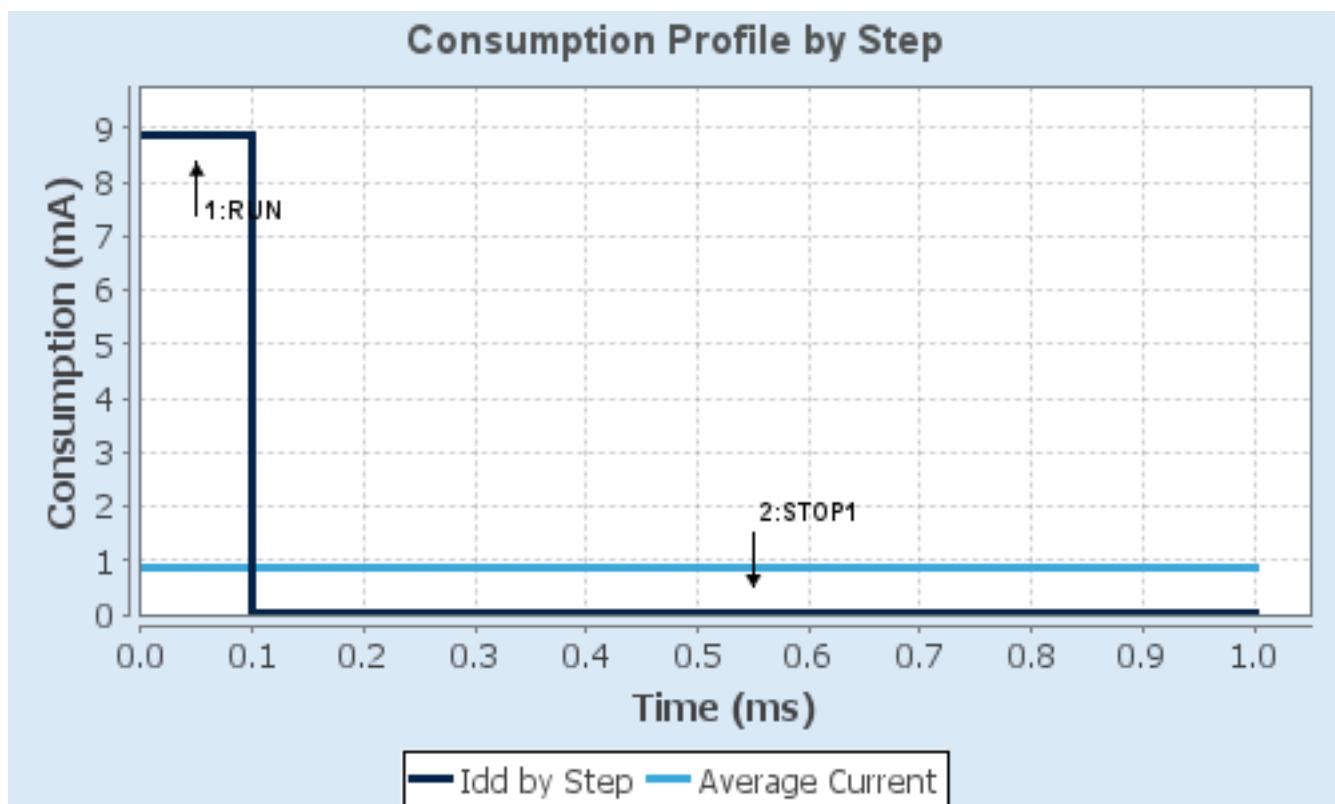
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	Range1-High
Fetch Type	SRAM1/Flash-PowerDown/D_SRAM1	Flash-PowerDown/D_SRAM1/Cache
CPU Frequency	64 MHz	16 MHz
Clock Configuration	HSI PLL	HSI
Clock Source Frequency	16 MHz	16 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.85 mA	7.05 µA
Duration	0.1 ms	0.9 ms
DMIPS	80.0	20.0
T_a Max	127.77	130
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	891.34 µA
Battery Life	5 months, 6 days, 4 hours	Average DMIPS	26.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. DAC1

OUT1 connected to: only external pin

2.1.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

2.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Master Clock Output 2

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE
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2.3. SYS

mode: Debug

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

2.4. TIM1

Clock Source : Internal Clock

Channel1: Output Compare CH1

Channel2: Output Compare CH2

Channel3: Output Compare CH3

Channel4: Output Compare CH4

2.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	64000 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Enable *
Off State Selection for Idle Mode (OSSI)	Enable *
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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Output Compare Channel 1:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Toggle on match *
Pulse (16 bits value)	8000 *
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Toggle on match *
Pulse (16 bits value)	16000 *
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	Toggle on match *
Pulse (16 bits value)	24000 *
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

2.5. USART2

Mode: Asynchronous

2.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

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Configuration Report

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN (PF0)	RCC_OSC_IN	n/a	n/a	n/a	MCO
	PB2	RCC_MCO_2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	TMS
	PA14-BOOT0	SYS_SWCLK	n/a	n/a	n/a	TCK
TIM1	PC11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BTN_USER
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LED_GREEN

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 capture compare interrupt	true	0	0
PVD through EXTI line 16, PVM (monit. VDDIO2) through EXTI line 34		unused	
Flash global interrupt		unused	
RCC global Interrupt		unused	
TIM1 break, update, trigger and commutation interrupts		unused	
TIM6, DAC and LPTIM1 global Interrupts		unused	
USART2 + LPUART2 Interrupt		unused	

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 capture compare interrupt	false	true	false

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Computing	Utilities
DMA	DAC1	TIM1	USART2			
GPIO						
I2VIC						
RCC						
SYS						

5. Docs & Resources

Type	Link
IBIS models	https://www.st.com/resource/en/ibis_model/stm32g0_ibis.zip
System View	https://www.st.com/resource/en/svd/stm32g0_svd.zip
Description	
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
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Device Option https://www.st.com/resource/en/device_option_list/opl_stm32g0b1.txt

Lists

Errata Sheets https://www.st.com/resource/en/errata_sheet/es0548-stm32g0b1xbxcxe-

	device-errata-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00748675.pdf
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