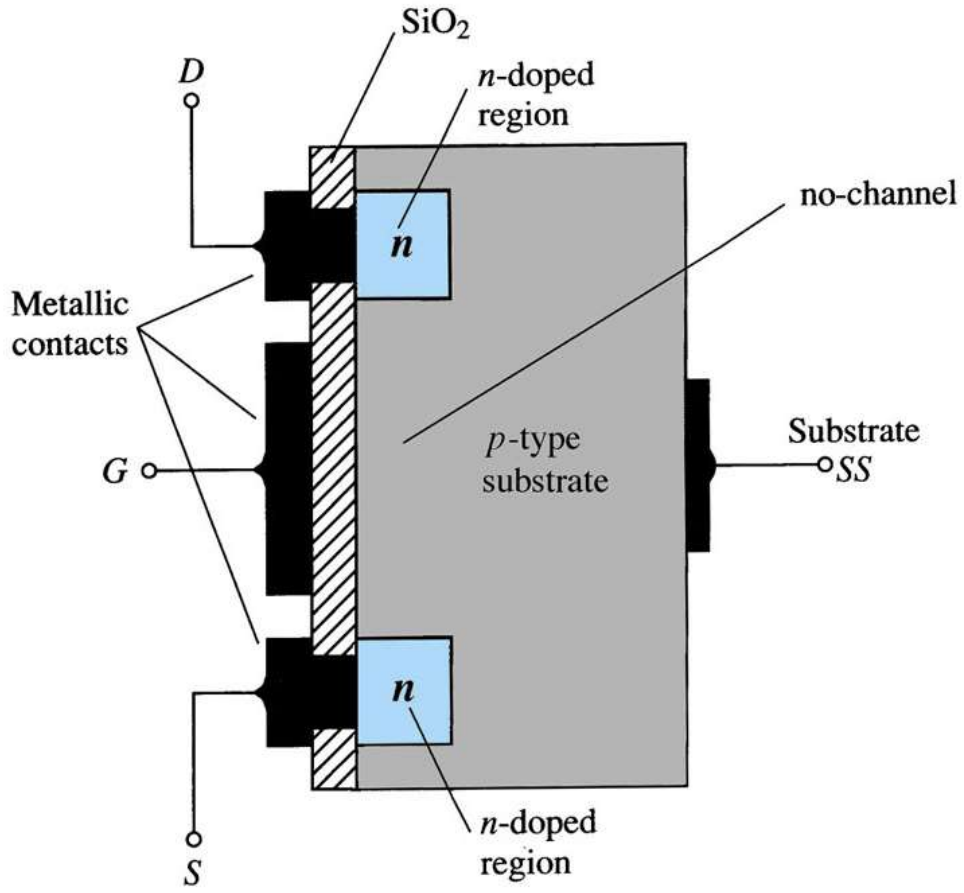
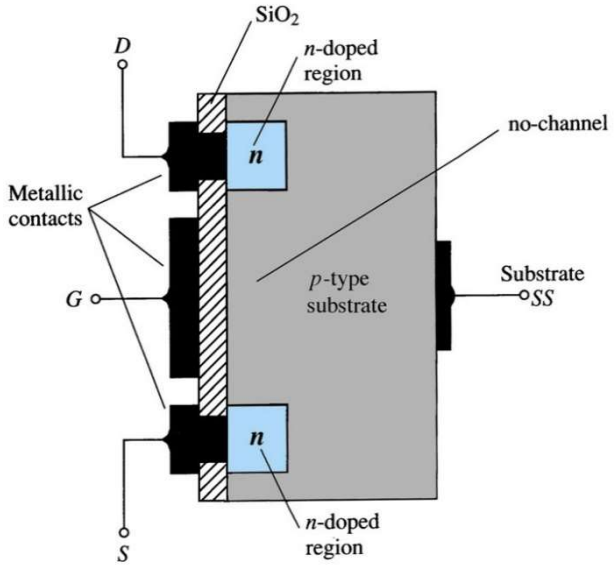
MOSFETs



1971: Intel 4004, ~2300 transistores MOSFETs

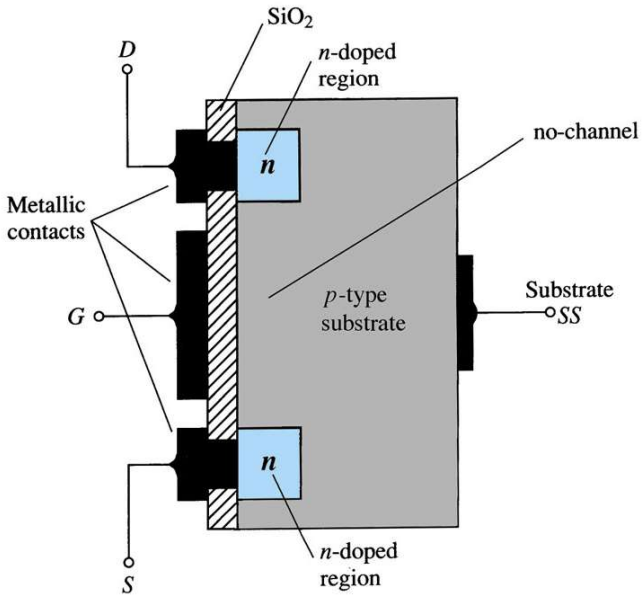
MOSFETs

Metal
Oxide
Semiconductor



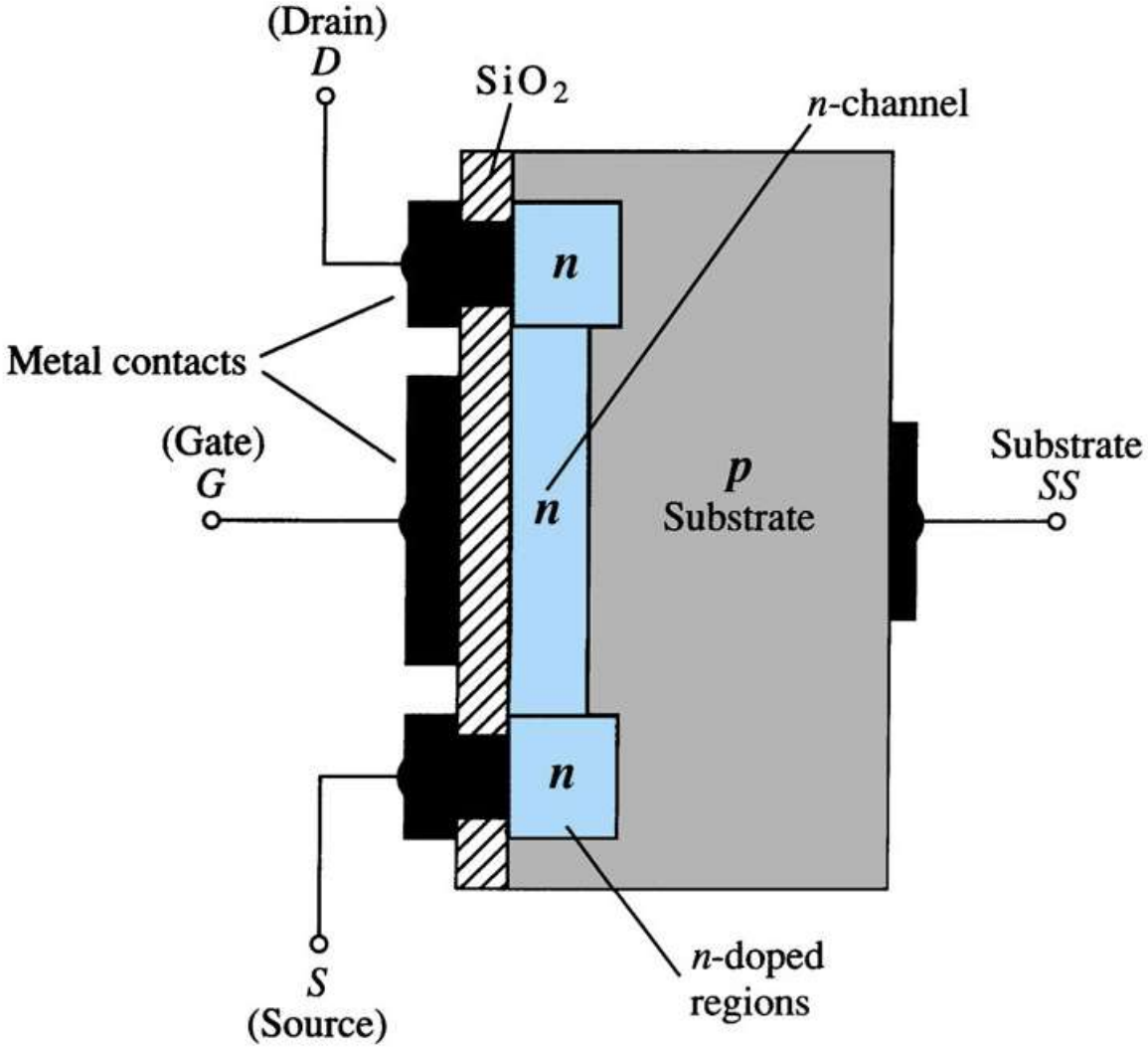
- Motivação
- Estrutura
- Funcionamento
- Polarização (alimentação)
- Chave digital (porta lógica)

MOSFET x TBJ

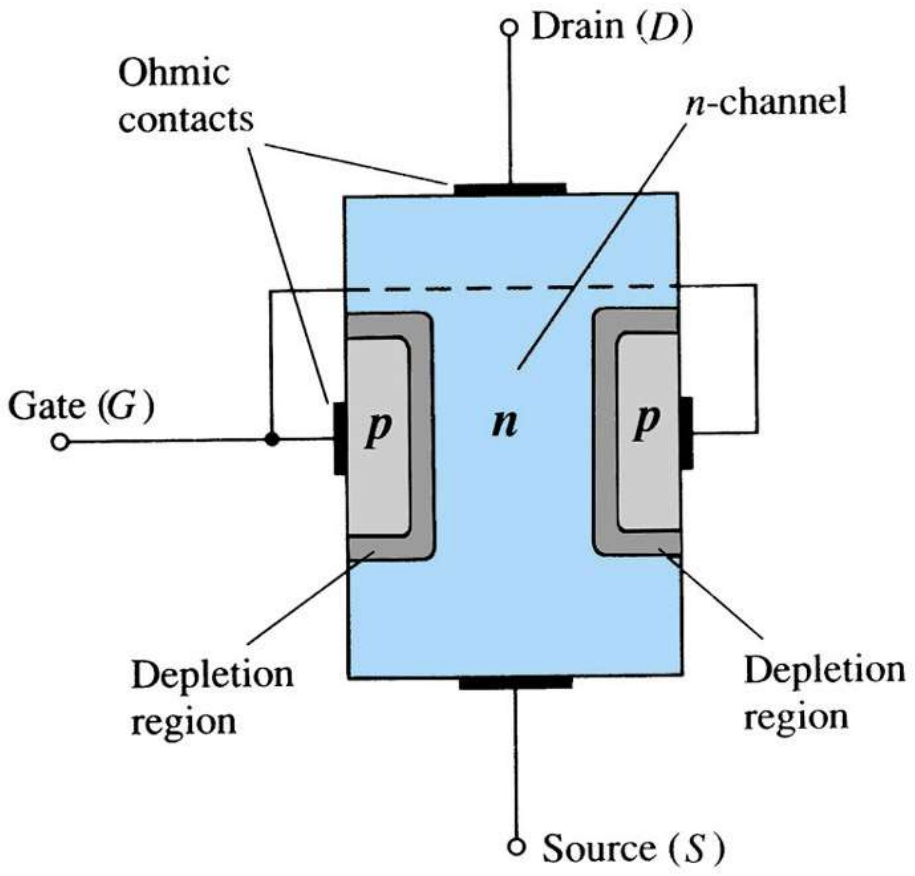


- Menor tamanho
- Menor consumo de energia
- Não necessita de resistor de polarização em circuitos digitais (CMOS)

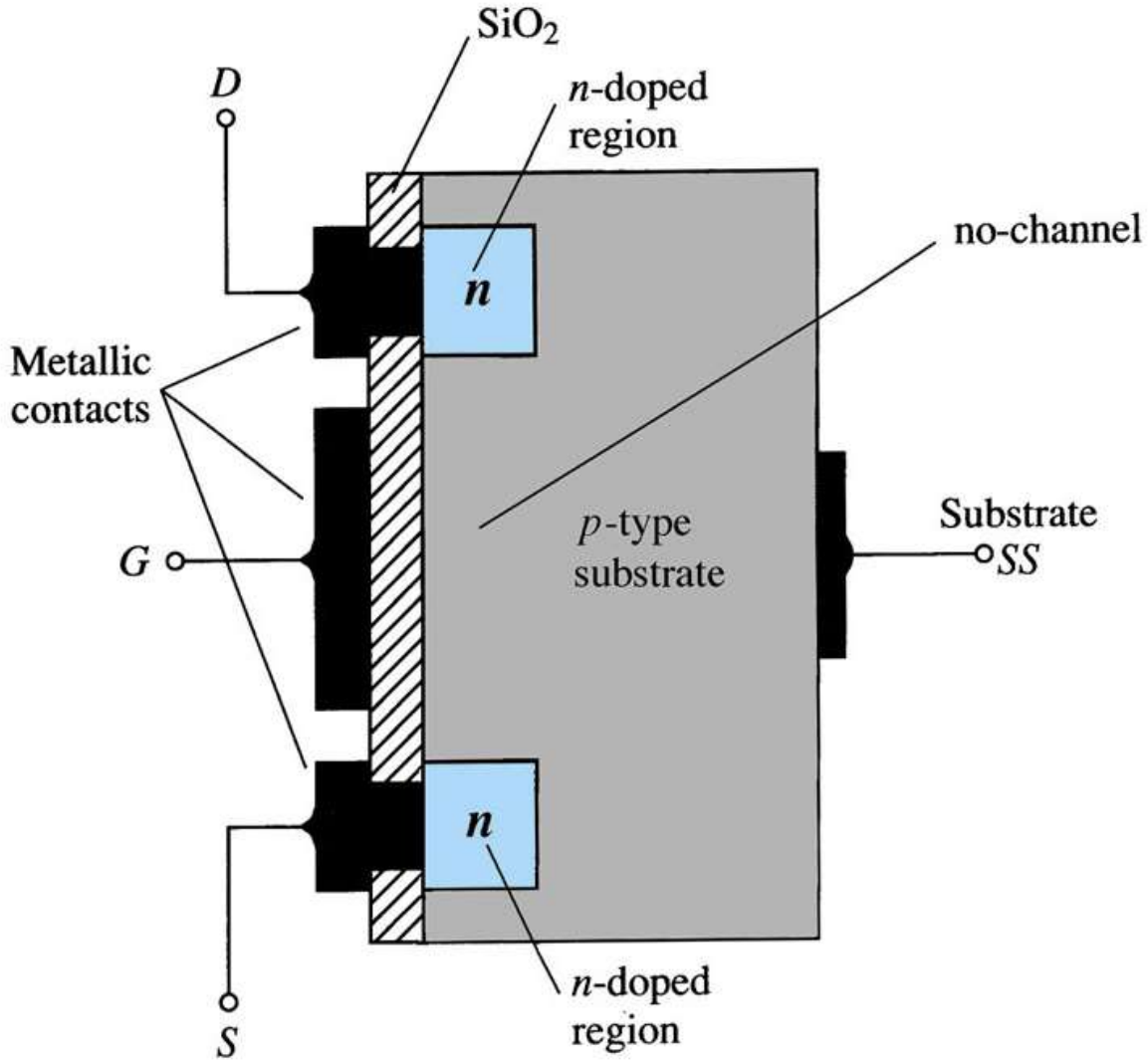
1 - MOSFET de Depleção



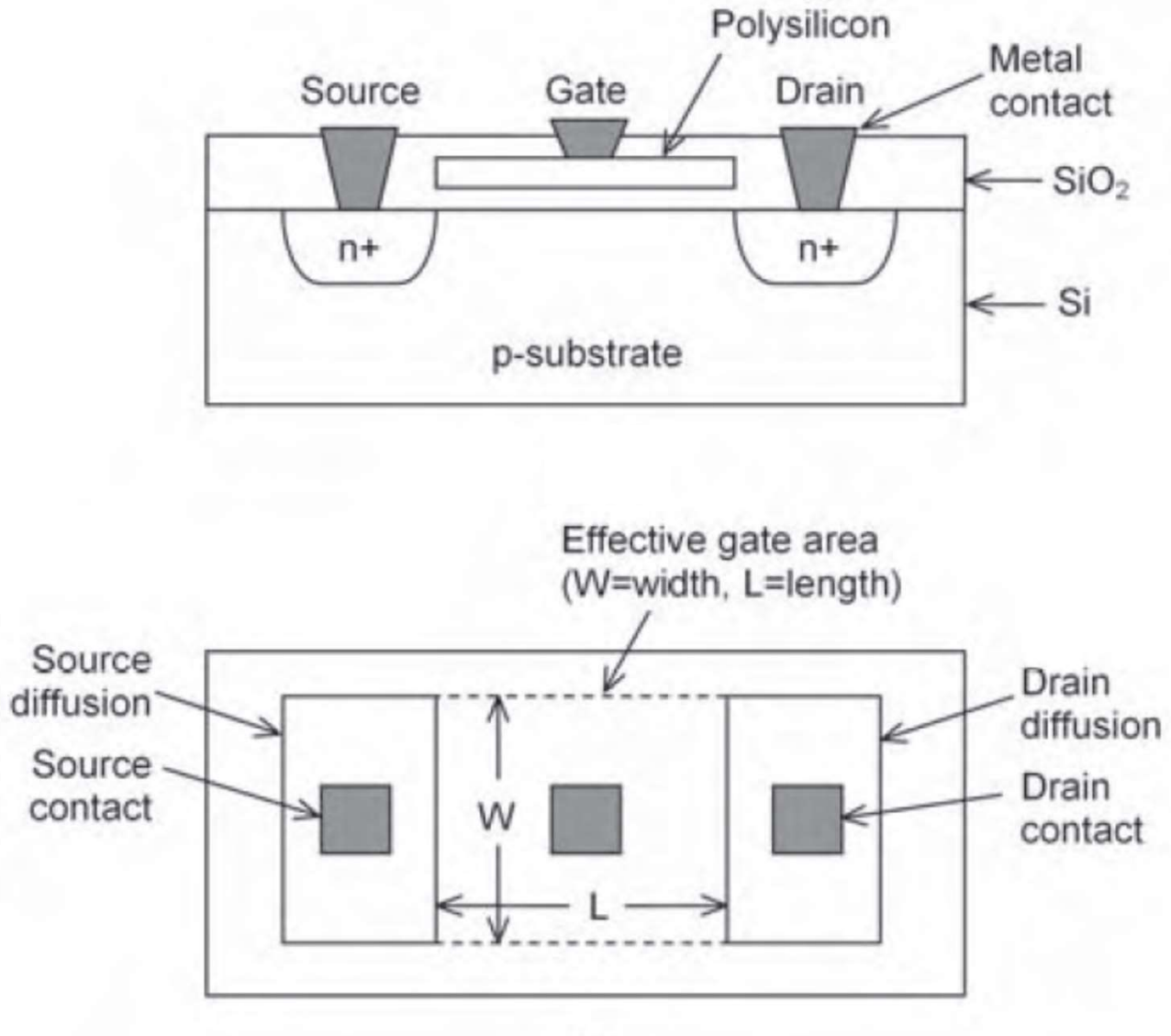
Relembrando o JFET



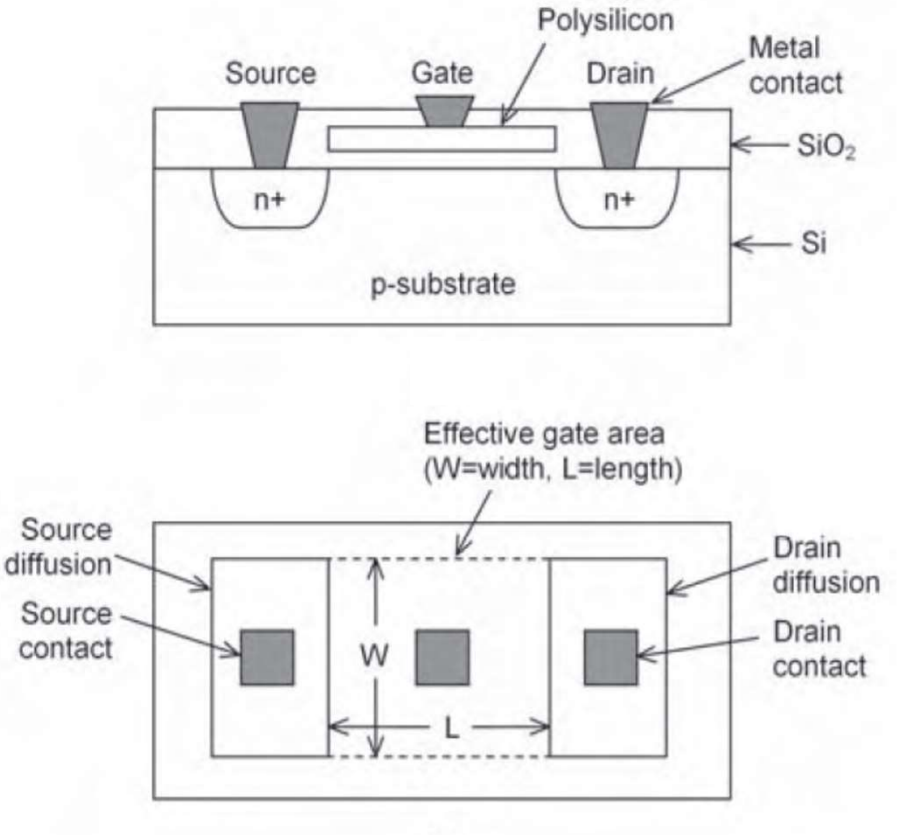
2 - MOSFET de Intensificação



Estrutura - MOSFET de Intensificação



Parâmetros construtivos



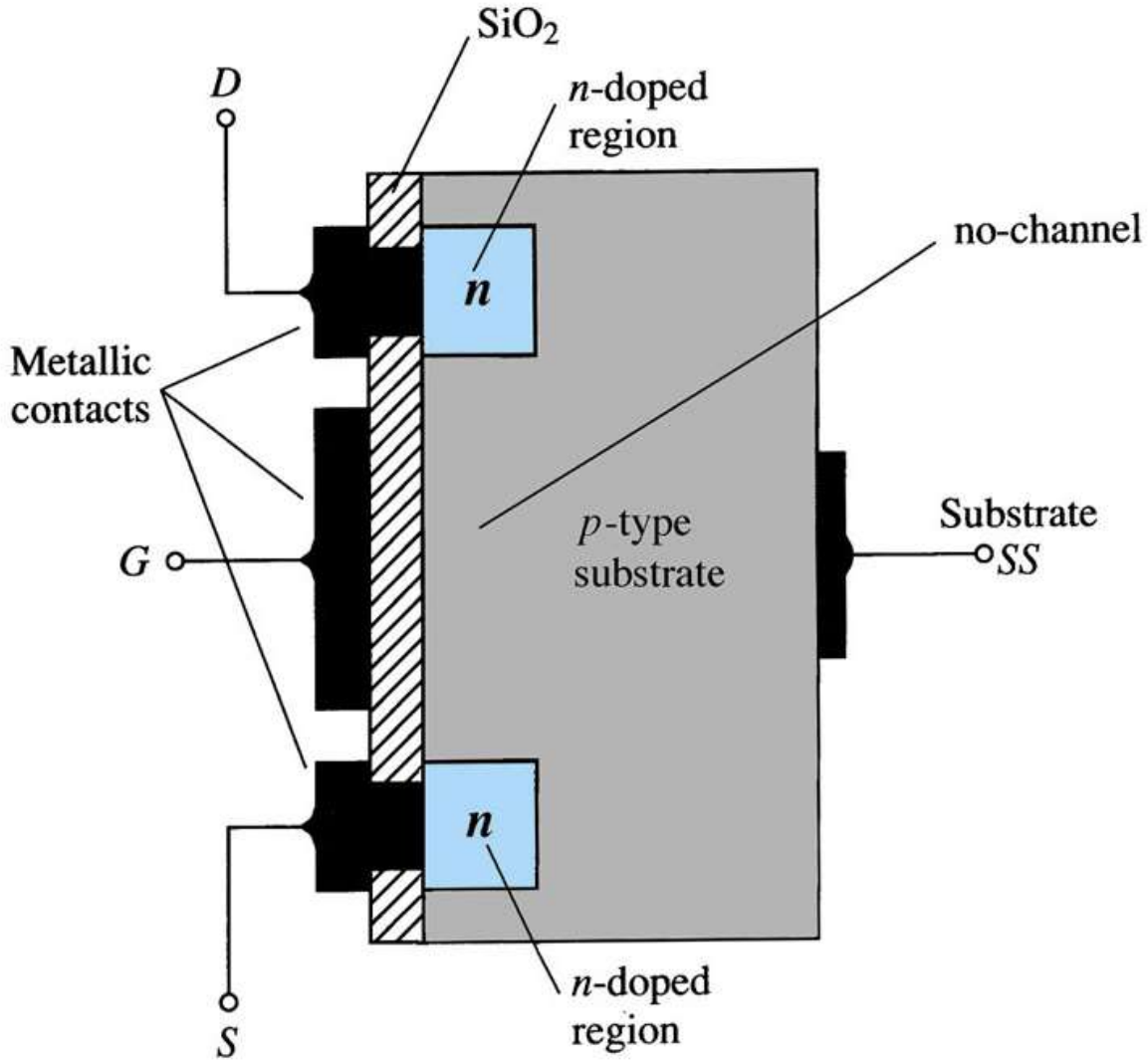
$$\beta = \mu C_{OX}\left(\frac{W}{L}\right)$$

$V_T \rightarrow$ Tensão de limiar

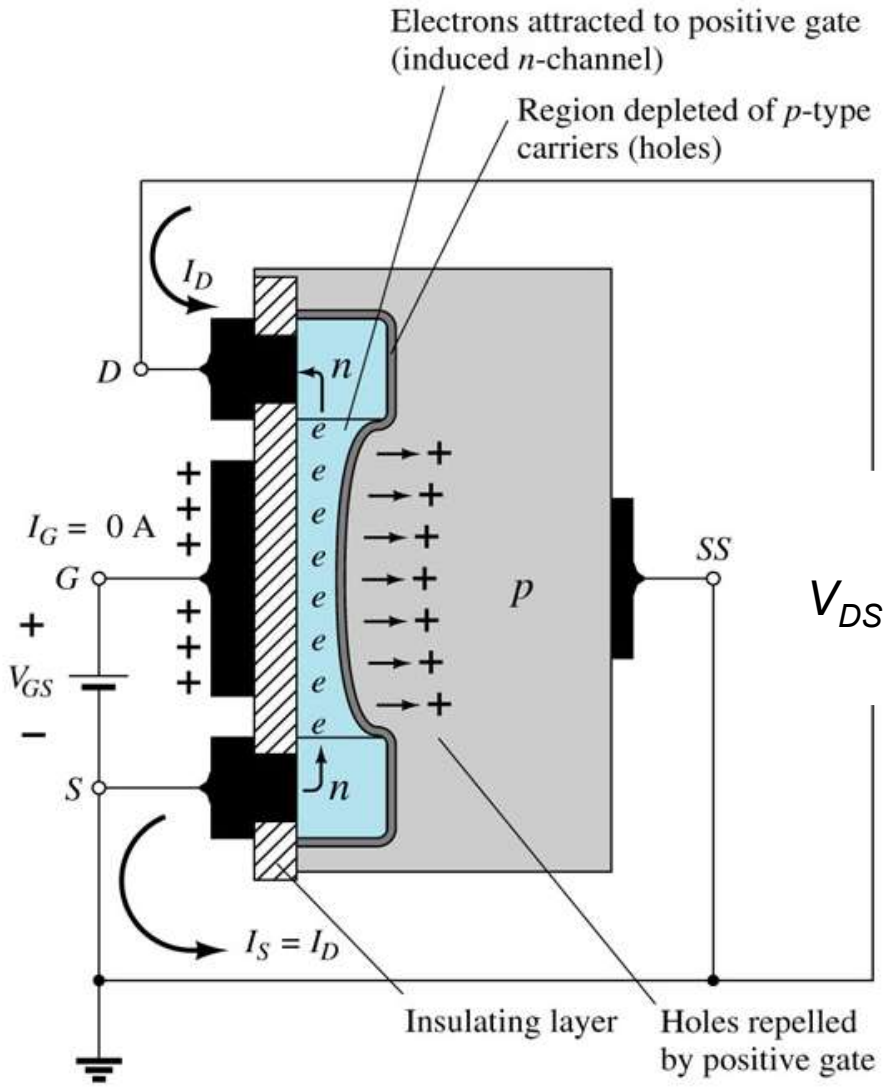
Funcionamento

nMOSFET de Intensificação

nMOSFET de Intensificação



Formação do Canal

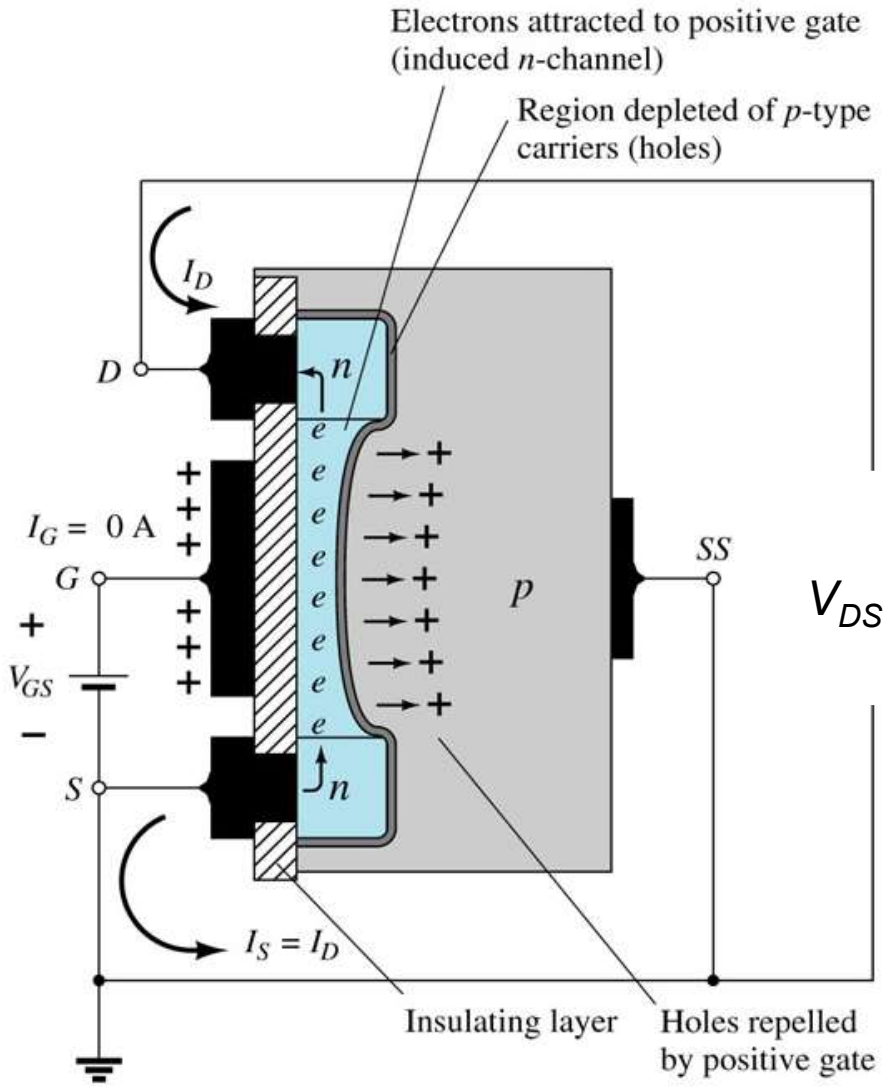


$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} = 0\ V$

Formação do Canal

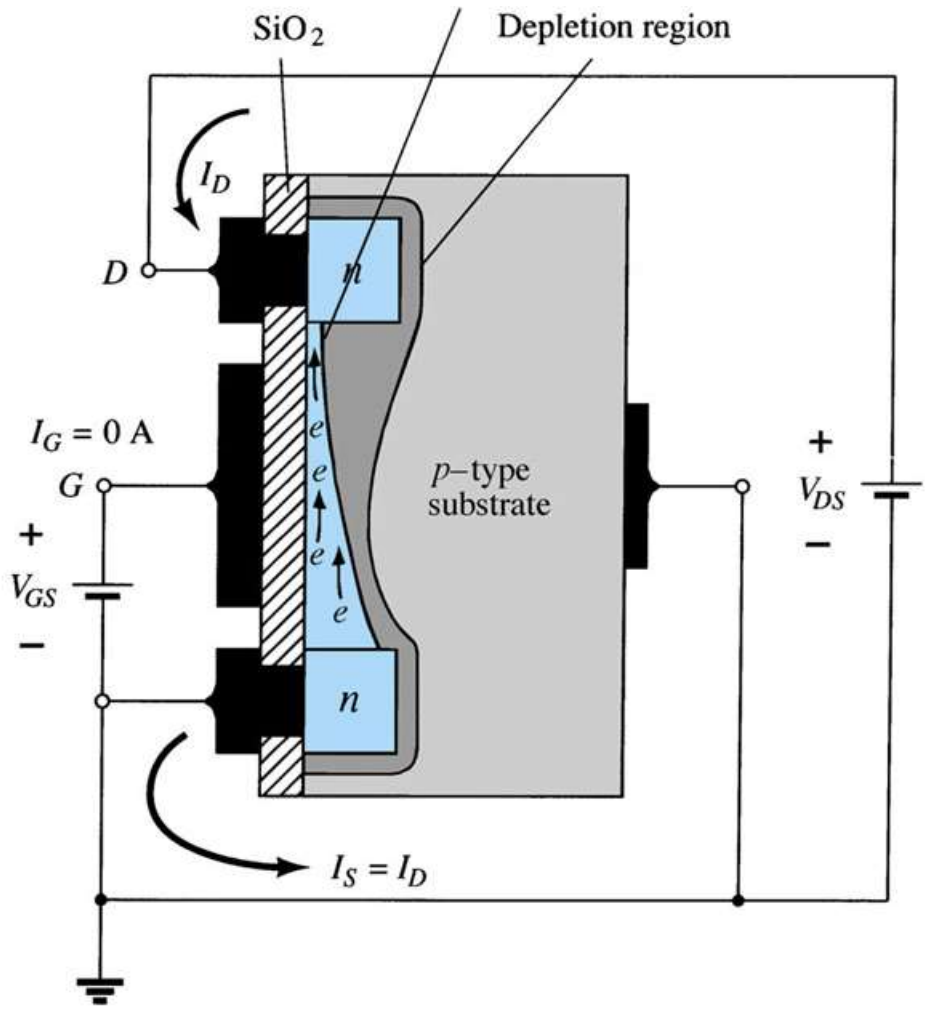


$V_{GS} > V_T$

V_T – Tensão de Limiar

V_{DS} = 0 V Canal pronto para conduzir.

Formação do Canal



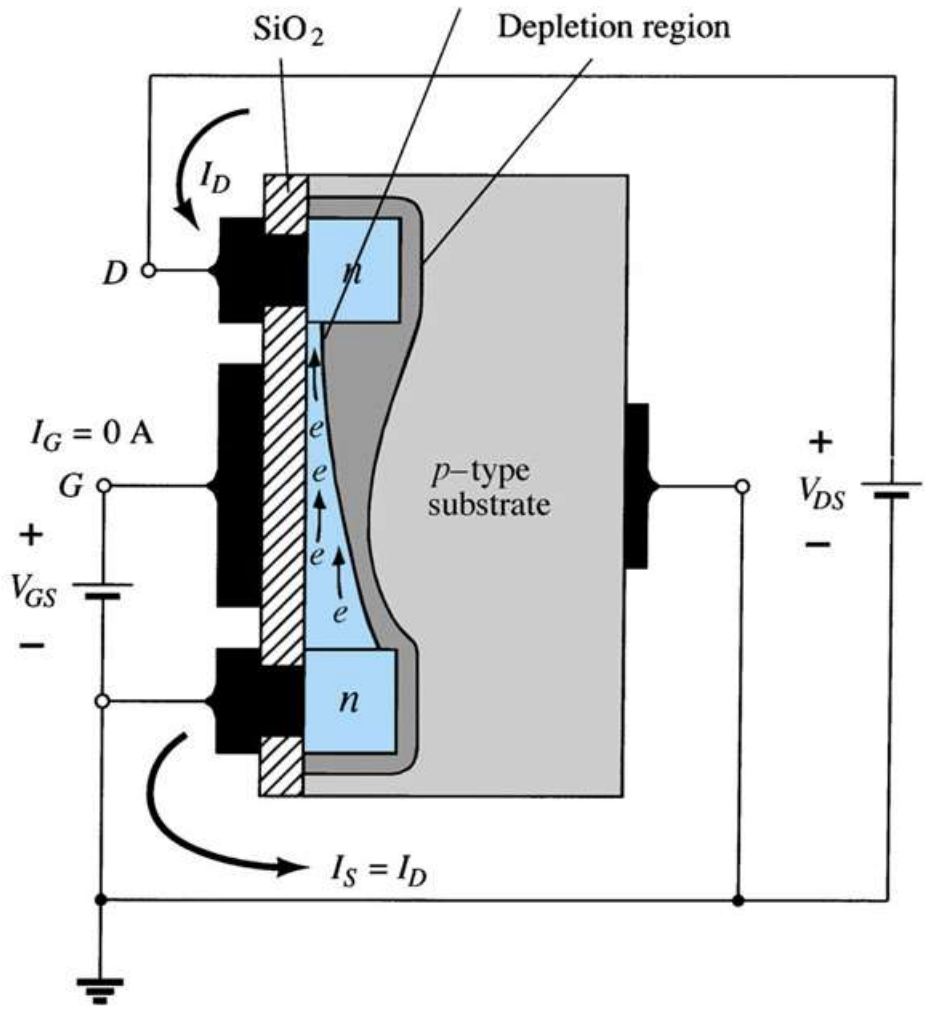
$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} > 0$

Canal conduzindo.

Formação do Canal



$V_{GS} > V_T$

V_T – Tensão de Limiar

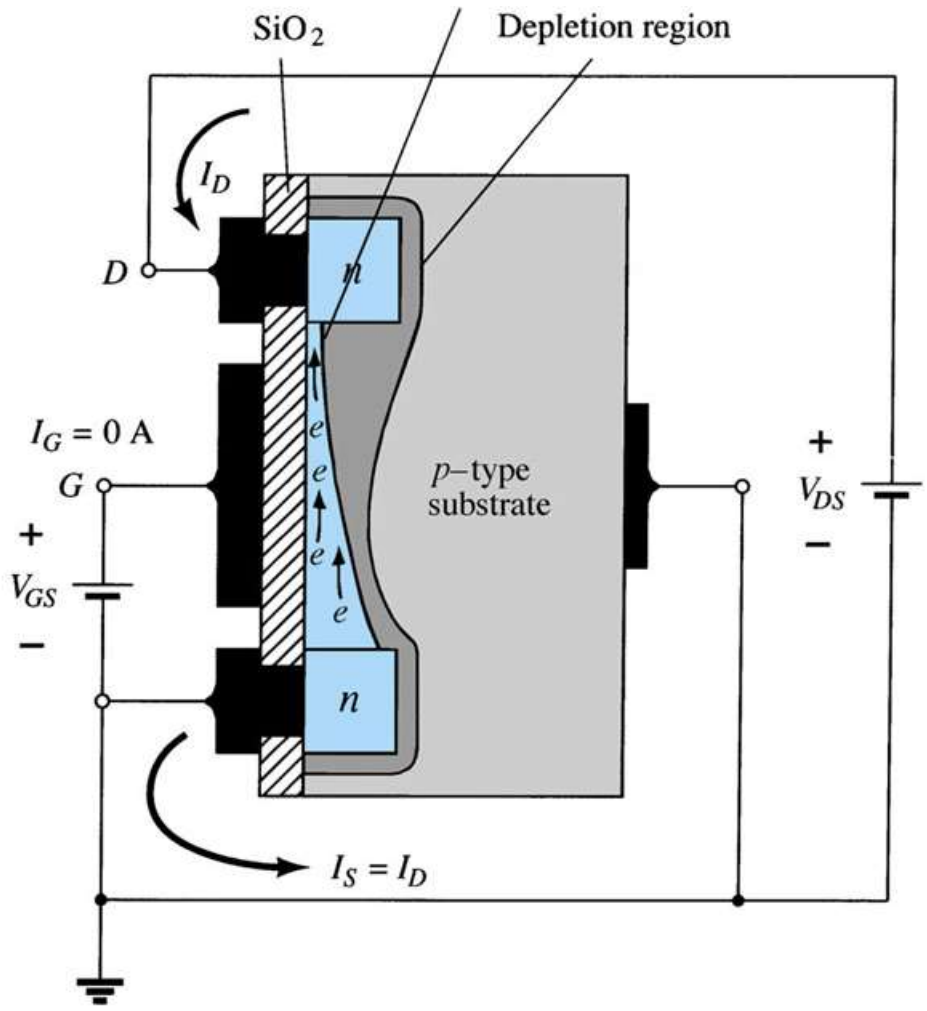
$V_{DS} > 0$

Canal conduzindo.

LKT :

$V_{DS} + V_{GD} - V_{GS} = 0$

Formação do Canal



$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} > 0$

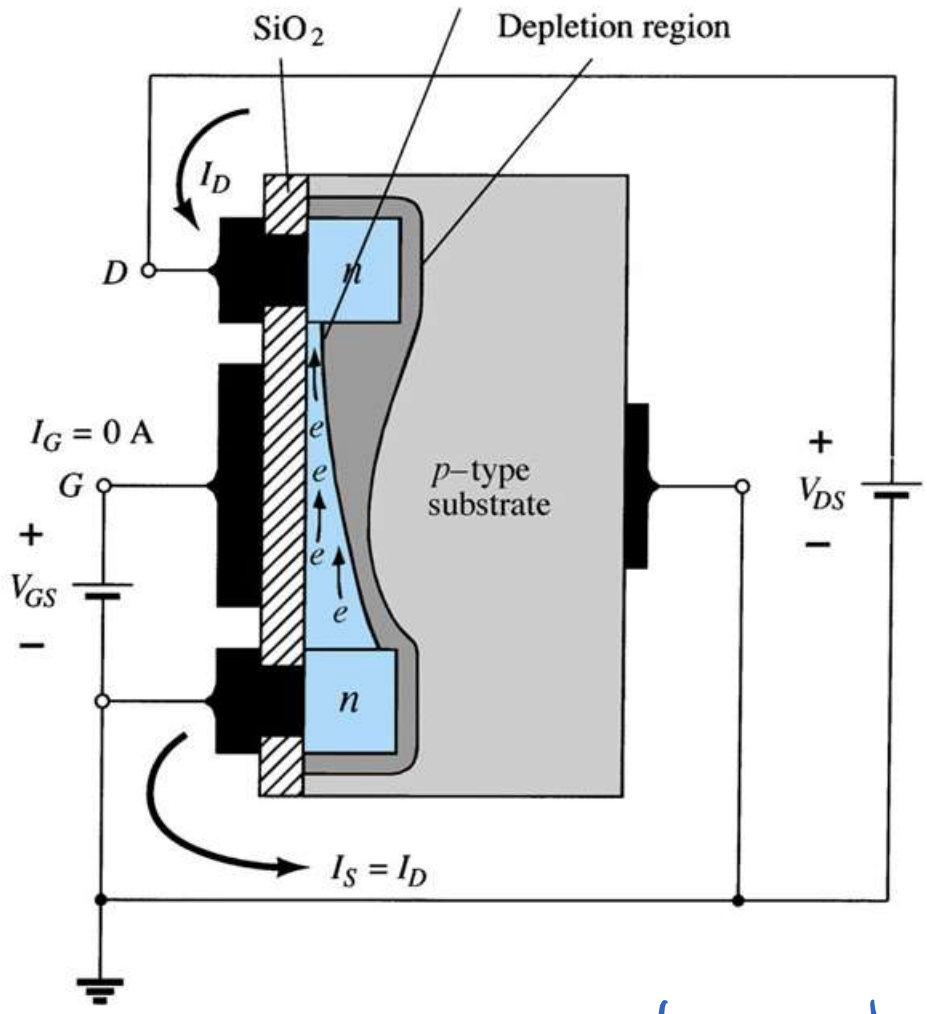
Canal conduzindo.

LKT :

$V_{DS} + V_{GD} - V_{GS} = 0$

$\Rightarrow V_{GD} = V_{GS} - V_{DS}$

Formação do Canal



$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} > 0$

Canal conduzindo.

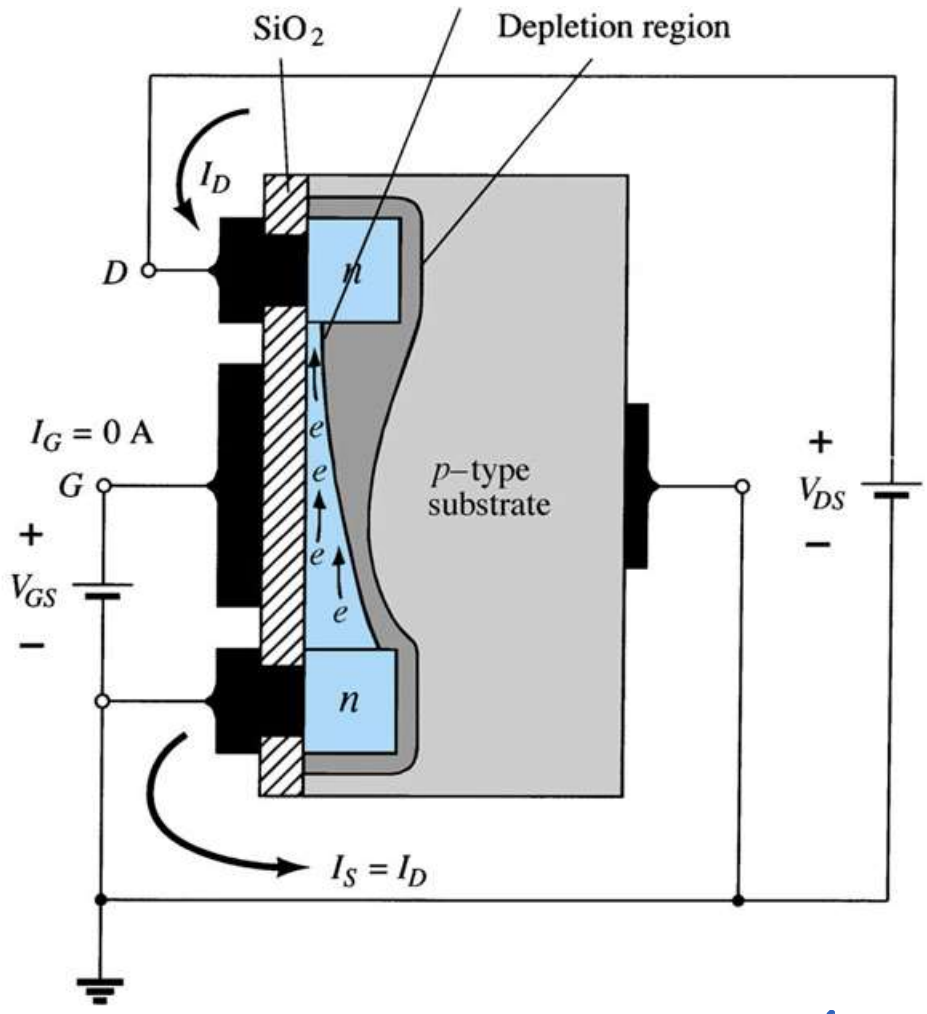
LKT:

$V_{DS} + V_{GD} - V_{GS} = 0$

$\Rightarrow V_{GD} = V_{GS} - V_{DS}$

$\Rightarrow$ Se V_{GS} = cte e V_{DS} aumenta:

Formação do Canal



$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} > 0$

Canal conduzindo.

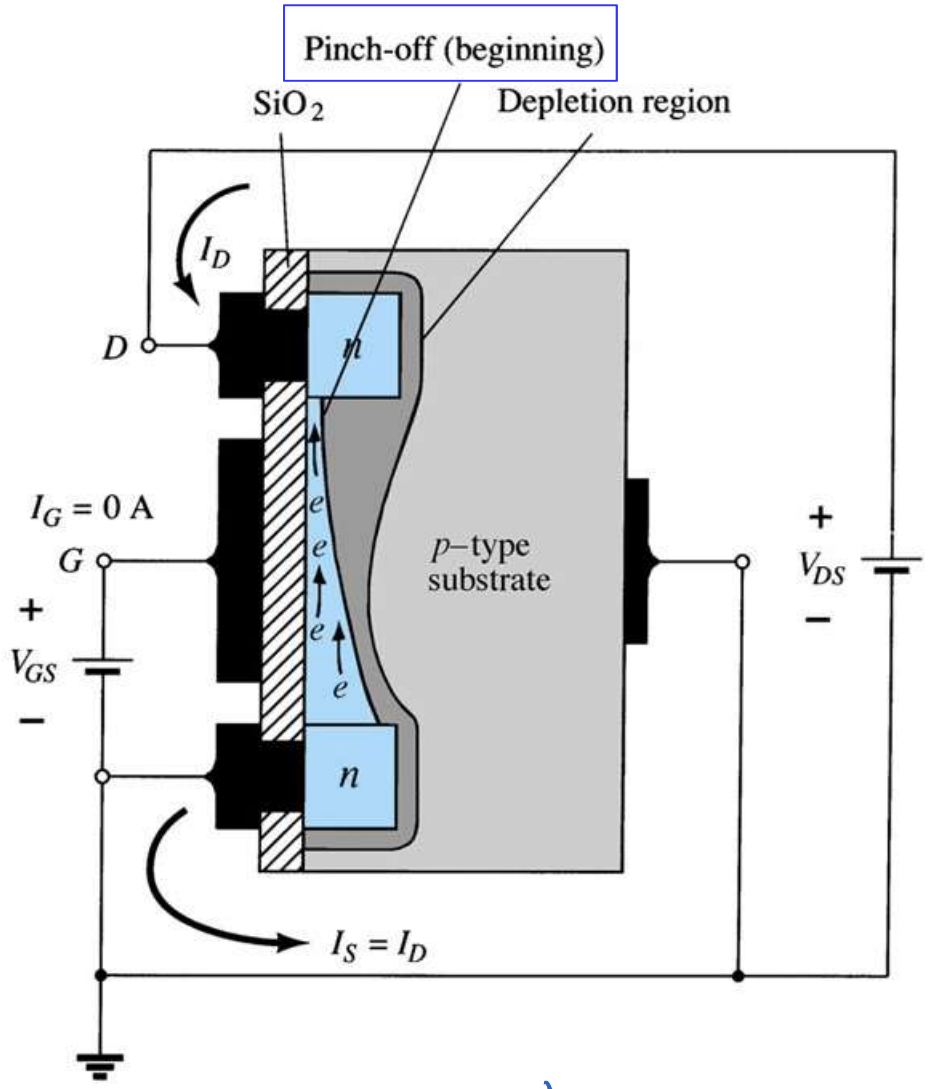
LKT:

$V_{DS} + V_{GD} - V_{GS} = 0$

$\Rightarrow V_{GD} = V_{GS} - V_{DS}$

$\Rightarrow V_{GD} = V_G - V_D$ diminui!

Formação do Canal



$V_{GS} > V_T$

V_T – Tensão de Limiar

$V_{DS} > 0$

Canal conduzindo.

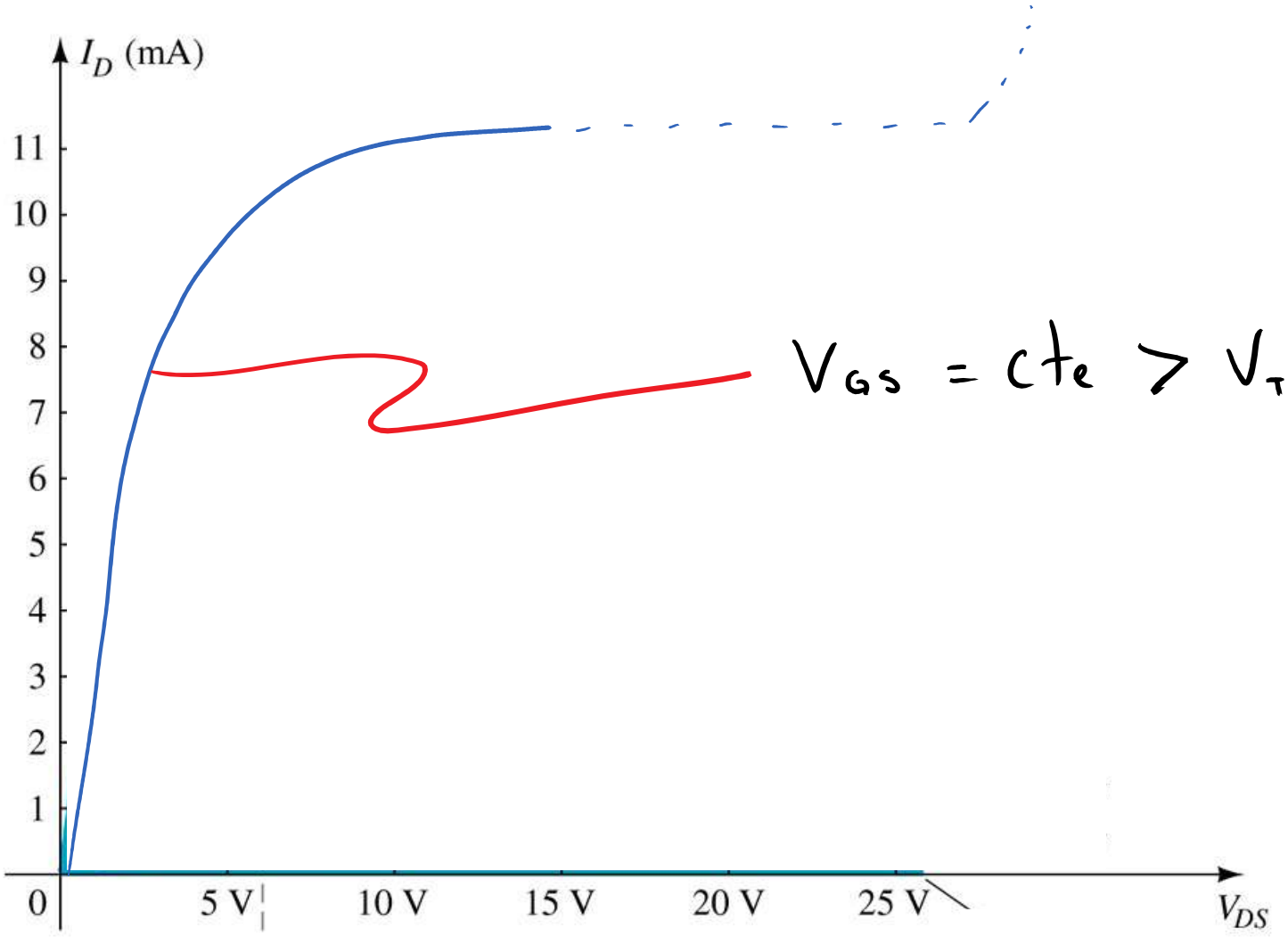
LKT:

$V_{DS} + V_{GD} - V_{GS} = 0$

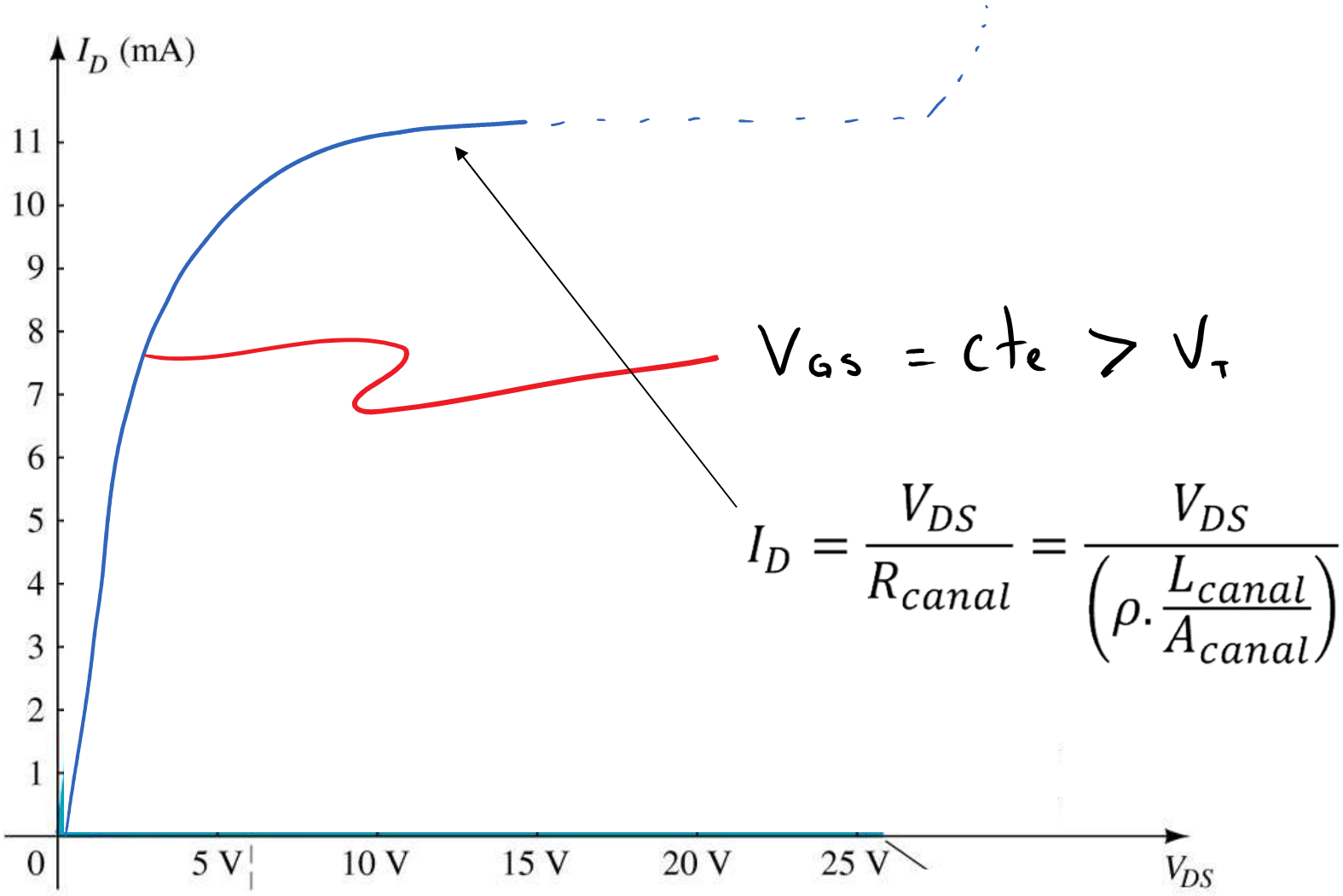
$\Rightarrow V_{GD} = V_{GS} - V_{DS}$

$\Rightarrow$ Até que o canal é "estrangulado"

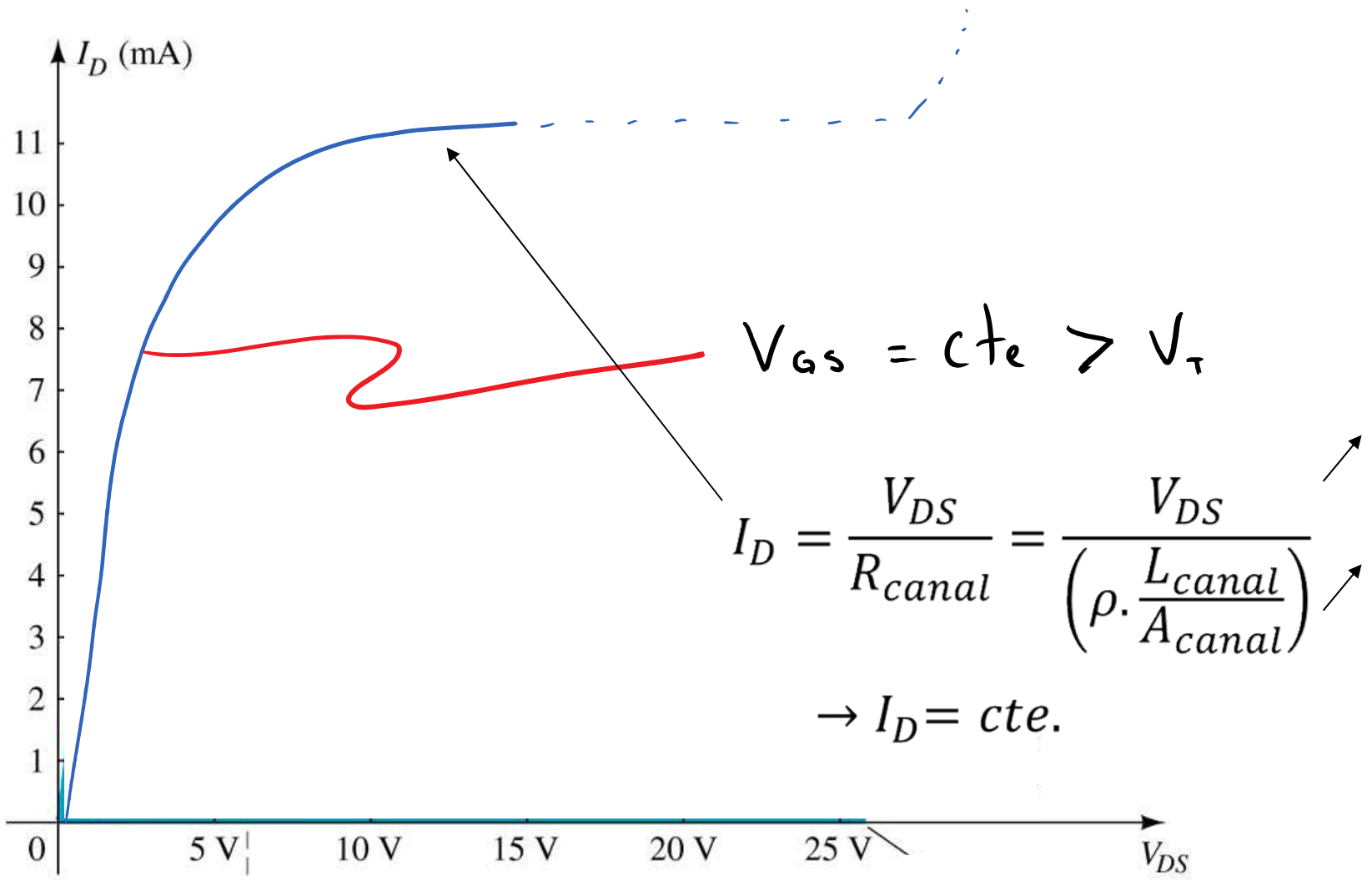
Curvas Características



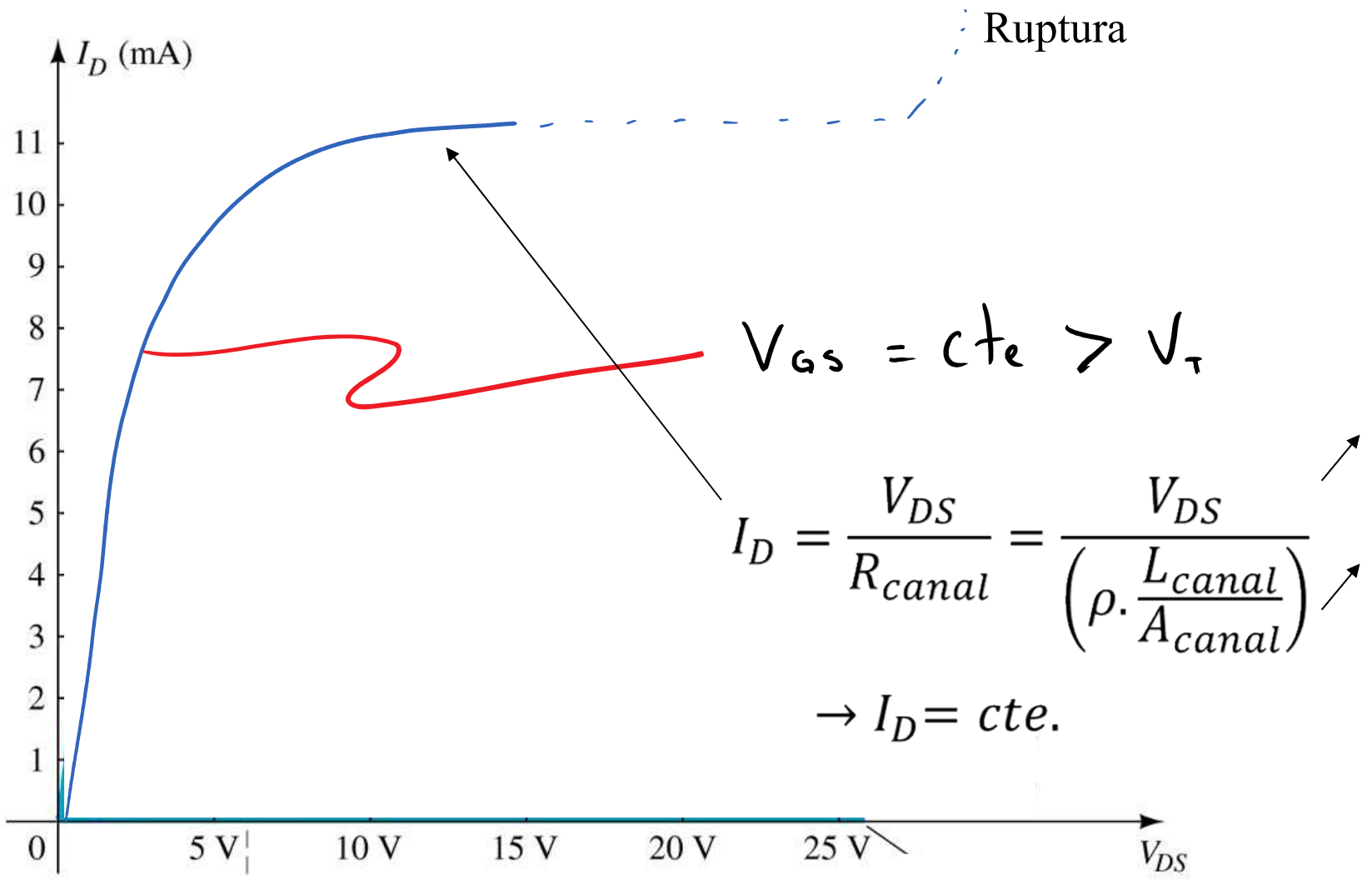
Curvas Características



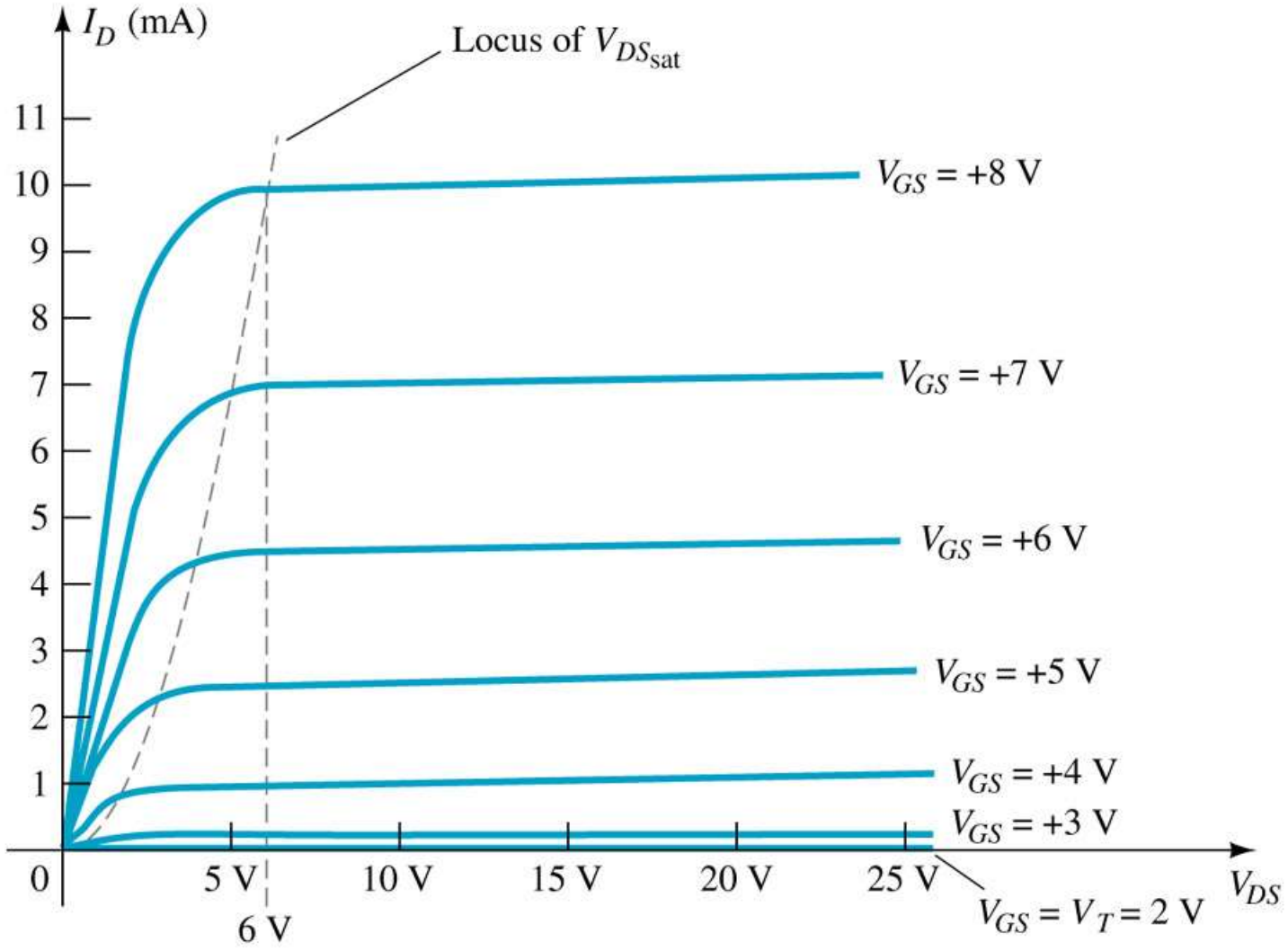
Curvas Características



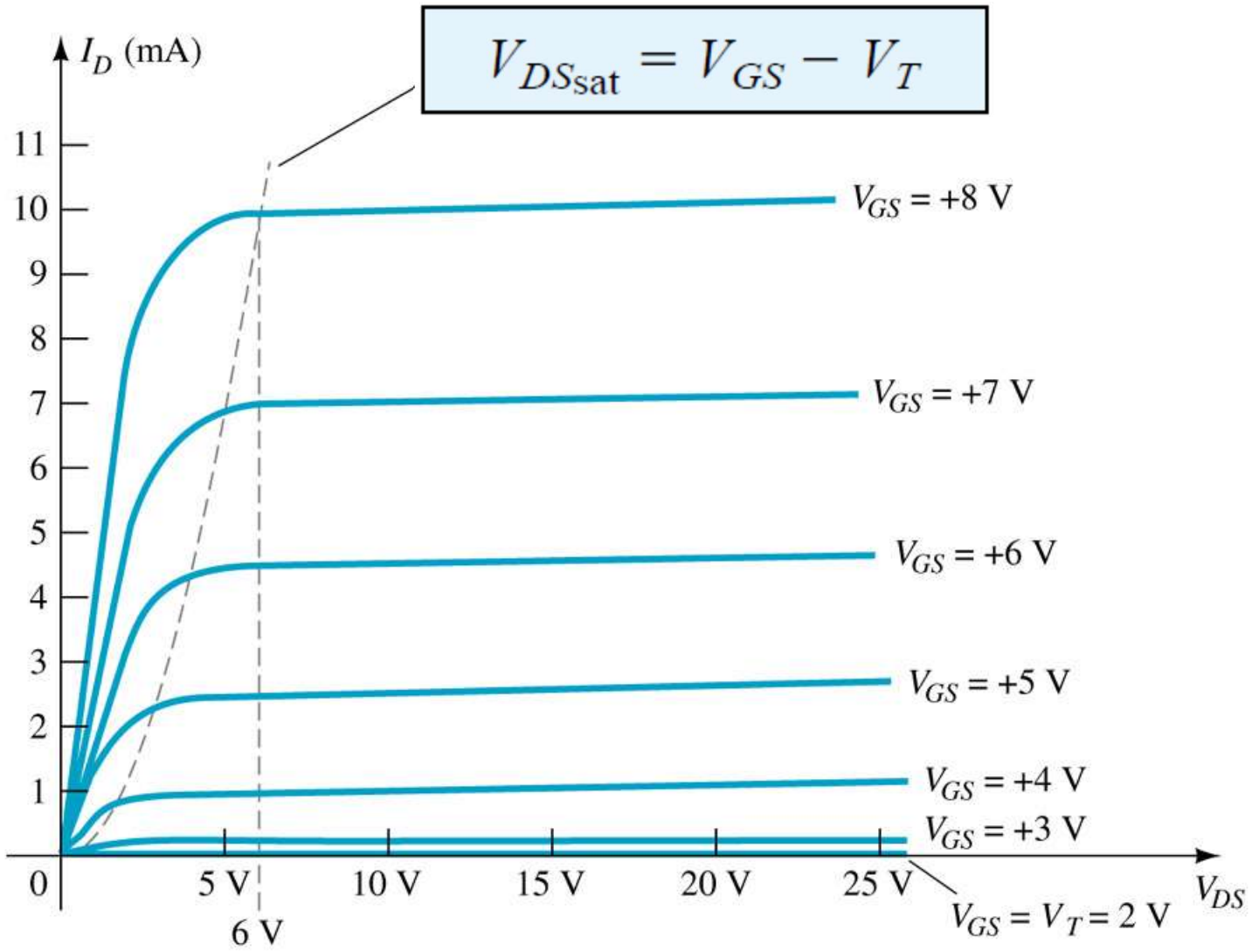
Curvas Características



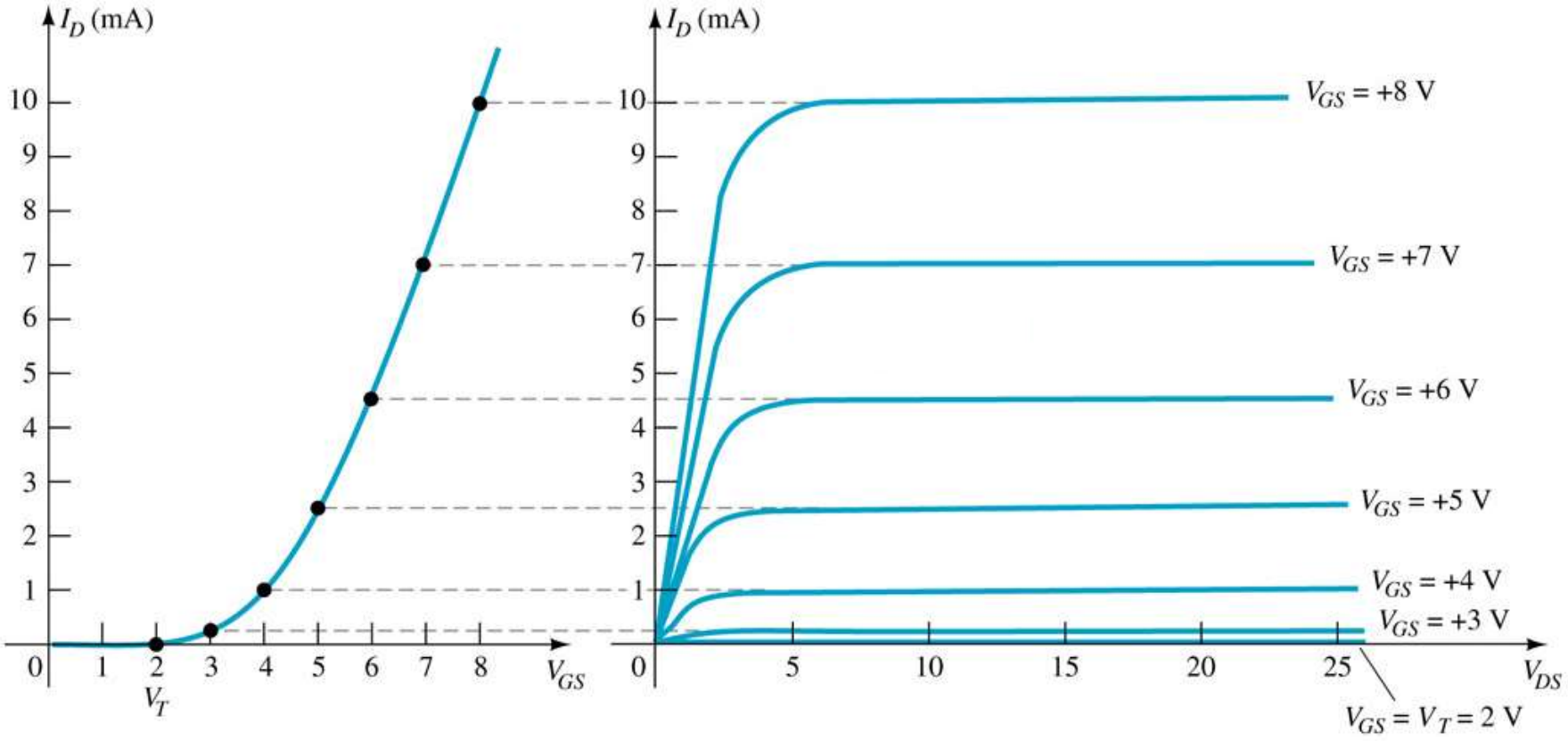
Curvas Características



Curvas Características



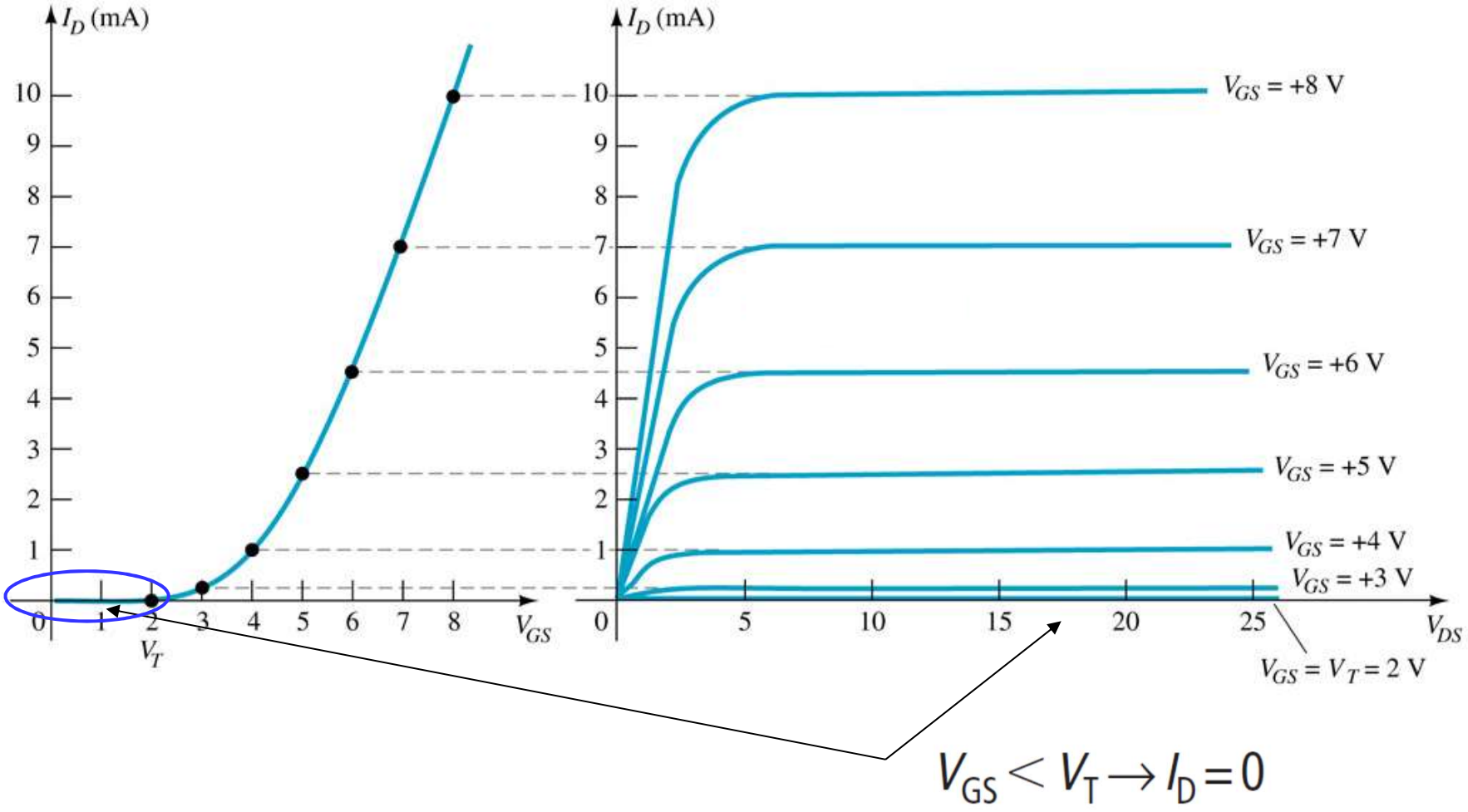
Função Transferência



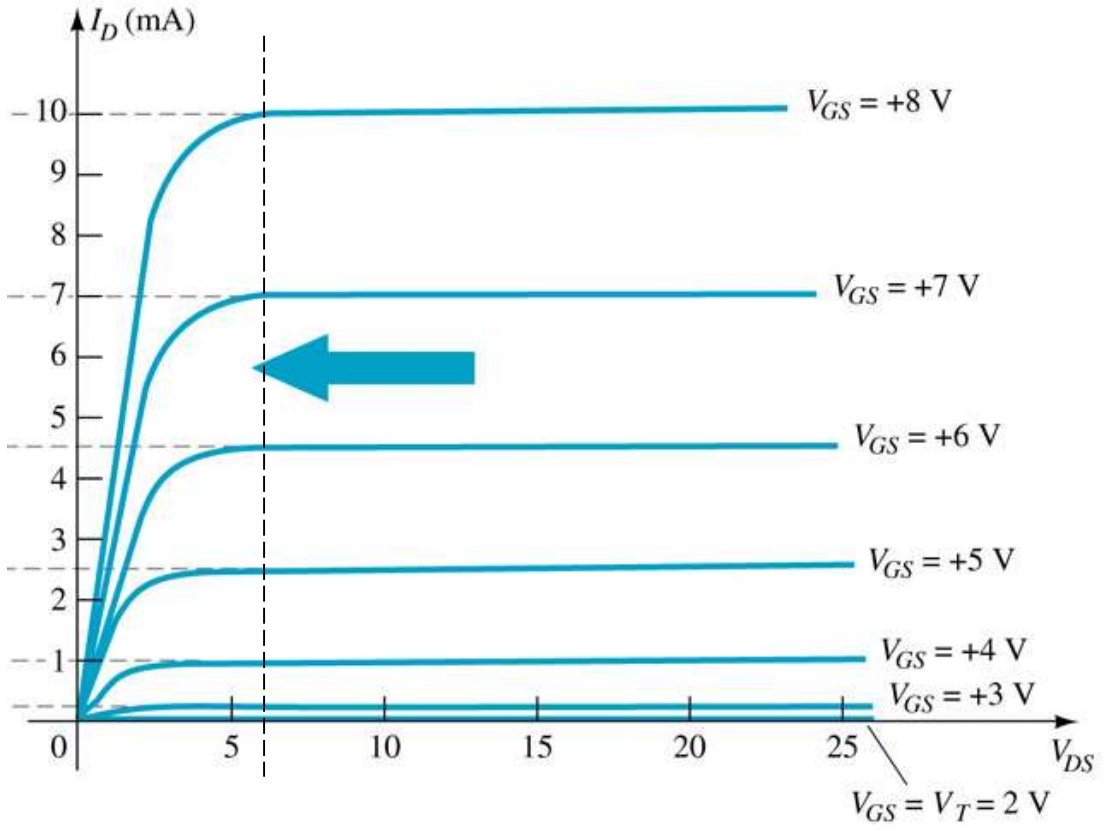
Funcionamento

Regiões de Operação

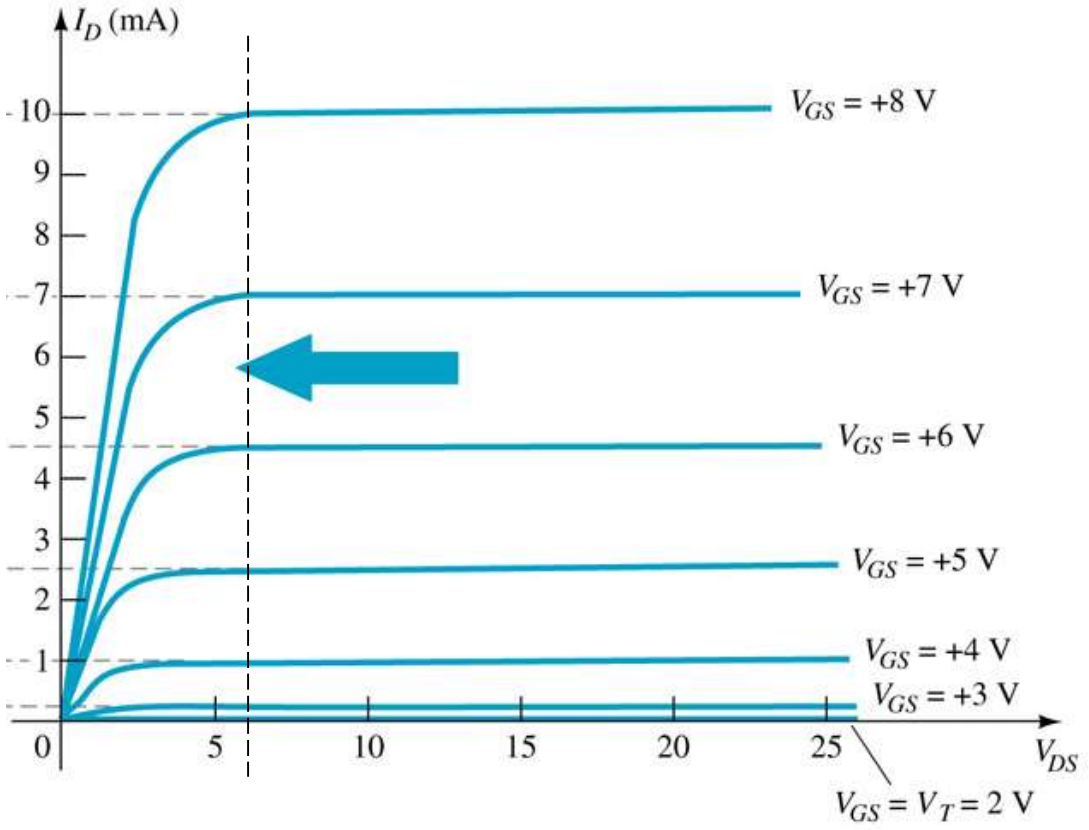
Função Transferência – região de corte



Função Transferência – região de triodo



Função Transferência – região de triodo



$$V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \rightarrow I_D = \beta\,[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

Função Transferência – região e triodo

$$I_D = \beta \left[(V_{GS} - V_T) V_{DS} - V_{DS}^2/2 \right]$$

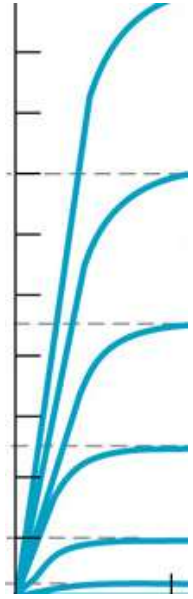
➡ Parábola

$$\beta = \mu C_{ox} (W/L) \quad [A/V^2]$$

Função Transferência – região e triodo

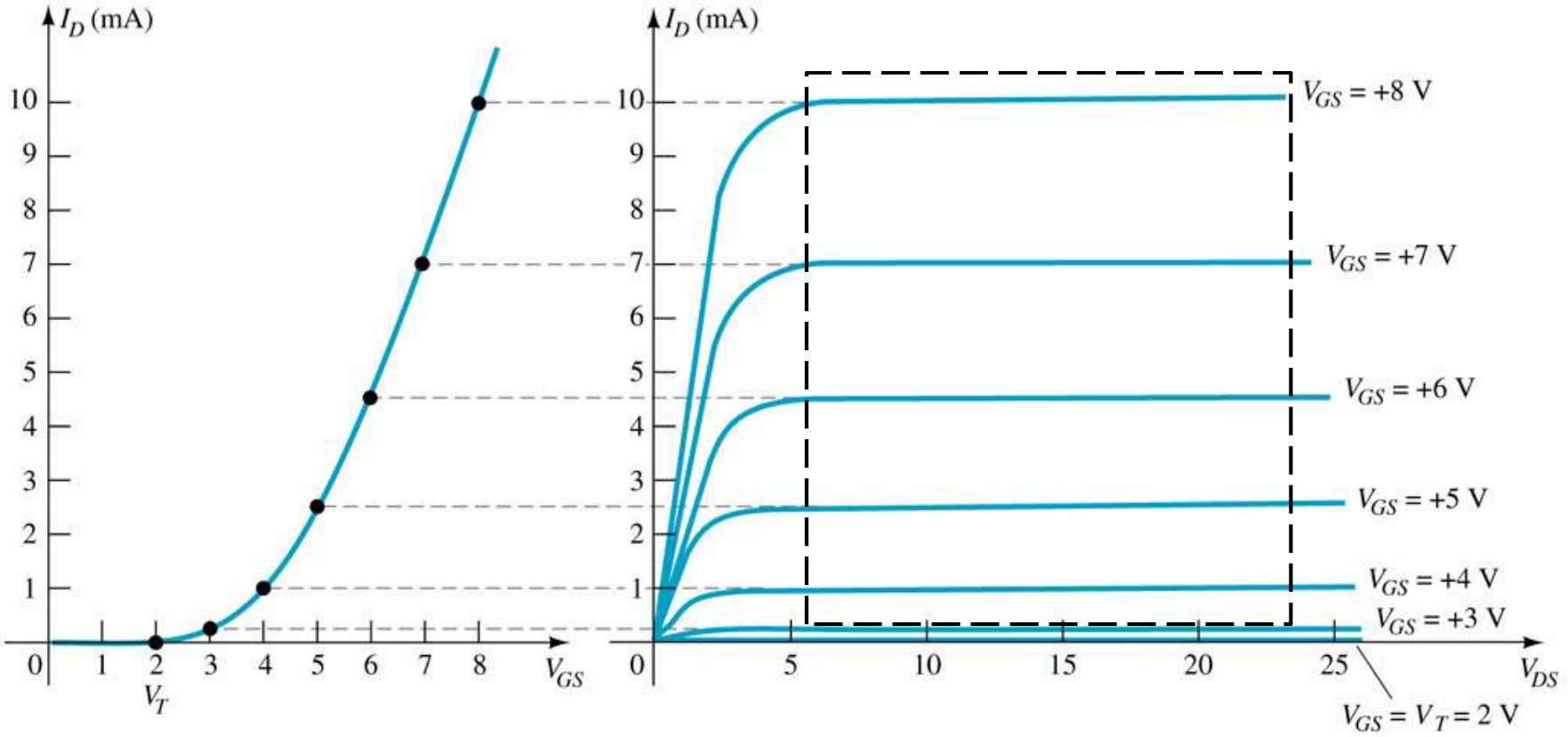
$$I_D = \beta\,[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

⇒ Parábola



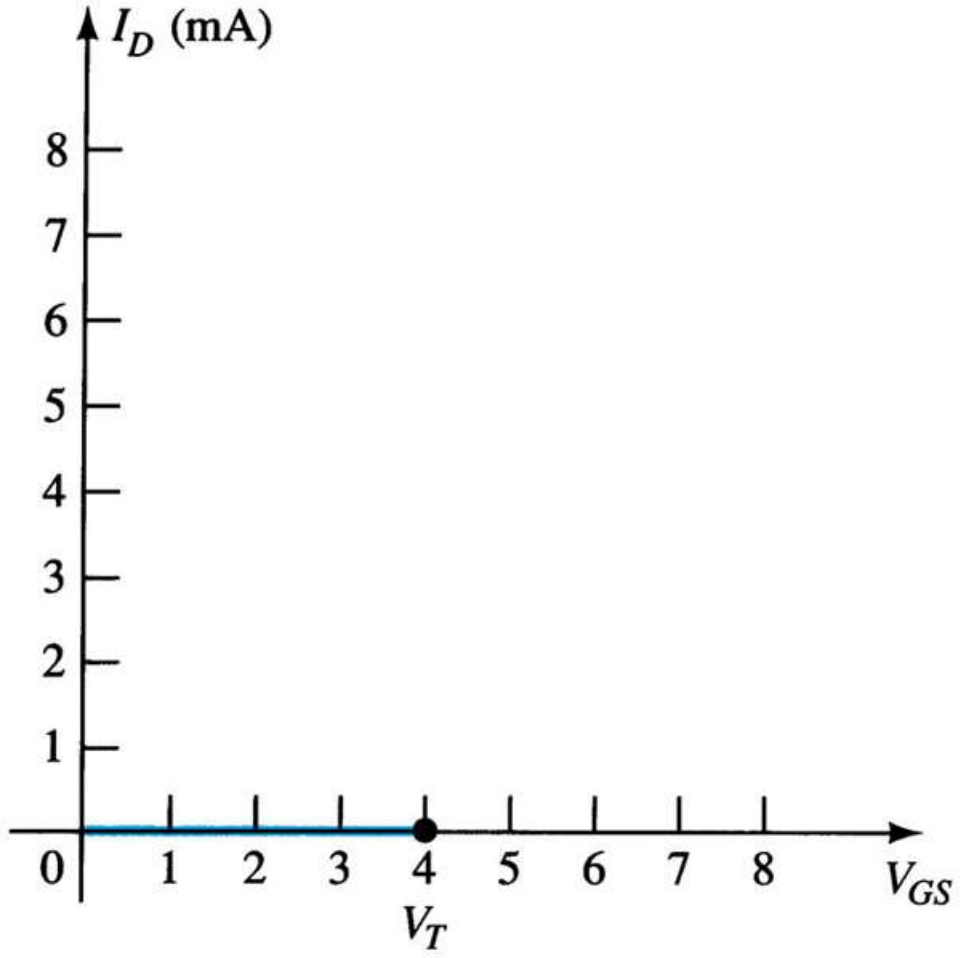
$$\beta = \mu C_{ox}(W/L) \quad [A/V^2]$$

Função Transferência – região de saturação

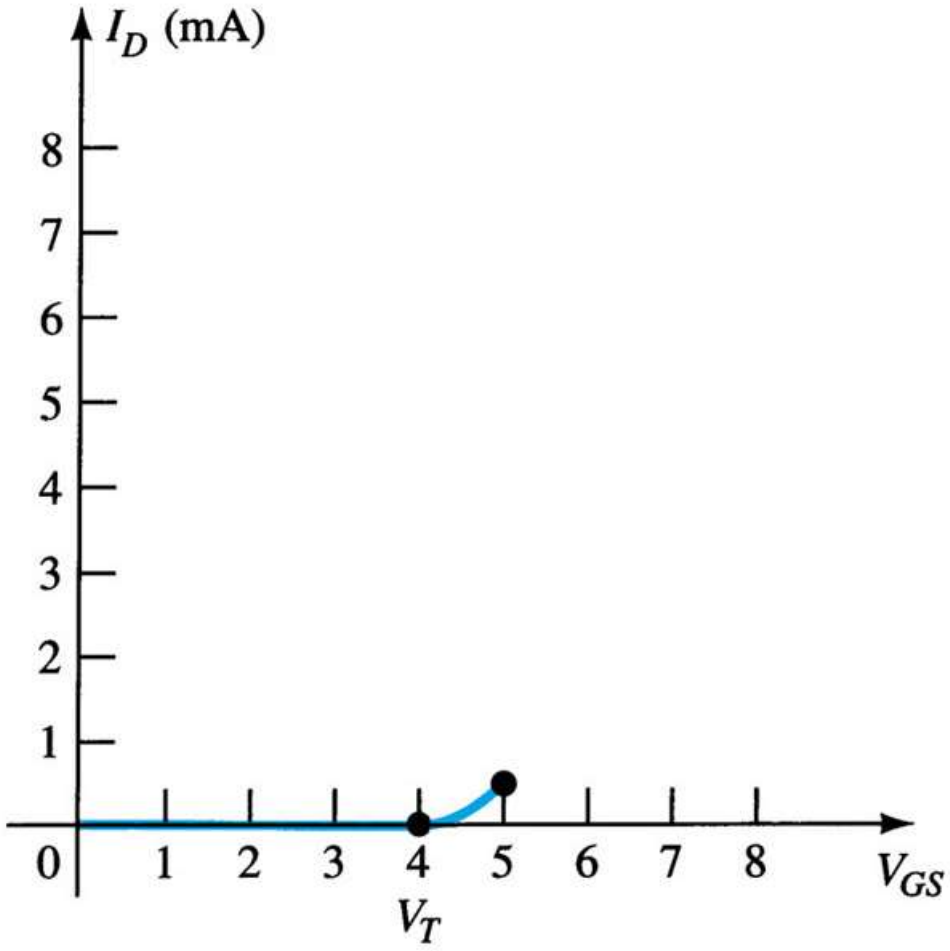


$$V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T$$

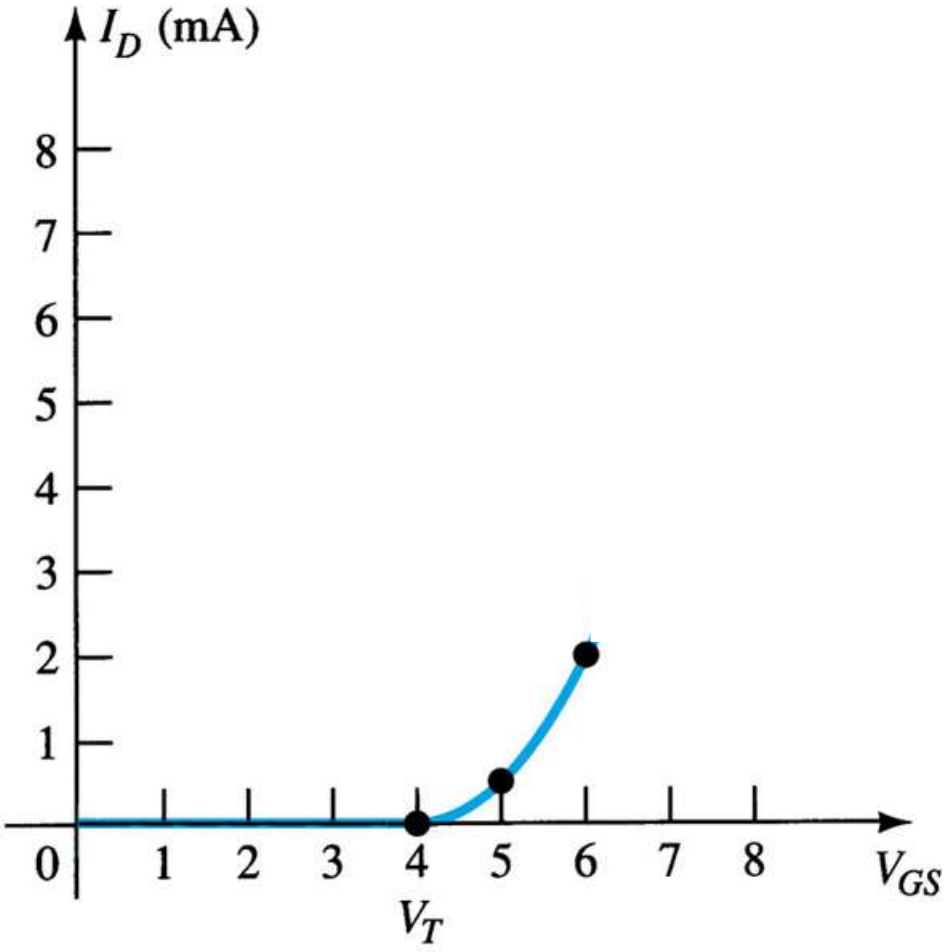
Função Transferência – região de saturação



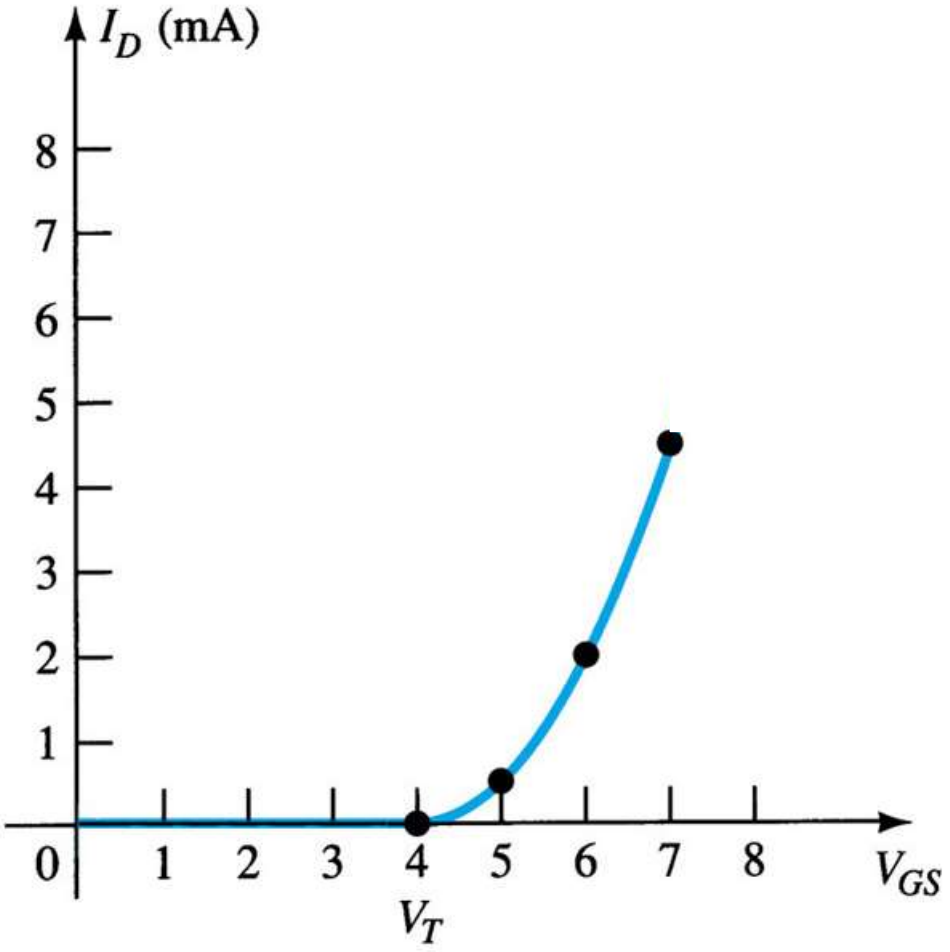
Função Transferência – região de saturação



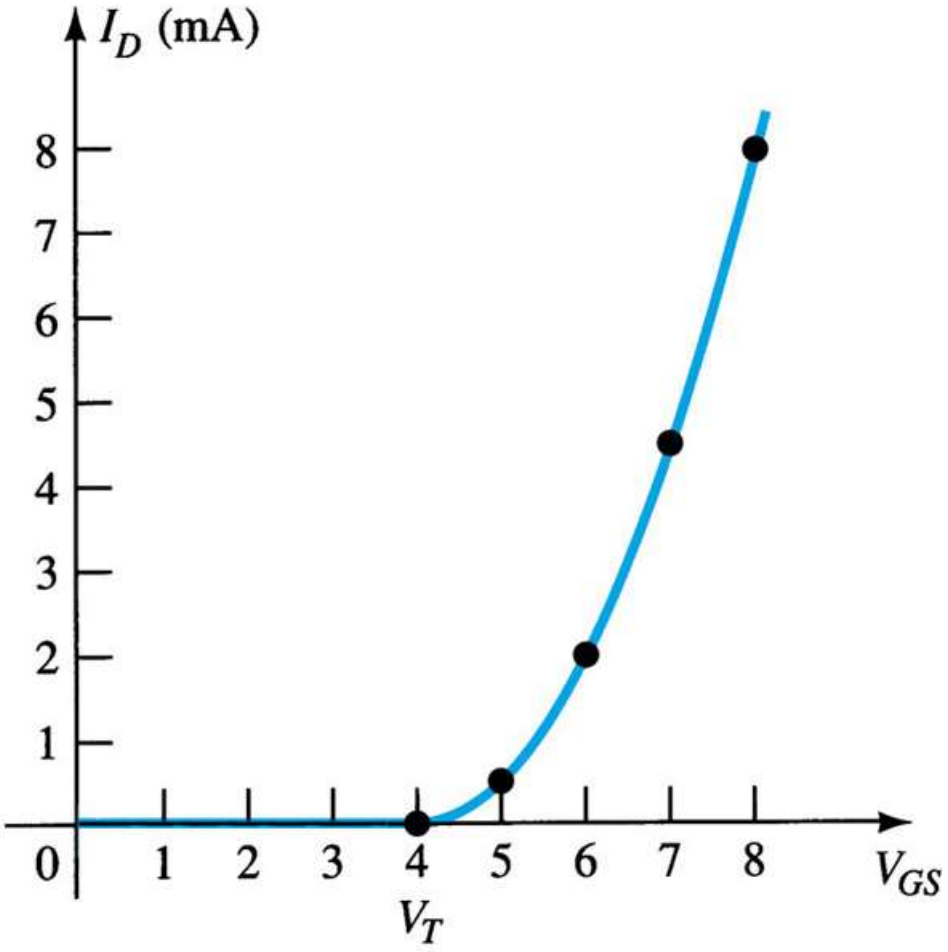
Função Transferência – região de saturação



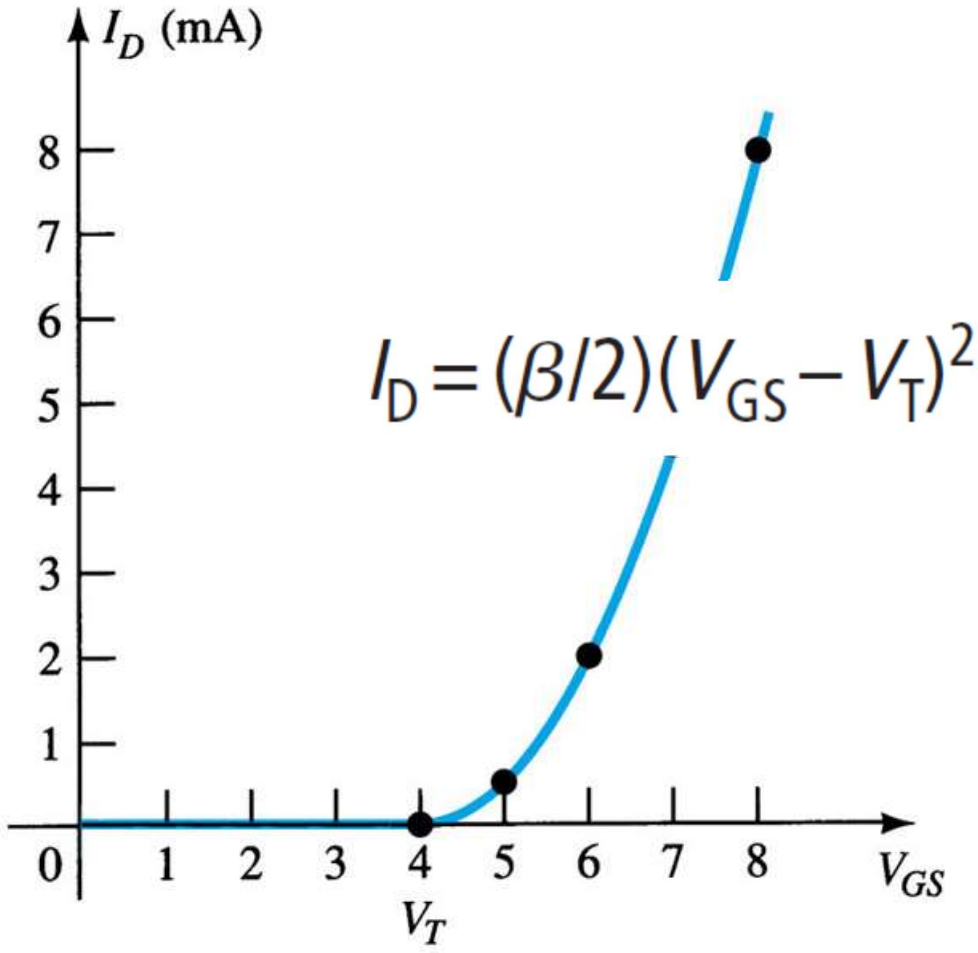
Função Transferência – região de saturação



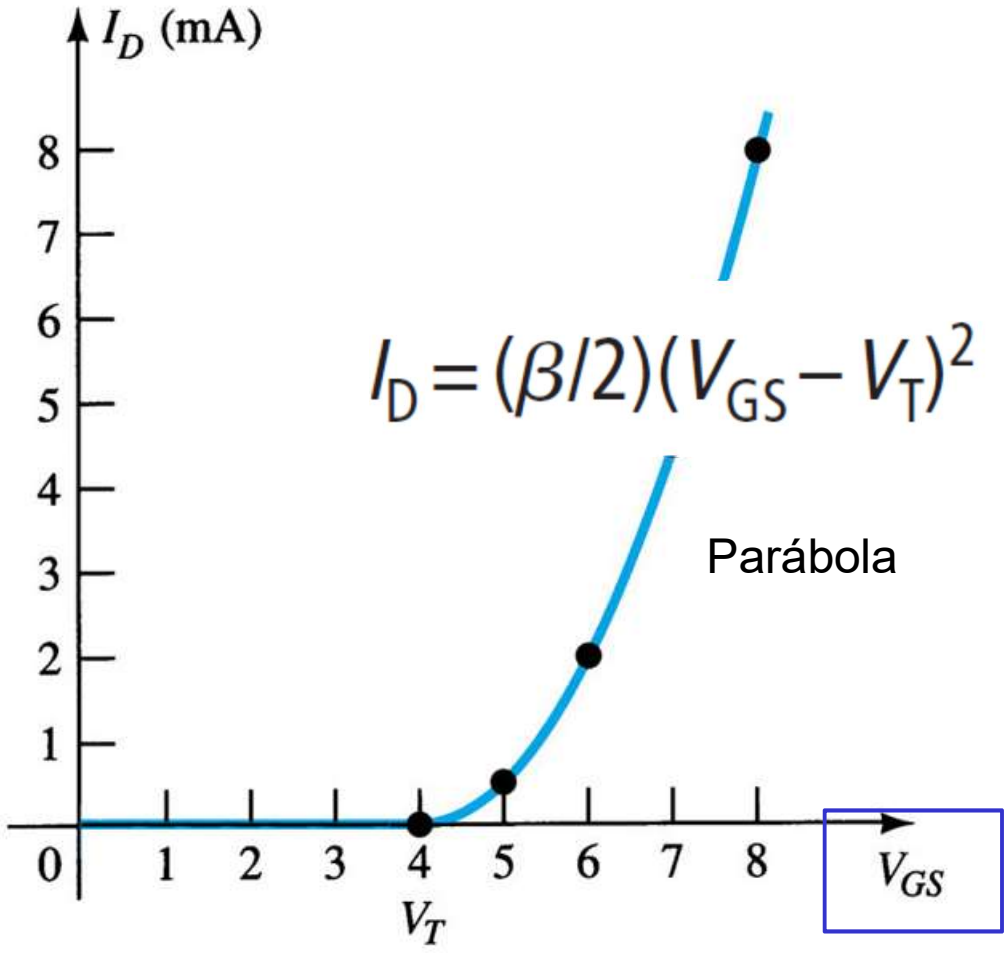
Função Transferência – região de saturação



Função Transferência – região de saturação

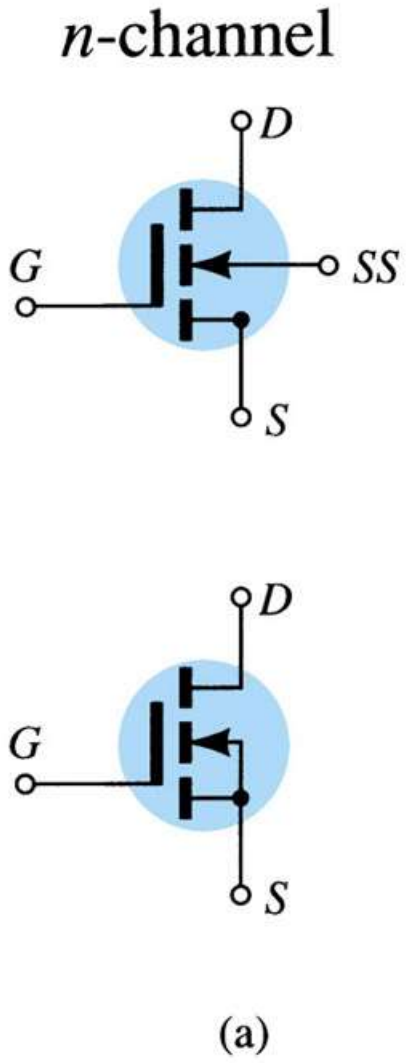


Função Transferência – região de saturação



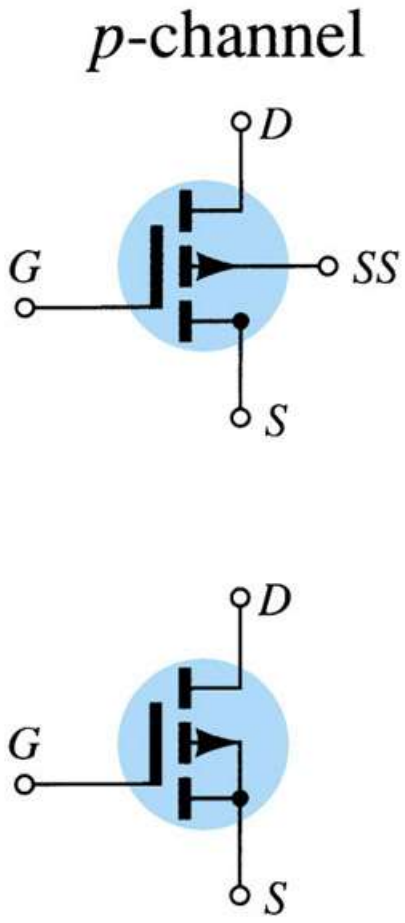
Independente de V_{DS}

Símbolo



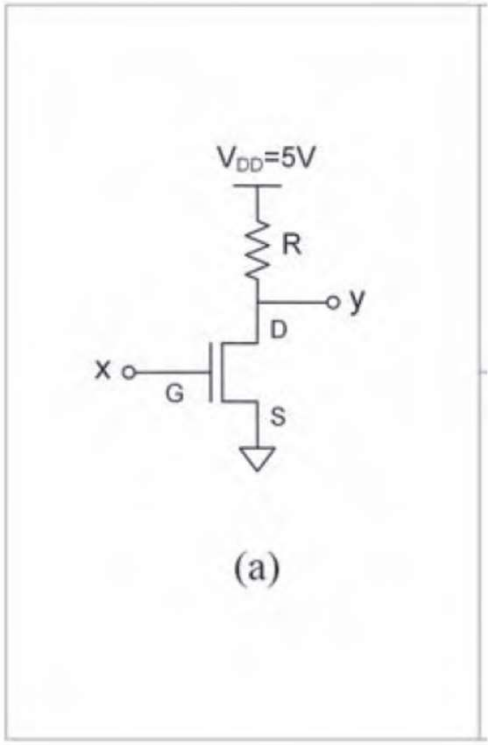
(a)

Símbolo

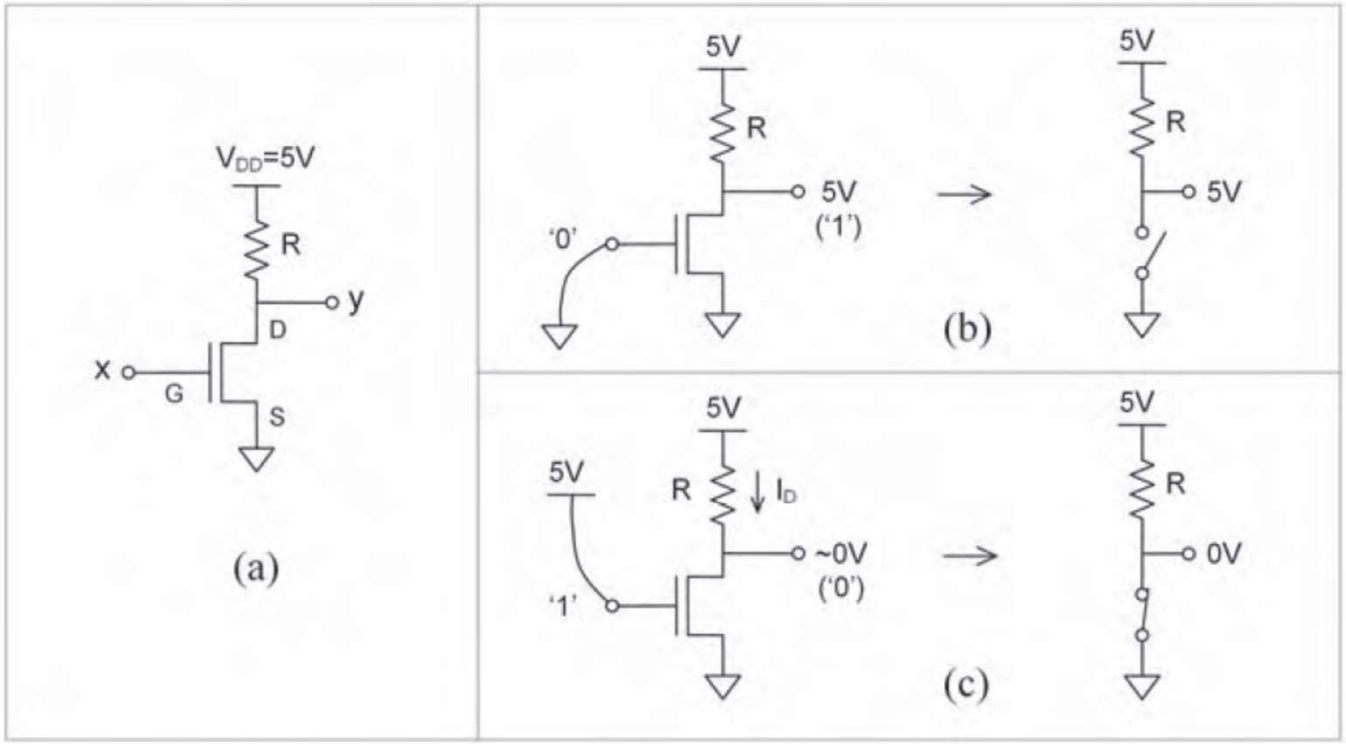


(b)

nMOS – Funcionamento como chave *digital*

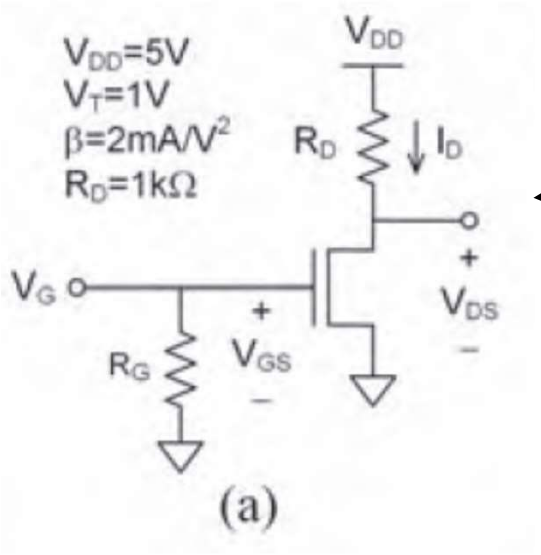


nMOS – Funcionamento como chave *digital*



$5\,V > V_T$

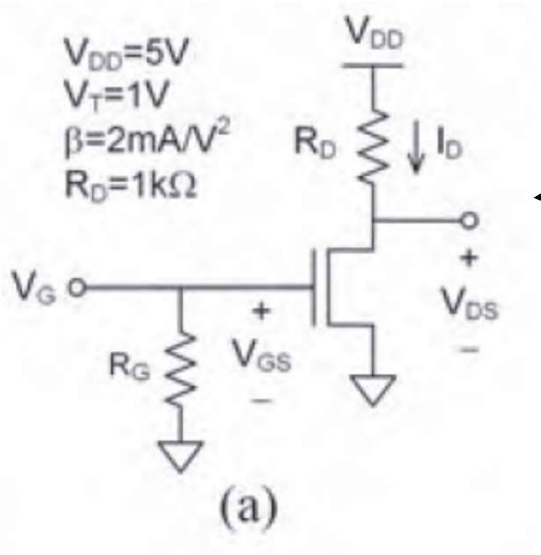
nMOS – Funcionamento como chave *digital*



$$V_{DS} = V_{DD} - R_D I_D$$

(LKT)

nMOS – Funcionamento como chave *digital*

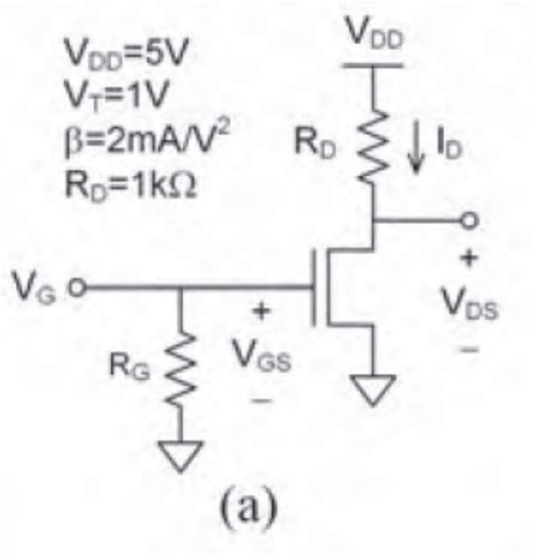


$$V_{DS} = V_{DD} - R_D I_D$$

(LKT)

Análise $\Rightarrow$ $\quad V_{DS} = f(V_{GS}) = ?$

nMOS – Funcionamento como chave *digital*

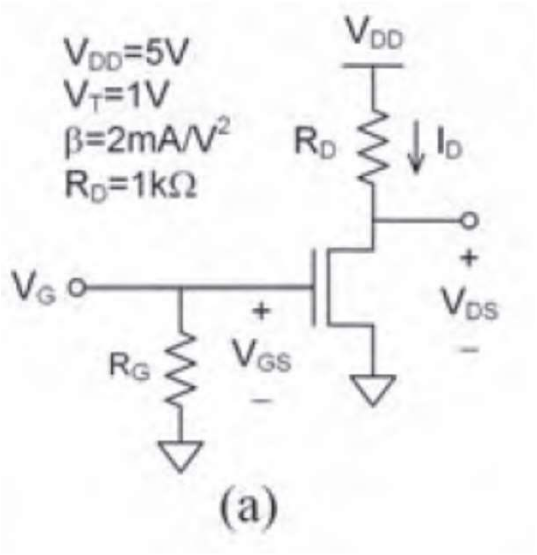


$$V_{DS} = V_{DD} - R_D I_D$$

Análise $\Rightarrow$ $V_{DS} = f(V_{GS})$ =?

Considerando $\Rightarrow$ $V_{DS} = f(I_D)$

nMOS – Funcionamento como chave *digital*

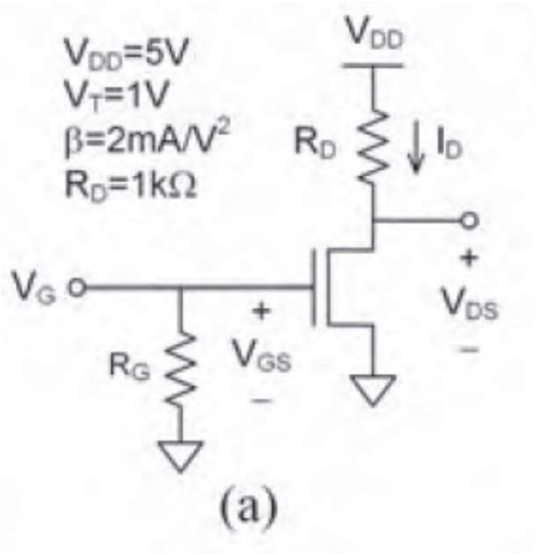


$$V_{DS} = V_{DD} - R_D I_D$$

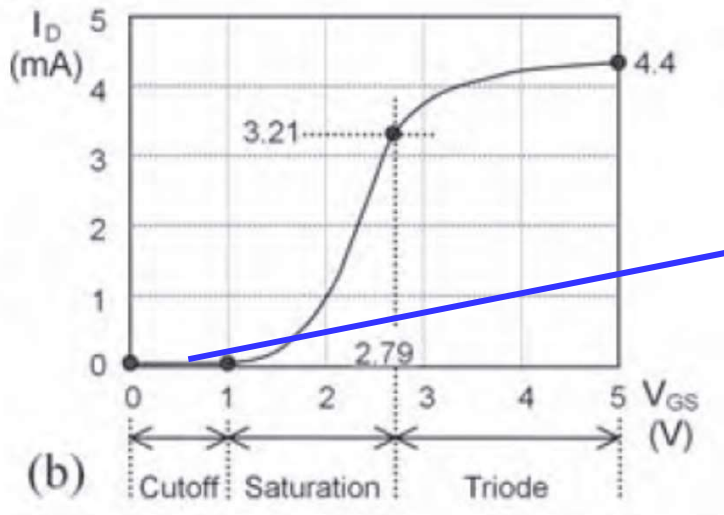
Análise ⇒ $V_{DS} = f(V_{GS})$ =?

Considerando ⇒ $V_{DS} = f(I_D)$ e $I_D = f(V_{DS}, V_{GS})$

nMOS – i) Região de Corte

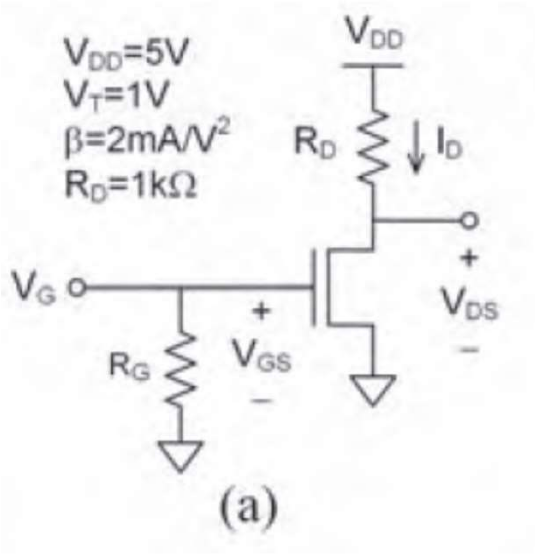


$$V_{DS} = V_{DD} - R_D I_D$$

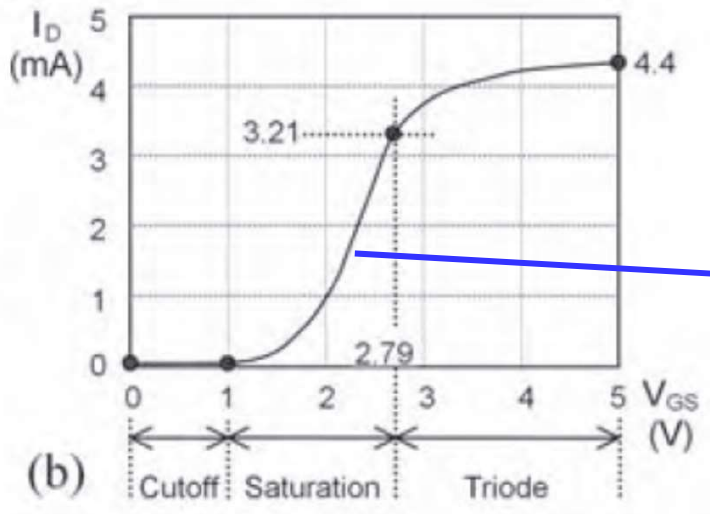


$$V_{GS} < V_T \rightarrow I_D = 0$$

nMOS – ii) Região de Saturação



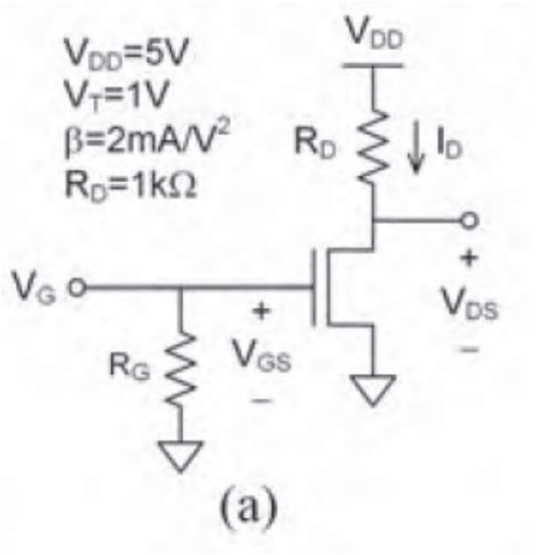
$$V_{DS} = V_{DD} - R_D I_D$$



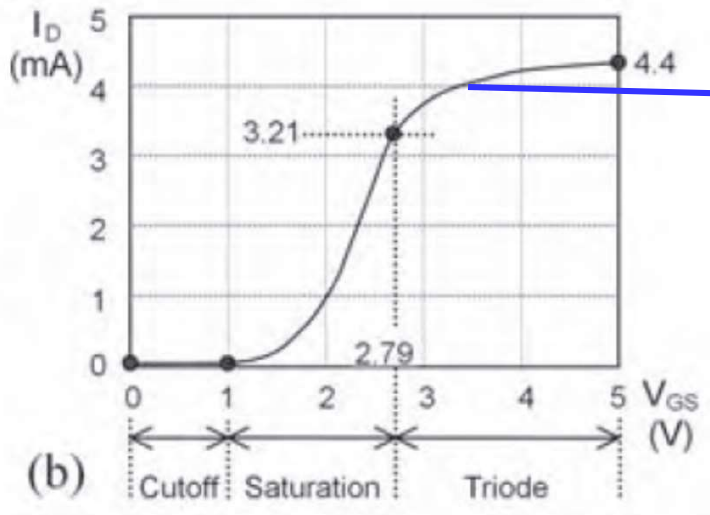
$$V_{DS} \geq V_{GS} - V_T$$

$$I_D = (\beta/2)(V_{GS} - V_T)^2$$

nMOS – iii) Região de Triodo



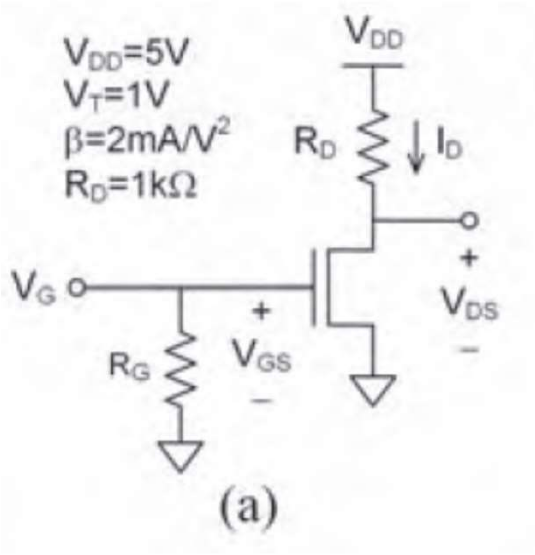
$$V_{DS} = V_{DD} - R_D I_D$$



$$V_{DS} < V_{GS} - V_T$$

$$I_D = \beta\,[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

nMOS – V_{DS} x V_{GS}

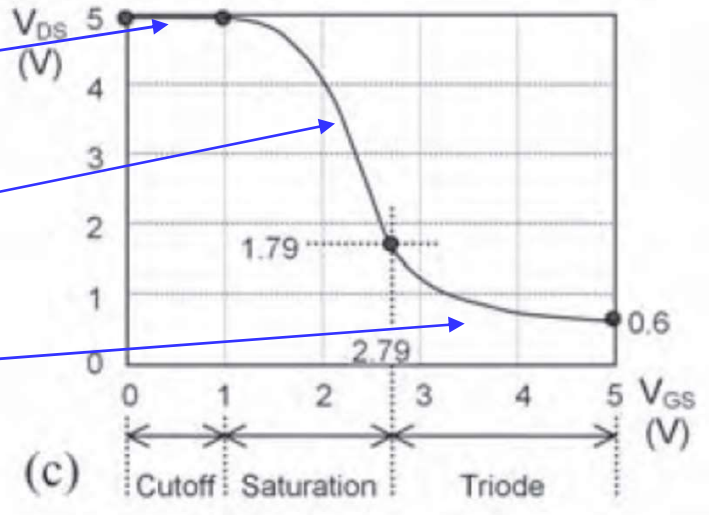


$$V_{DS} = V_{DD} - R_D I_D$$

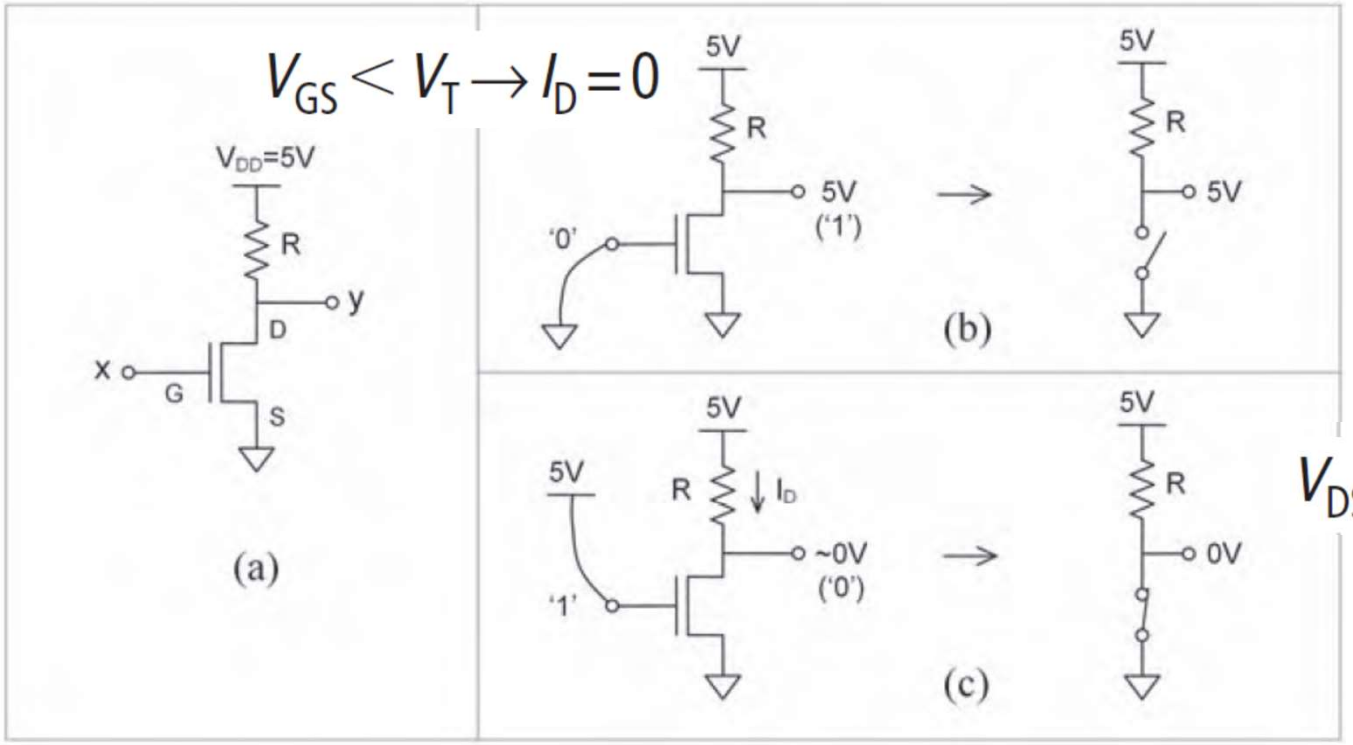
$$I_D = 0$$

$$I_D = (\beta/2)(V_{GS} - V_T)^2$$

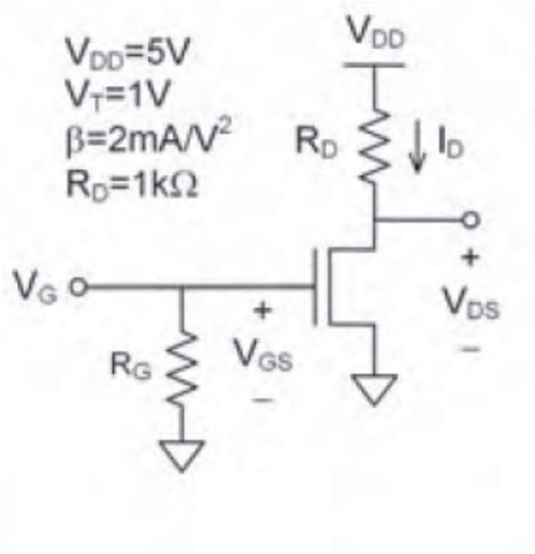
$$I_D = \beta\,[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

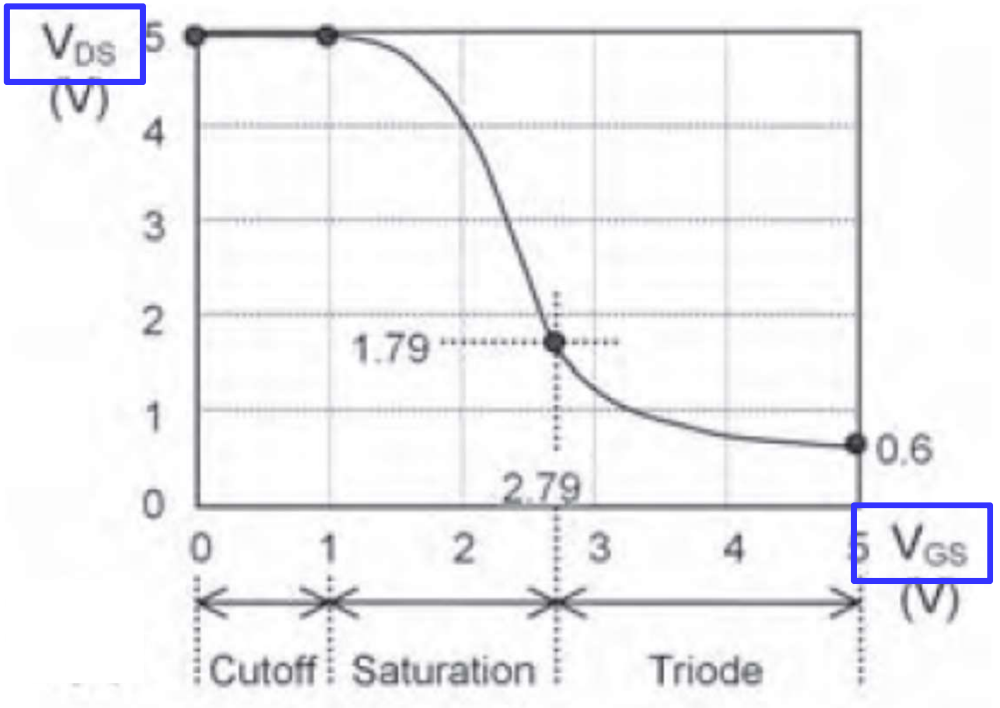


nMOS – Funcionamento como chave *digital*



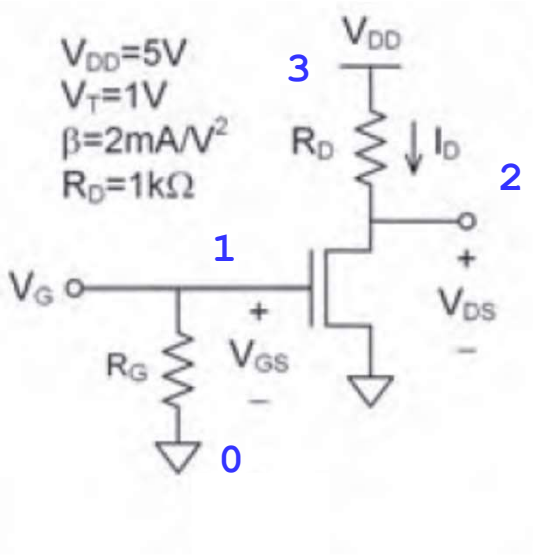
Função de transferência



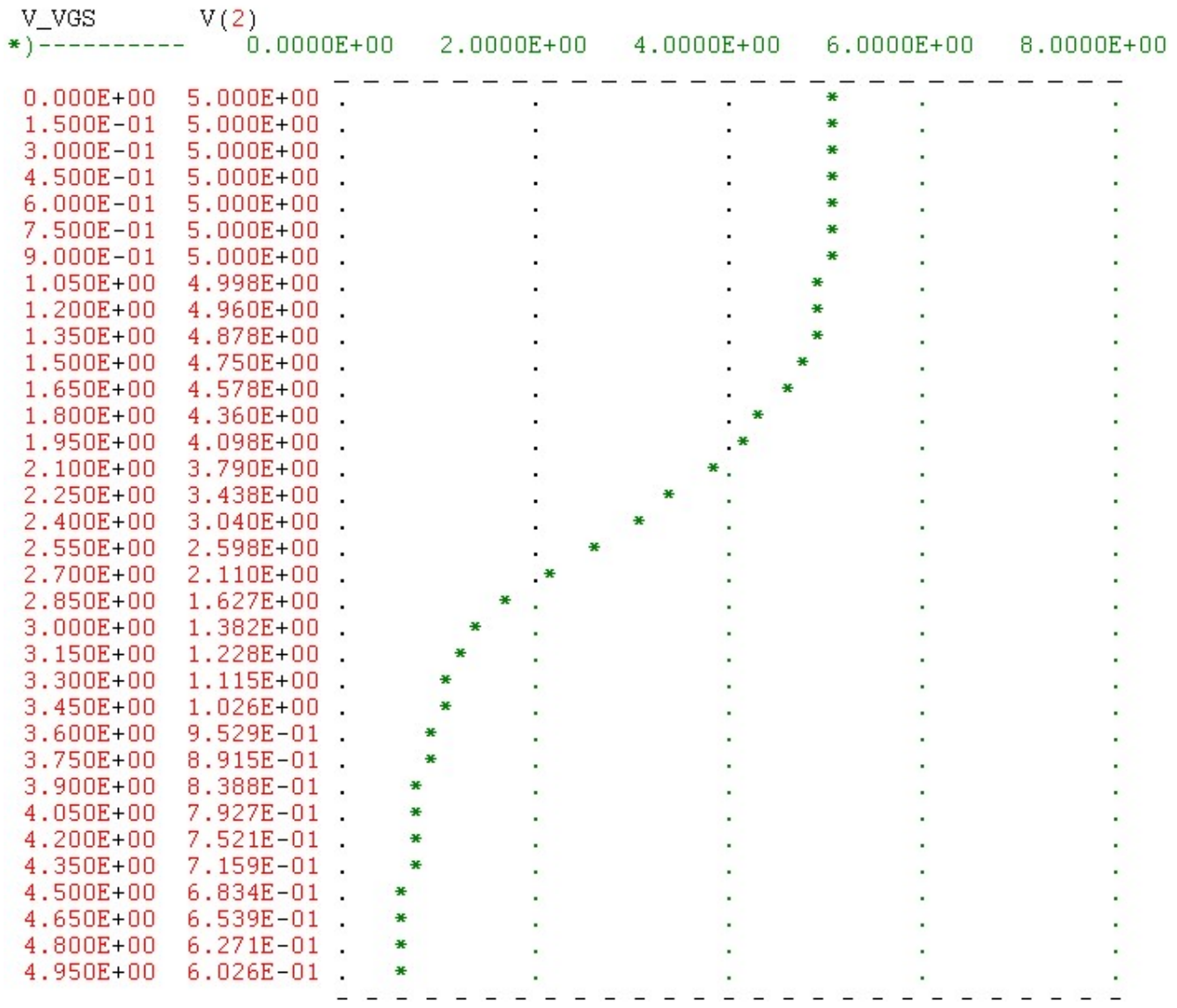


Função de transferência - PSPice

```
* source EXEMPLO N-MOS

R_RD    3       2       1k      TC=0,0
V_VDD   3       0       DC 5V
V_VGS   1       0       DC 5V

M_M1    2       1       0       0       M1
.model M1 NMOS(Vto = 1V Kp = 2e-3)

.DC V_VGS       0       5       0.15
.PLOT           DC      V[2]    I(R_RD)
```



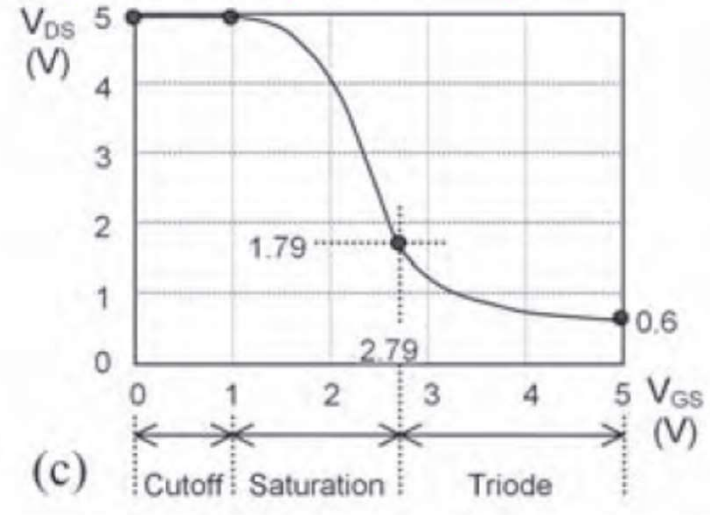
Função de transferência - PSPice



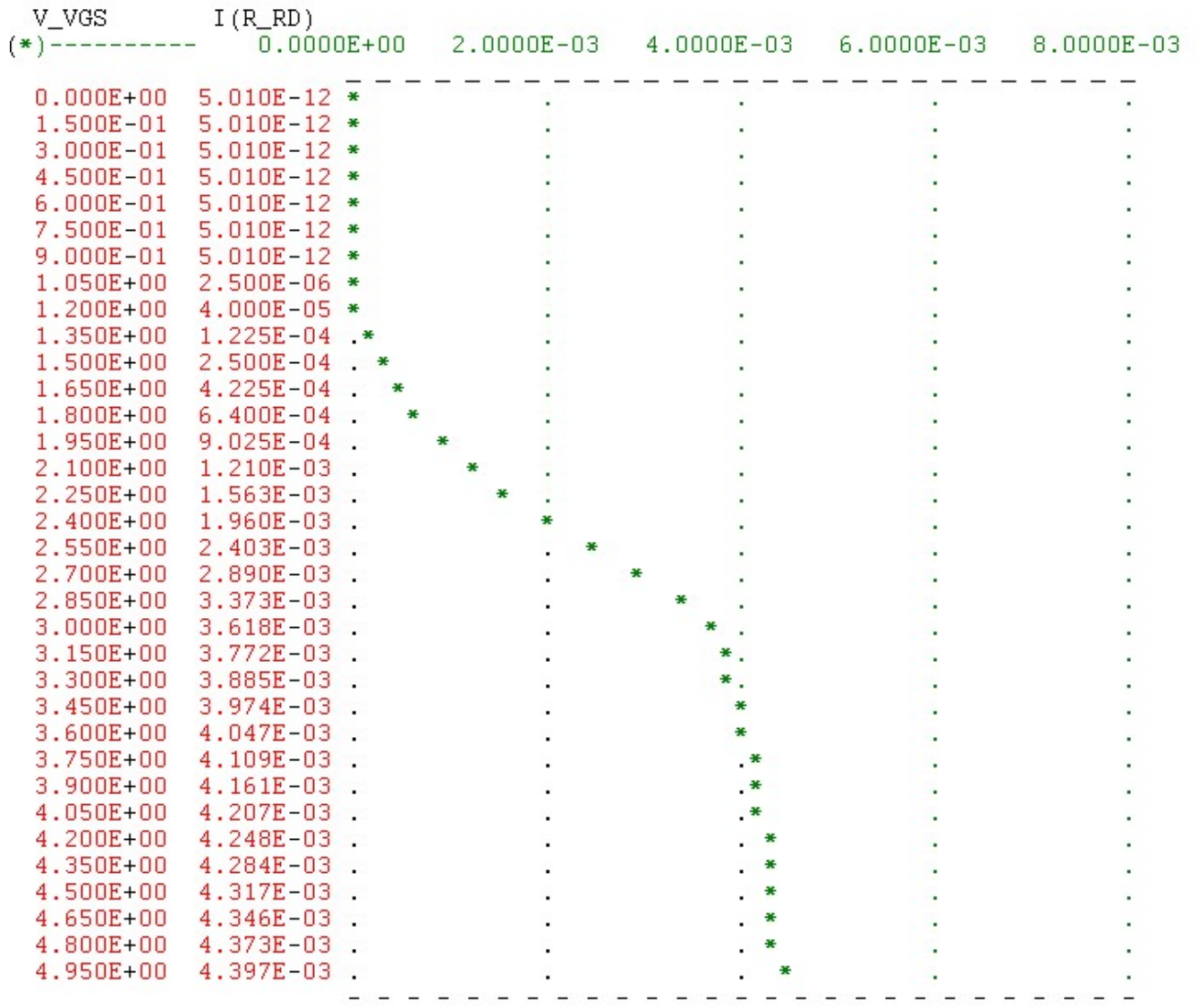
Função de transferência - PSPice

V_VGS	V(2)
0.000E+00	5.000E+00
1.500E-01	5.000E+00
3.000E-01	5.000E+00
4.500E-01	5.000E+00
6.000E-01	5.000E+00
7.500E-01	5.000E+00
9.000E-01	5.000E+00
1.050E+00	4.998E+00
1.200E+00	4.960E+00
1.350E+00	4.878E+00
1.500E+00	4.750E+00
1.650E+00	4.578E+00
1.800E+00	4.360E+00
1.950E+00	4.098E+00
2.100E+00	3.790E+00
2.250E+00	3.438E+00
2.400E+00	3.040E+00
2.550E+00	2.598E+00
2.700E+00	2.110E+00
2.850E+00	1.627E+00
3.000E+00	1.382E+00
3.150E+00	1.228E+00
3.300E+00	1.115E+00
3.450E+00	1.026E+00
3.600E+00	9.529E-01
3.750E+00	8.915E-01
3.900E+00	8.388E-01
4.050E+00	7.927E-01
4.200E+00	7.521E-01
4.350E+00	7.159E-01
4.500E+00	6.834E-01
4.650E+00	6.539E-01
4.800E+00	6.271E-01
4.950E+00	6.026E-01

*) 0.0000E+00 2.0000E+00 4.0000E+00 6.0000E+00 8.0000E+00

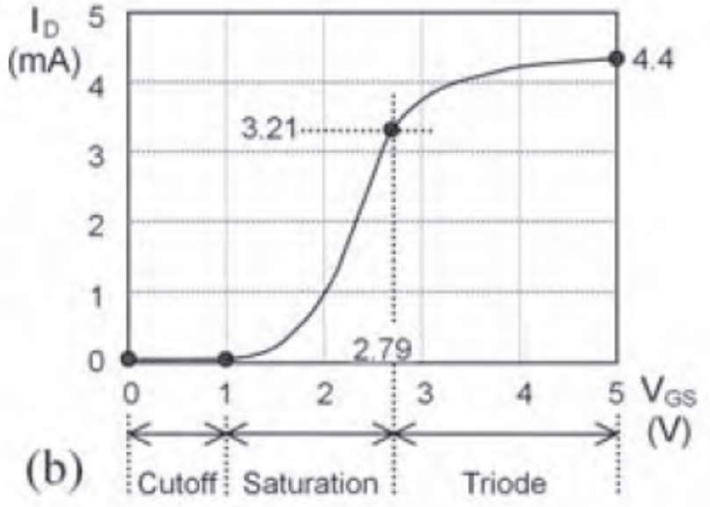


Corrente I_D - PSPice

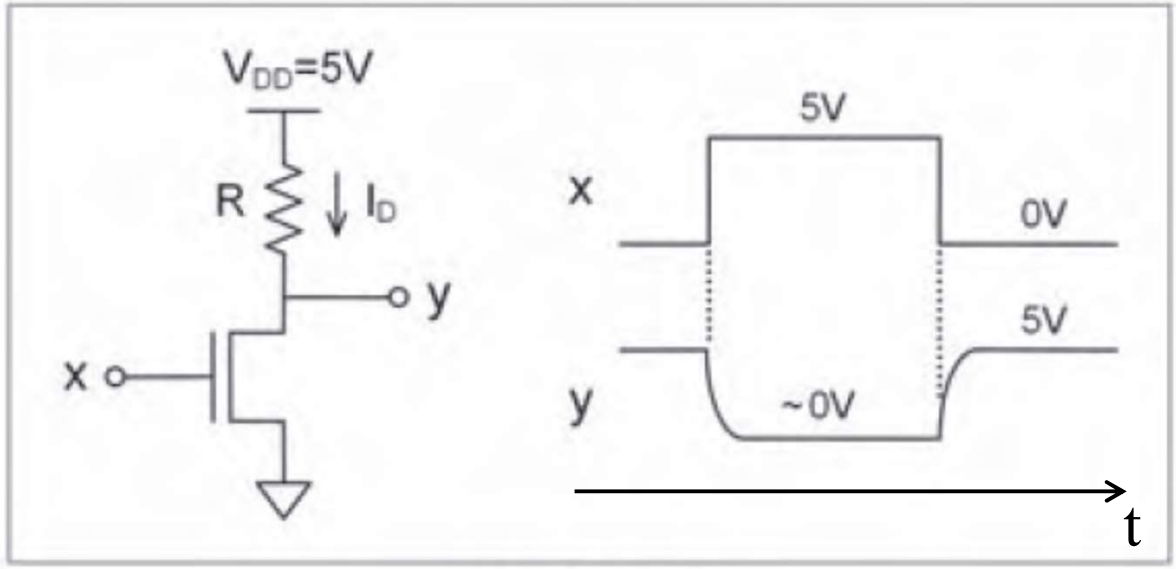


Corrente I_D - PSPice

```
  V_VGS       I(R_RD)
(*)----------    0.0000E+00   2.0000E-03   4.0000E-03   6.0000E-03   8.0000E-03
  0.000E+00  5.010E-12 *
  1.500E-01  5.010E-12 *
  3.000E-01  5.010E-12 *
  4.500E-01  5.010E-12 *
  6.000E-01  5.010E-12 *
  7.500E-01  5.010E-12 *
  9.000E-01  5.010E-12 *
  1.050E+00  2.500E-06 *
  1.200E+00  4.000E-05 *
  1.350E+00  1.225E-04 .*
  1.500E+00  2.500E-04 . *
  1.650E+00  4.225E-04 .  *
  1.800E+00  6.400E-04 .   *
  1.950E+00  9.025E-04 .    *
  2.100E+00  1.210E-03 .     *
  2.250E+00  1.563E-03 .      *
  2.400E+00  1.960E-03 .       *
  2.550E+00  2.403E-03 .        *
  2.700E+00  2.890E-03 .         *
  2.850E+00  3.373E-03 .          *
  3.000E+00  3.618E-03 .           *.
  3.150E+00  3.772E-03 .           *.
  3.300E+00  3.885E-03 .           *.
  3.450E+00  3.974E-03 .           *
  3.600E+00  4.047E-03 .           *
  3.750E+00  4.109E-03 .           .*
  3.900E+00  4.161E-03 .           .*
  4.050E+00  4.207E-03 .           .*
  4.200E+00  4.248E-03 .           . *
  4.350E+00  4.284E-03 .           . *
  4.500E+00  4.317E-03 .           . *
  4.650E+00  4.346E-03 .           . *
  4.800E+00  4.373E-03 .           . *
  4.950E+00  4.397E-03 .           .  *
```



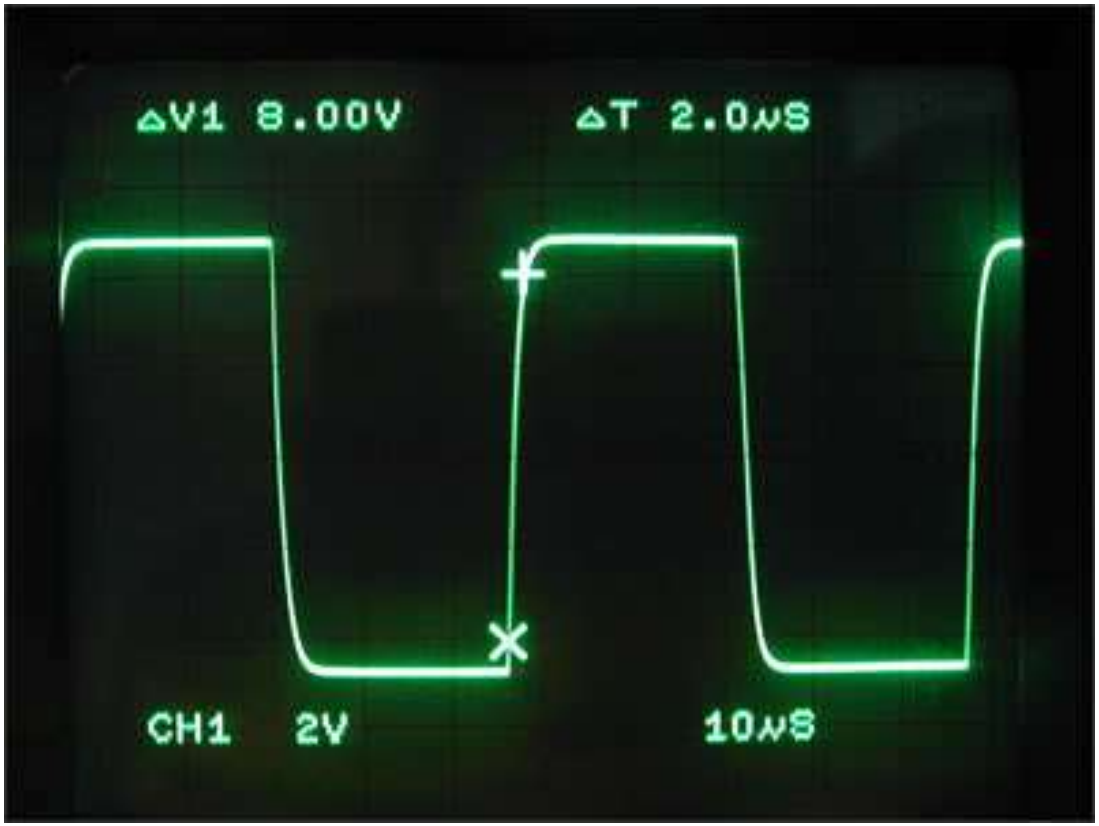
Resposta a Onda Quadrada (agora em **função do tempo**!)



(a) nMOS

Tempo de resposta devido à capacitância MOS

Resposta a Onda Quadrada (agora em função do tempo!)



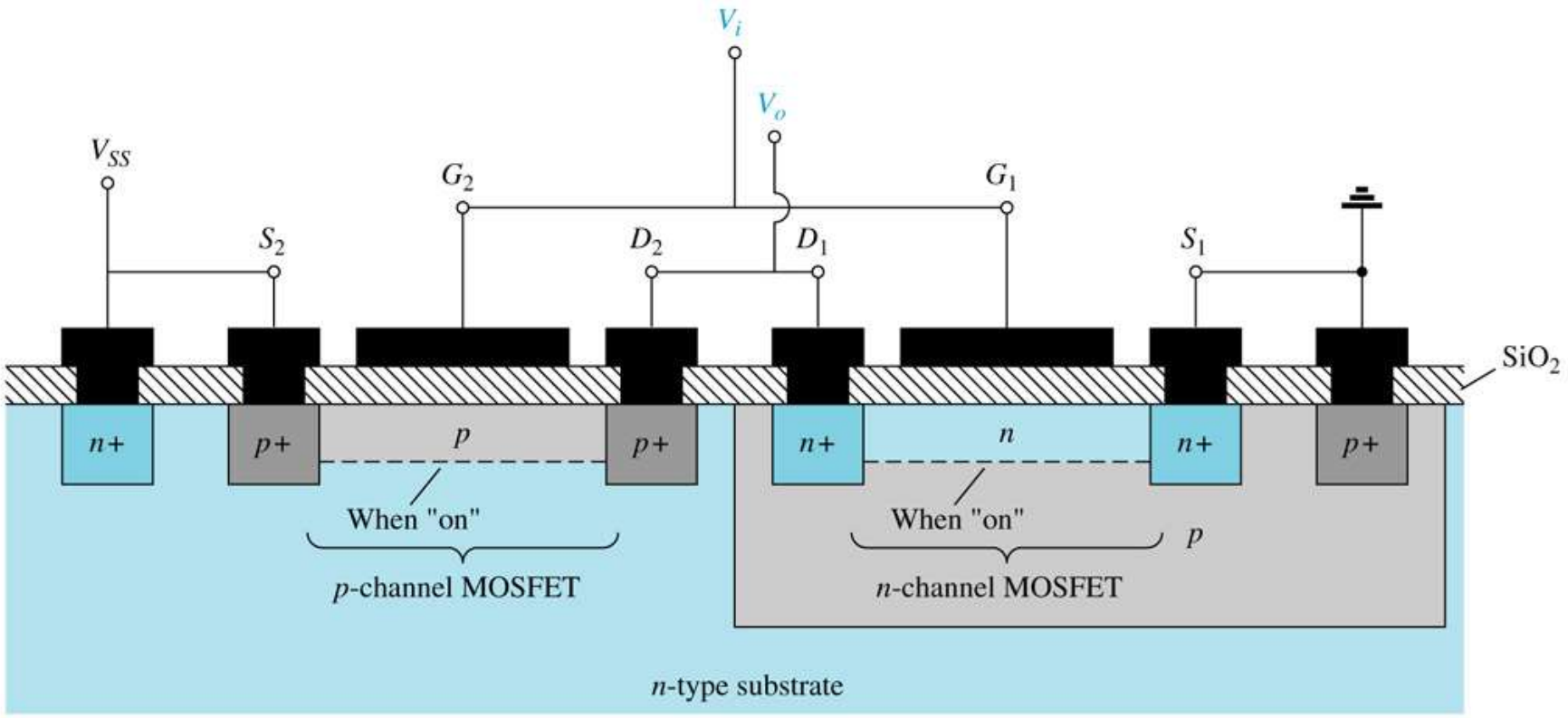
Tempo de resposta devido à capacitância MOS

Resposta a Onda Quadrada (agora em função do tempo!)

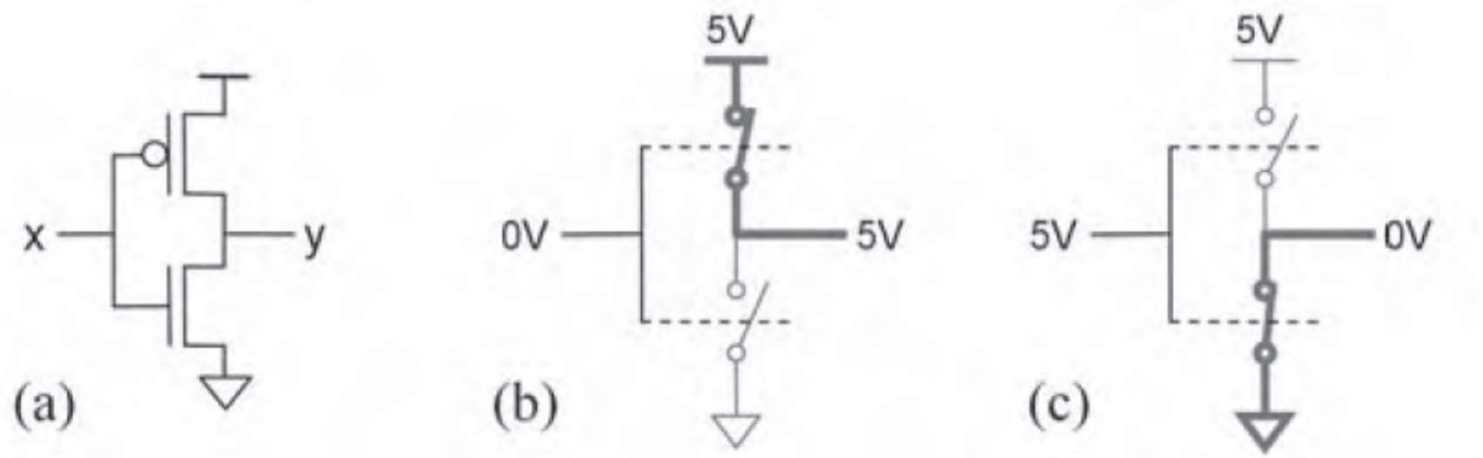
Exercício: simular a resposta transiente do circuito com N-MOS

```
* source EXEMPLO N-MOS

R_RD   3      2      1k     TC=0,0
V_VDD  3      0      DC 5V
V_VGS  1      0      DC 5V

M_M1   2      1      0      0      M1
.model M1 NMOS(Vto = 1V Kp = 2e-3)

.DC V_VGS     0      5      0.15
.PLOT         DC     V[2]   I(R_RD)
```

Inversor CMOS – Complementary MOS

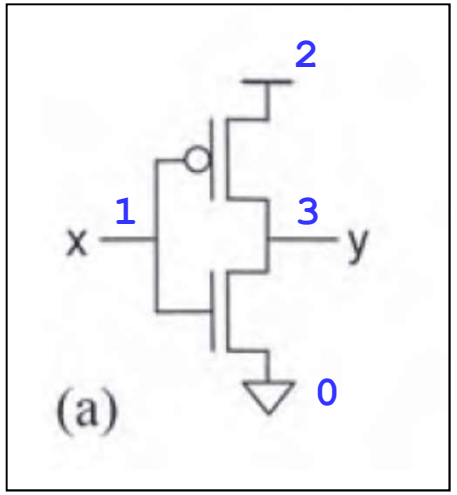


Inversor CMOS – Complementary MOS



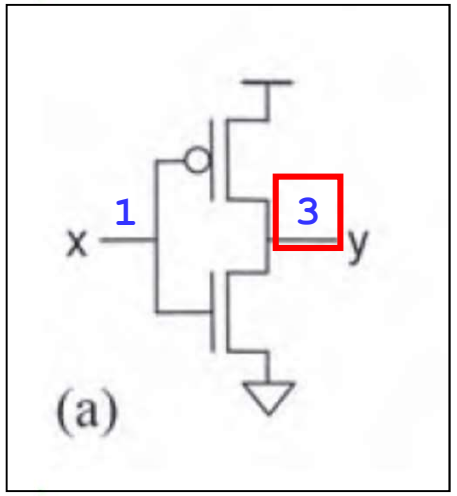
Inversor CMOS – Complementary MOS

```
* source EXEMPLO C-MOS

V_VDD  2   0   DC 5V

M_M1   3   1   0   0   M1
.model M1 NMOS(Vto = 1V Kp = 2e-3)
M_M2   3   1   2       2       M2
.model M2 PMOS(Vto = 1V Kp = 2e-3)

V_VGS  1   0   PULSE(0 5 0 1ns 1ns 10us 20us)

.TRAN 1us 80us
.PLOT TRAN  V[3]
.PLOT TRAN  V[1]
```



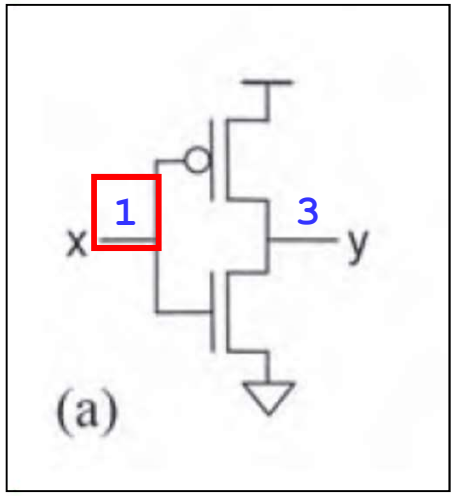
Inversor CMOS – Complementary MOS

TIME	V(3)
(*)----------	0.0000E+00 2.0000E+00 4.0000E+00 6.0000E+00 8.0000E+00
0.000E+00	5.000E+00
1.000E-06	1.270E-01
2.000E-06	1.270E-01
3.000E-06	1.270E-01
4.000E-06	1.270E-01
5.000E-06	1.270E-01
6.000E-06	1.270E-01
7.000E-06	1.270E-01
8.000E-06	1.270E-01
9.000E-06	1.270E-01
1.000E-05	1.270E-01
1.100E-05	5.000E+00
1.200E-05	5.000E+00
1.300E-05	5.000E+00
1.400E-05	5.000E+00
1.500E-05	5.000E+00
1.600E-05	5.000E+00
1.700E-05	5.000E+00
1.800E-05	5.000E+00
1.900E-05	5.000E+00
2.000E-05	5.000E+00
2.100E-05	1.270E-01
2.200E-05	1.270E-01
2.300E-05	1.270E-01
2.400E-05	1.270E-01
2.500E-05	1.270E-01
2.600E-05	1.270E-01
2.700E-05	1.270E-01
2.800E-05	1.270E-01
2.900E-05	1.270E-01
3.000E-05	1.270E-01
3.100E-05	5.000E+00
3.200E-05	5.000E+00
3.300E-05	5.000E+00
3.400E-05	5.000E+00
3.500E-05	5.000E+00
3.600E-05	5.000E+00
3.700E-05	5.000E+00
3.800E-05	5.000E+00
3.900E-05	5.000E+00

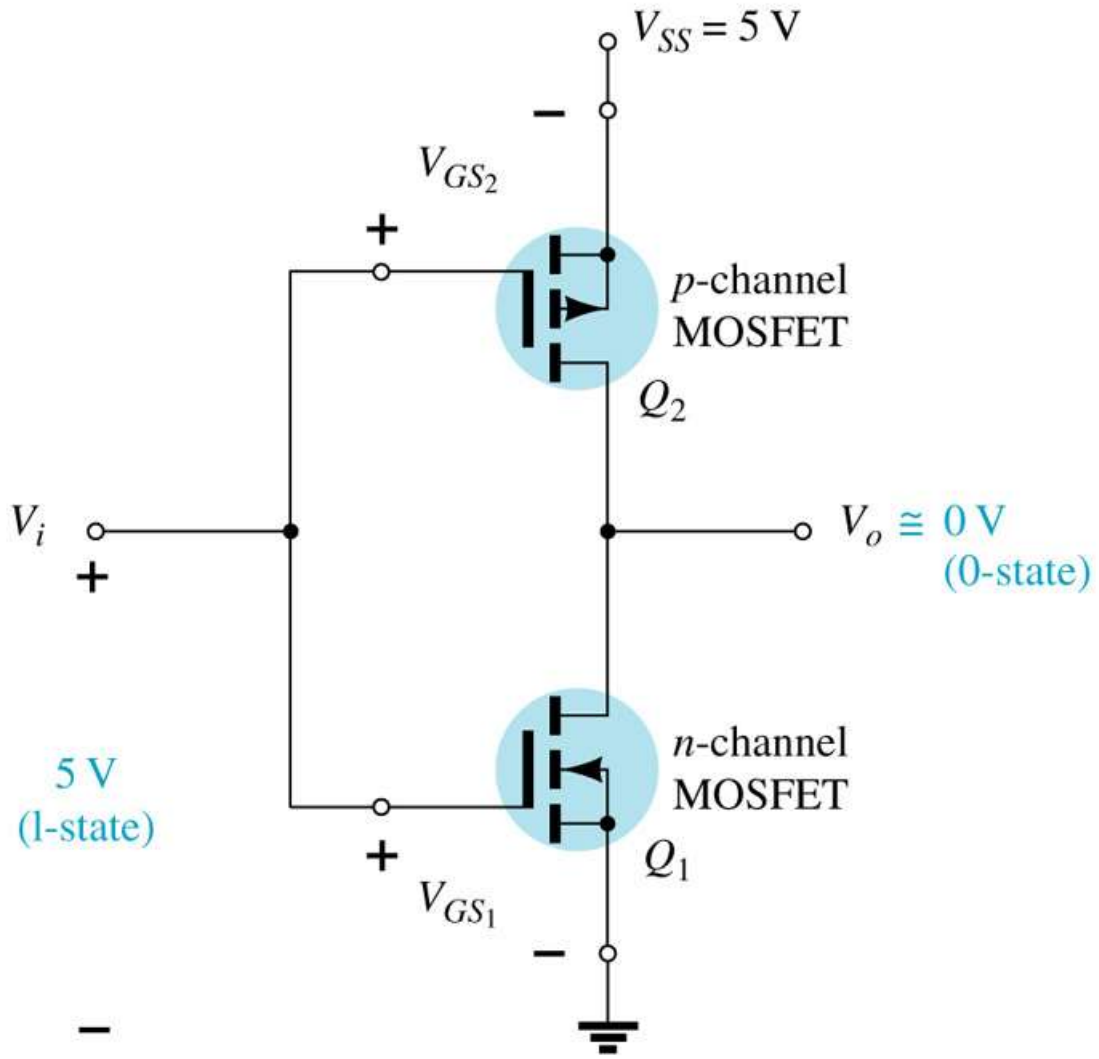


Inversor CMOS – Complementary MOS

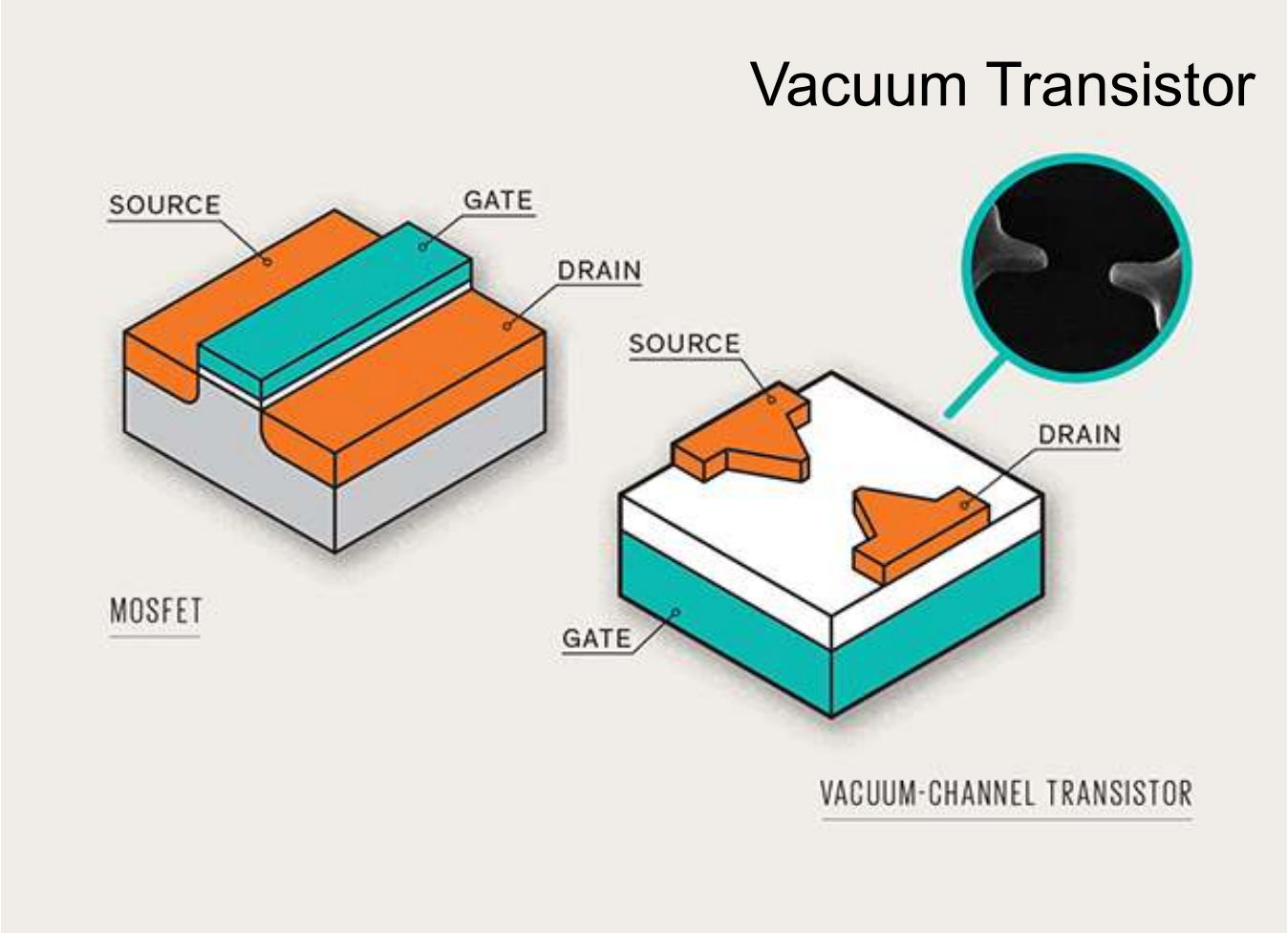
```
  TIME         V(1)
(*)----------    0.0000E+00   2.0000E+00   4.0000E+00   6.0000E+00   8.0000E+00
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  0.000E+00  0.000E+00 *           .            .            .            .
  1.000E-06  5.000E+00 .           .            .            *            .
  2.000E-06  5.000E+00 .           .            .            *            .
  3.000E-06  5.000E+00 .           .            .            *            .
  4.000E-06  5.000E+00 .           .            .            *            .
  5.000E-06  5.000E+00 .           .            .            *            .
  6.000E-06  5.000E+00 .           .            .            *            .
  7.000E-06  5.000E+00 .           .            .            *            .
  8.000E-06  5.000E+00 .           .            .            *            .
  9.000E-06  5.000E+00 .           .            .            *            .
  1.000E-05  5.000E+00 .           .            .            *            .
  1.100E-05  0.000E+00 *           .            .                         .
  1.200E-05  0.000E+00 *           .            .                         .
  1.300E-05  0.000E+00 *           .            .                         .
  1.400E-05  0.000E+00 *           .            .                         .
  1.500E-05  0.000E+00 *           .            .                         .
  1.600E-05  0.000E+00 *           .            .                         .
  1.700E-05  0.000E+00 *           .            .                         .
  1.800E-05  0.000E+00 *           .            .                         .
  1.900E-05  0.000E+00 *           .            .                         .
  2.000E-05  8.000E-07 *           .            .                         .
  2.100E-05  5.000E+00 .           .            .            *            .
  2.200E-05  5.000E+00 .           .            .            *            .
  2.300E-05  5.000E+00 .           .            .            *            .
  2.400E-05  5.000E+00 .           .            .            *            .
  2.500E-05  5.000E+00 .           .            .            *            .
  2.600E-05  5.000E+00 .           .            .            *            .           .
  2.700E-05  5.000E+00 .           .            .            *            .           .
  2.800E-05  5.000E+00 .           .            .            *            .           .
  2.900E-05  5.000E+00 .           .            .            *            .           .
  3.000E-05  5.000E+00 .           .            .            *            .           .
  3.100E-05  0.000E+00 *           .            .                         .           .
  3.200E-05  0.000E+00 *           .            .                         .           .
  3.300E-05  0.000E+00 *           .            .                         .           .
  3.400E-05  0.000E+00 *           .            .                         .           .
  3.500E-05  0.000E+00 *           .            .                         .           .
  3.600E-05  0.000E+00 *           .            .                         .           .
  3.700E-05  0.000E+00 *           .            .                         .           .
  3.800E-05  0.000E+00 *           .            .                         .           .
  3.900E-05  0.000E+00 *           .            .                         .           .
  4.000E-05  8.000E-07 *           .            .                         .           .
  4.100E-05  5.000E+00 .           .            .            *            .           .
```



Inversor CMOS – Complementary MOS



Novas Tecnologias de Transistores



http://spectrum.ieee.org/semiconductors/devices/introducing-the-vacuum-transistor-a-device-made-of-nothing/?utm_source=techalert&utm_medium=email&utm_campaign=062614

26 Feb 2018 | 16:00 GMT

Chipmakers Test Ferroelectrics as a Route to Ultralow-Power Chips

But doubts linger over ferroelectric transistors' ability to jump from lab to fab

By **Katherine Bourzac**

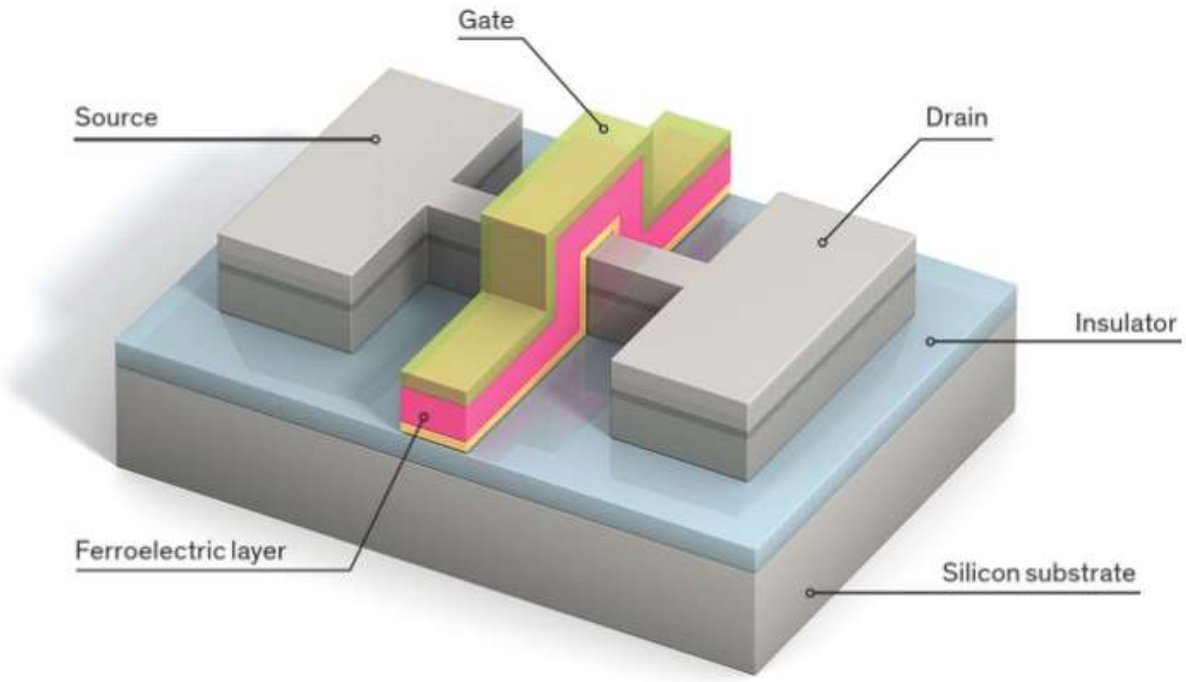


Illustration: Emily Cooper

Power Down: Chipmakers are adding a thin layer of ferroelectric material to transistors, including fin-shaped field-effect transistors (FinFETs), to reduce the gate voltage required for switching.