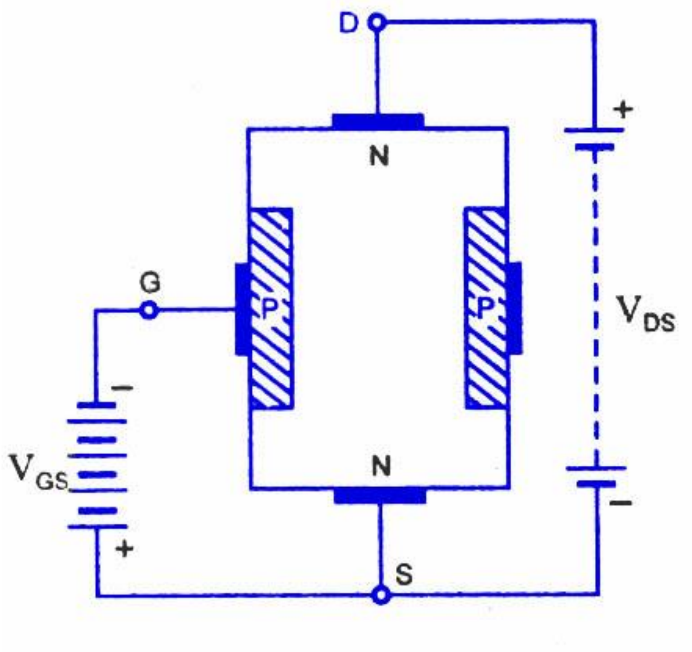
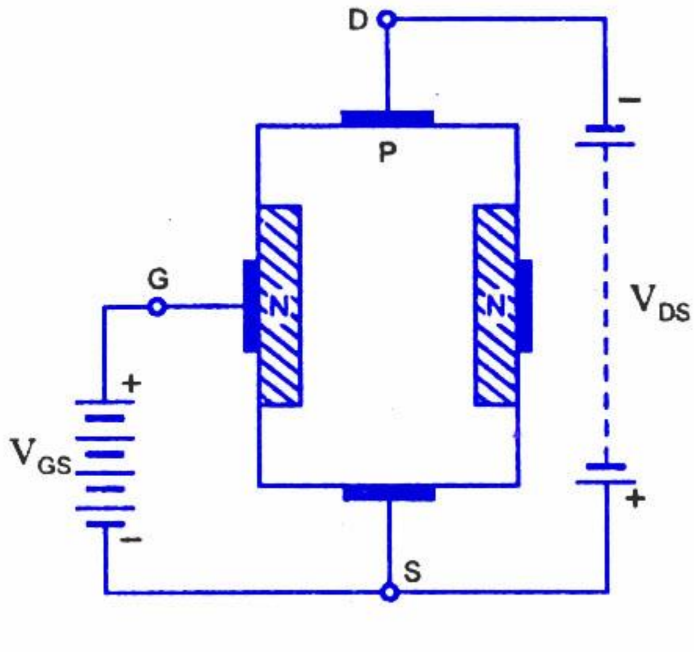
Transistores de Efeito de Campo - FET



N-Channel JFET



P-Channel JFET

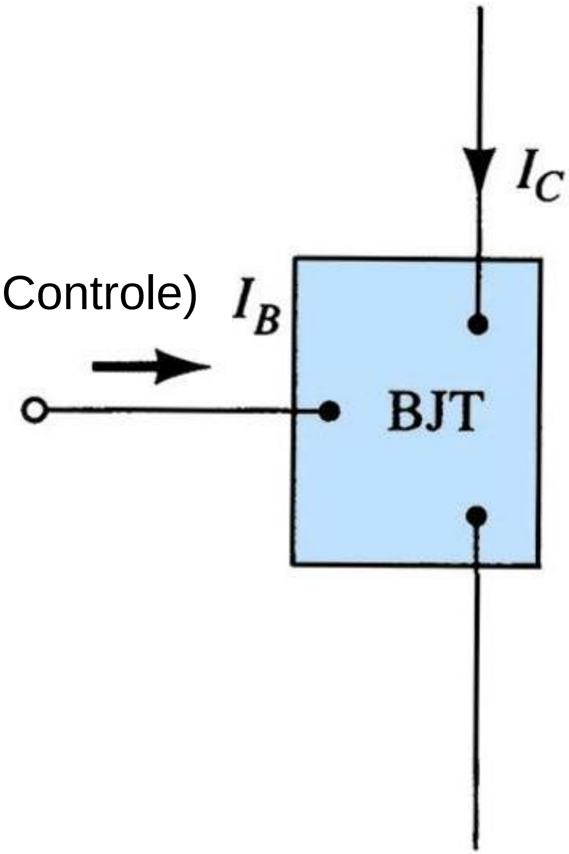
Conteúdo

- Estrutura dos JFETs
- Controle do canal (aberto/fechado)
- Análise qualitativa
- Análise quantitativa
- Regiões de operação
- Aplicações
  - Chave série
  - Chave paralela
  - *Chopper*

Comparação:

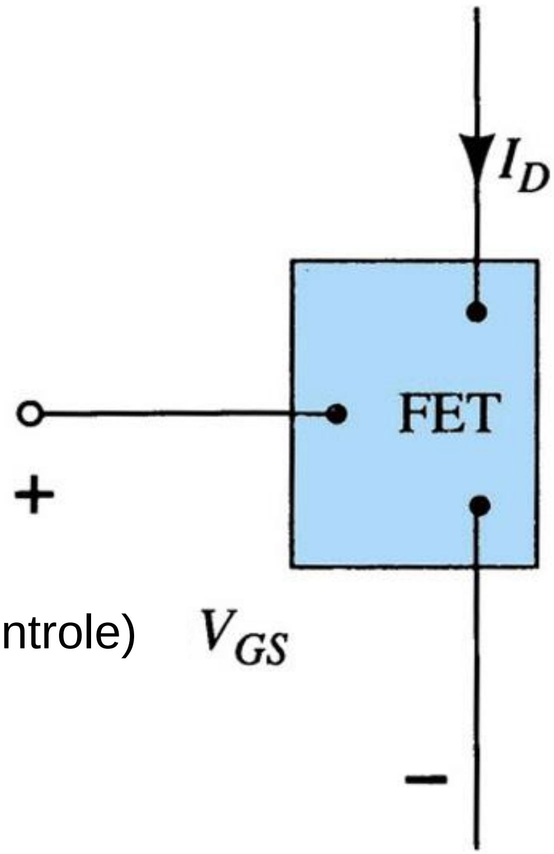
TBJ – Amplificador controlado por Corrente

(Corrente de Controle)



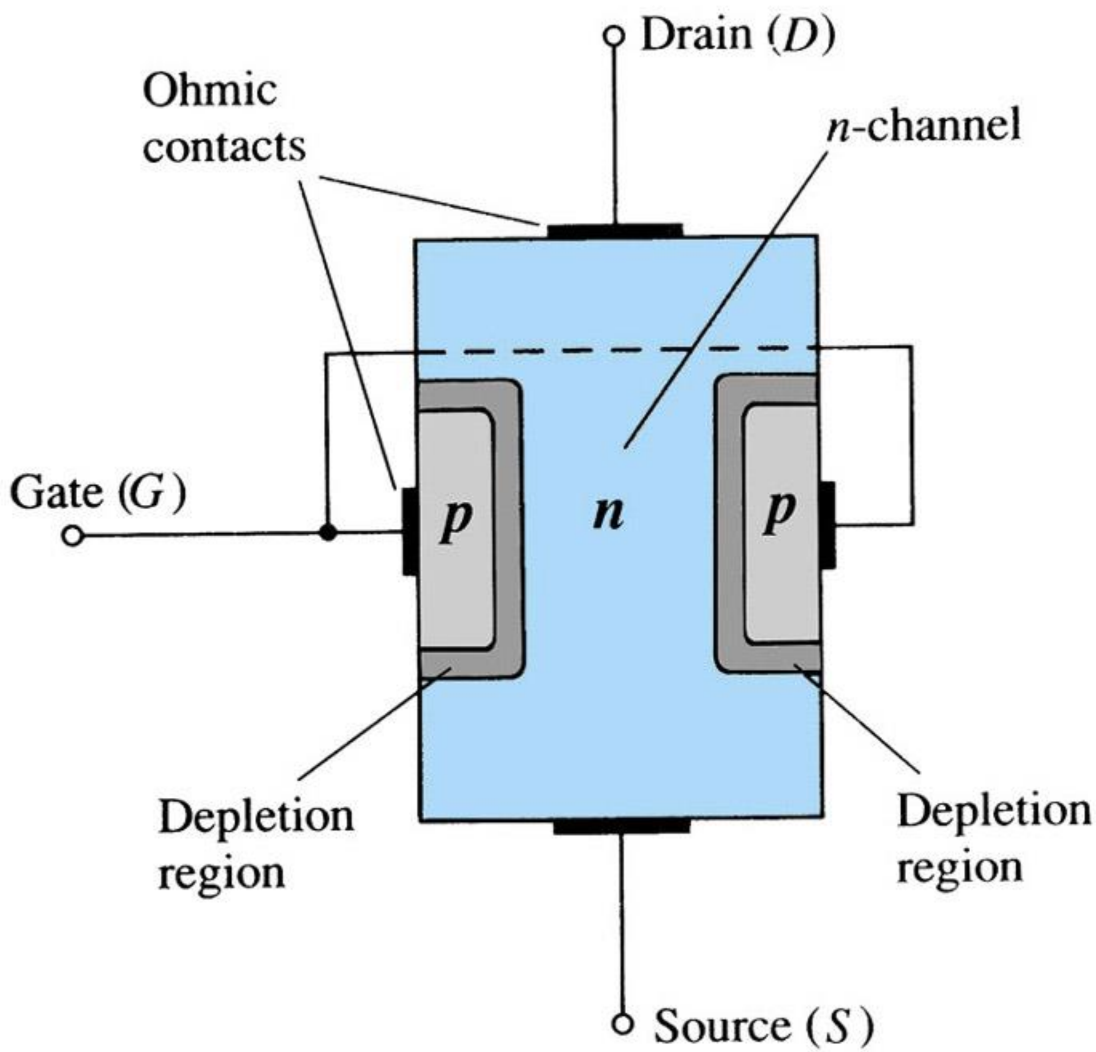
Comparação:

FET– Amplificador controlado por Tensão

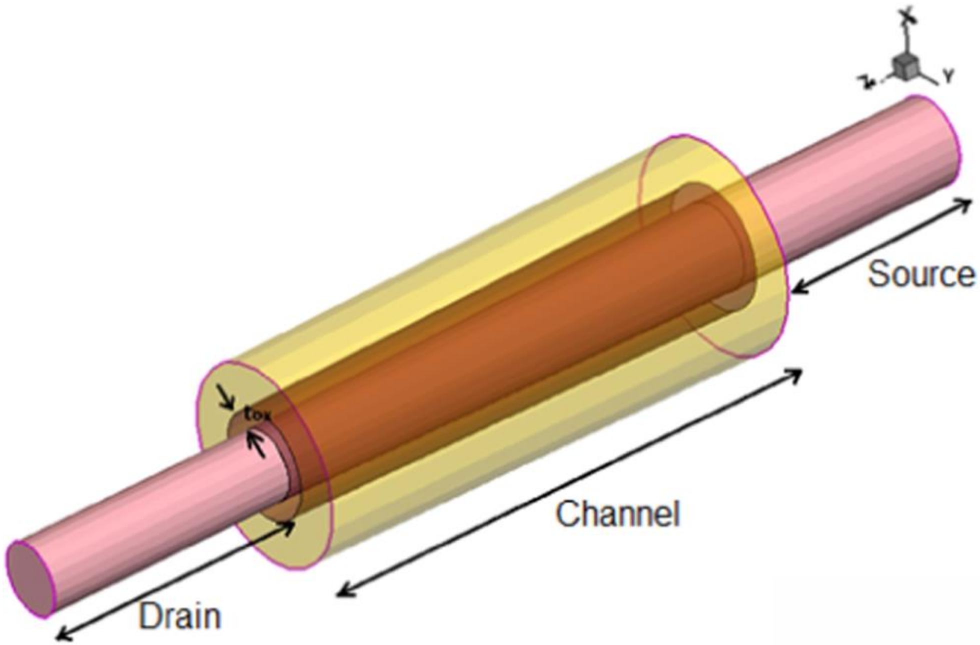


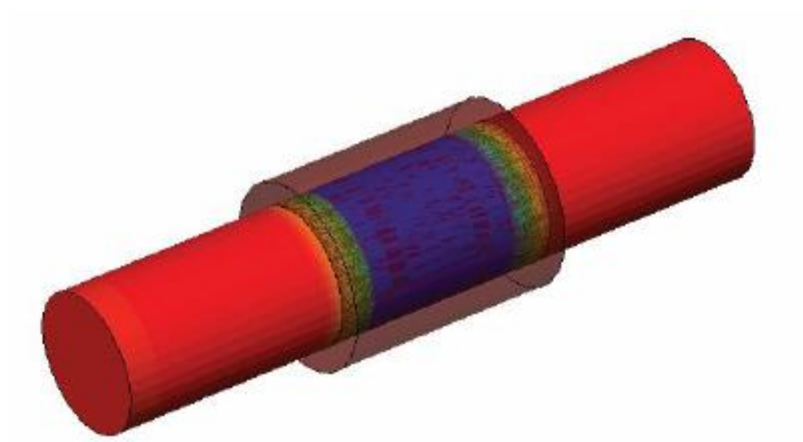
(Tensão de Controle)

FET - Estrutura

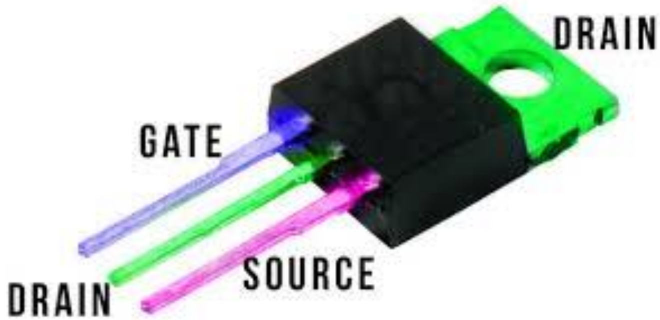


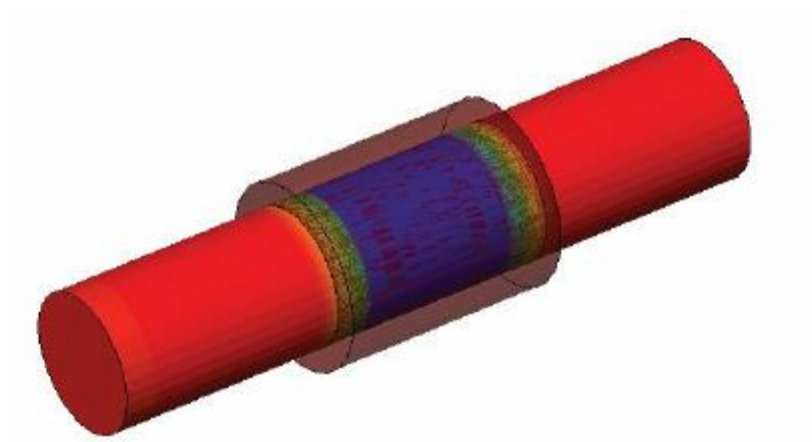
FET - Estrutura



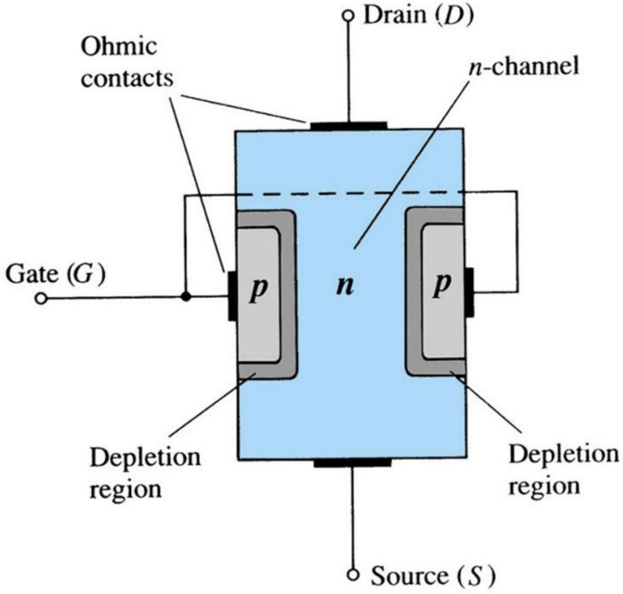


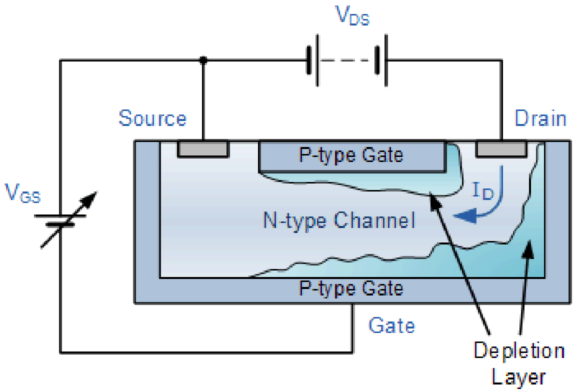
FET - Estrutura



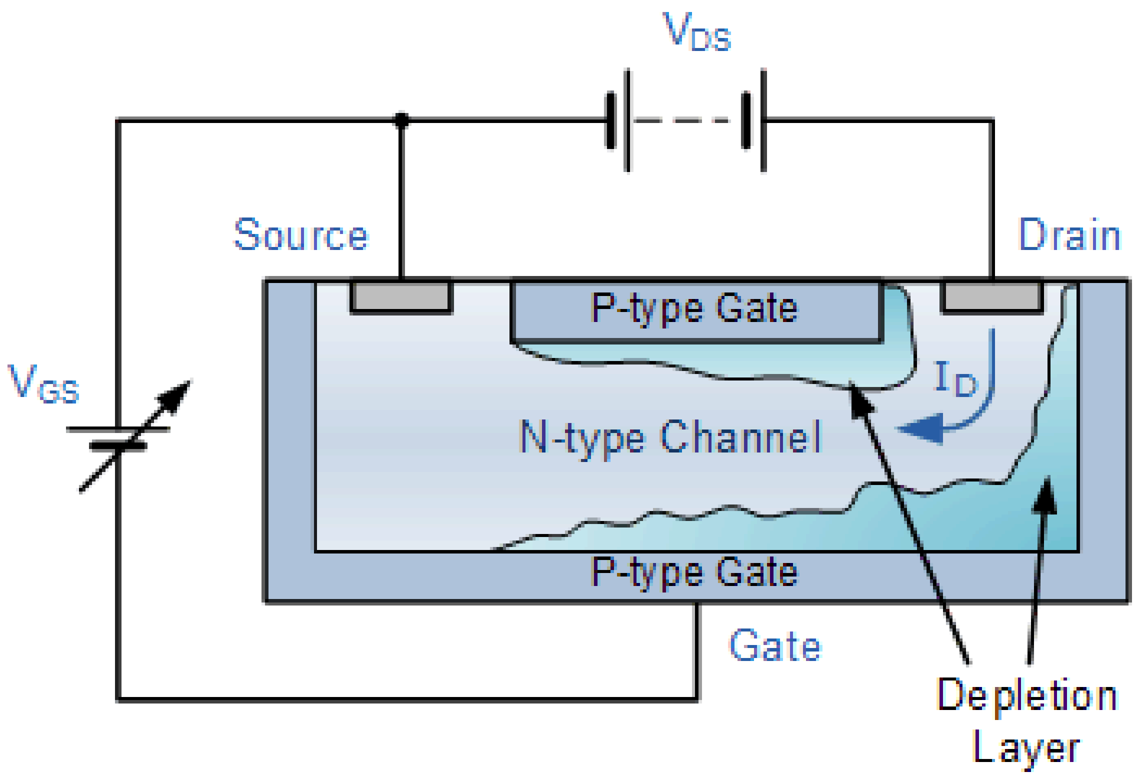


FET – Análise – *canal N*

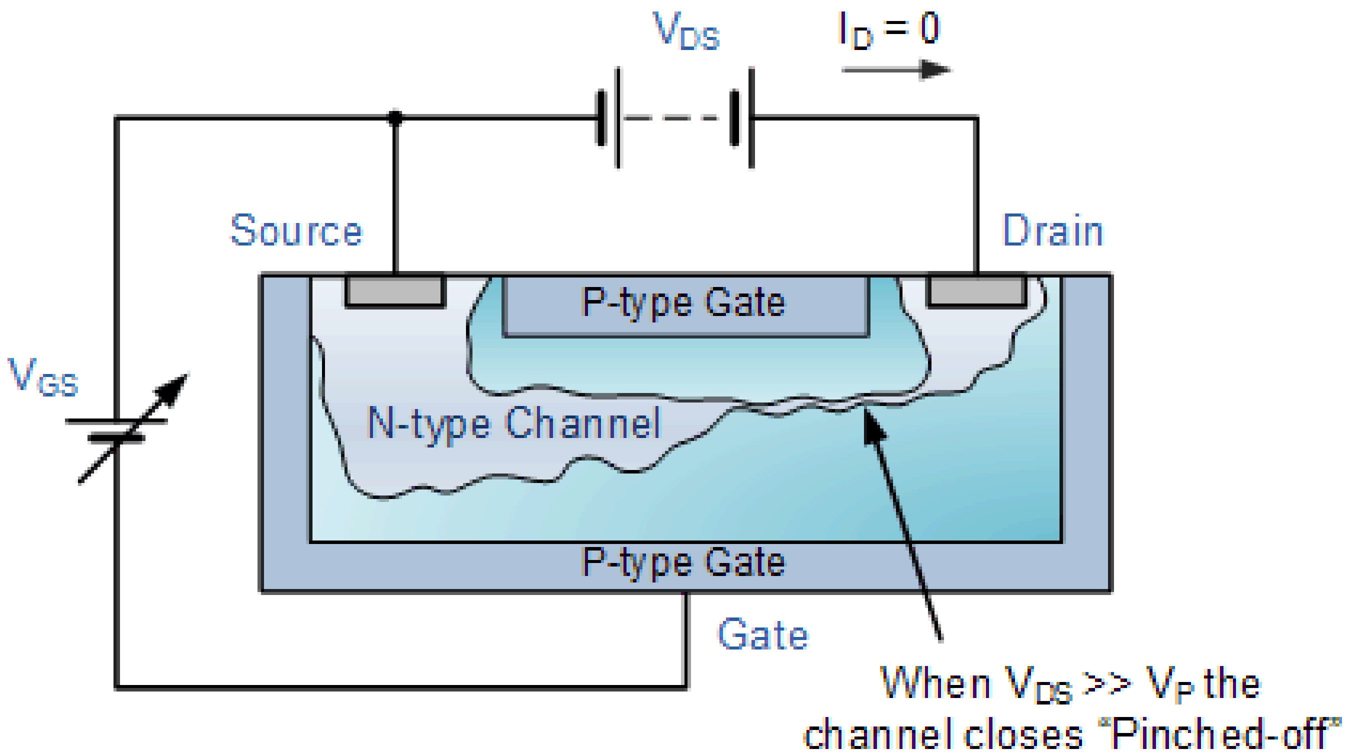




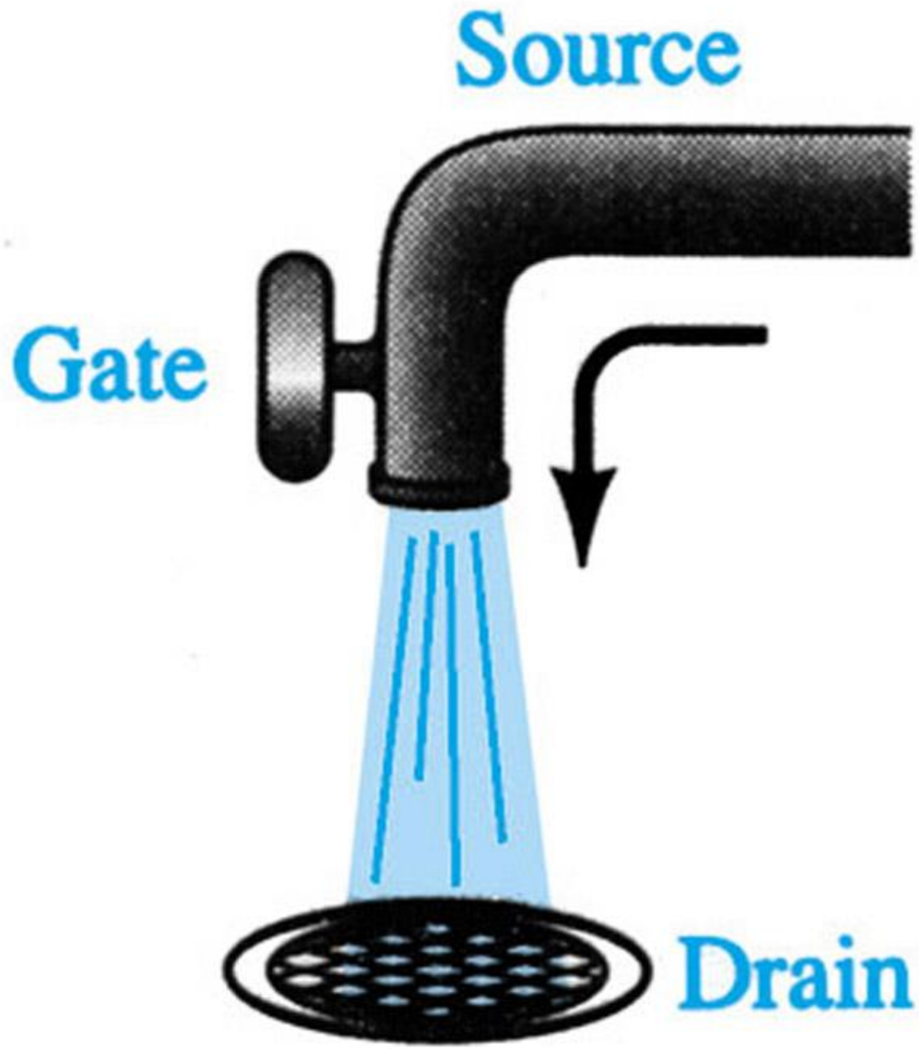
FET – Canal aberto



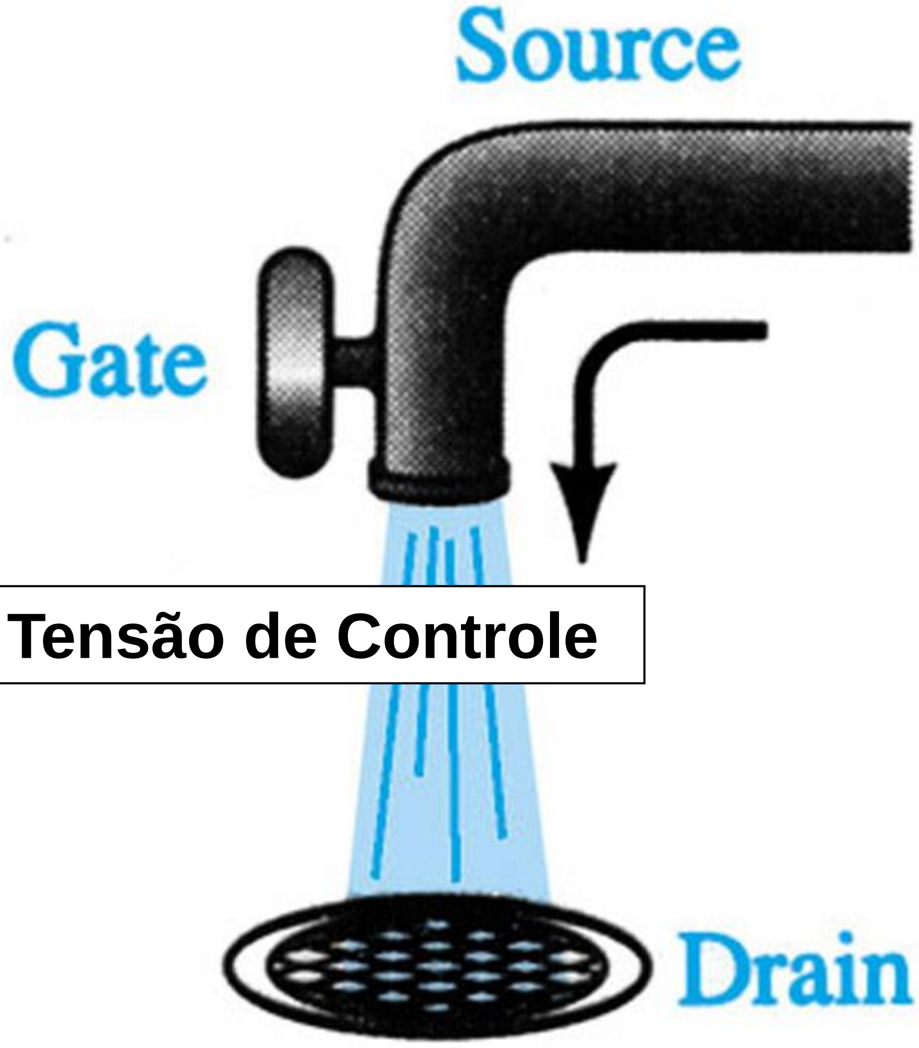
FET – Canal fechado



FET – Mecanismo de Controle



FET – Mecanismo de Controle



V_{GS} => Tensão de Controle

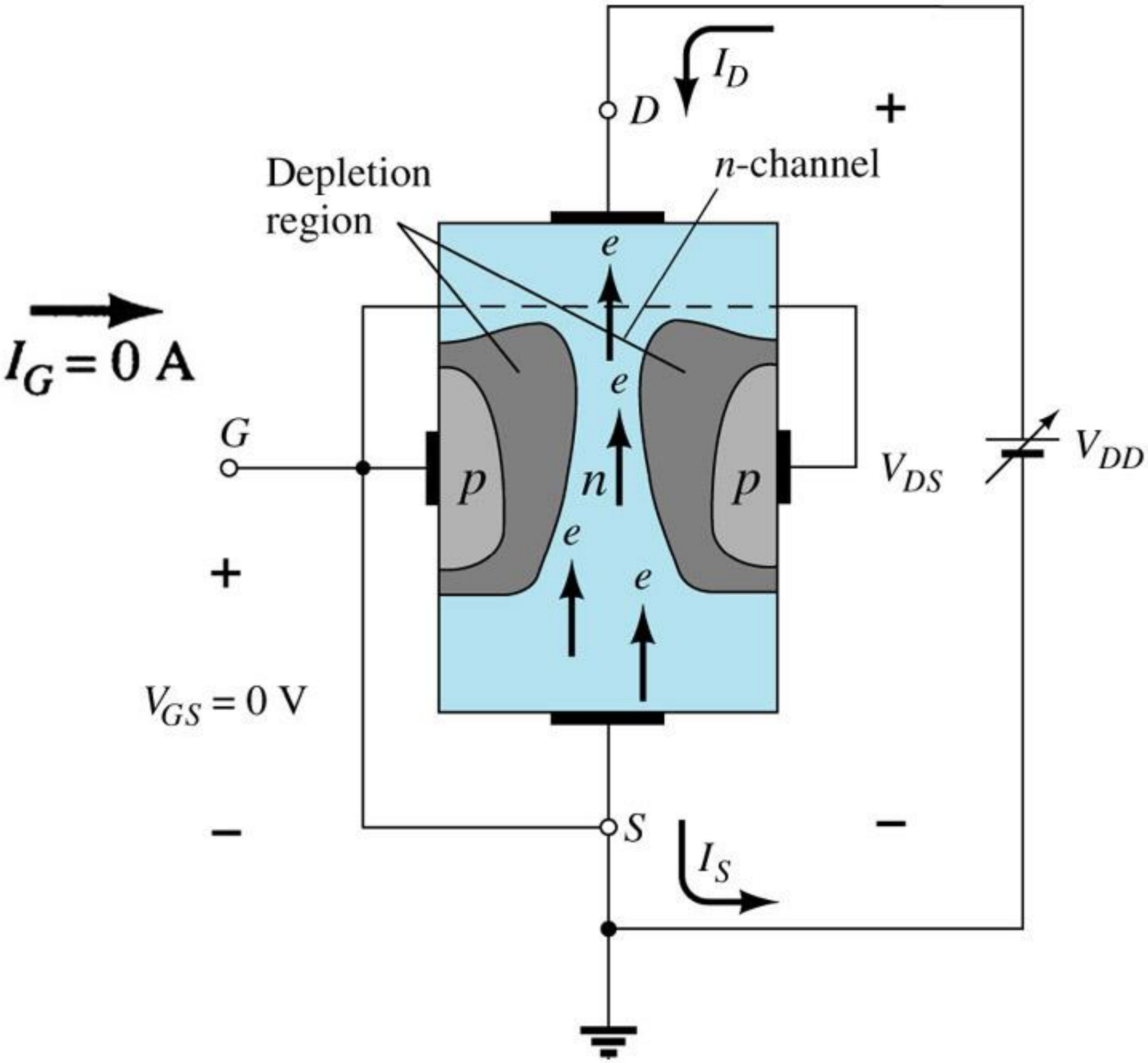
i - Análise com $V_{GS} = 0$ V and $V_{DS} > 0$ V

ii - Análise com $V_{GS} < 0$ V and $V_{DS} > 0$ V

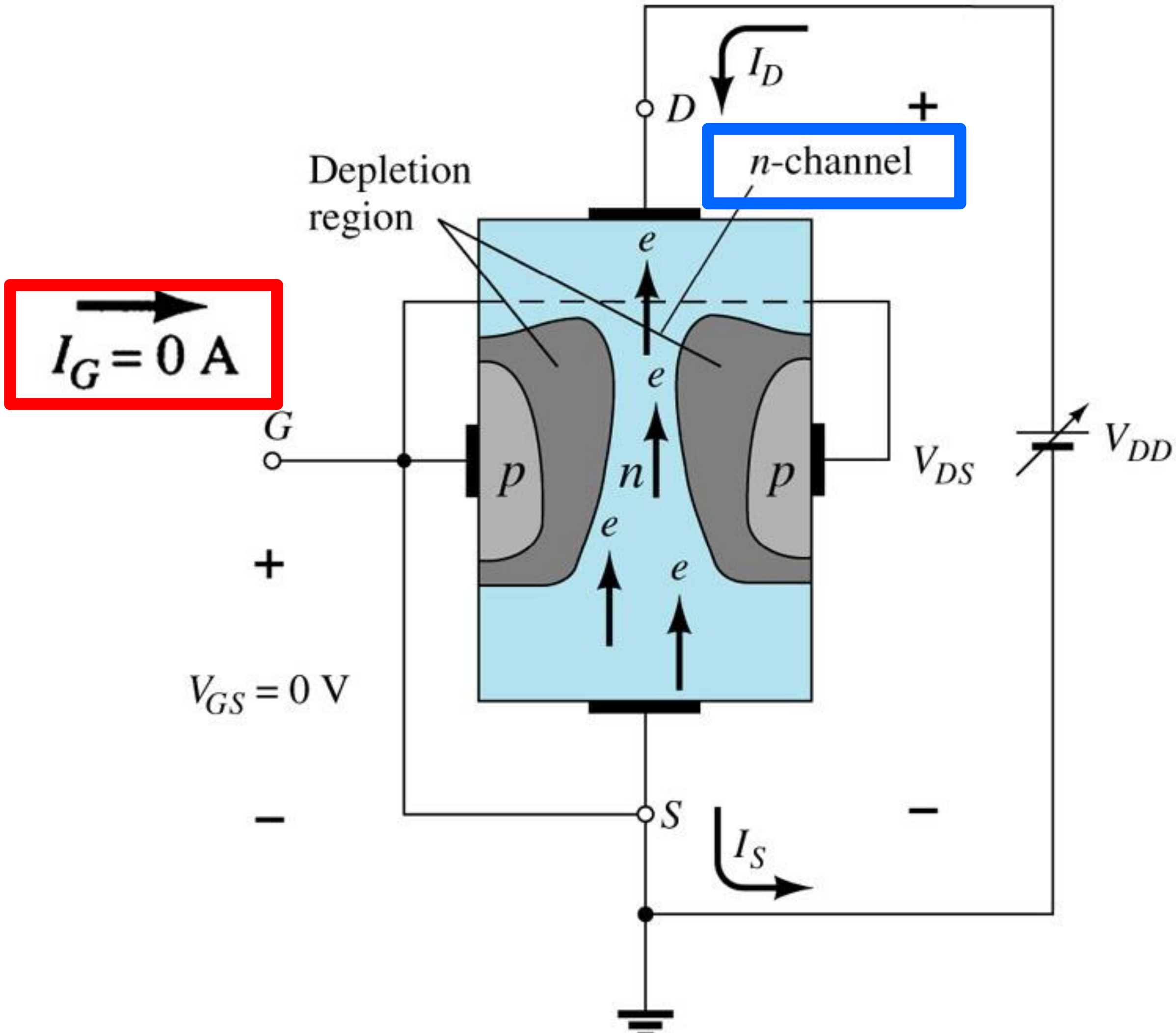
i - Análise com $V_{GS} = 0$ V and $V_{DS} > 0$ V

ii - Análise com $V_{GS} < 0$ V and $V_{DS} > 0$ V

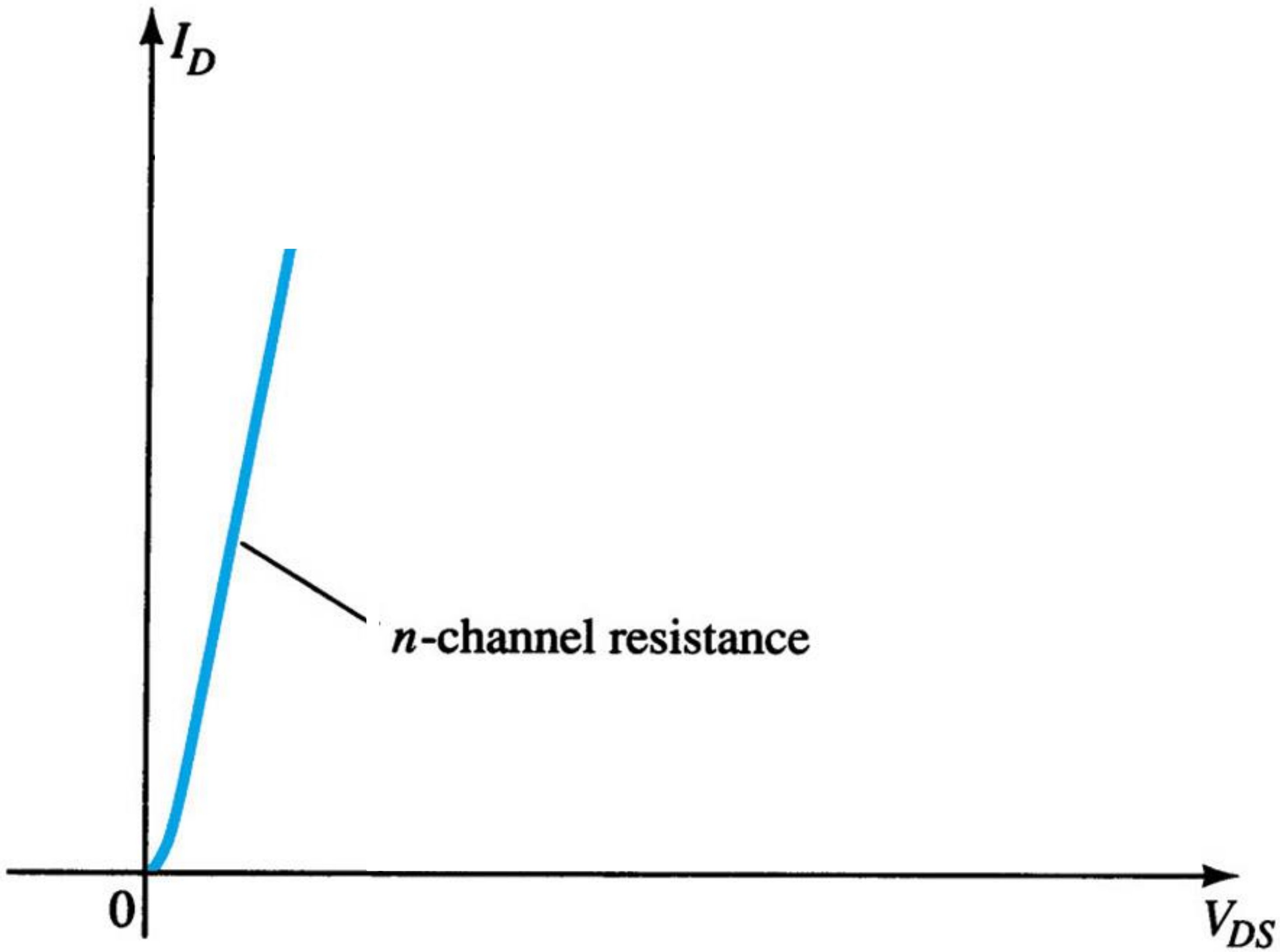
FET com V_{GS} = 0 V and V_{DS} > 0 V



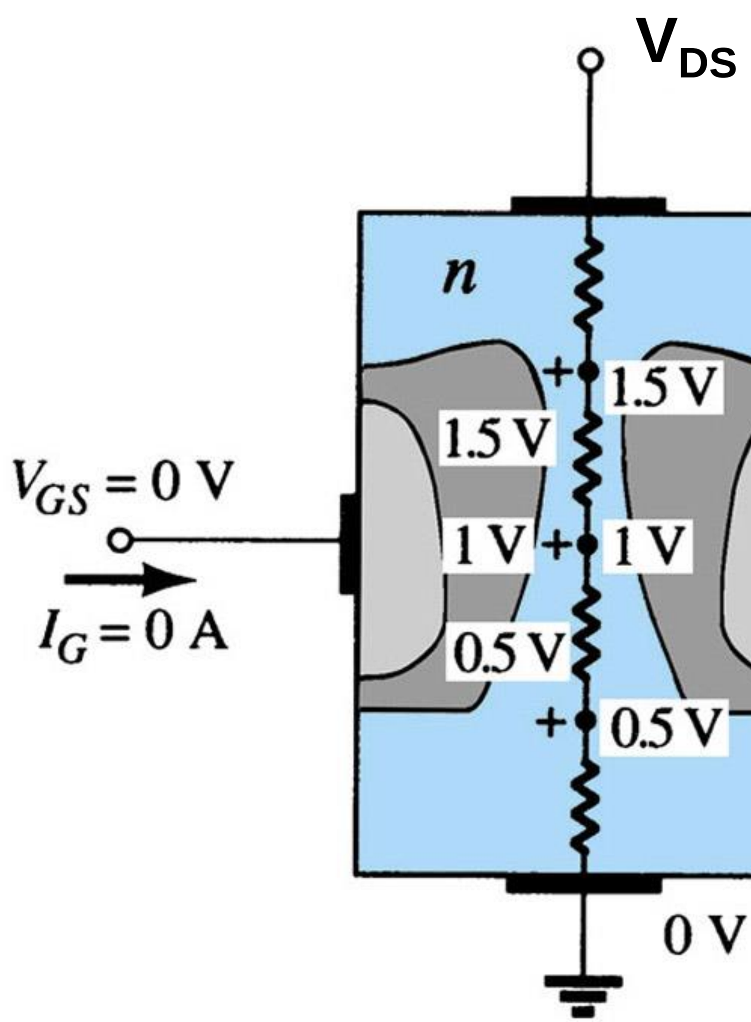
FET com V_{GS} = 0 V and V_{DS} > 0 V



I_D versus V_{DS} com $\boldsymbol{V_{GS}}$ **= 0 V**

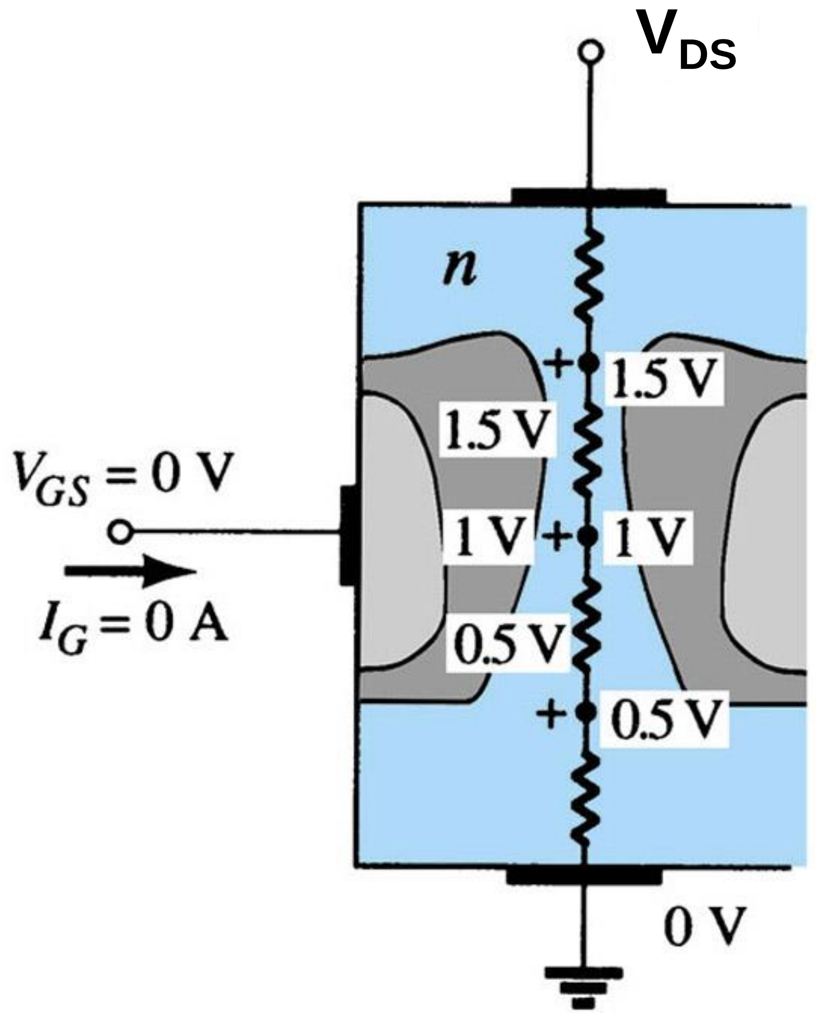


Se V_{DS} continua a aumentar?



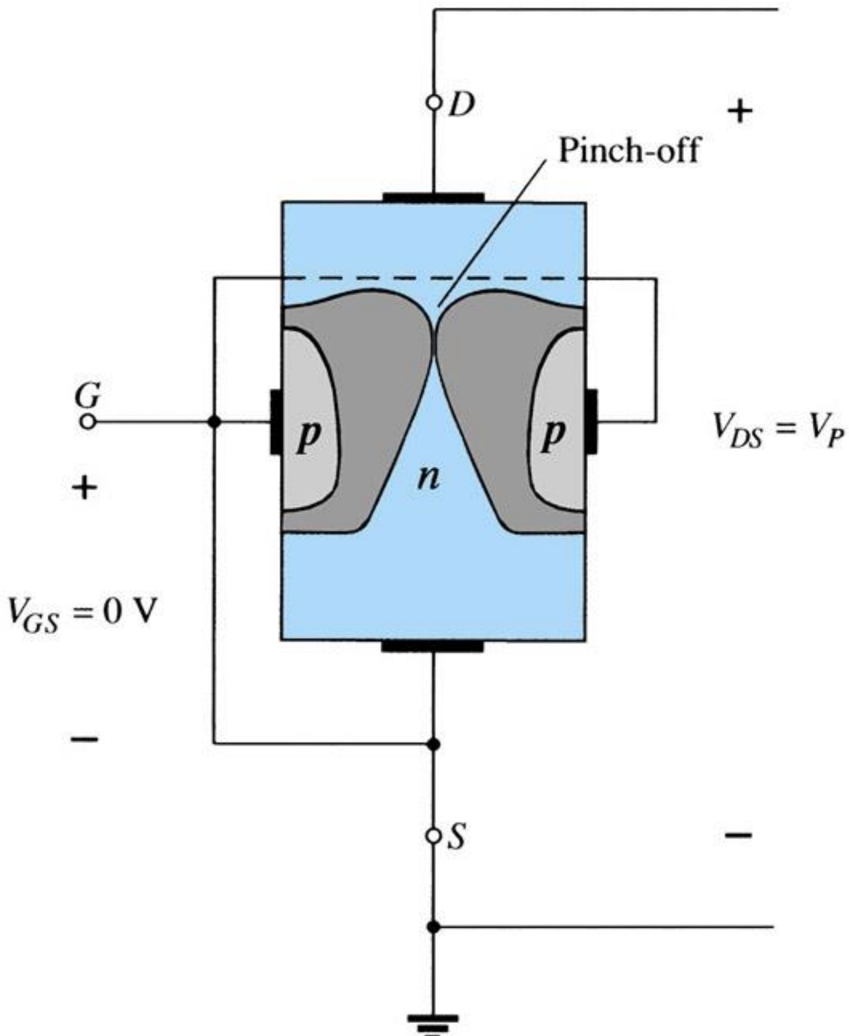
V_{GS} = 0 V and V_{DS} > 0 V

Potencial reverso na junção PN



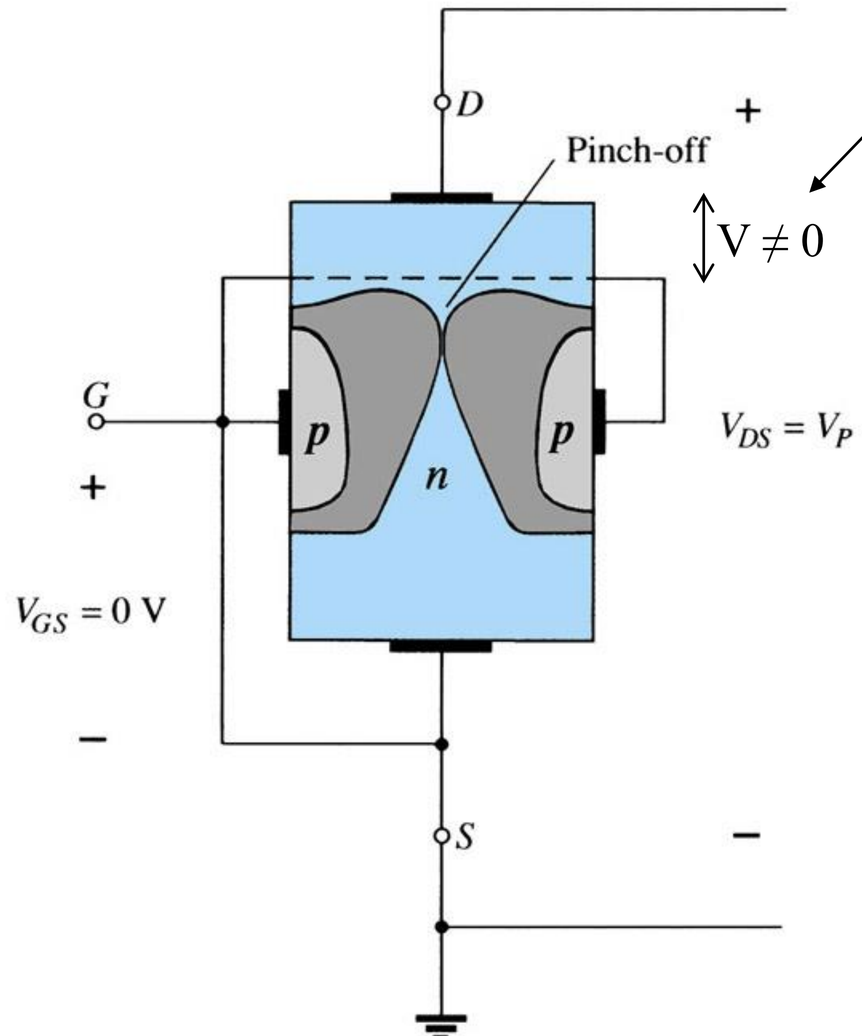
$V_{GS} = 0$ V and $V_{DS} > 0$ V

Pinch-off (V_{GS} = 0 V, $V_{DS} = V_P$)

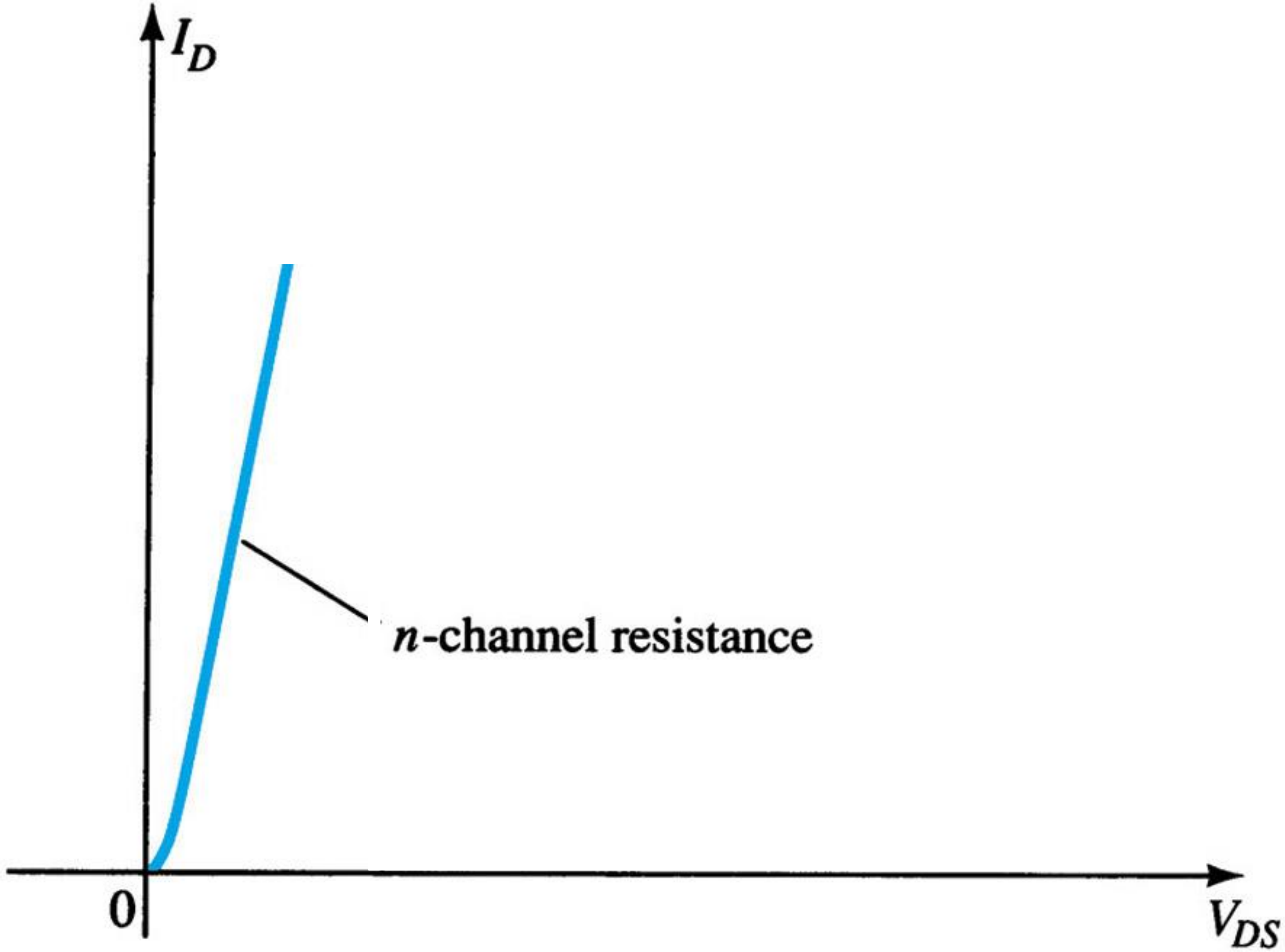


Pinch-off (V_{GS} = 0 V, V_{DS} = V_P)

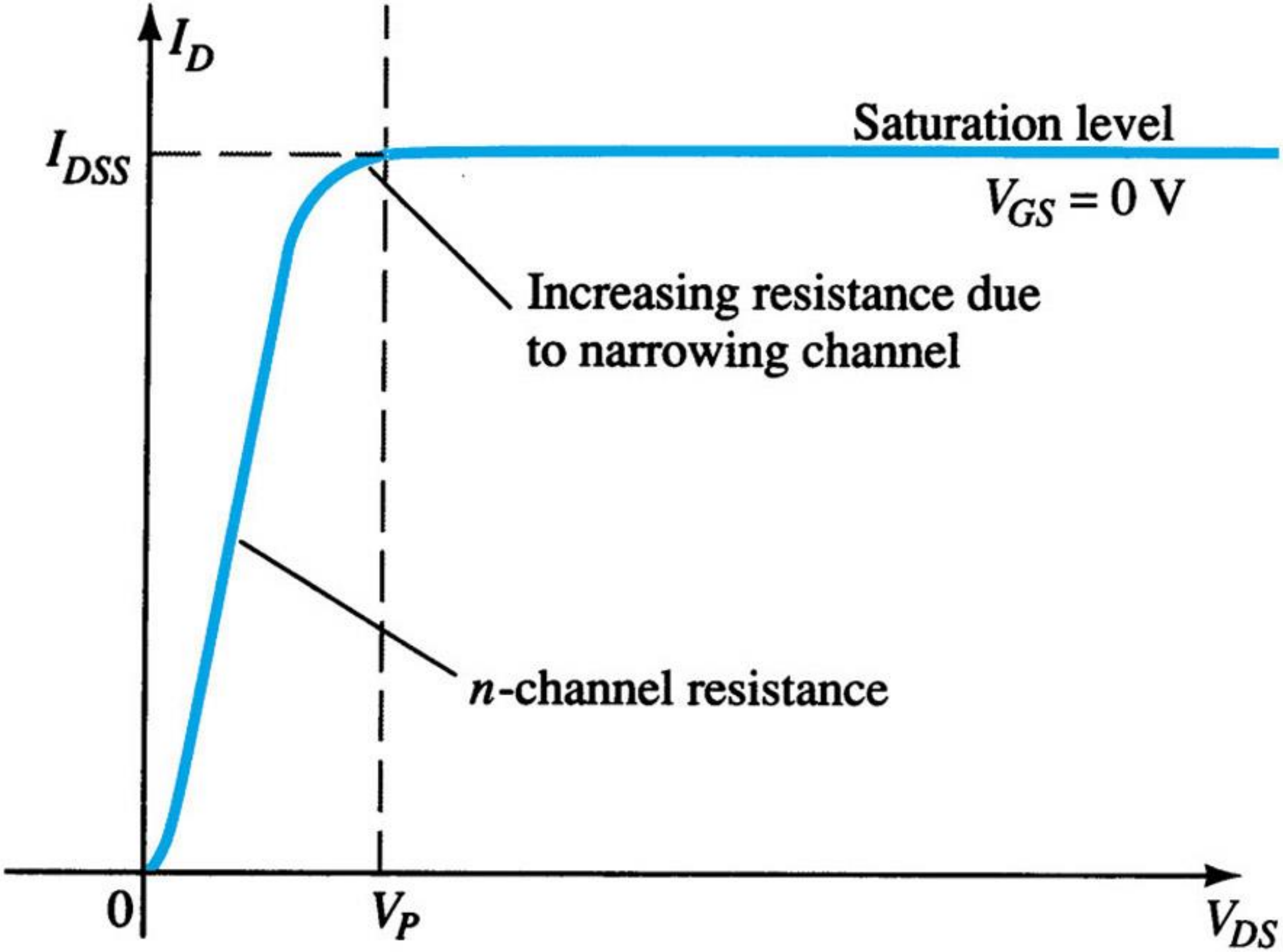
A corrente não cessa!



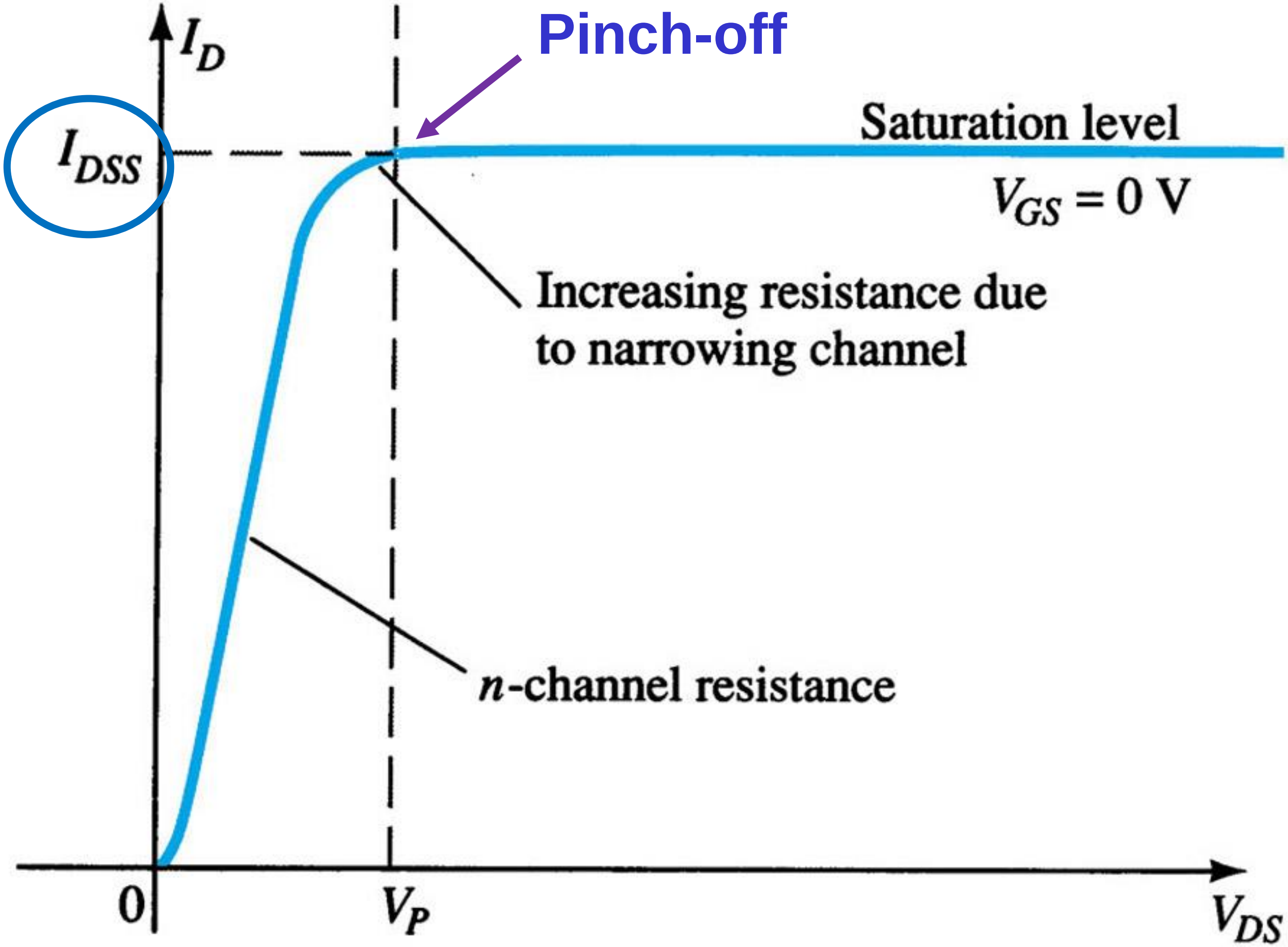
I_D versus V_{DS} com V_{GS} = 0 V



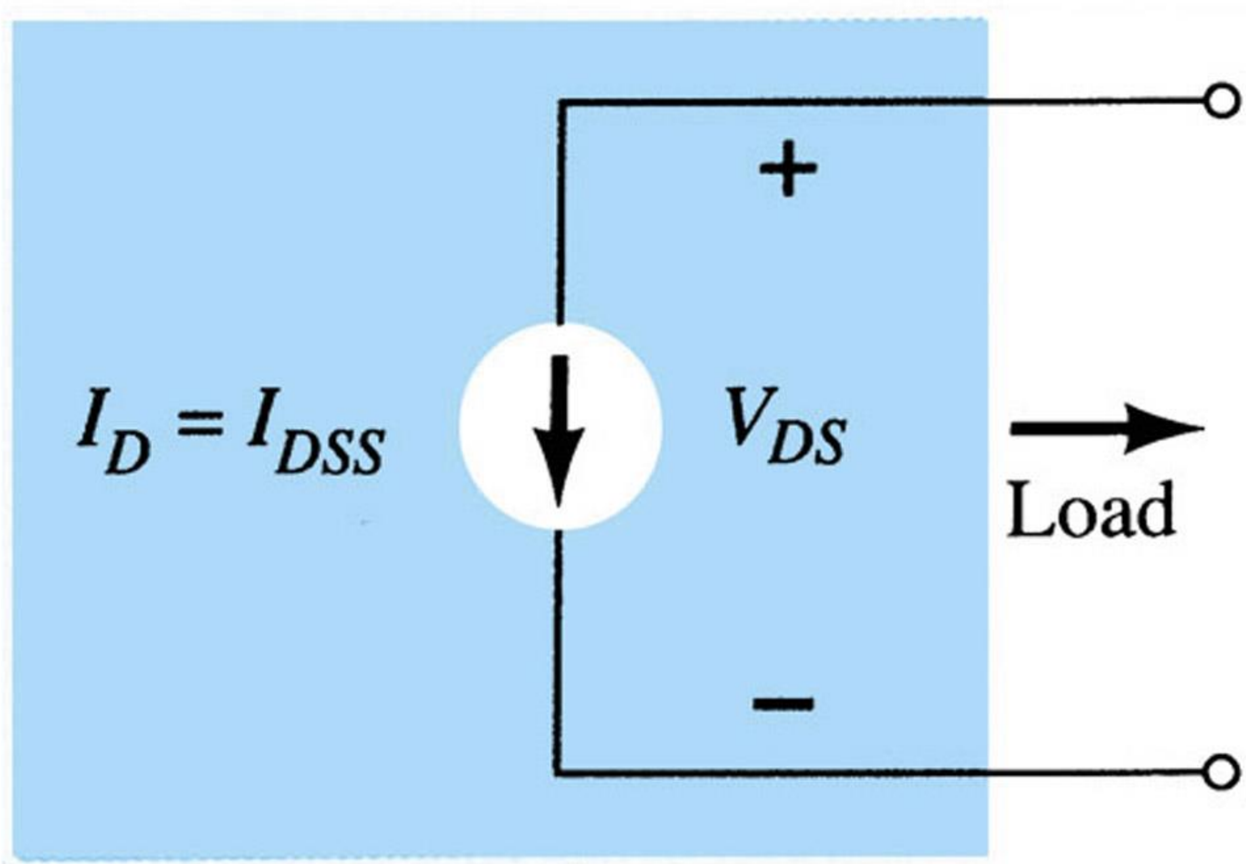
I_D versus V_{DS} com $\boldsymbol{V_{GS}}$ **= 0 V**



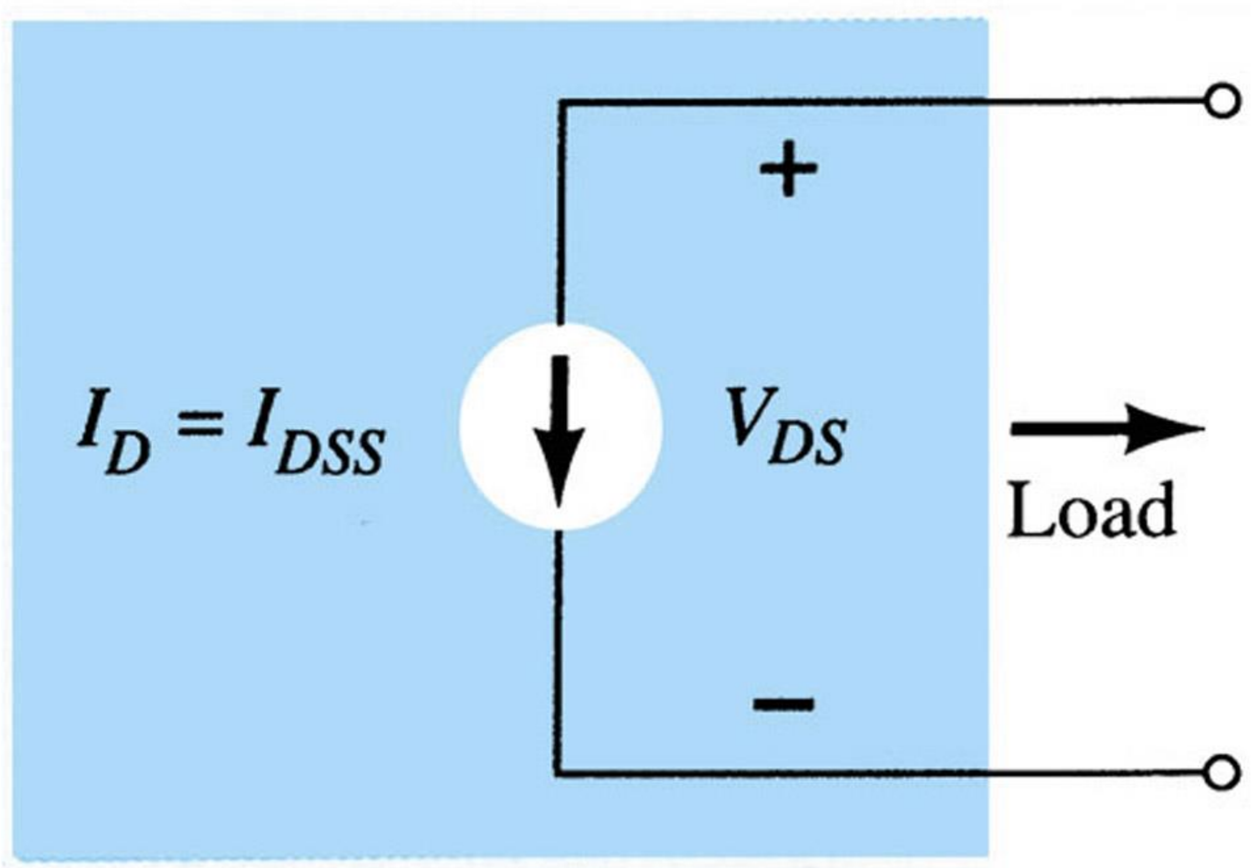
I_D versus V_{DS} com $\boldsymbol{V_{GS}}$ **= 0 V**



Fonte de corrente equivalente V_{GS} = 0 V, $V_{DS} > V_P$



Fonte de corrente equivalente V_{GS} = 0 V, $V_{DS} > V_P$

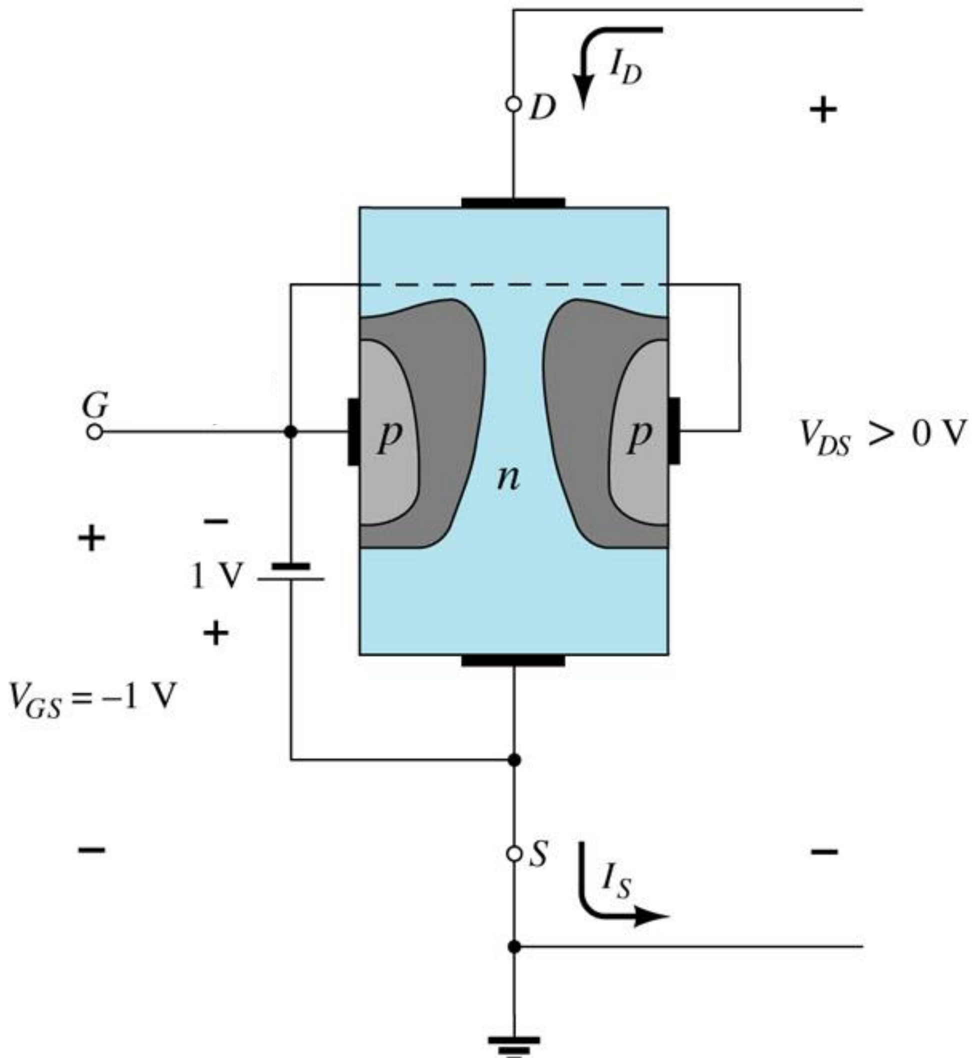


$I_D = I_{DSS} = Cte.$

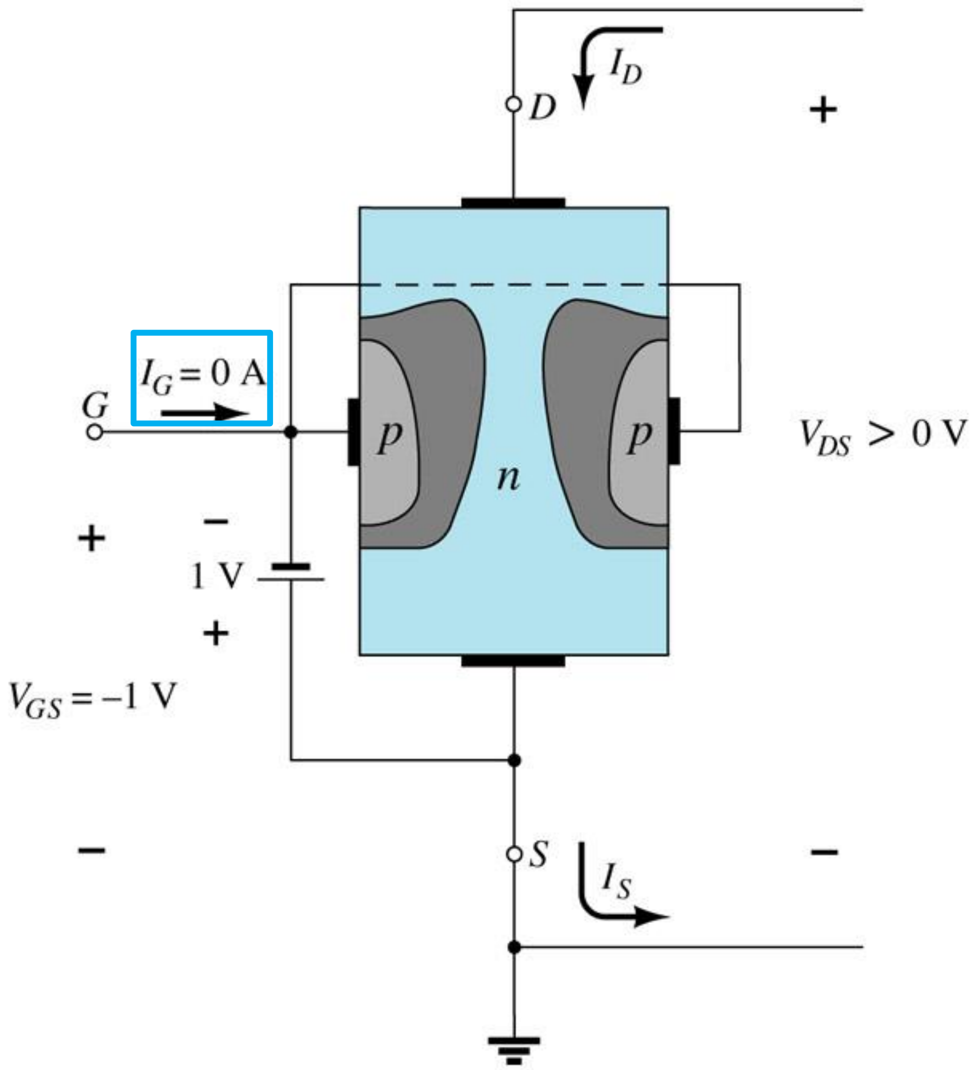
i - Análise com VGS = 0 V and VDS > 0 V

ii - Análise com V_{GS} < 0 V and V_{DS} > 0 V

Aplicando tensão negativa à porta

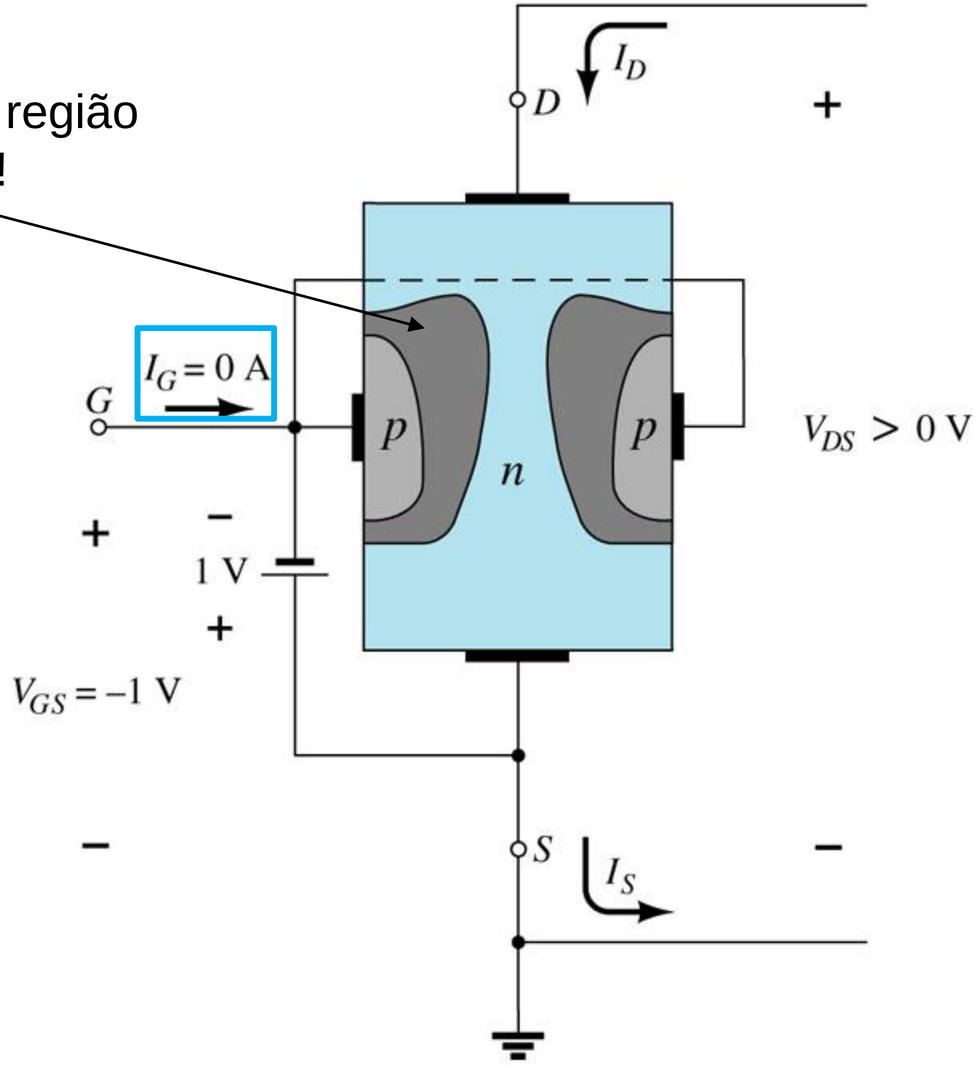


Aplicando tensão negativa à porta

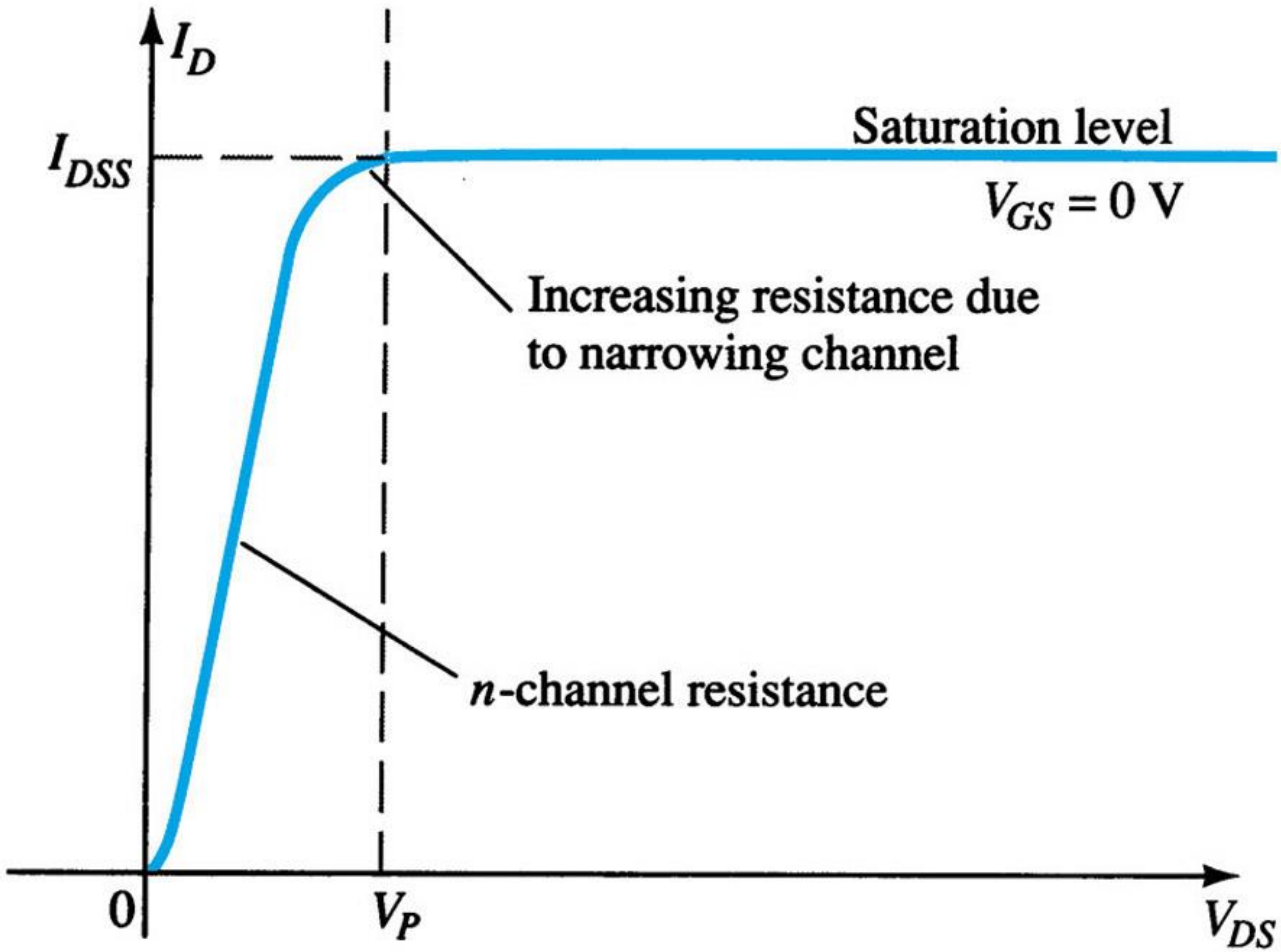


Aplicando tensão negativa à porta

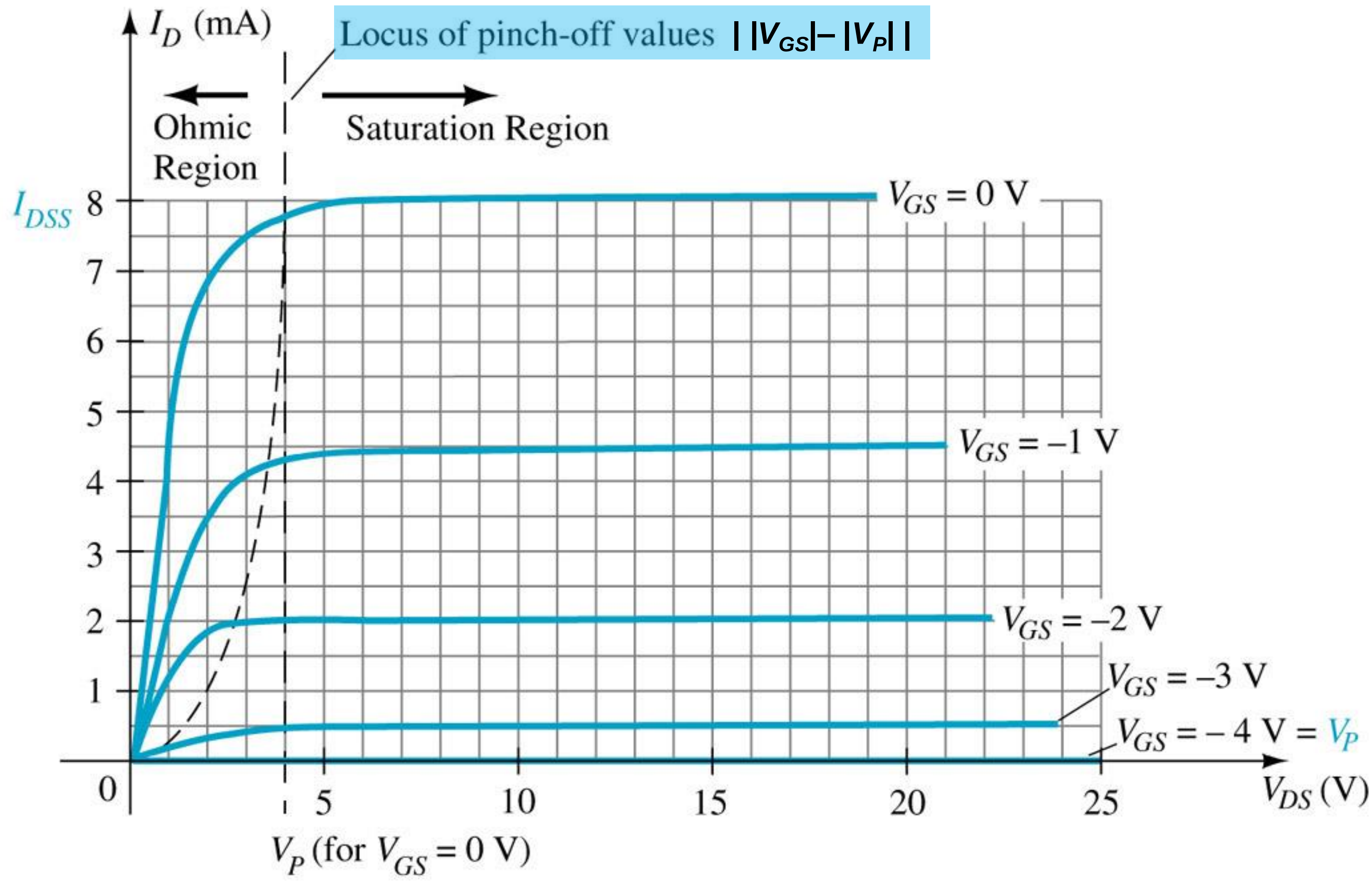
Aumento da região
de depleção!



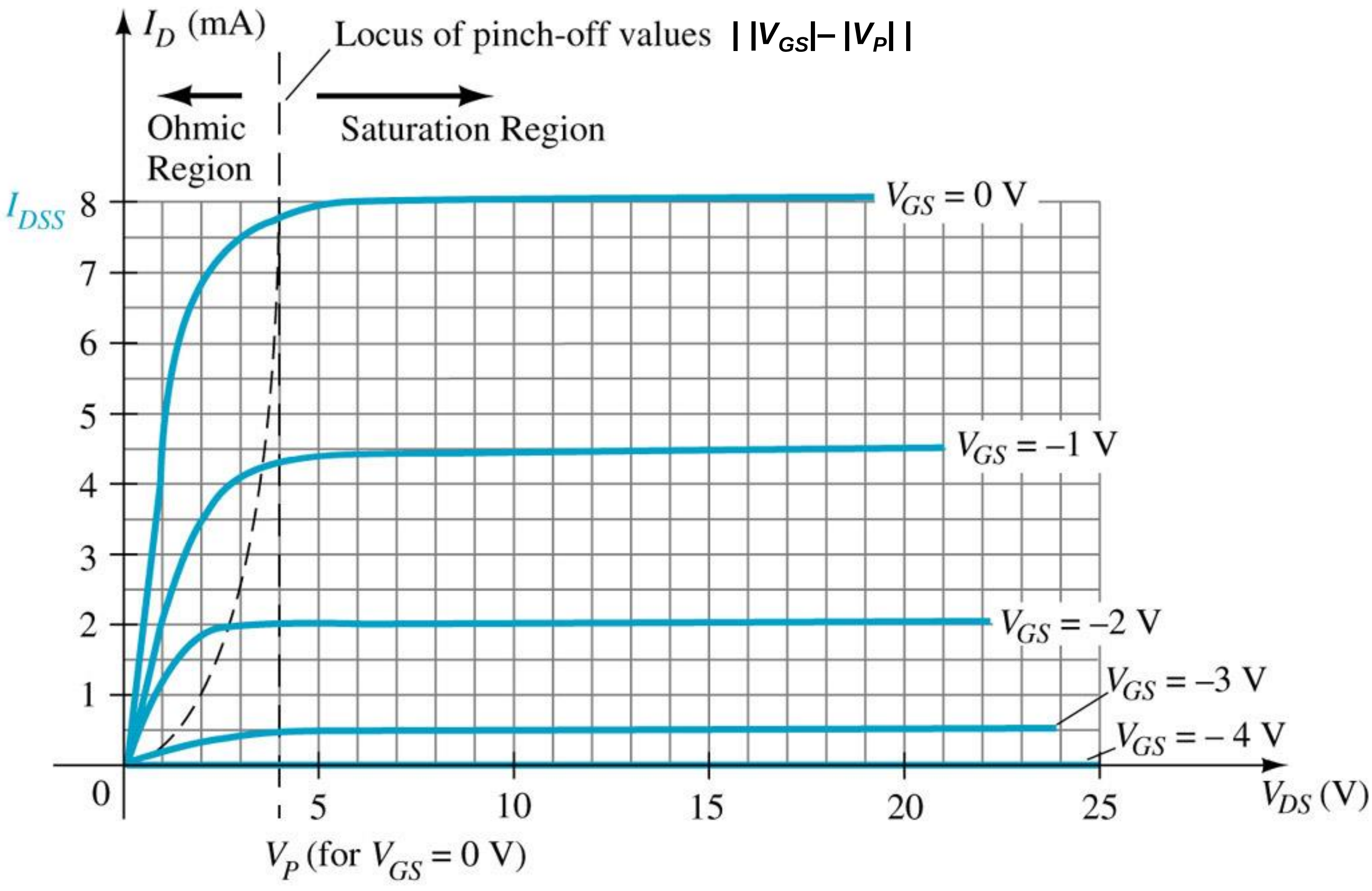
Relembrando: I_D versus V_{DS} com $\boldsymbol{V_{GS}}$ **= 0 V**



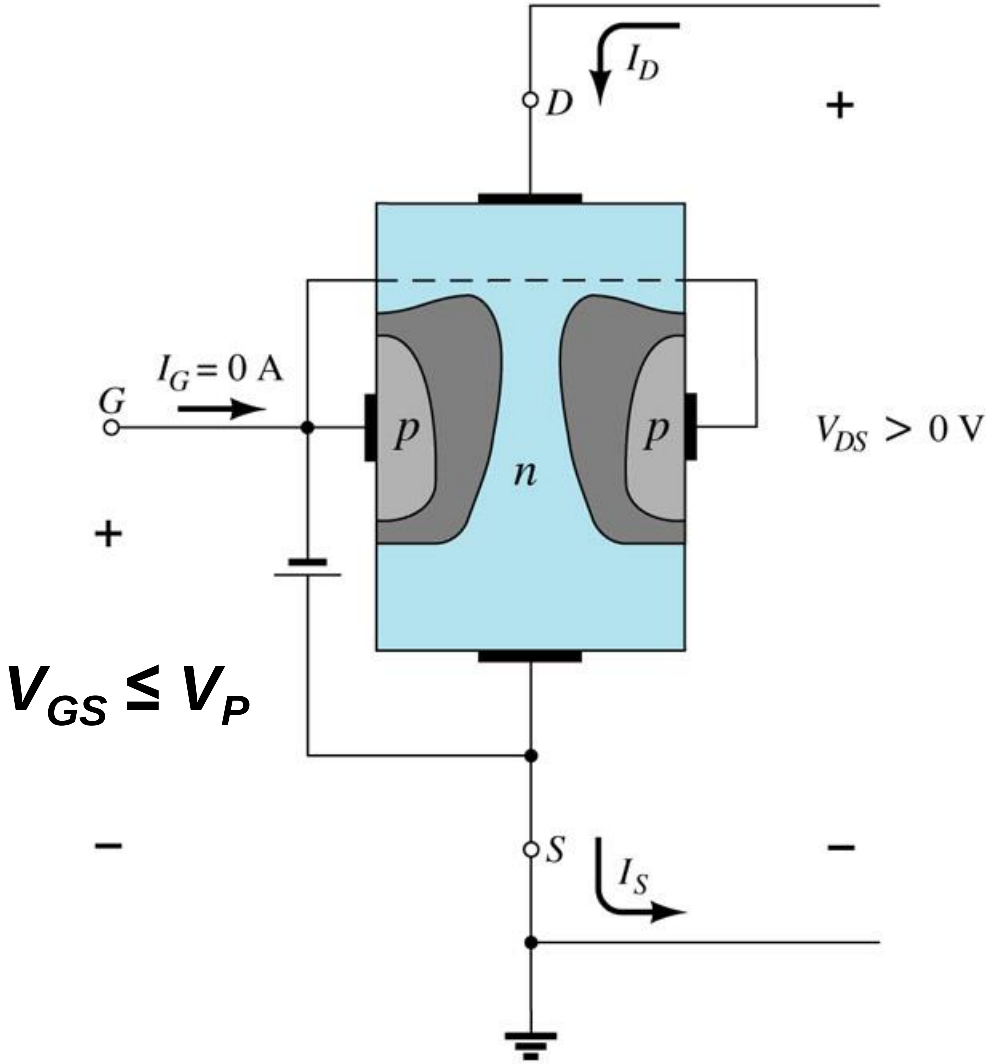
I_D versus V_{DS} com V_{GS} < 0 V



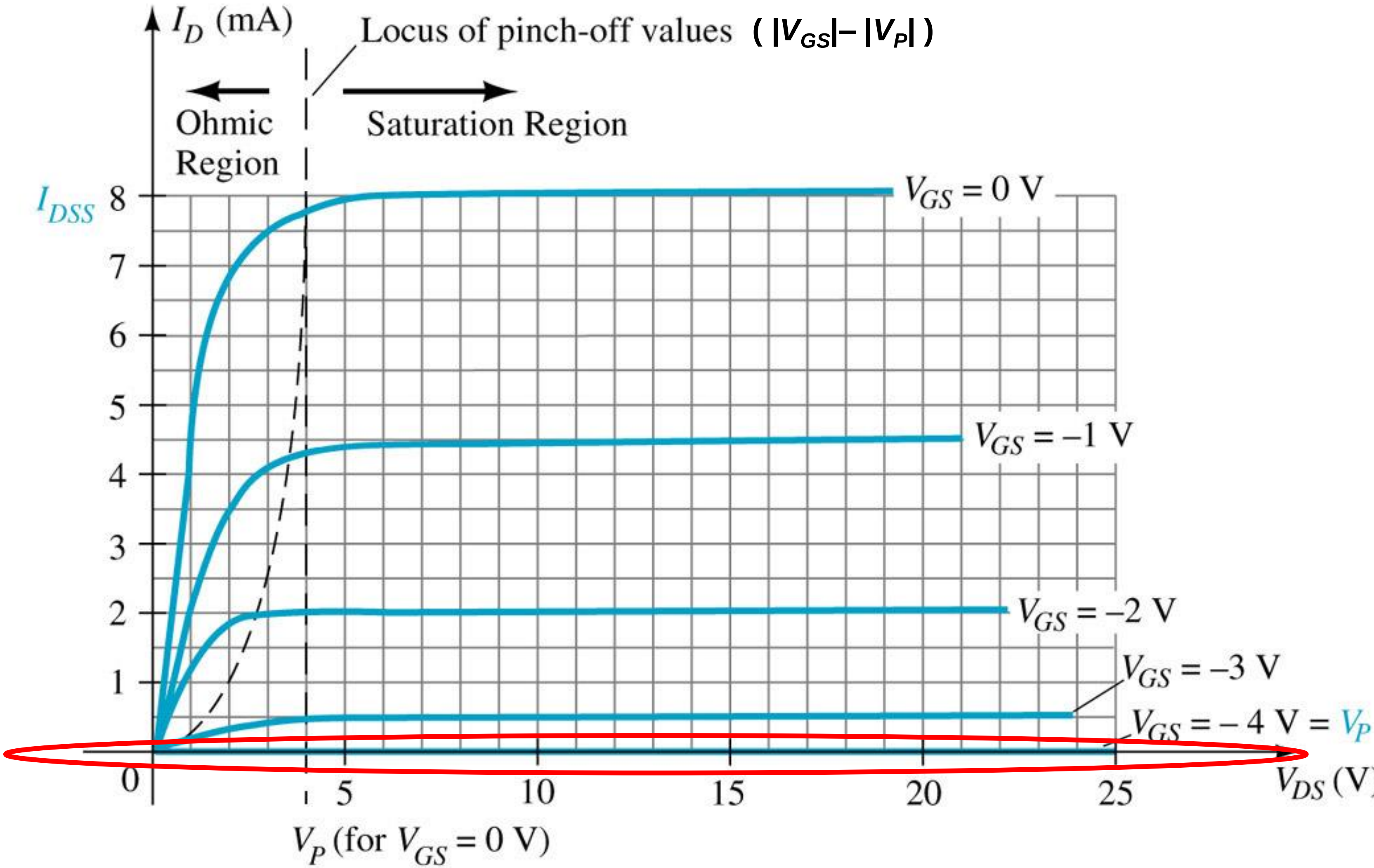
Ex.: FET canal-n com I_{DSS} = 8 mA e V_P = 4 V



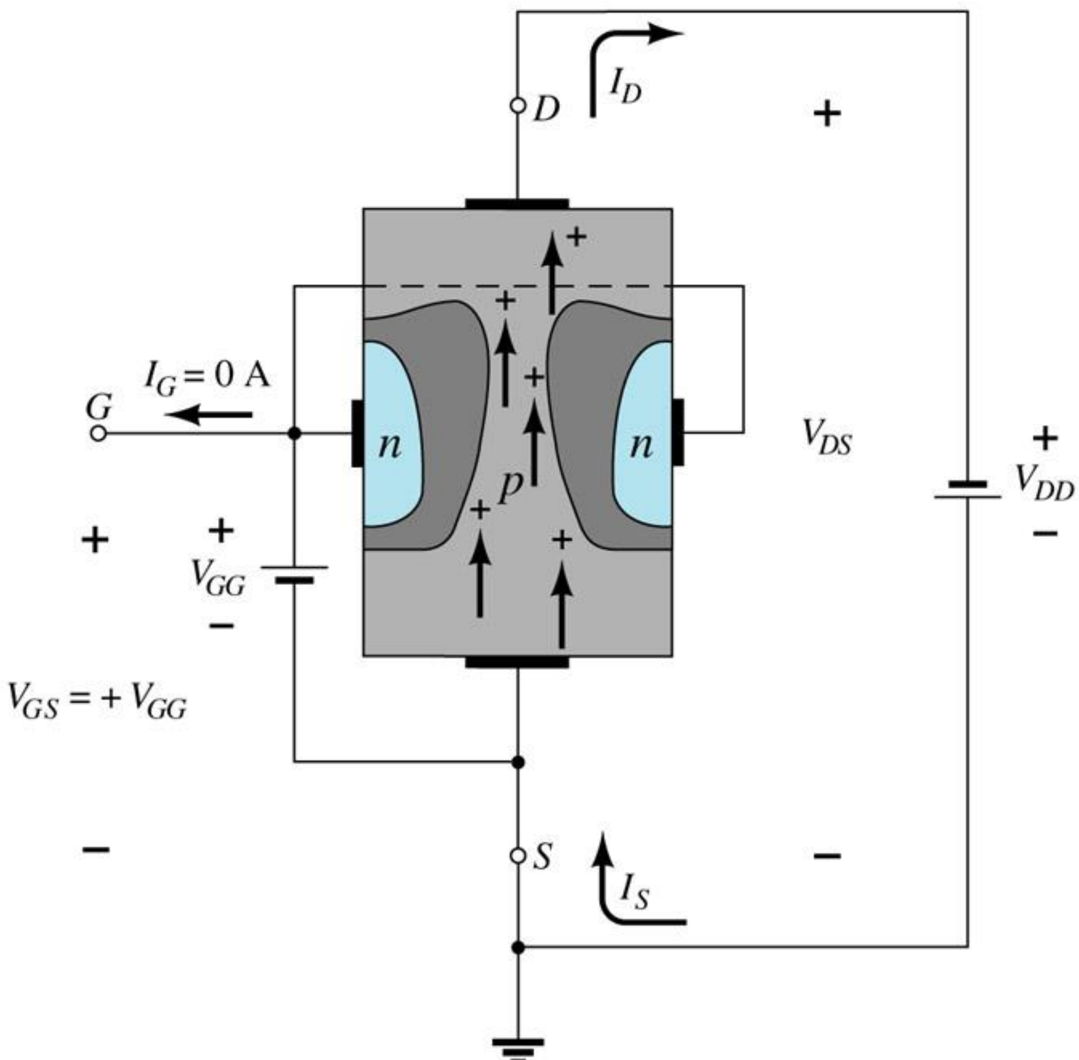
Aplicando tensão $V_{GS} \leq V_P$ à porta



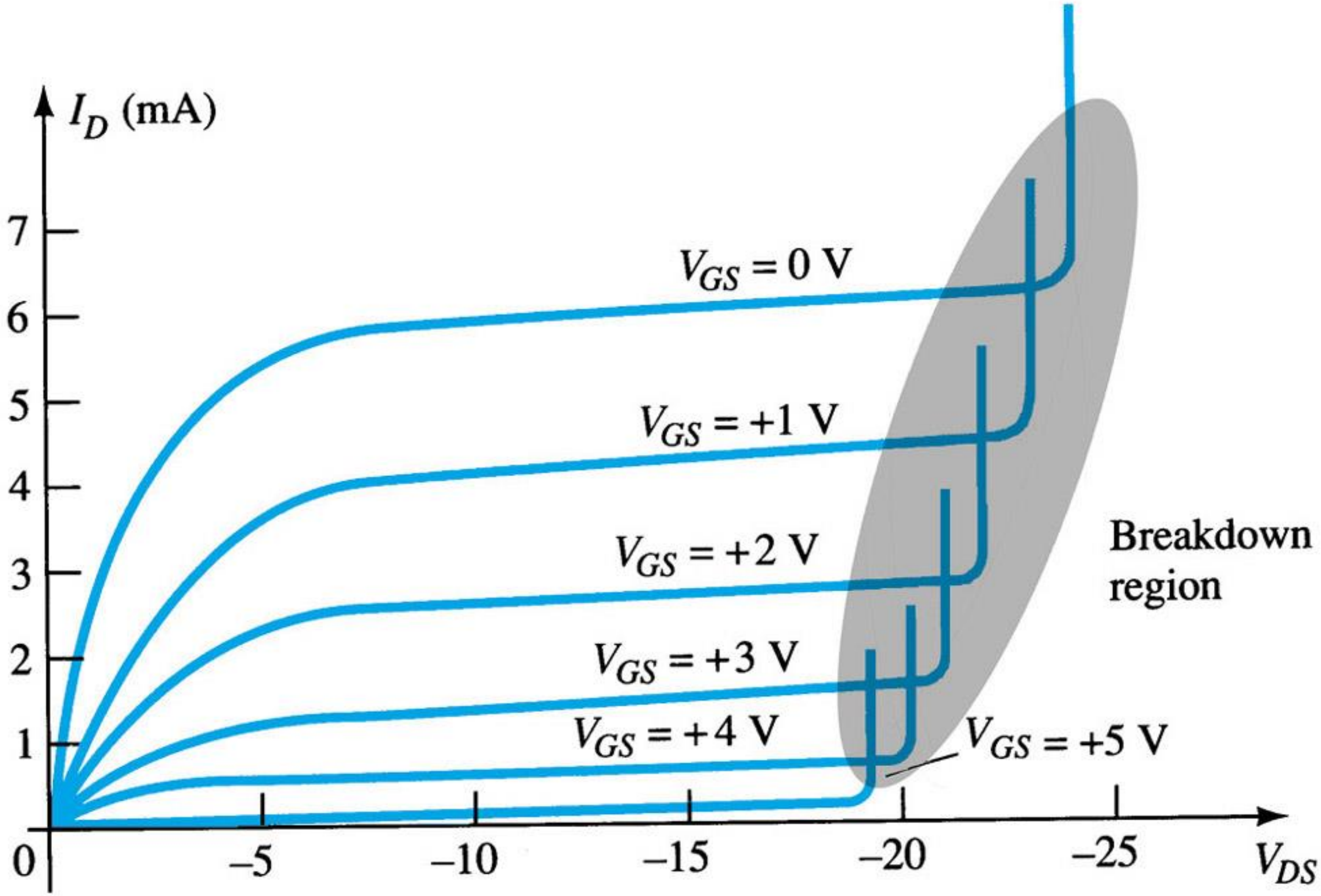
Ex.: FET canal-n com I_{DSS} = 8 mA e V_P = 4 V



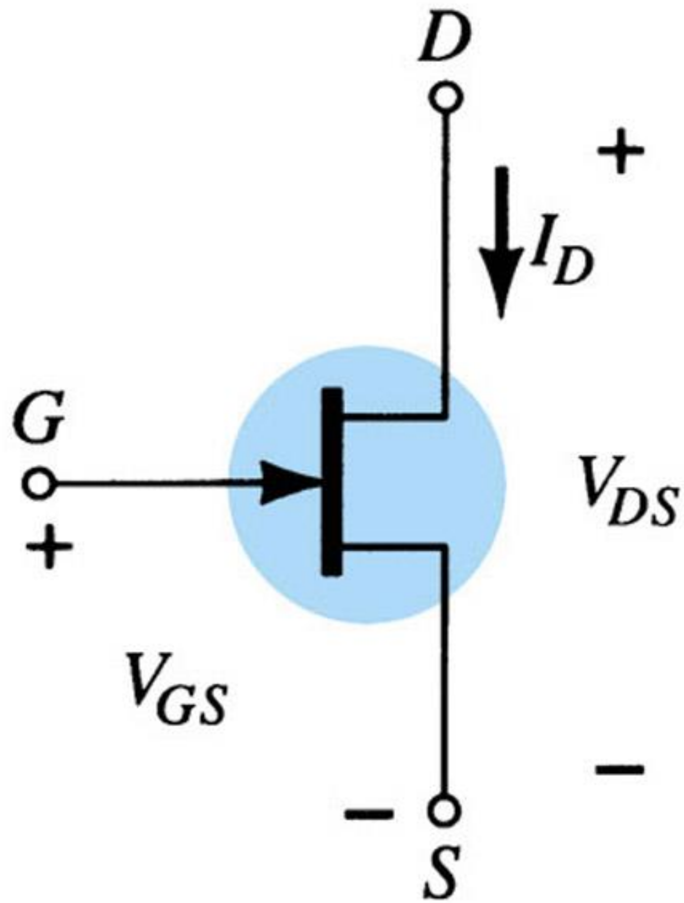
FET canal-p



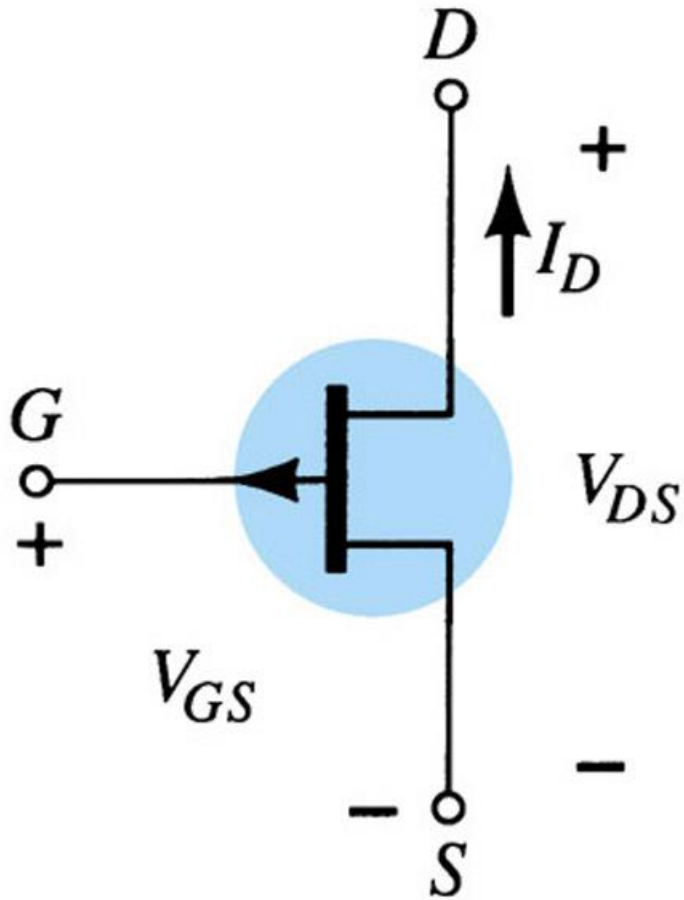
Ex.: FET canal-p com I_{DSS} = 6 mA e V_P = - 6 V



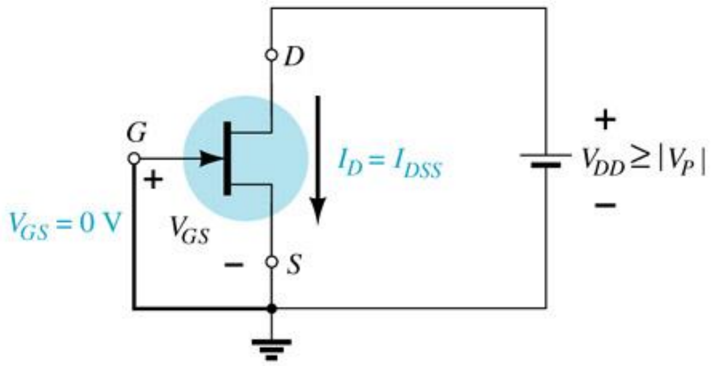
FET símbolos: canal-n

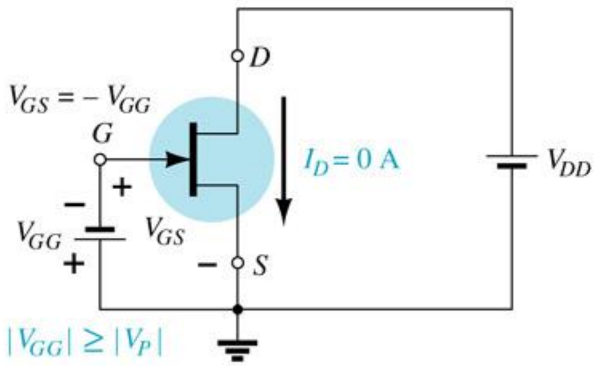


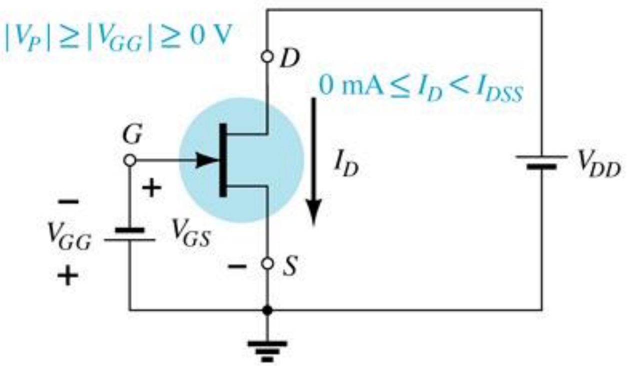
FET símbolos: canal-p



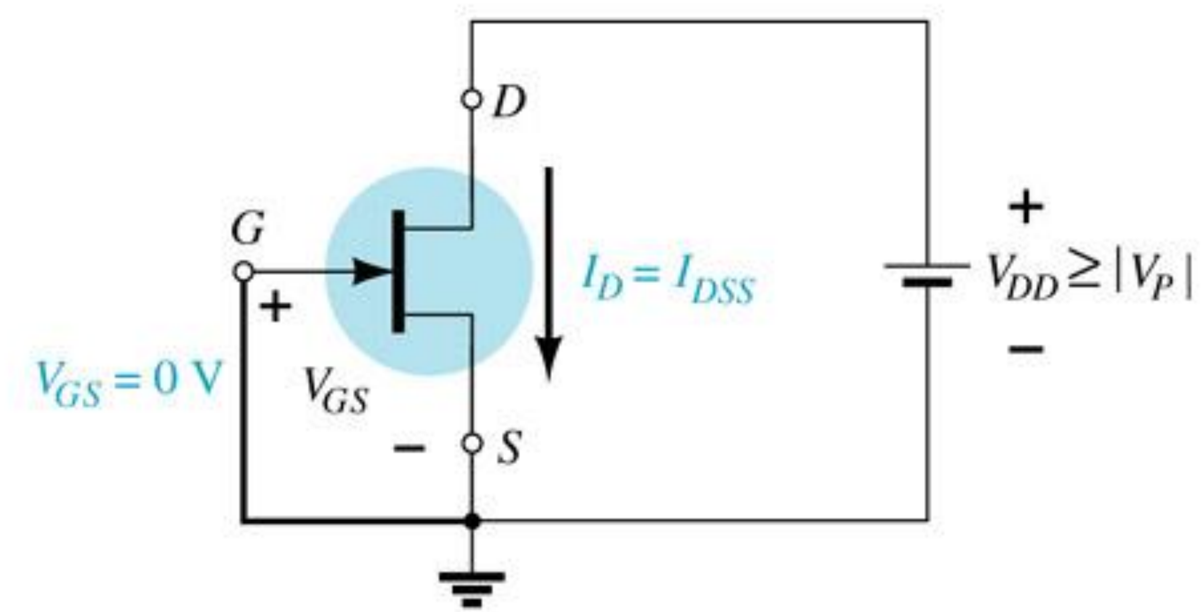
Regiões de Operação





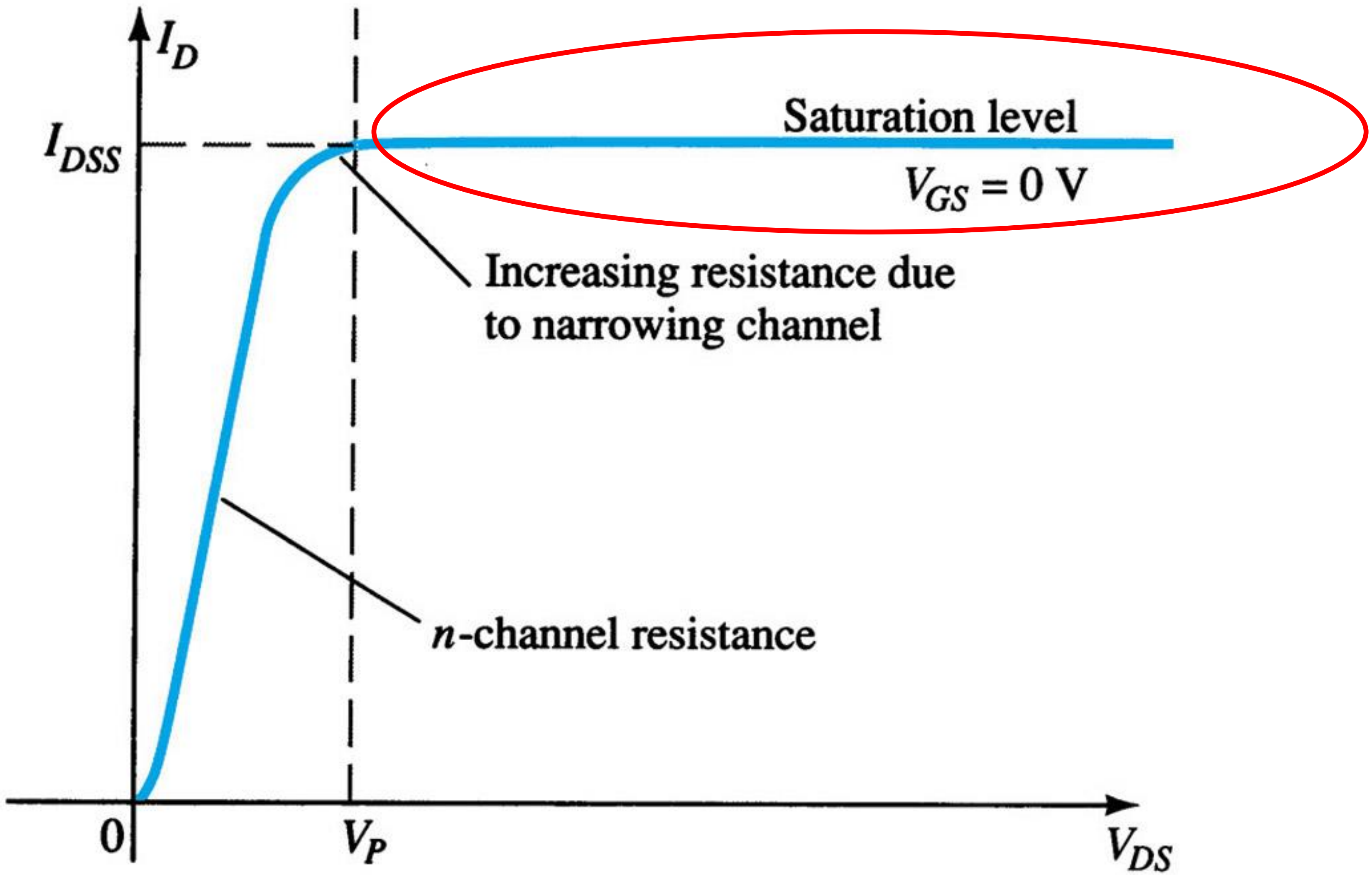


Regiões de Operação

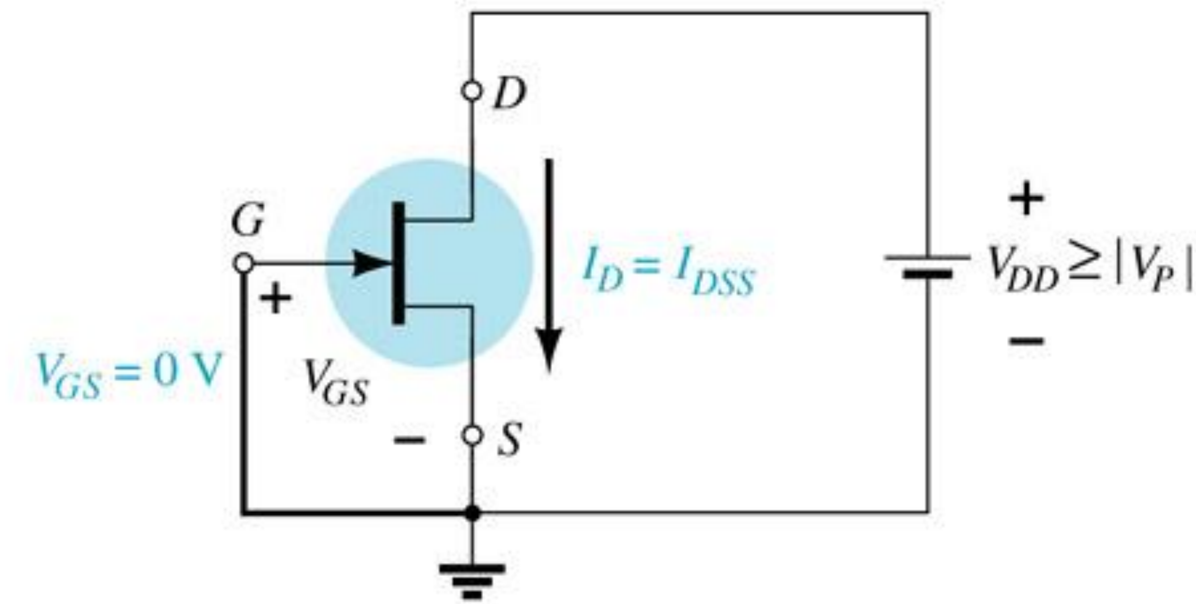


(1.1) Saturação $V_{GS} = 0$ V, $V_{DD} \geq V_P$, $I_D = I_{DSS}$

(1.1) $V_{GS} = 0$ V, $V_{DD} \geq V_P$, $I_D = I_{DSS}$

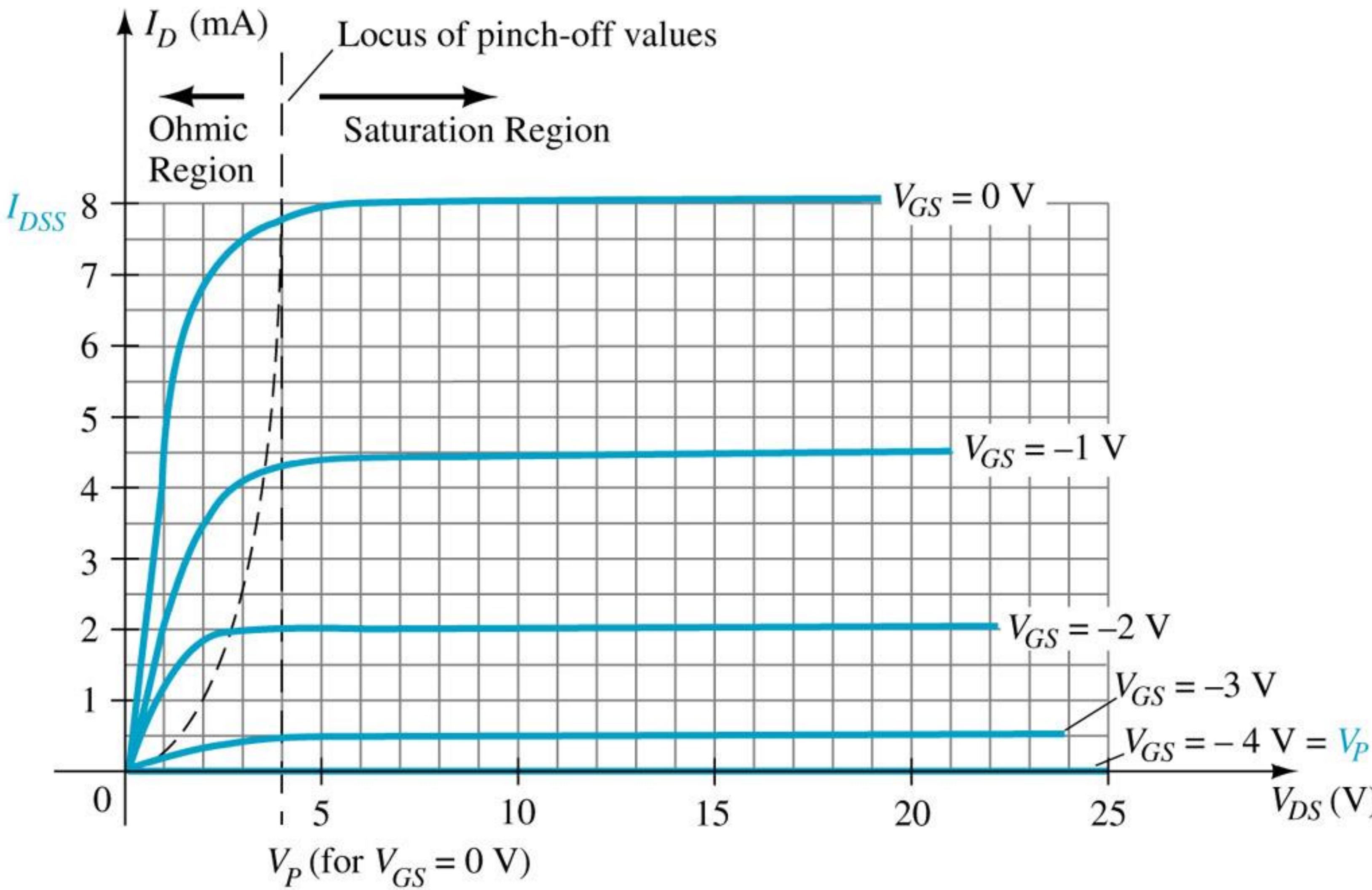


Regiões de Operação

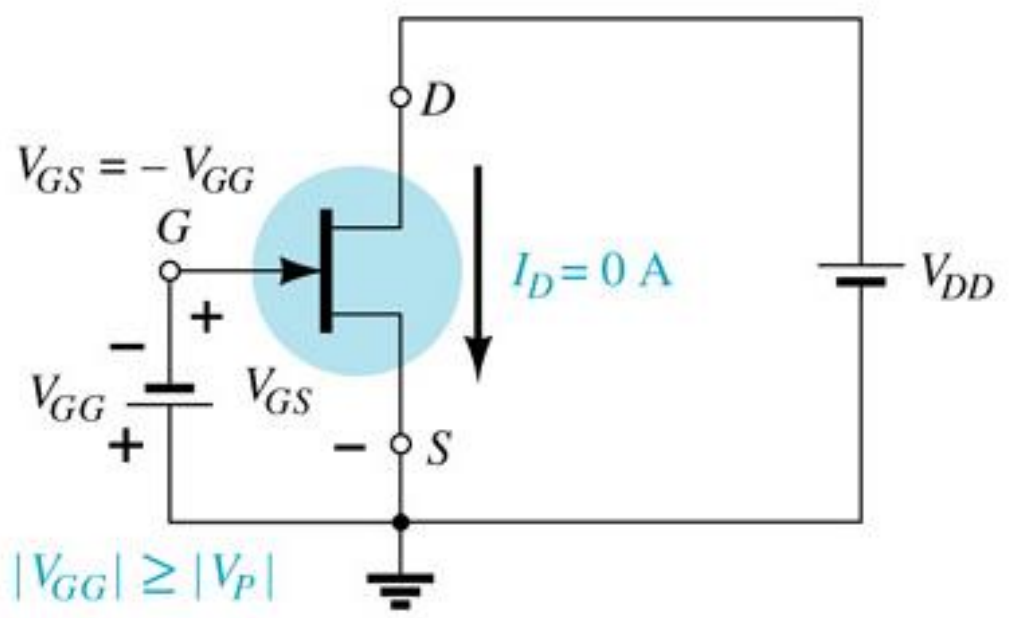


(1.2) Saturação $V_{GS} < 0,\ V_{GS} > V_P,\ V_{DD} \geq |V_P - V_{GS}|,\ I_D < I_{DSS}$

(1.2) Saturação $V_{GS} < 0,\ V_{GS} > V_P,\ V_{DD} \geq |V_P - V_{GS}|,\ I_D < I_{DSS}$

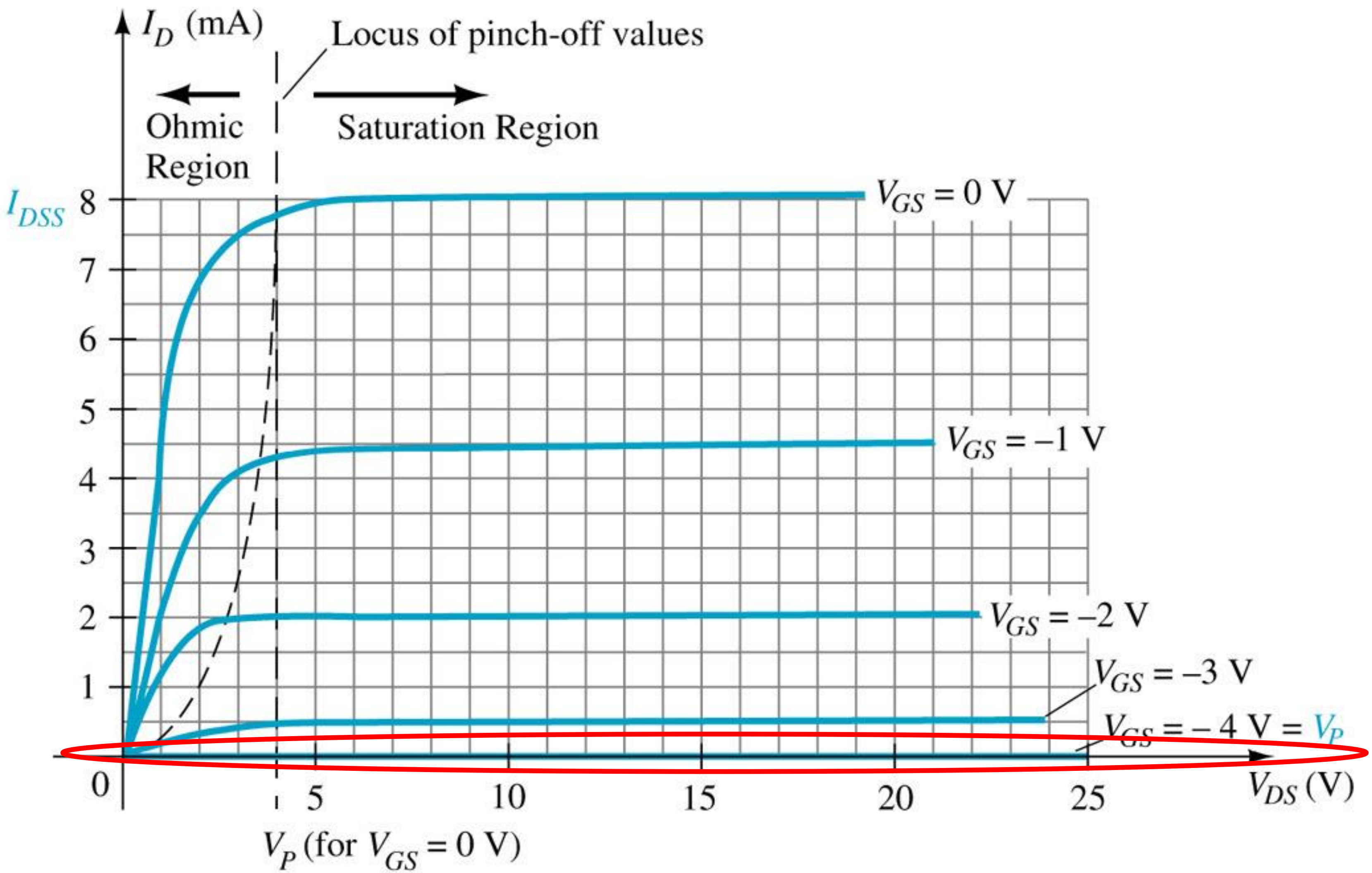


Regiões de Operação

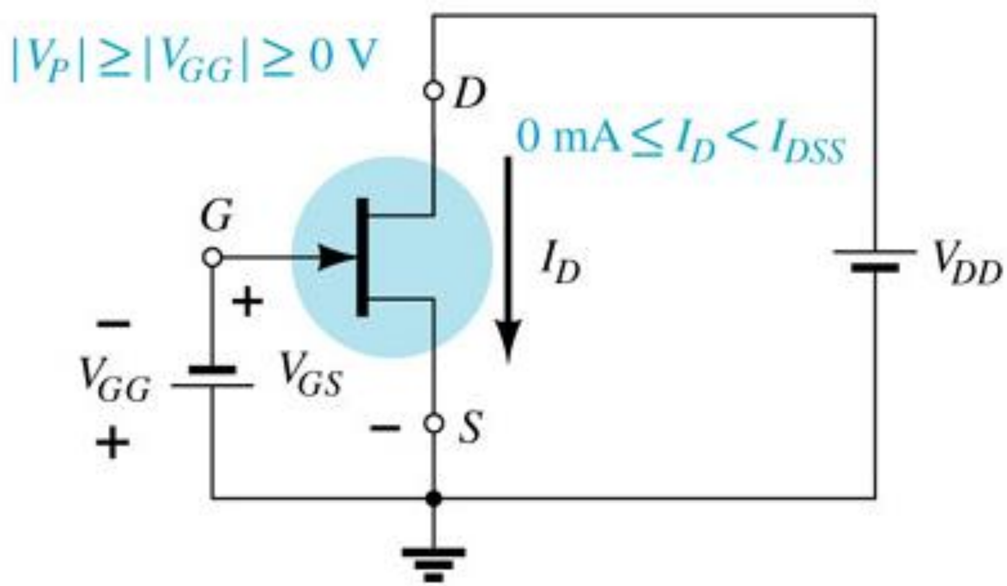


(2) Corte ($I_D = 0$ A) $|V_{GS}| \geq |V_P|$, $V_{GS} < 0$

(2) Corte ($I_D = 0$ A) $|V_{GS}| \geq |V_P|$

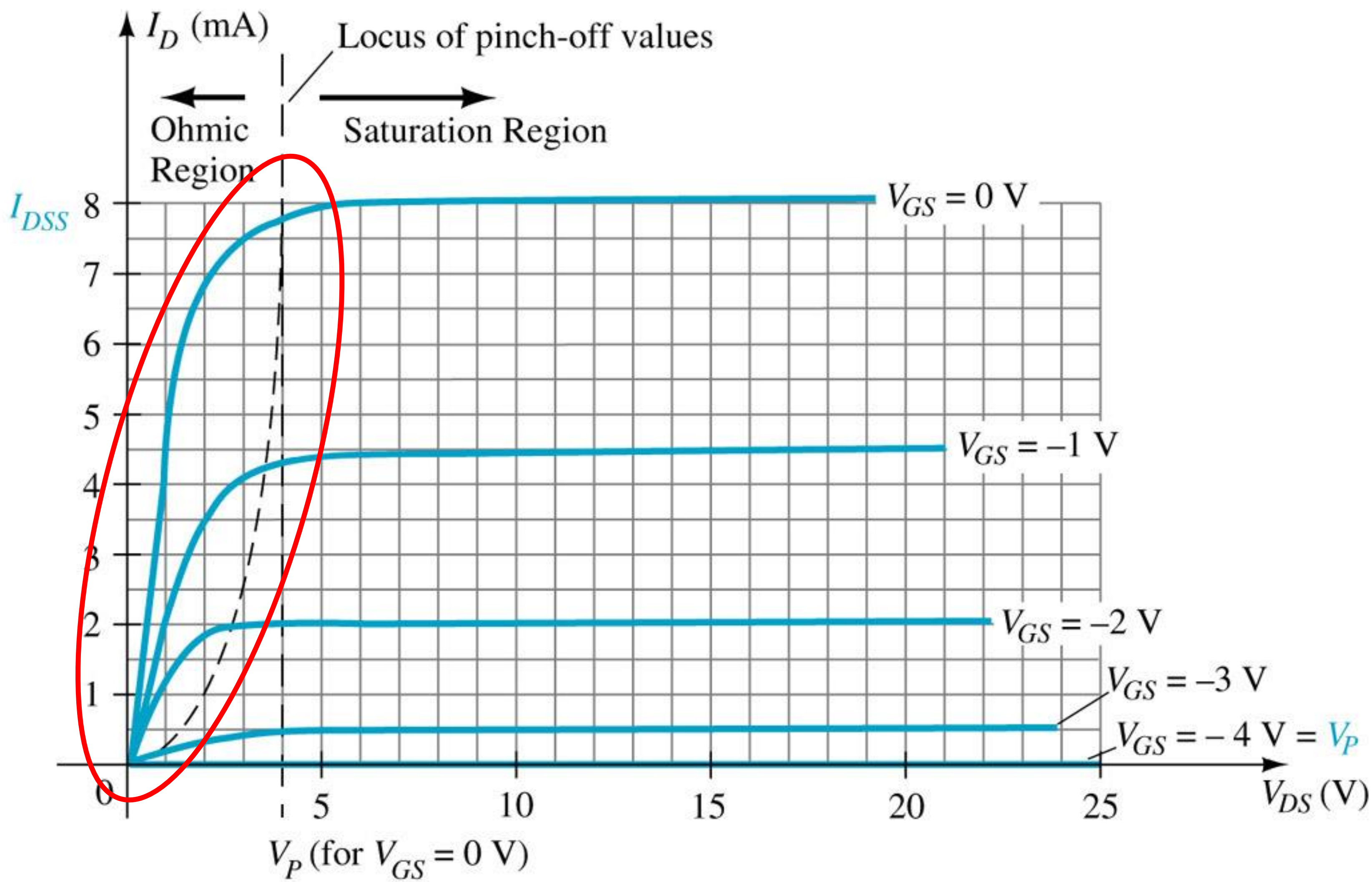


Regiões de Operação

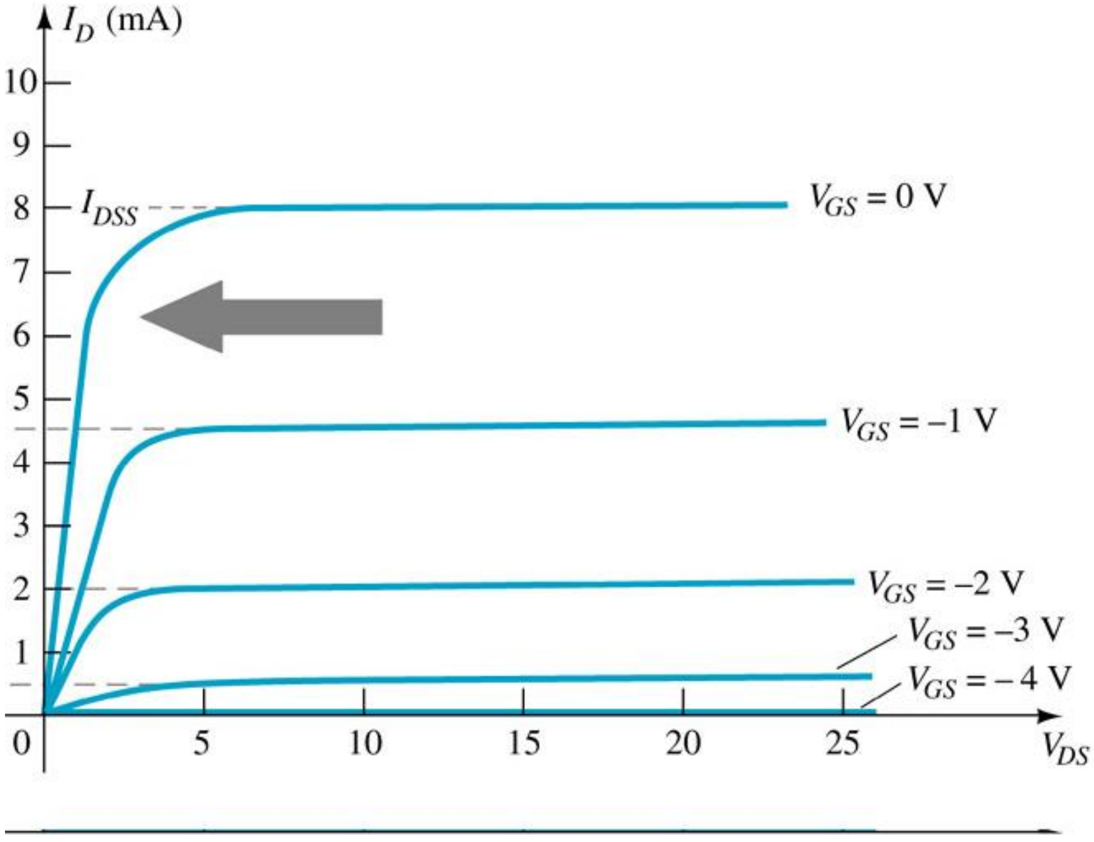


(3) I_D entre 0 e I_{DSS} para $V_{GS} \leq 0$ V, $V_{DS} < |V_{GS} - V_P|$
e $V_{GS} > V_P$.

(3) I_D entre 0 A e I_{DSS} para $V_{GS} \leq 0$ V, $V_{DS} < V_P$ e $|V_{GS}| < |V_P|$.



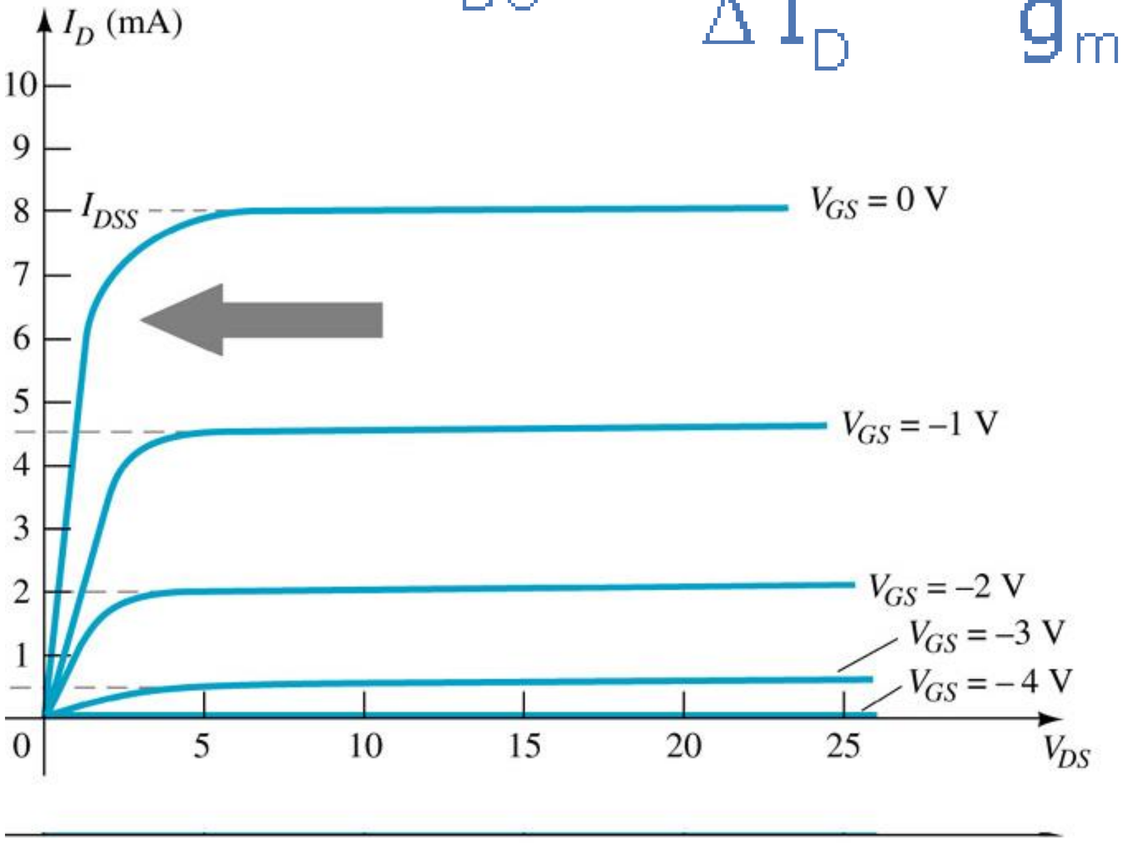
Curva Característica



Curva Característica – Resistência do canal

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Região Ôhmica

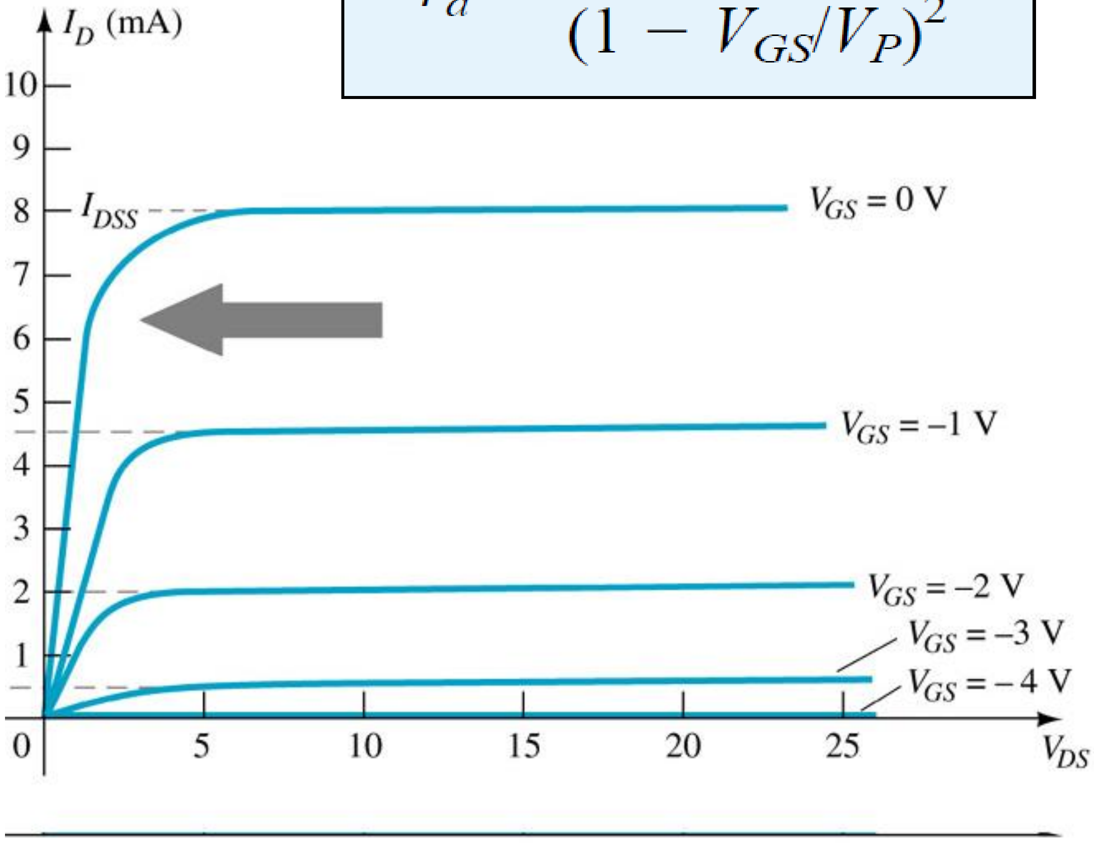


Curva Característica – Resistência do canal

Aproximação:

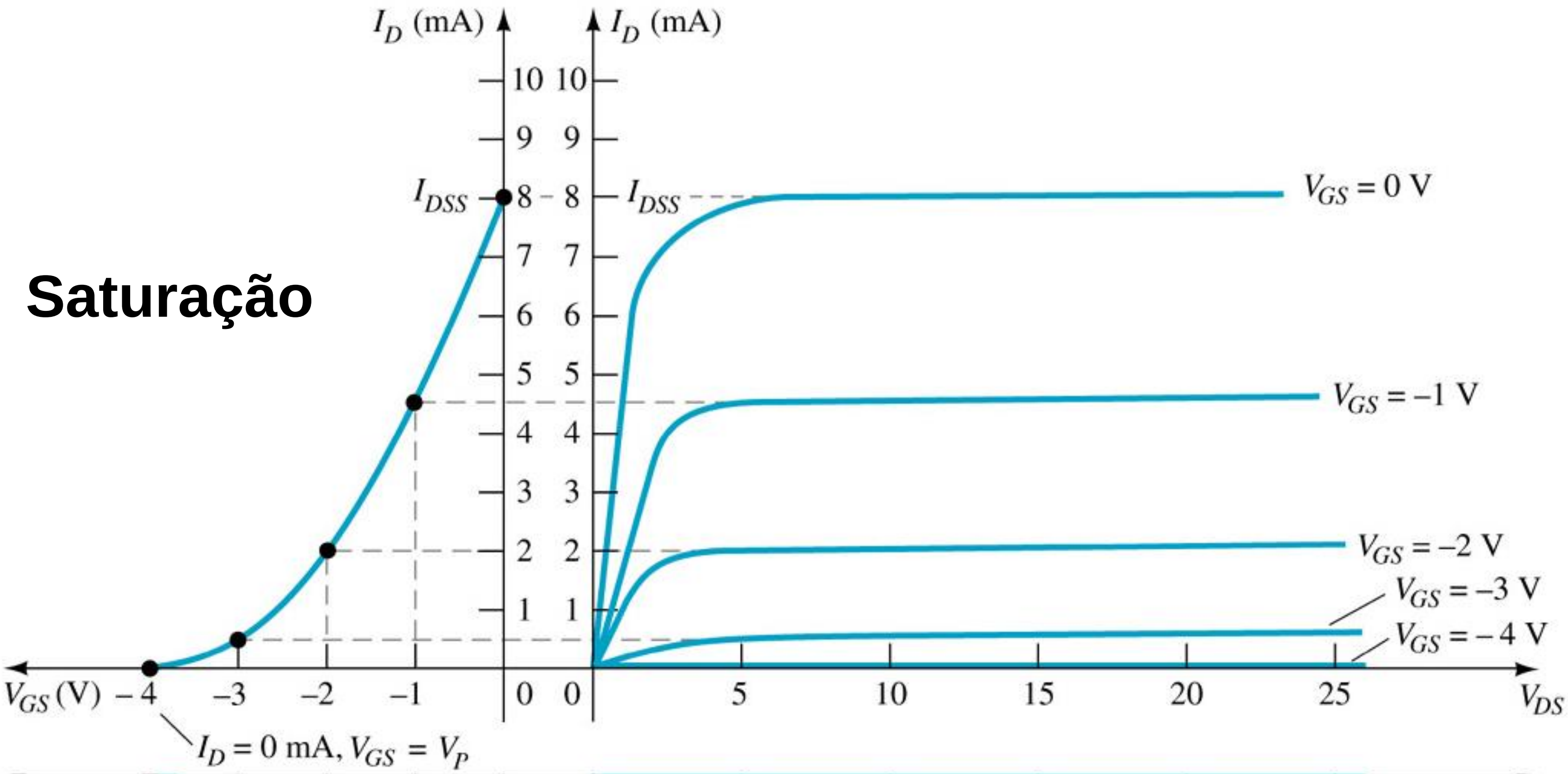
$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

Região Ôhmica



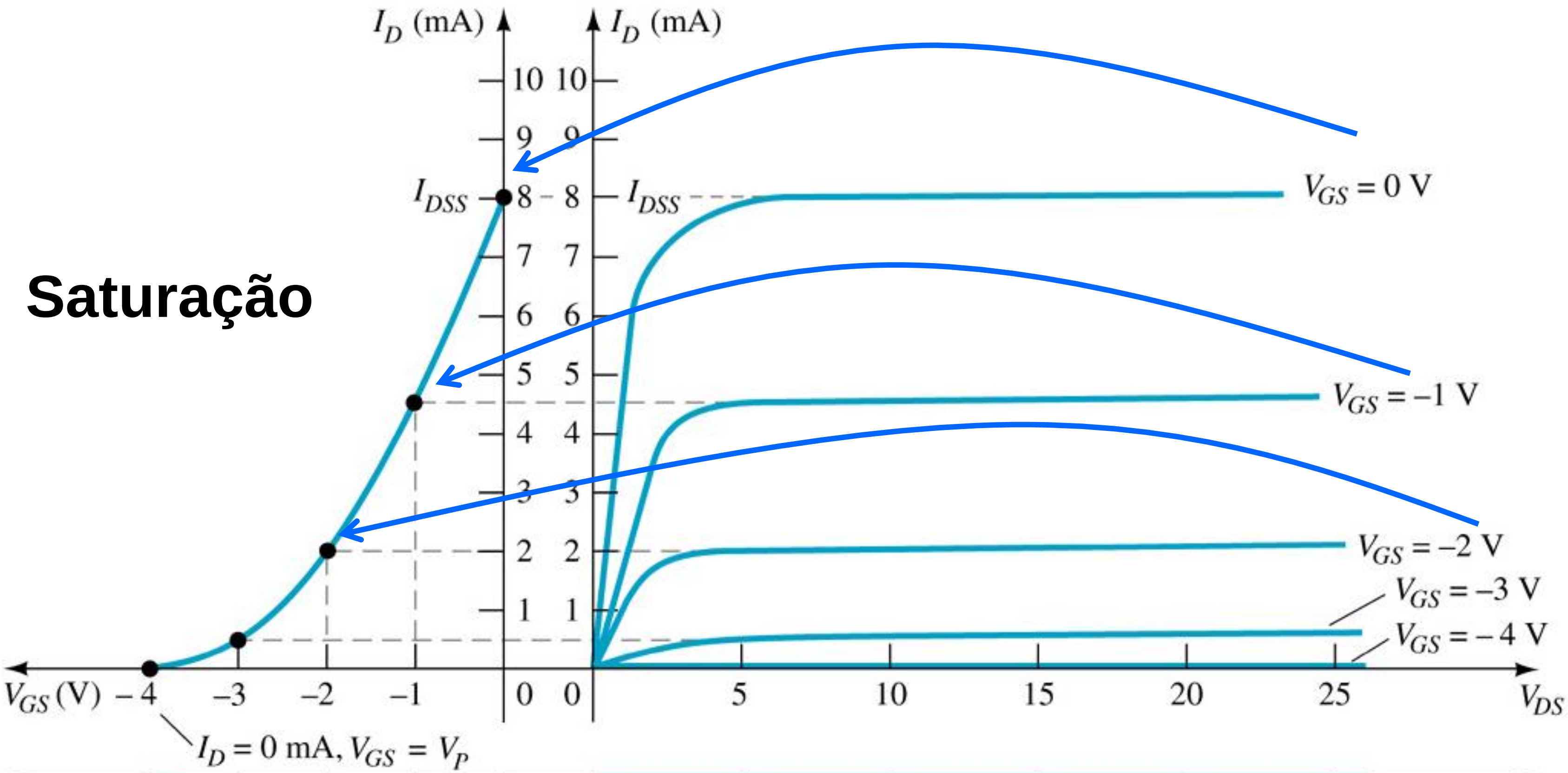
Curva Característica - Curva de Transferência

Saturação



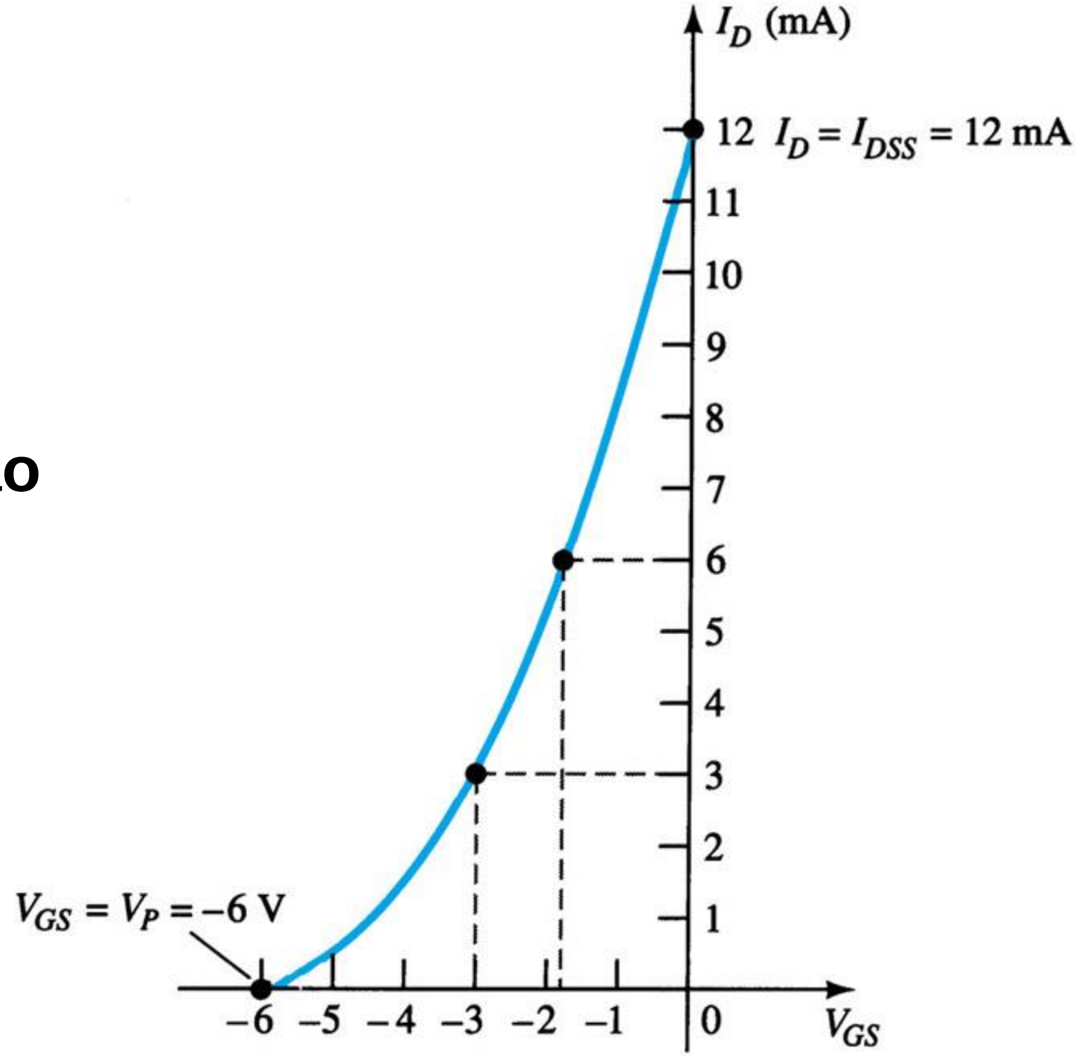
Curva Característica - Curva de Transferência

Saturação



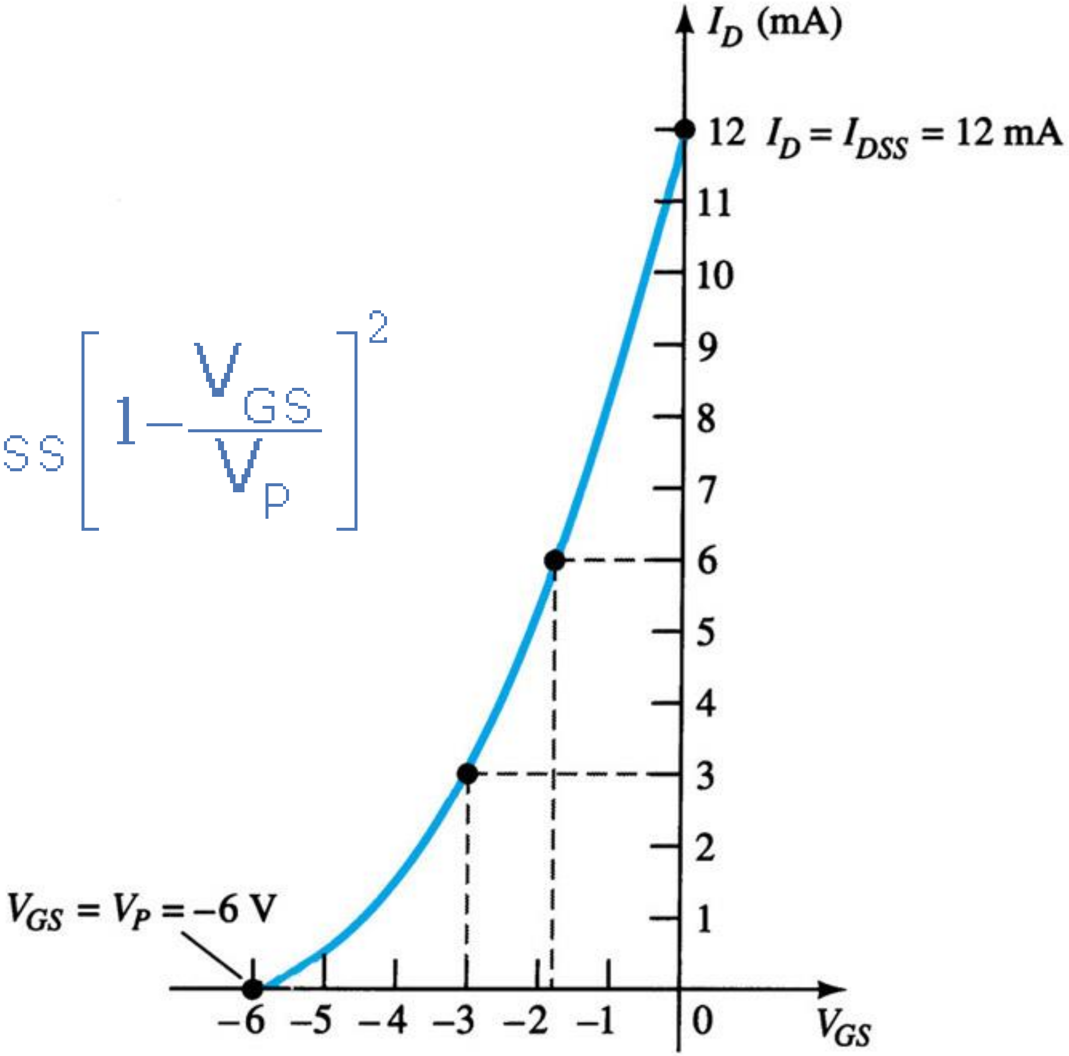
Curva de Transferência – I_D x V_{DS}

Saturação



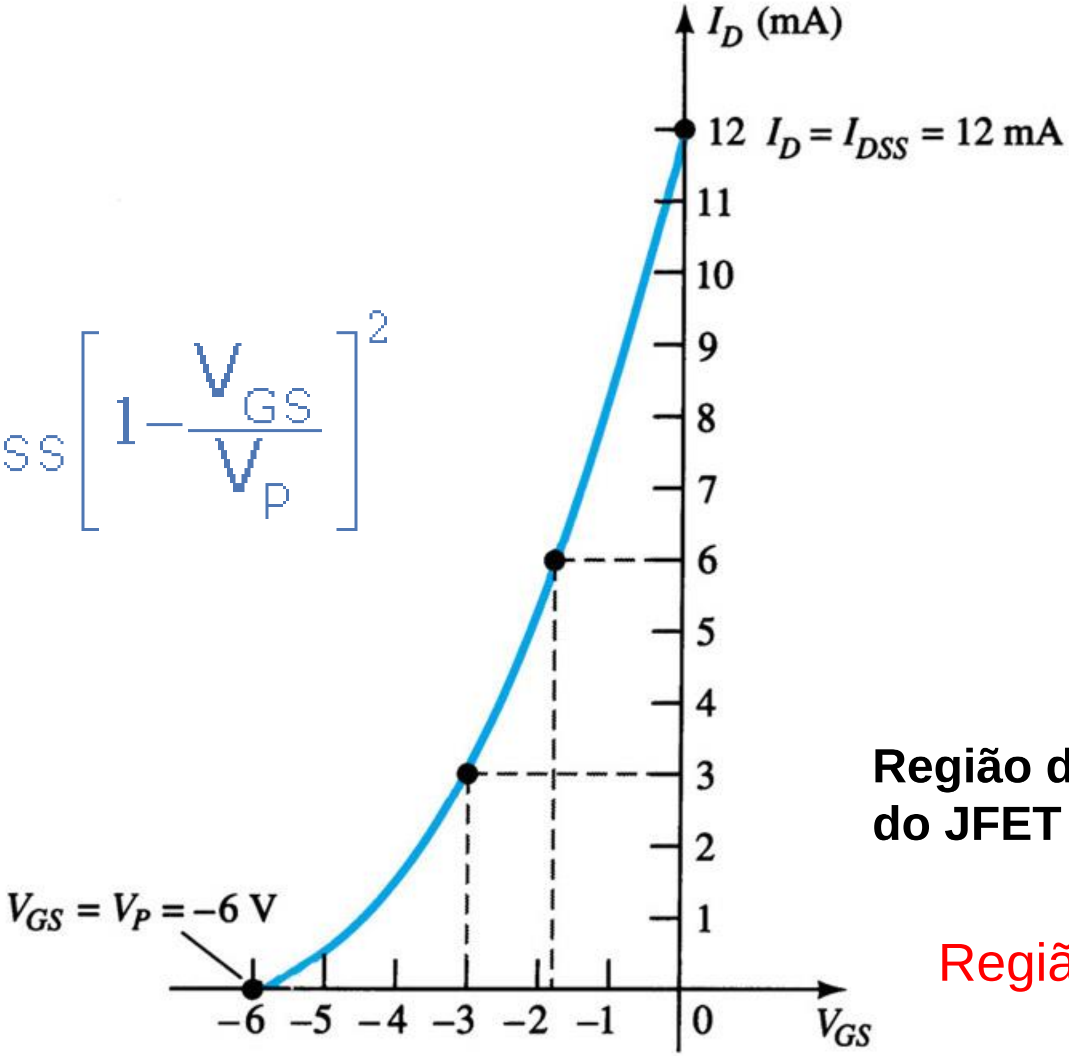
Equação de Schockley

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$



Região de Saturação

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

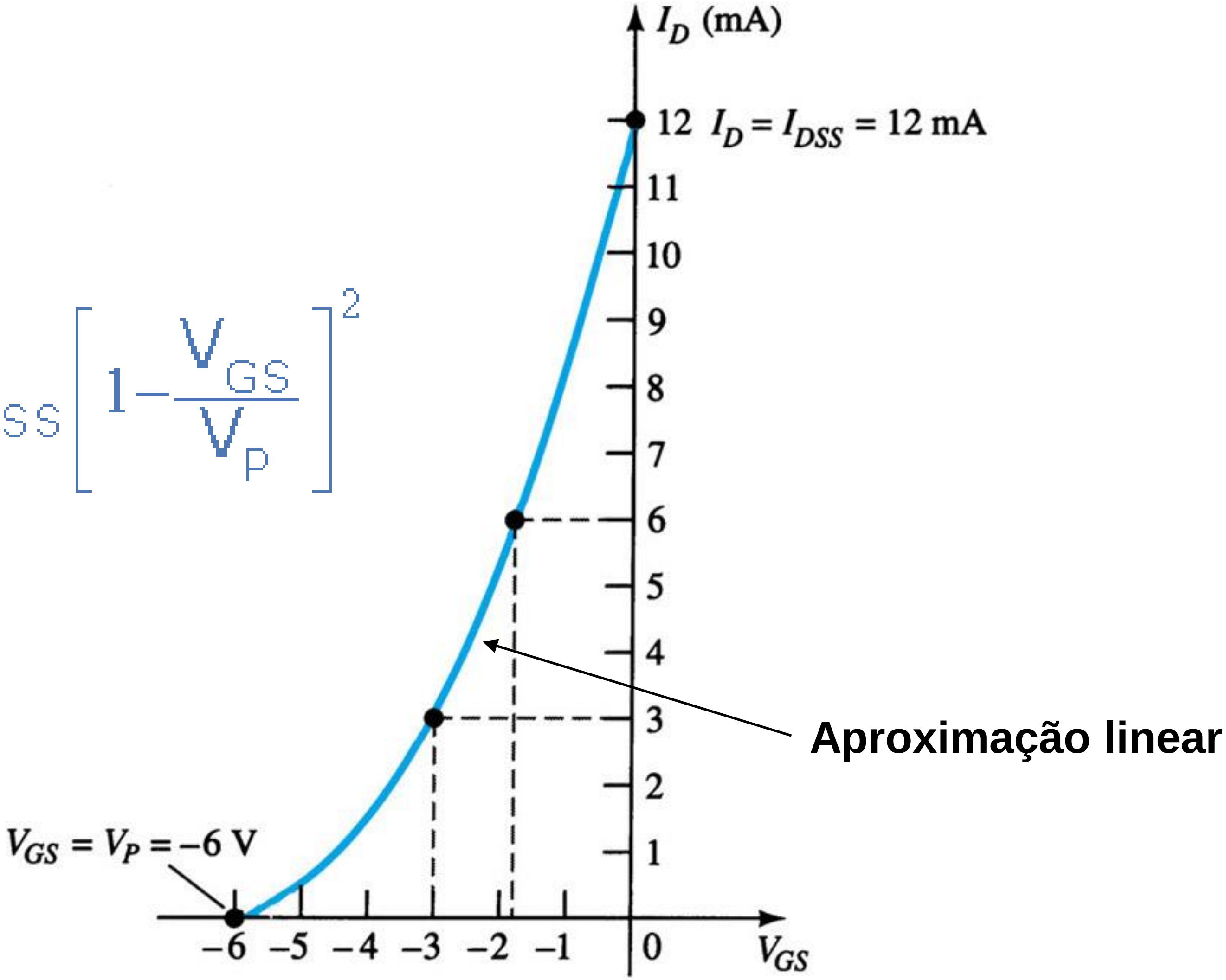


Região de amplificação do JFET

Região de Saturação

Região de Saturação

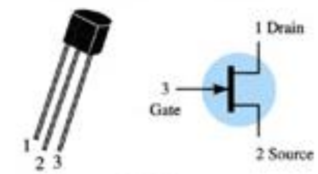
$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$



Folha de Dados

2N5457

CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL—DEPLETION

Refer to 2N4220 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

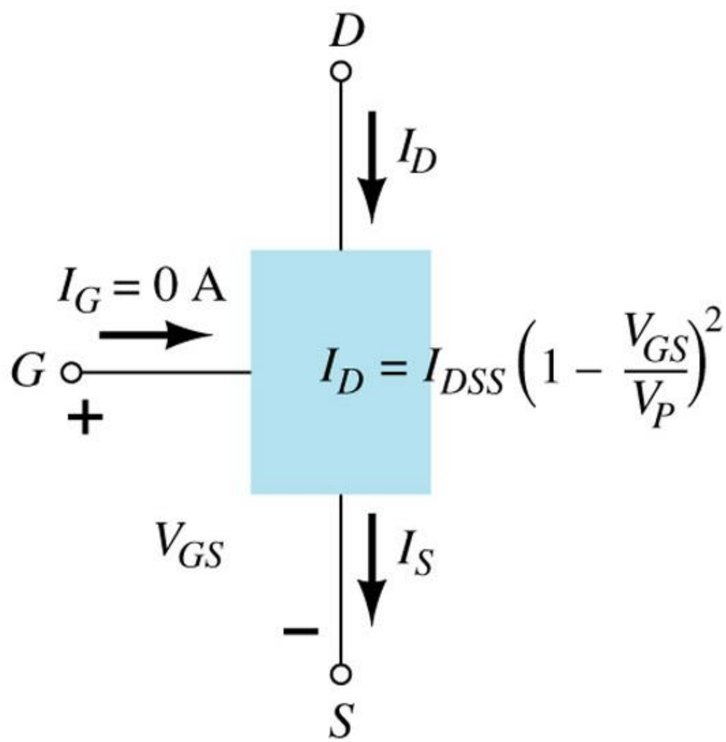
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($I_G = -10\ \mu$Adc, $V_{DS} = 0$)		$V_{(BR)GSS}$	–25	–	–	Vdc
Gate Reverse Current ($V_{GS} = -15$ Vdc, $V_{DS} = 0$) ($V_{GS} = -15$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)		I_{GSS}	– –	– –	–1.0 –200	nAdc
Gate Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 10$ nAdc)	2N5457	$V_{GS(off)}$	–0.5	–	–6.0	Vdc
Gate Source Voltage ($V_{DS} = 15$ Vdc, $I_D = 100\ \mu$Adc)	2N5457	V_{GS}	–	–2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz)	2N5457	$\|y_{fs}\|$	1000	–	5000	µmhos
Output Admittance Common Source* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz)		$\|y_{os}\|$	–	10	50	µmhos
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

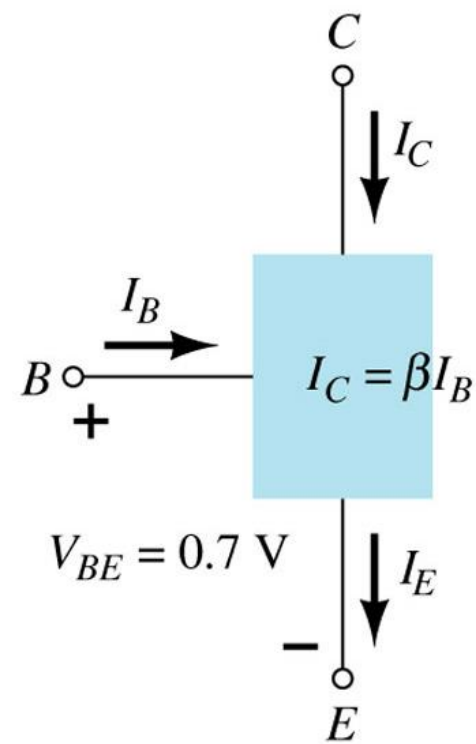
*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

FET versus TBJ

FET



TBJ



JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

Exercícios

1. A corrente de fuga do JFET 2N5951, Segundo sua folha de dados, é 5 pA para uma tensão de 20 V. Qual sua resistência de entrada?

2. A folha de dados do 2N5191 fornece os seguintes valores típicos: I_{DSS} = 10 mA; $V_{GS\ (corte)} = V_p = -3{,}5$ V. Calcule a corrente de dreno para $V_{GS} = -1$ V, -2 V, -3 V e -4 V na região de saturação.

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$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Equação de Schockley

Exercícios

2. Using the characteristics of Fig. 5.10, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$).

(a) $V_{GS} = 0$ V.
(b) $V_{GS} = -1$ V.
(c) $V_{GS} = -1.5$ V.

3. (a) Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 5.10.
(b) Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.
(c) Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.
(d) Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.
(e) Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.

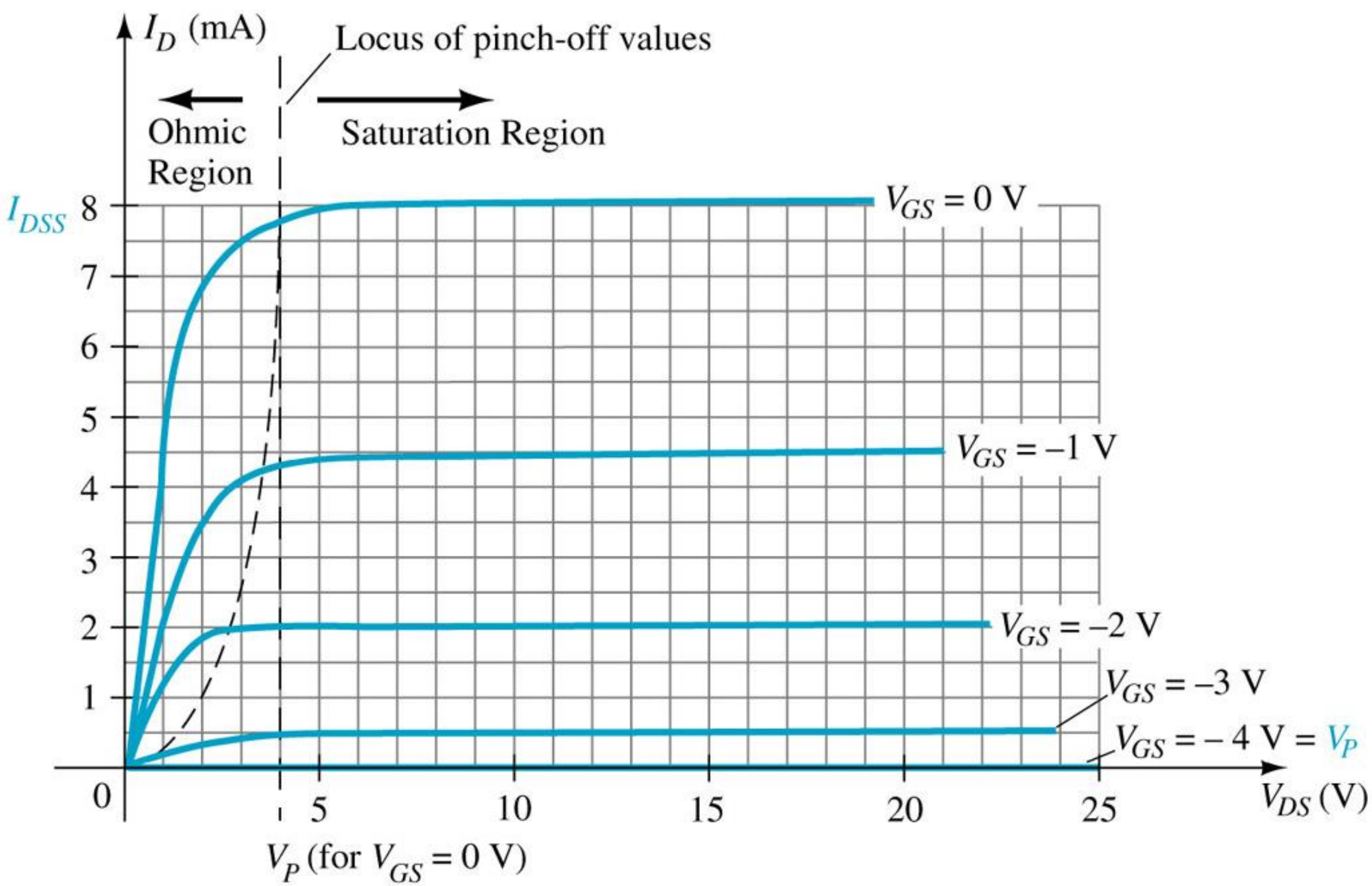
Exercícios

2. Using the characteristics of Fig. 5.10, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$).

(a) $V_{GS} = 0$ V.

(b) $V_{GS} = -1$ V.

(c) $V_{GS} = -1.5$ V.



Exercícios

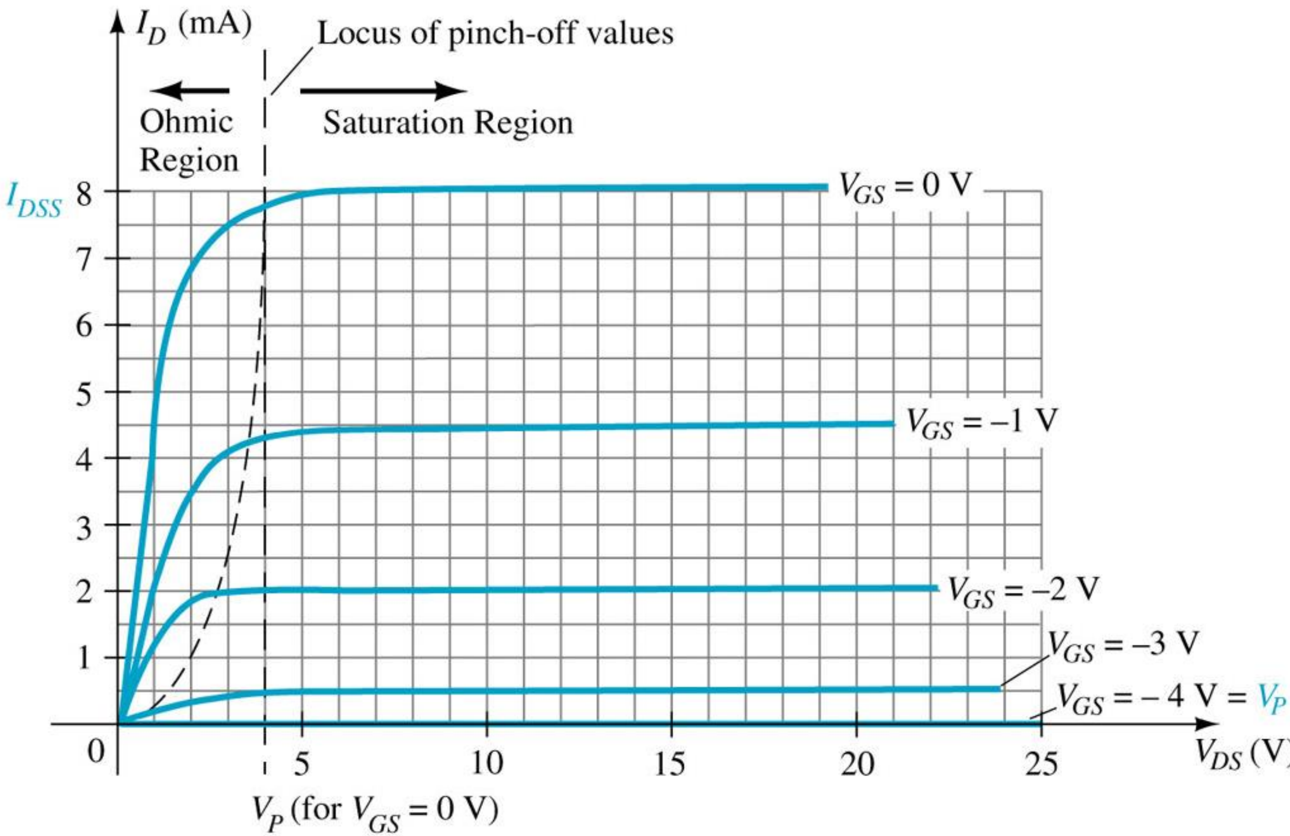
3. (a) Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 5.10.

(b) Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.

(c) Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.

(d) Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.

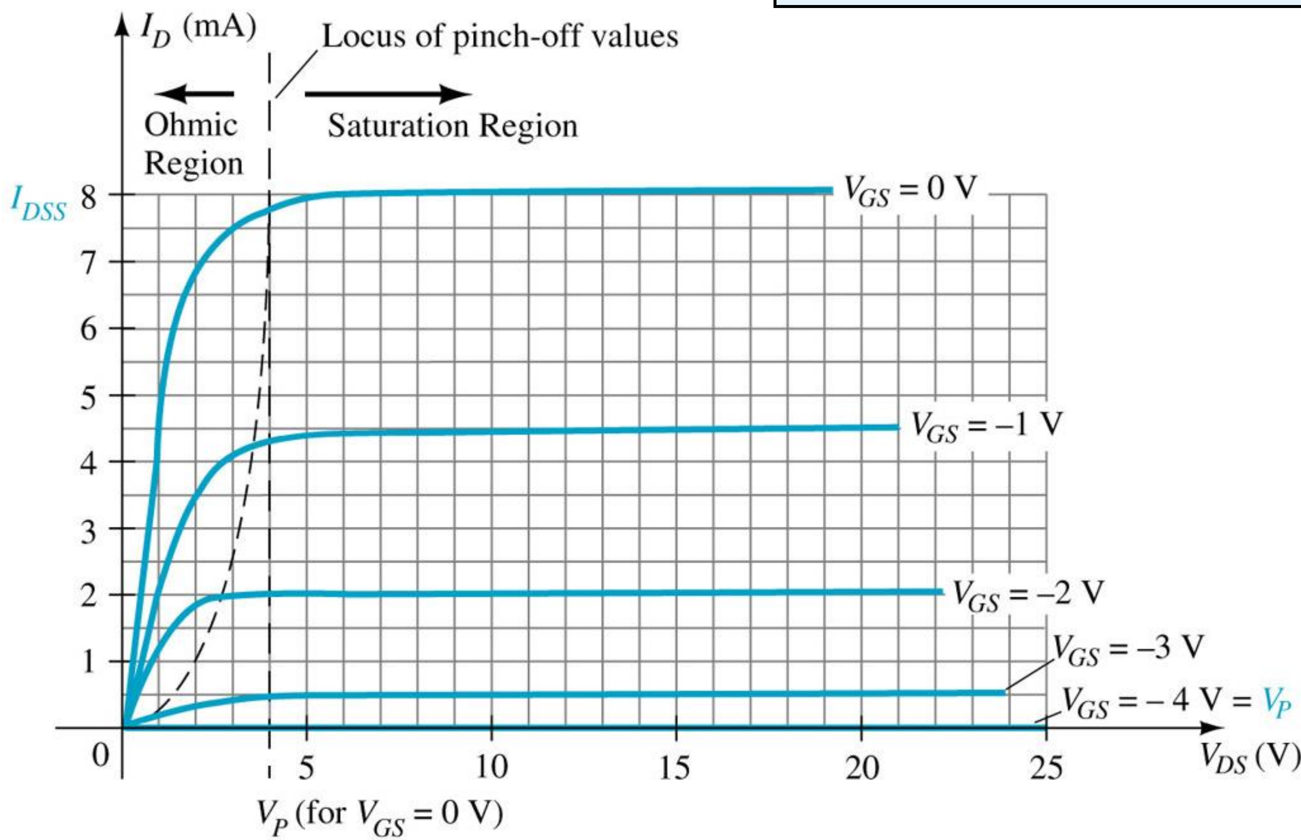
(e) Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.



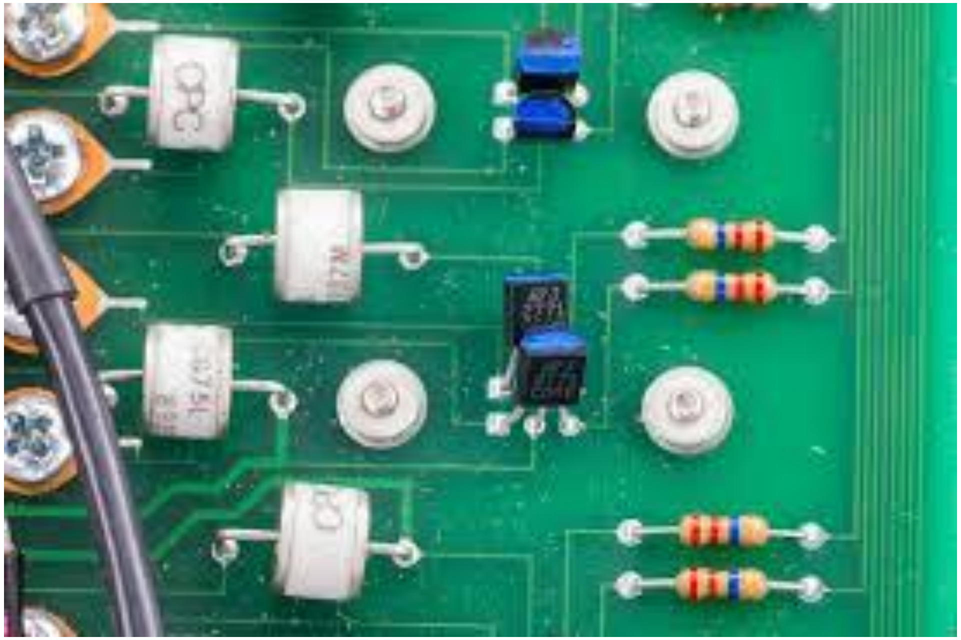
Exercícios

Compare os resultados com aqueles obtidos com a fórmula aproximada:

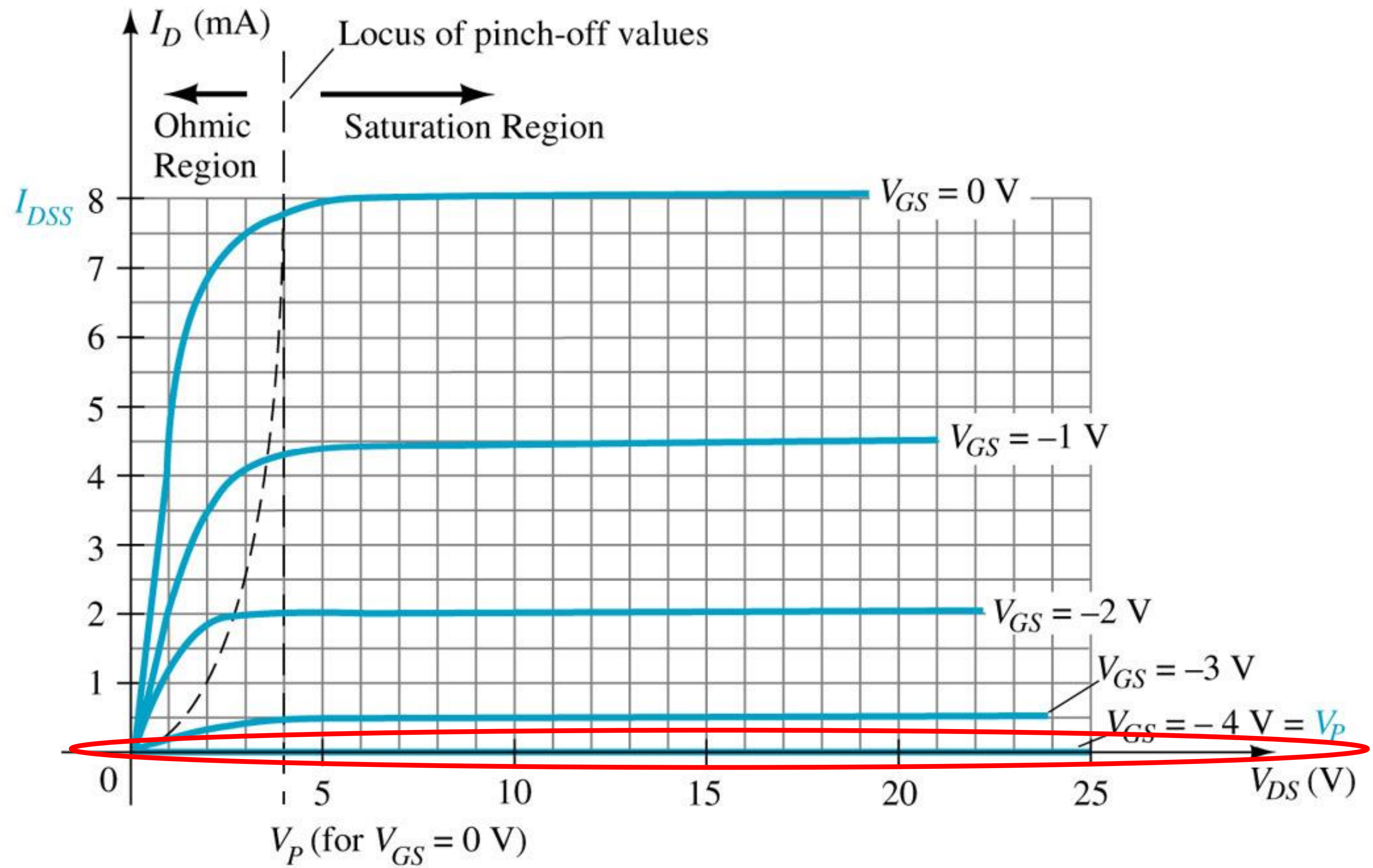
$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$



JFET - Aplicações



JFET - Resumo

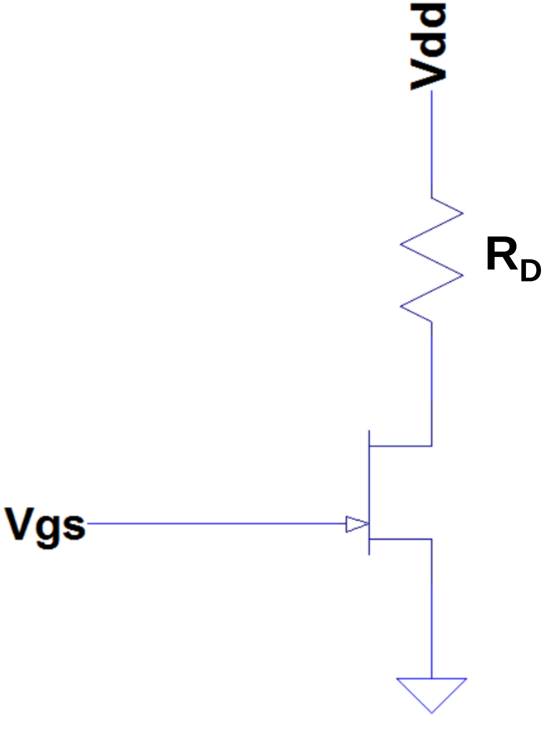


I_D (mA)
Locus of pinch-off values
Ohmic Region
Saturation Region
I_{DSS}
8
7
6
5
4
3
2
1
0
$V_{GS} = 0$ V
$V_{GS} = -1$ V
$V_{GS} = -2$ V
$V_{GS} = -3$ V
$V_{GS} = -4$ V $= V_P$
5
10
15
20
25
V_{DS} (V)
V_P (for $V_{GS} = 0$ V)

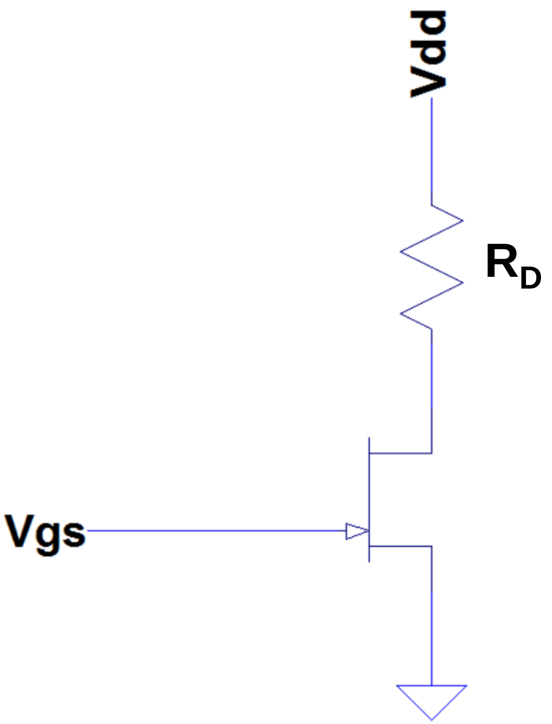
JFET - Aplicações

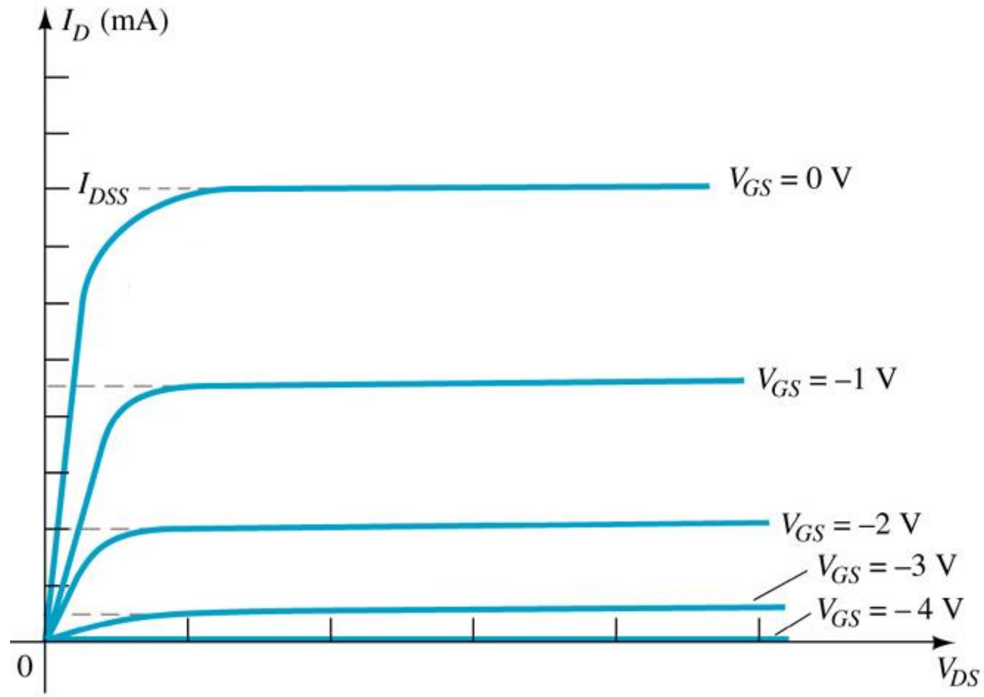
- Aplicações
  - Chave paralela
  - Chave série
  - *Chopper*
  - Limitador de corrente

1 - JFET como Chave Analógica



1 - JFET como Chave Analógica





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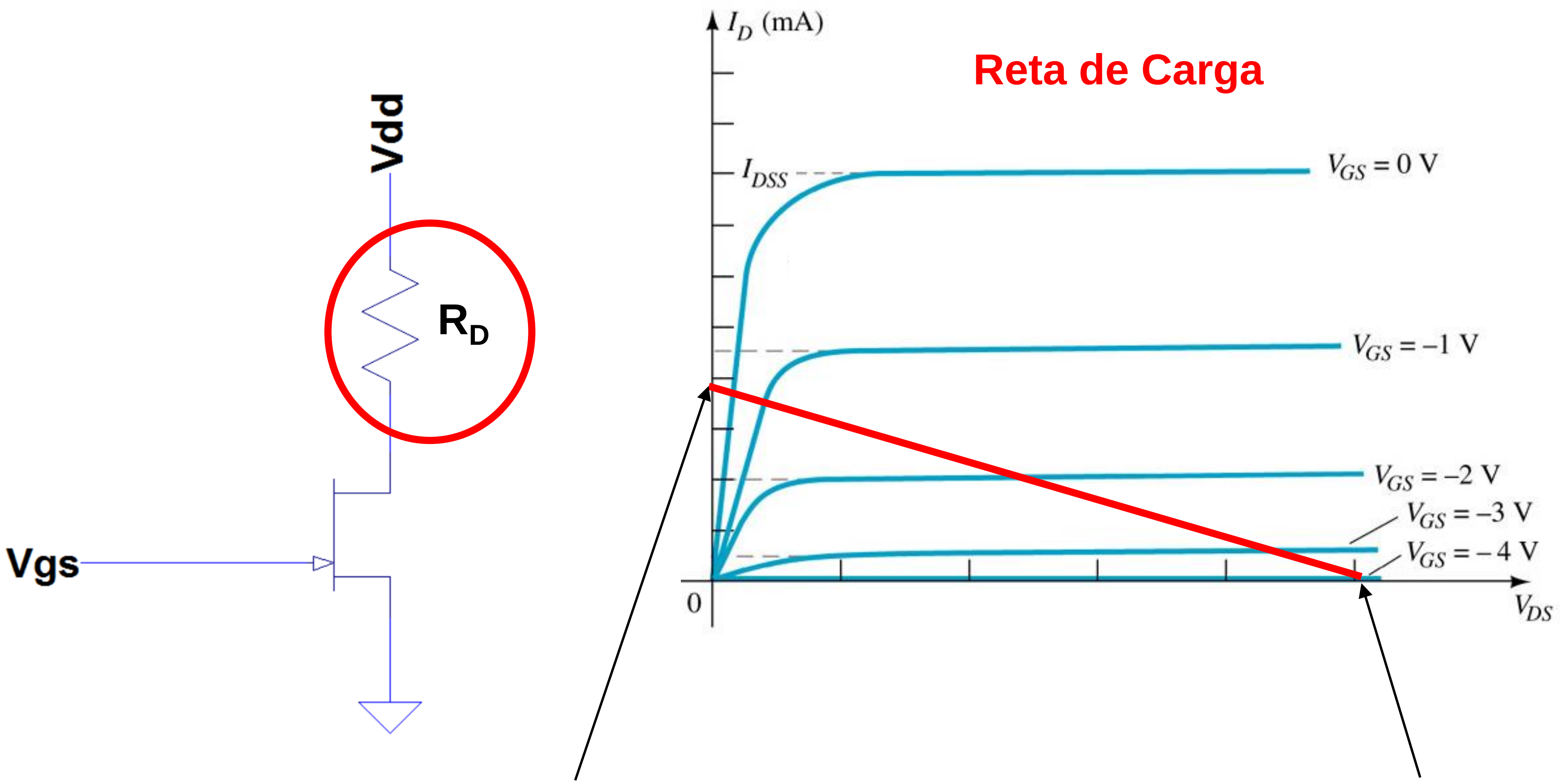
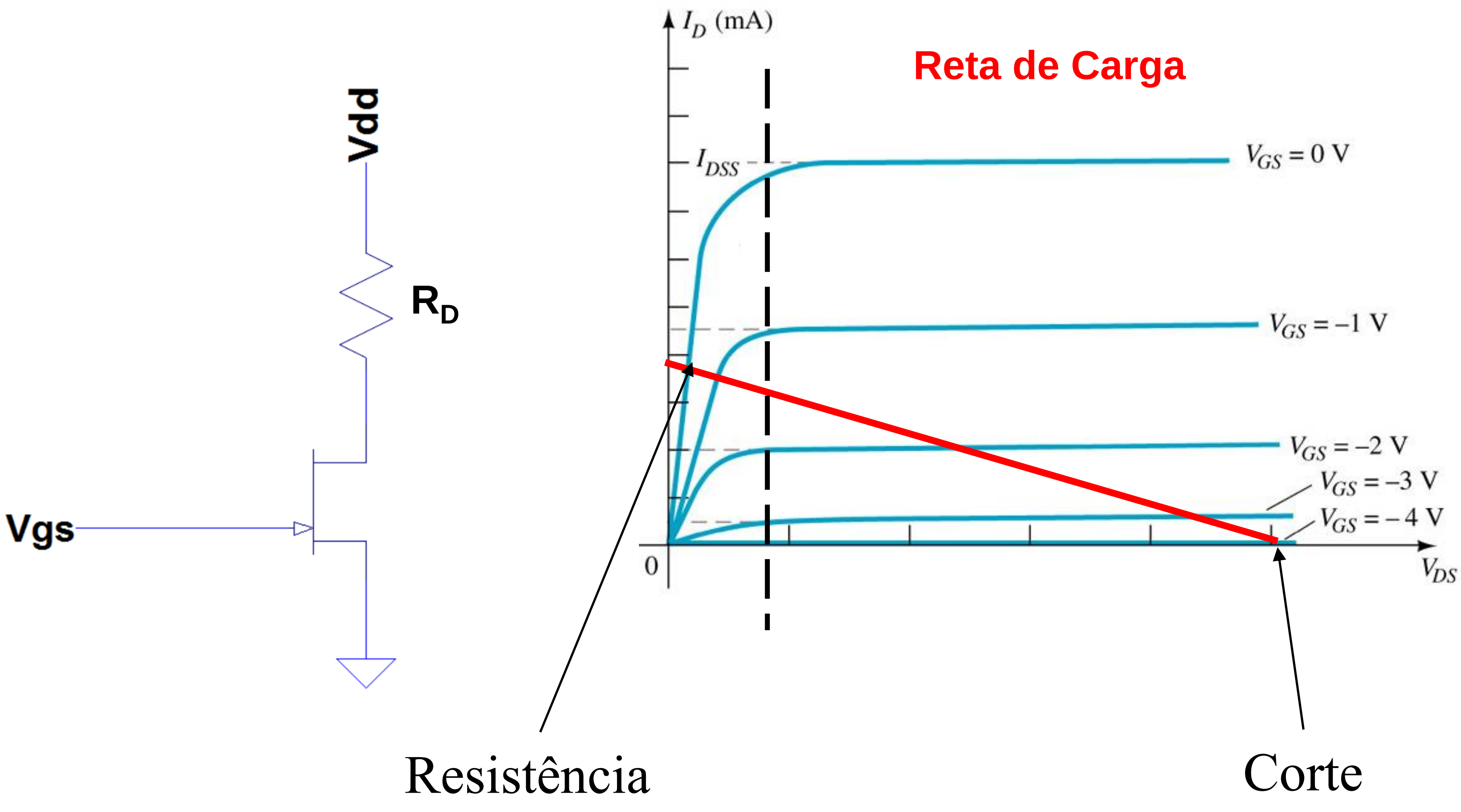


$I_D = V_{DD}/R_D$

$I_D = 0$ A

1 - JFET como Chave Analógica



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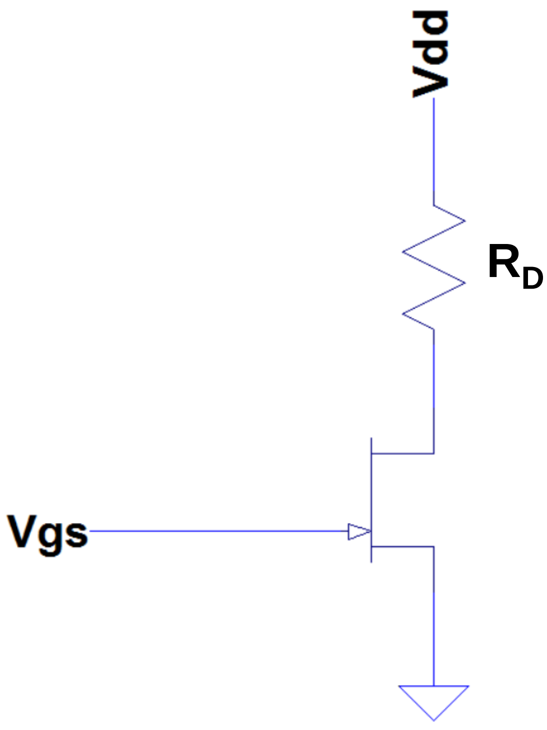
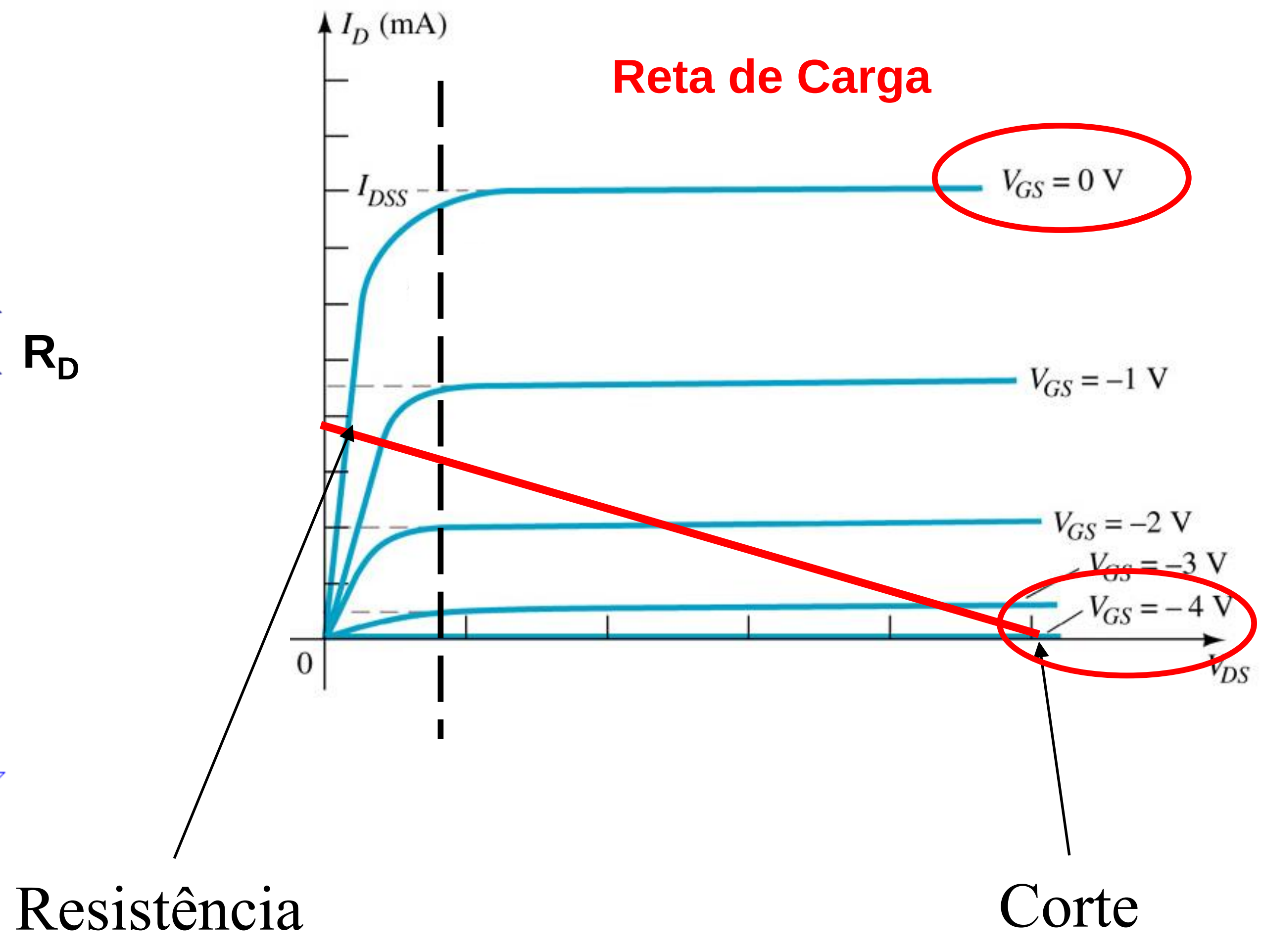
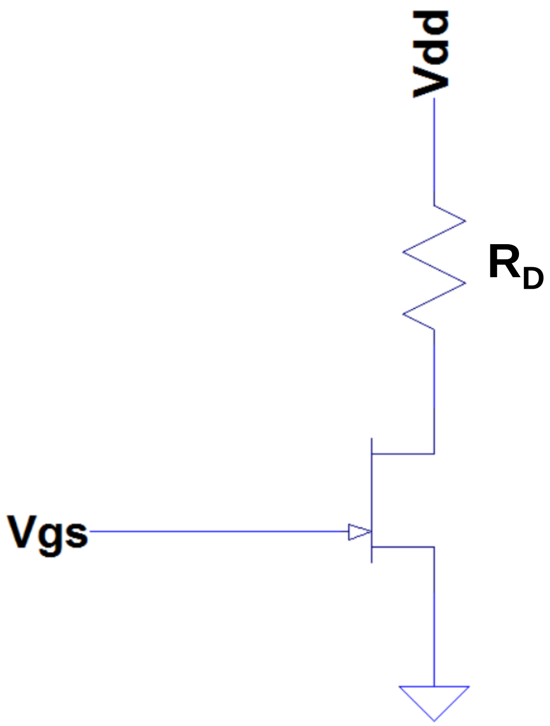
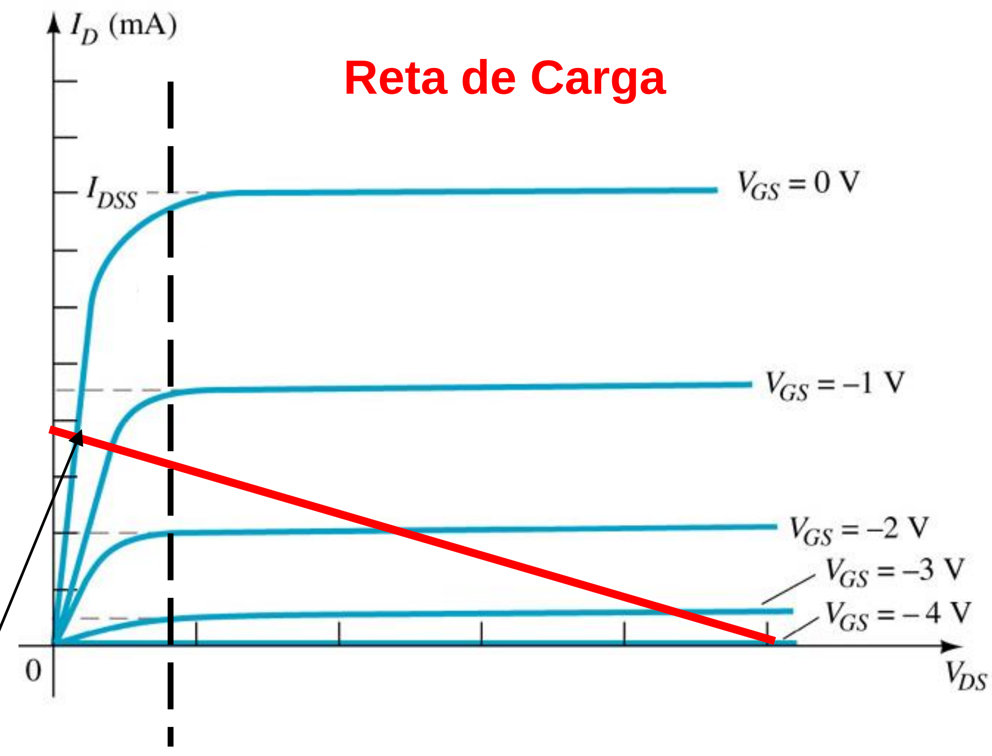




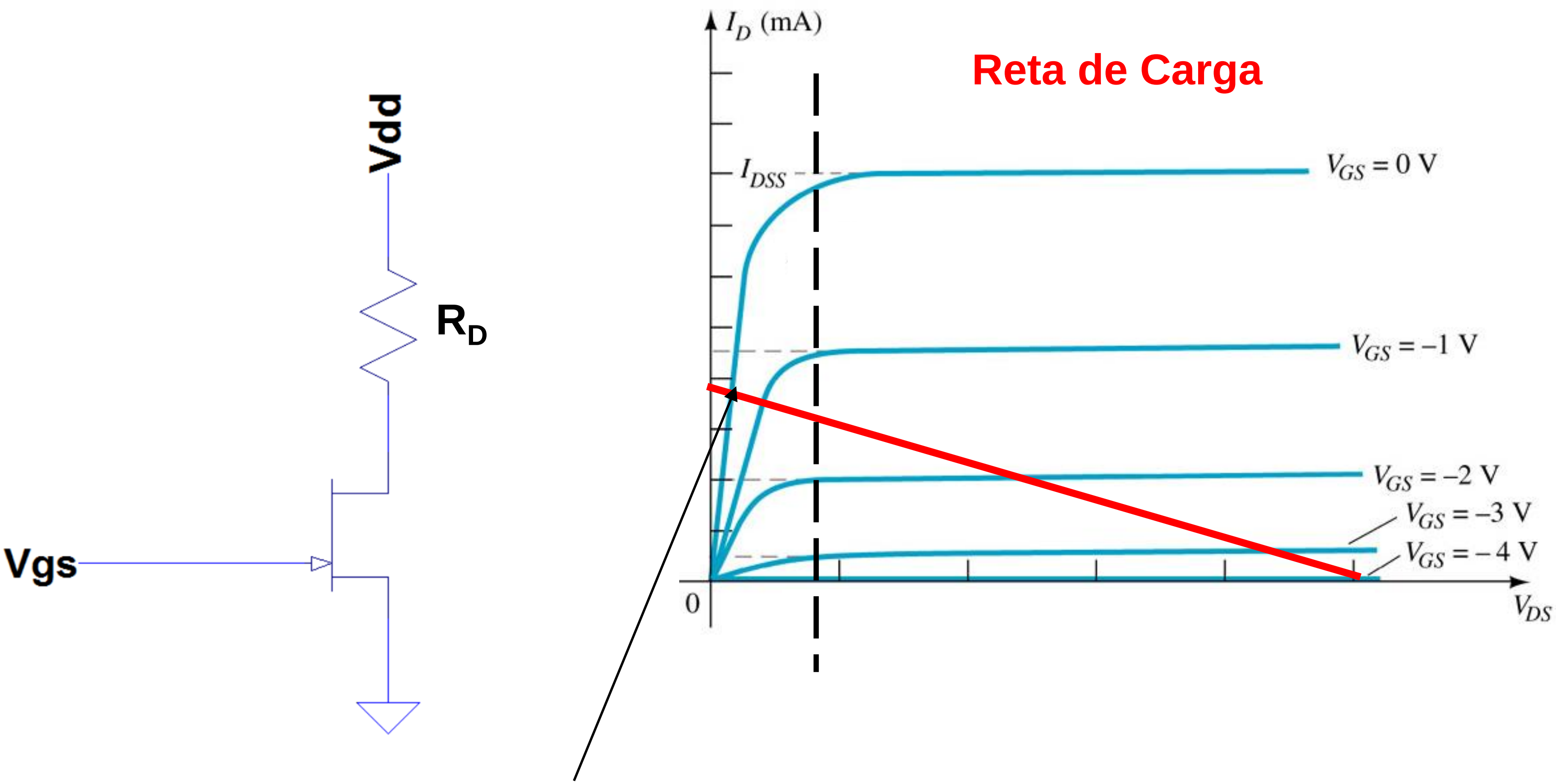
1 - JFET como Chave Analógica





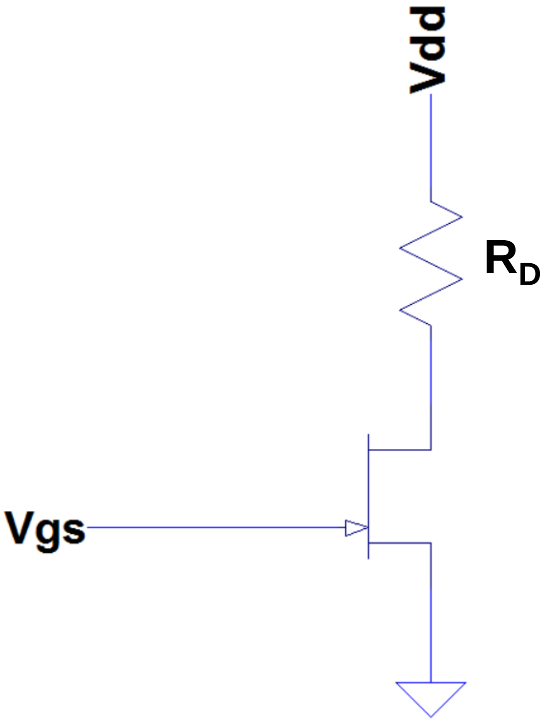
Resistência $R_{DS\,(ON)} = \Delta V_{DS} / \Delta I_D = V_{DS}/I_D$

1 - JFET como Chave Analógica



Resistência $R_{DS\,(ON)} = V_{DS}/I_D \rightarrow$ Muito pequena

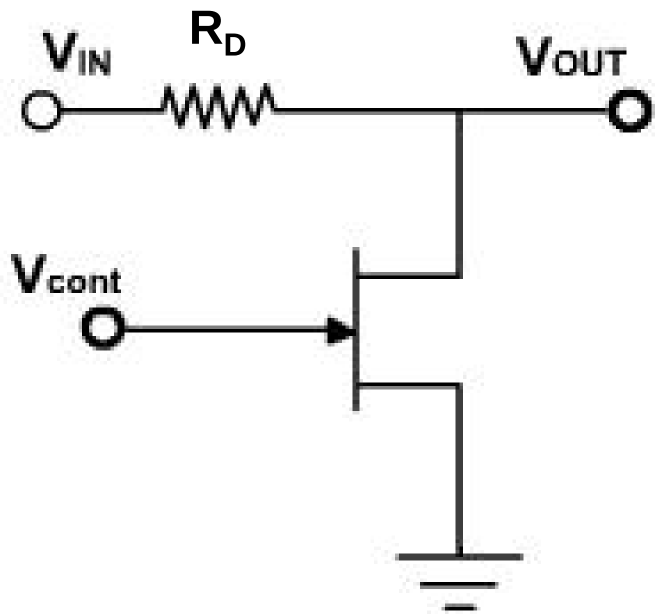
1 - JFET como Chave Analógica



Funcionamento como chave:

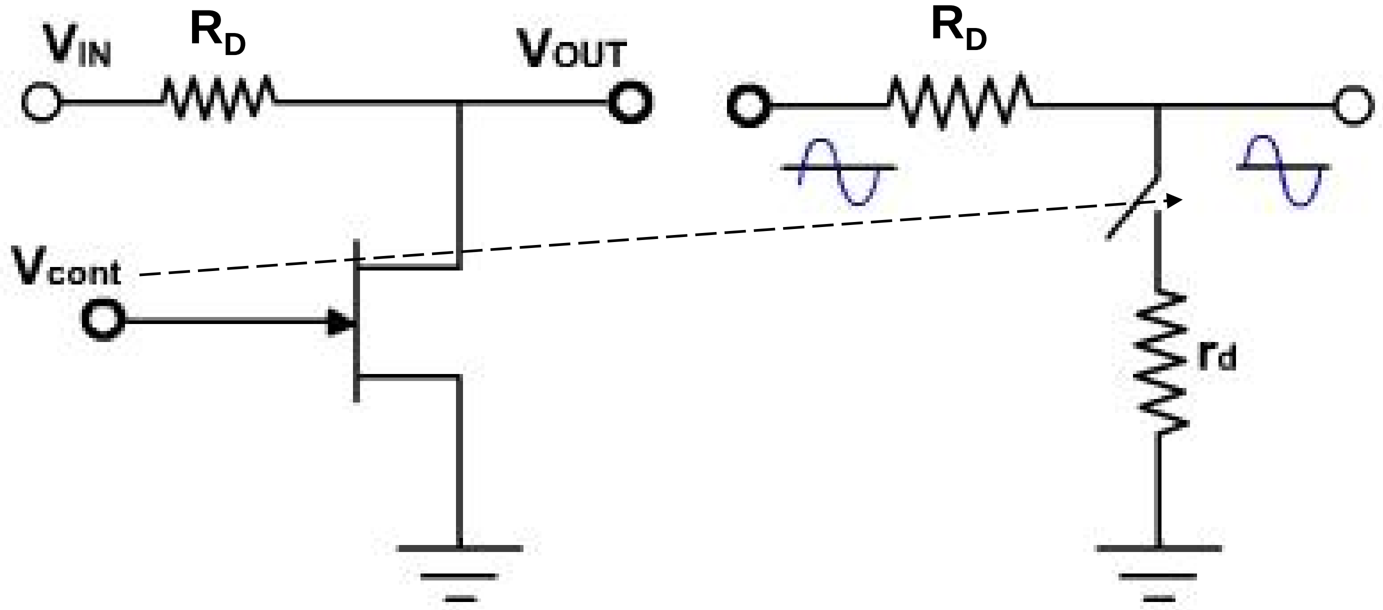
- $V_{GS} = 0V \Rightarrow R_D \sim 0$
- $V_{GS} \leq -V_P \Rightarrow R_D \sim \infty$

1.1 - Chave *Paralela*



1.1 - Chave *Paralela*

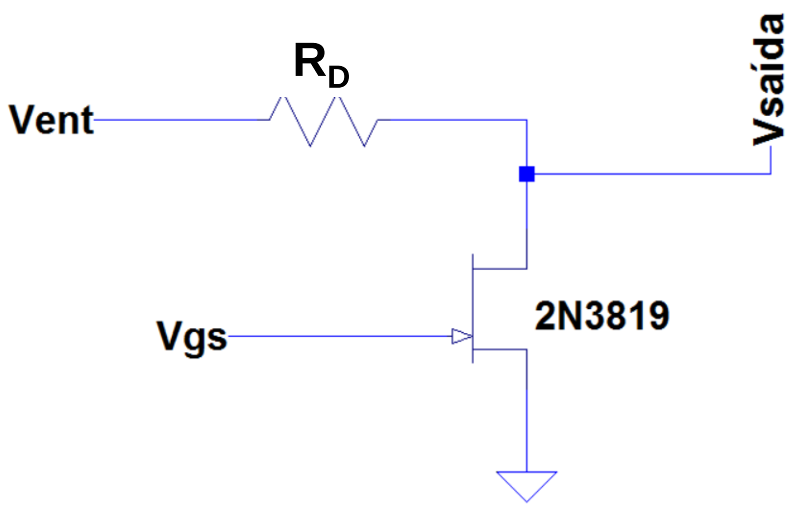
Circuito equivalente



Exemplo

1) O FET do circuito abaixo possui $r_d = R_{DS(ON)} = 10\ \Omega$. Supondo que $V_{ent} = 20$ mV, qual é o valor de $V_{saída}$ quando $V_{GS} = 0$ V? E quando V_{GS} for mais negativo que V_p?

$R_D = 2{,}2\ k\Omega$

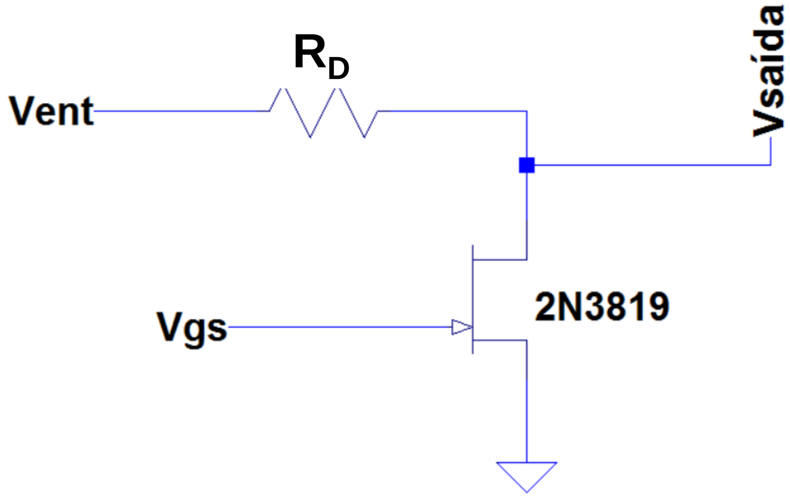


Exemplo

1) O FET do circuito abaixo possui $r_d = R_{DS(ON)} = 10\ \Omega$. Supondo que $V_{ent} = 20$ mV, qual é o valor de $V_{saída}$ quando $V_{GS} = 0$ V? E quando V_{GS} for mais negativo que V_p?

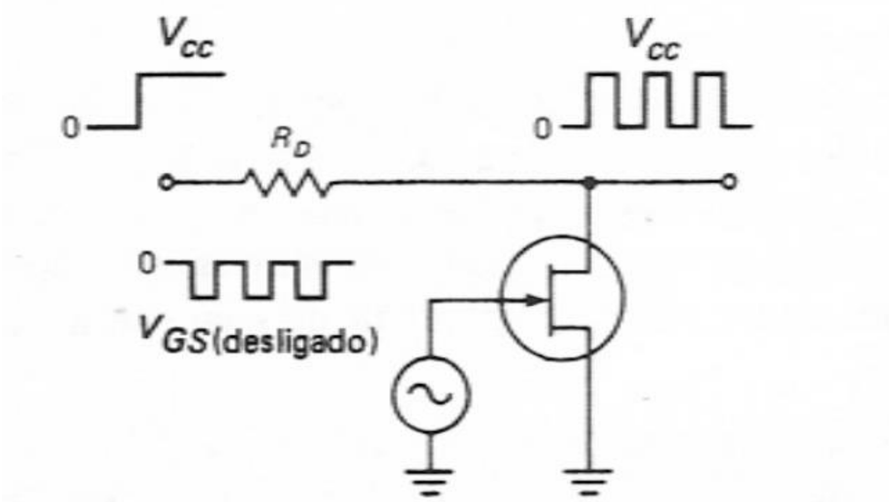
(R:0,09 mV e 20 mV)

$R_D = 2{,}2\ k\Omega$



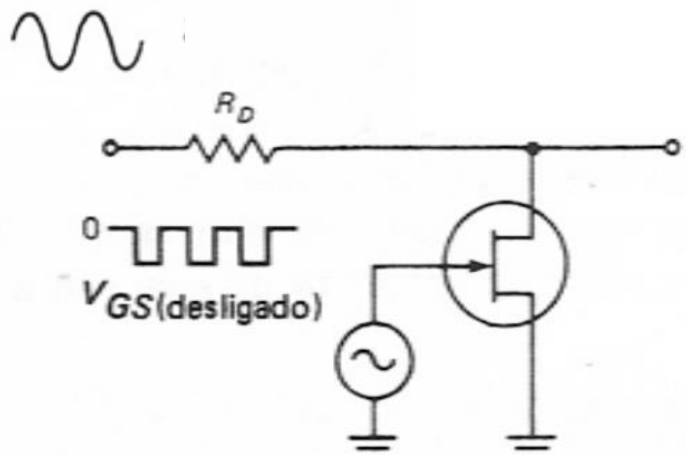
Chopper

Chopper



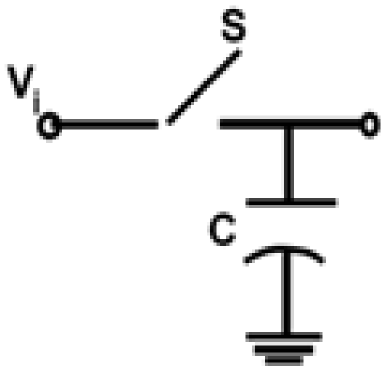
Chopper

Chopper entrada senoidal



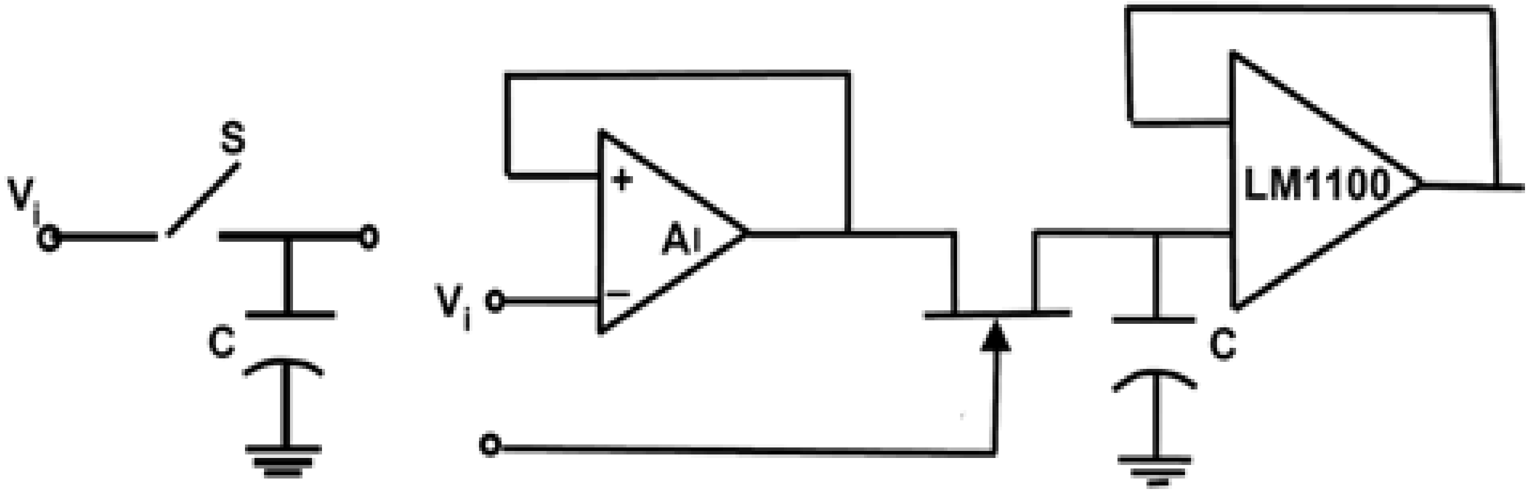
(c)

Chopper: exemplo de aplicação



Controle
conversor AD

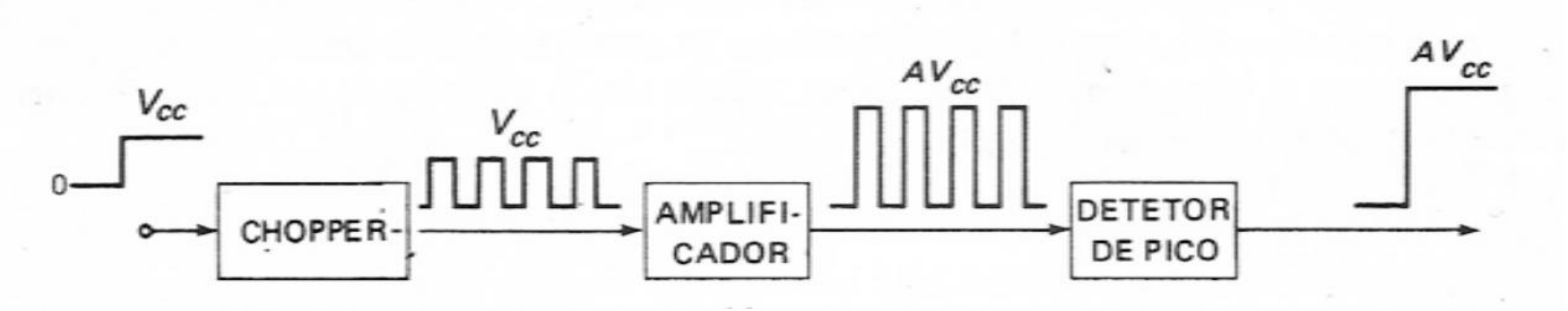
Chopper: exemplo de aplicação



Controle
conversor AD

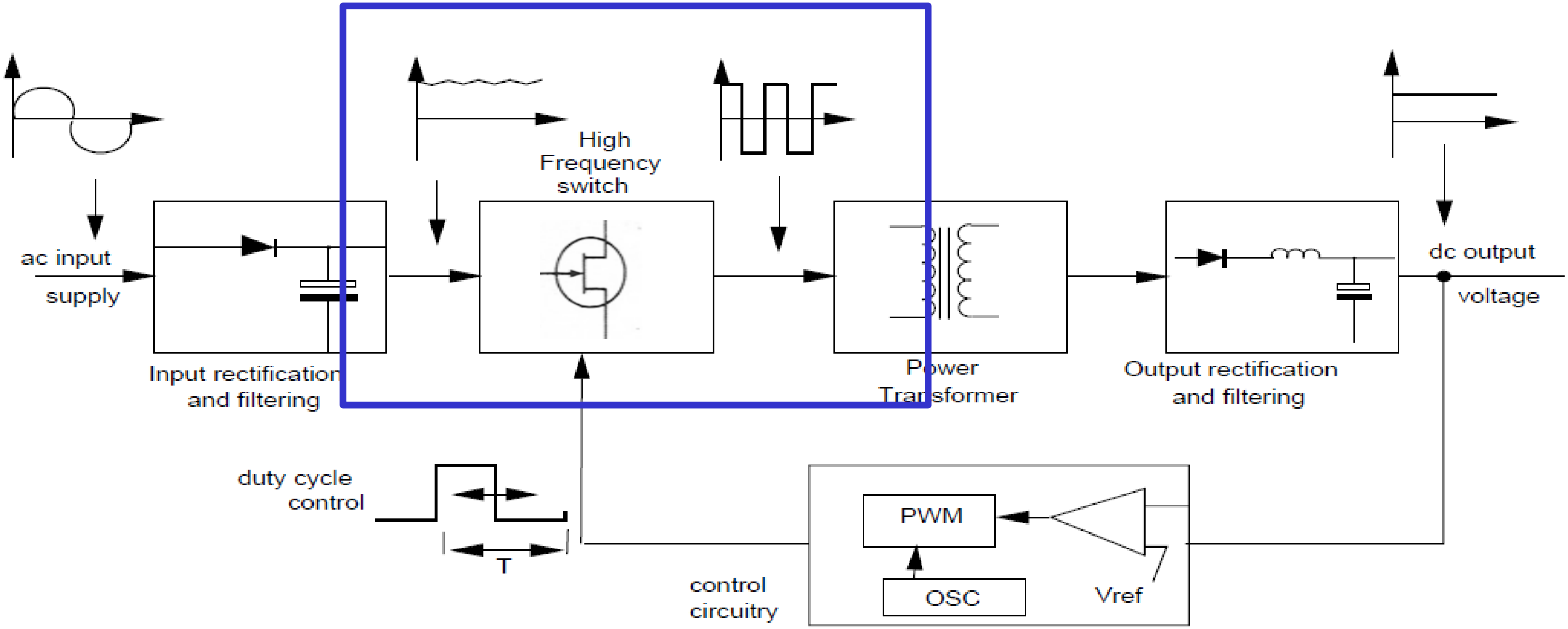
Chopper: exemplo de aplicação

Amplificador DC



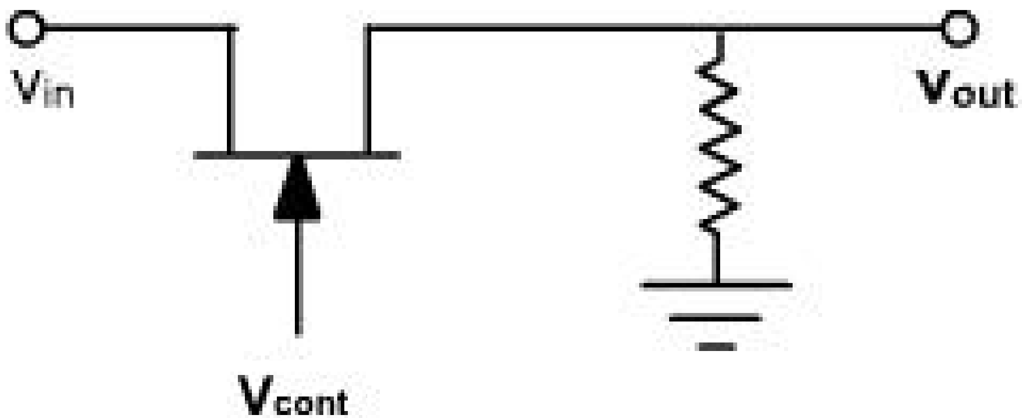
Chopper: exemplo de aplicação

Ex.: Chopper entrada DC com flutuação (*ripple*)



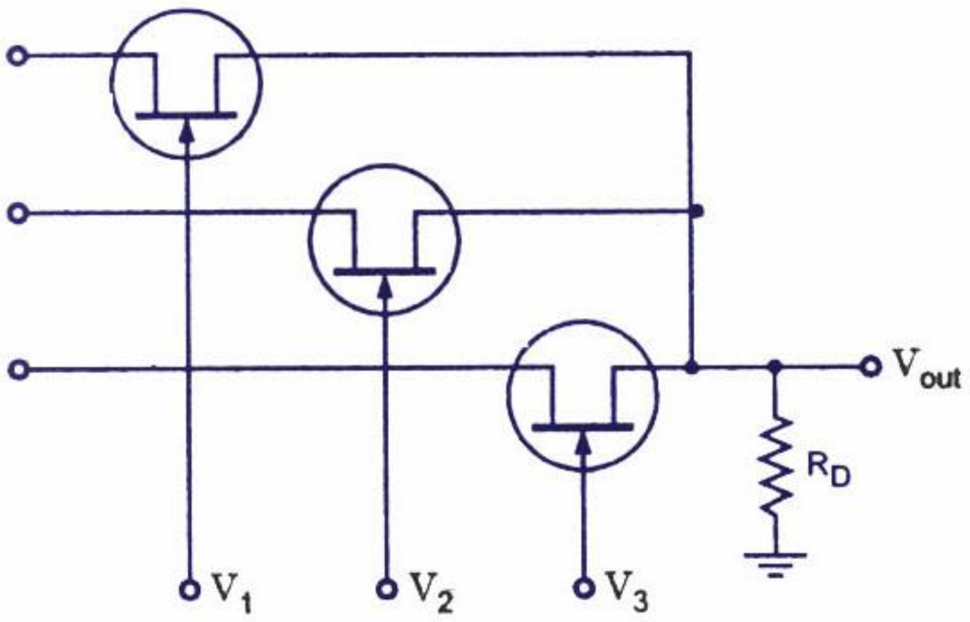
Obs.: Na prática os MOSFETs e TBJs são utilizados em fontes chaveadas.

1.2 - Chave *Série*



1.2 - Chave *Série - exemplo de aplicação*

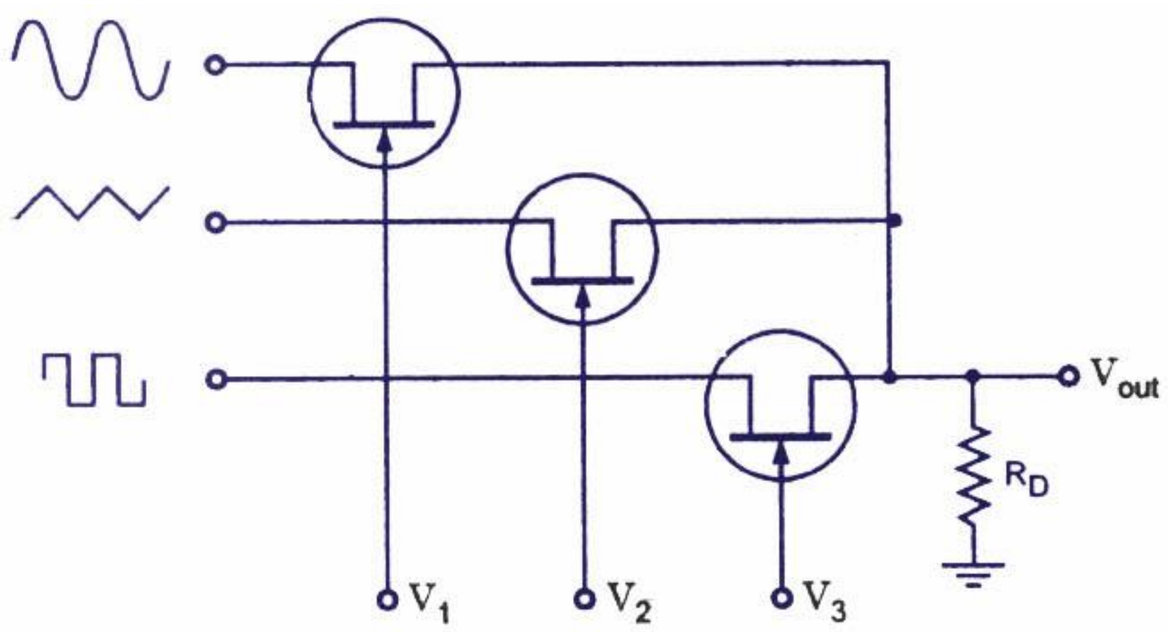
Multiplexador Analógico (Seletor)



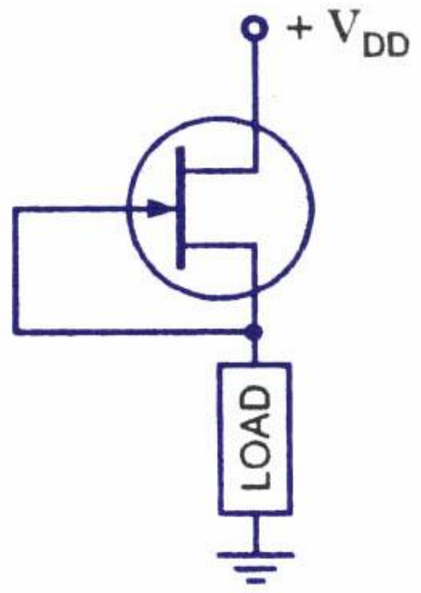
1.2 - Chave *Série - exemplo de aplicação*

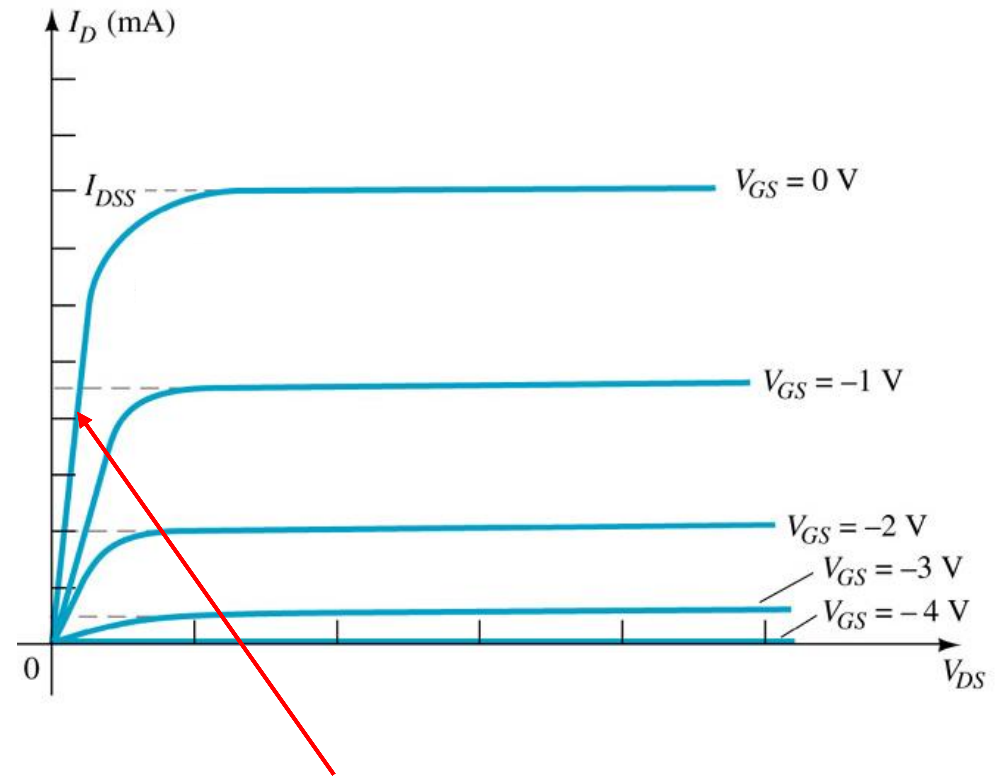
Multiplexador Analógico (Seletor)

Entradas
Analógicas



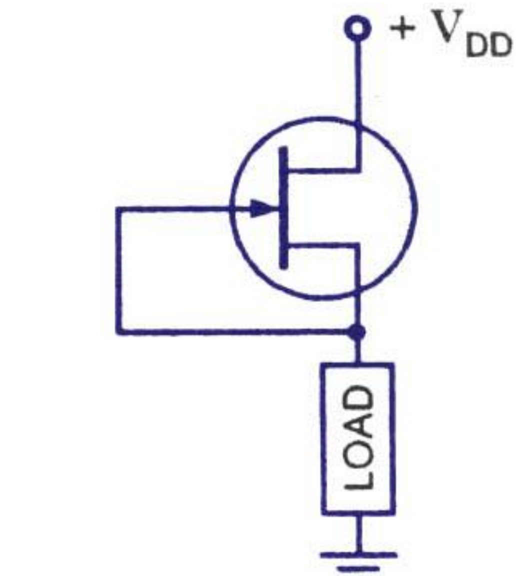
2 – Limitador de corrente

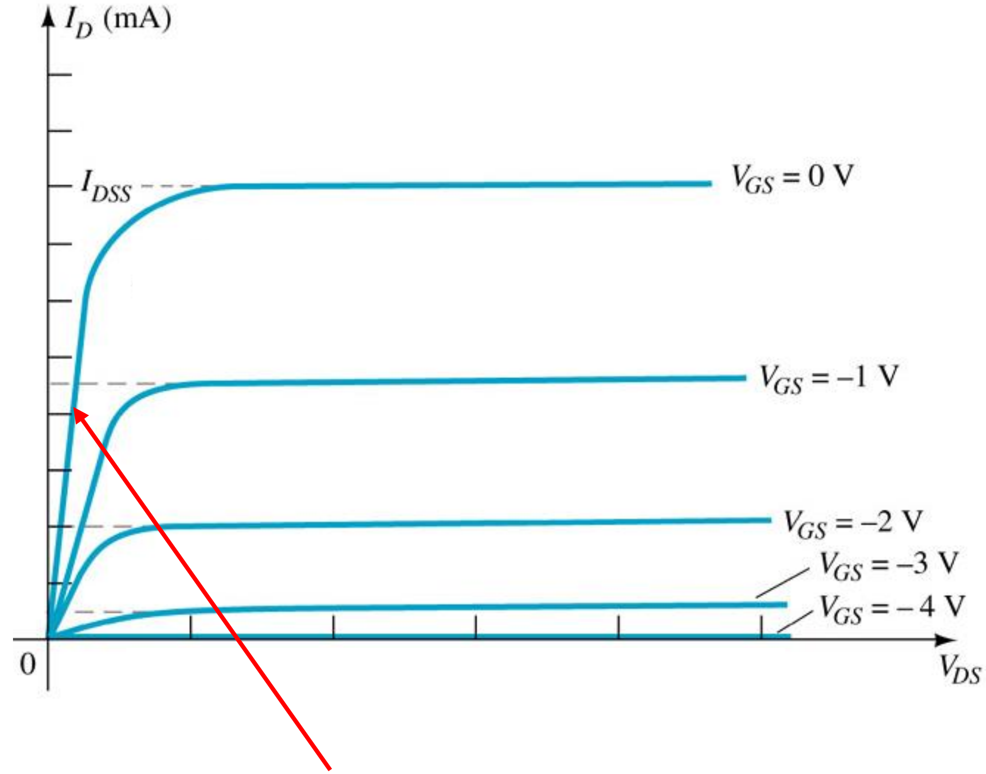




Pra valores "baixos" de corrente de carga (I_D), o JFET trabalha na região de baixa resistência.

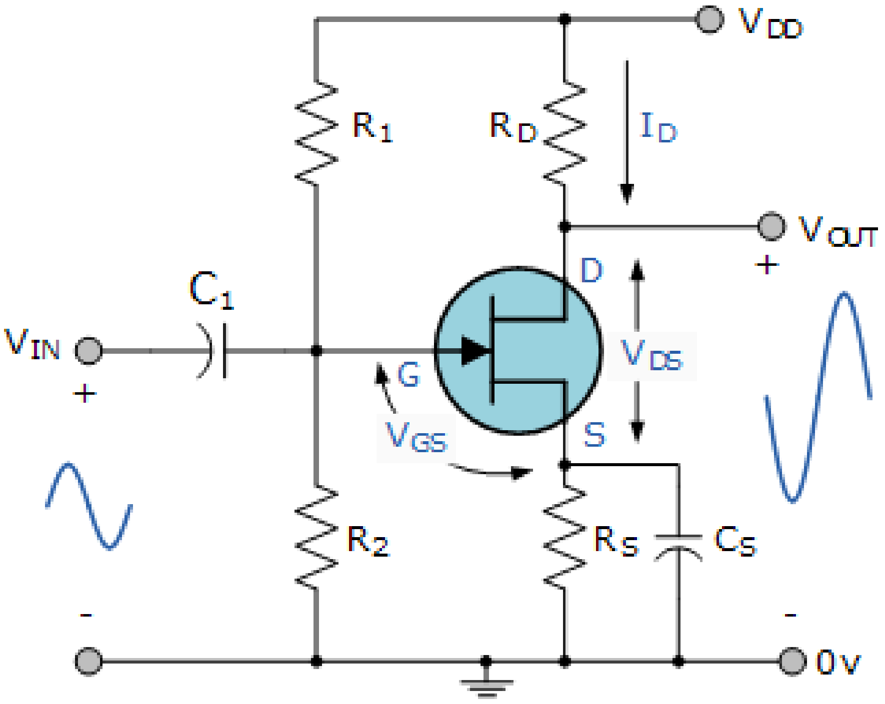
2 – Limitador de corrente





Se a corrente da carga I_D aumentar (e. g., curto-circuito), o JFET limita seu valor em I_{DSS}.

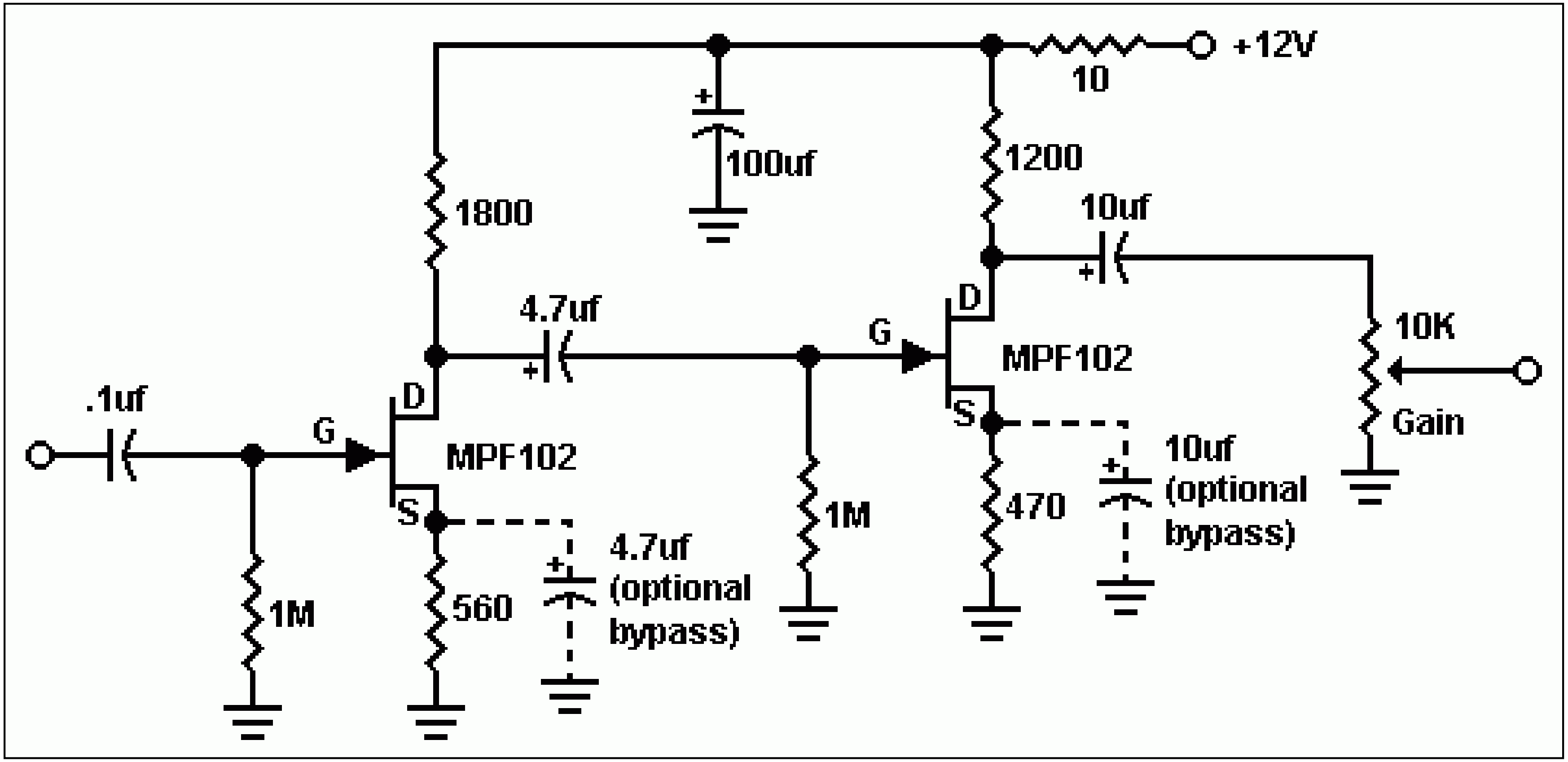
3 - Amplificador de sinais



Vantagens (comparado ao TBJ):

- Alta R_i
- Baixo ruído

3 - Amplificador de sinais



Fonte: http://www.rason.org/Projects/jfetamp/jfetamp.htm