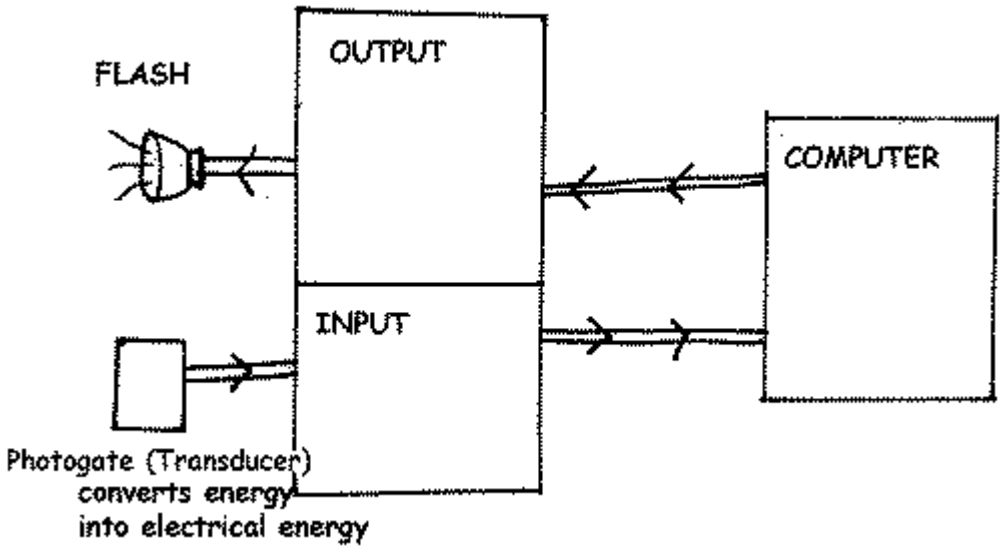
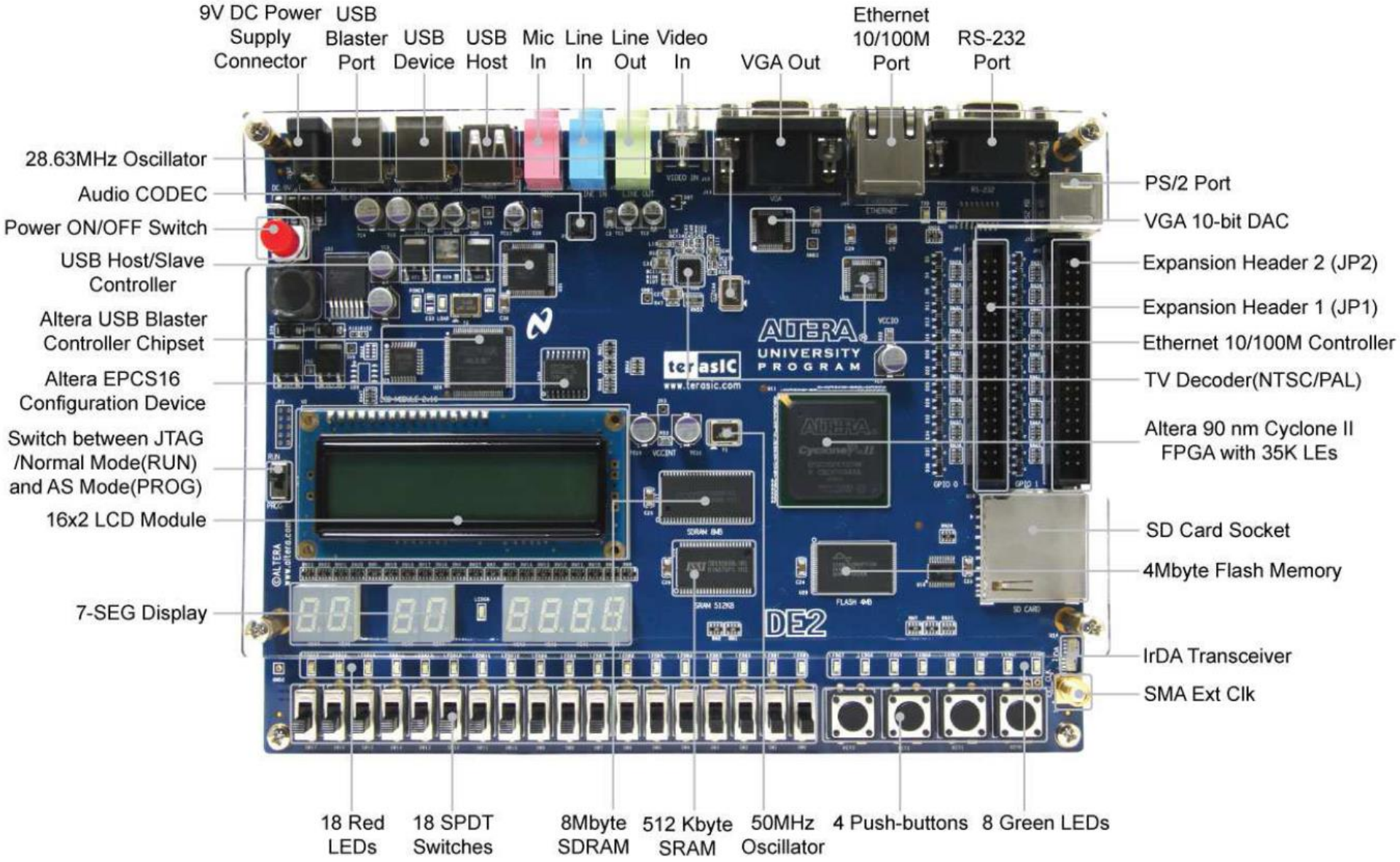
Interfaces de E/S



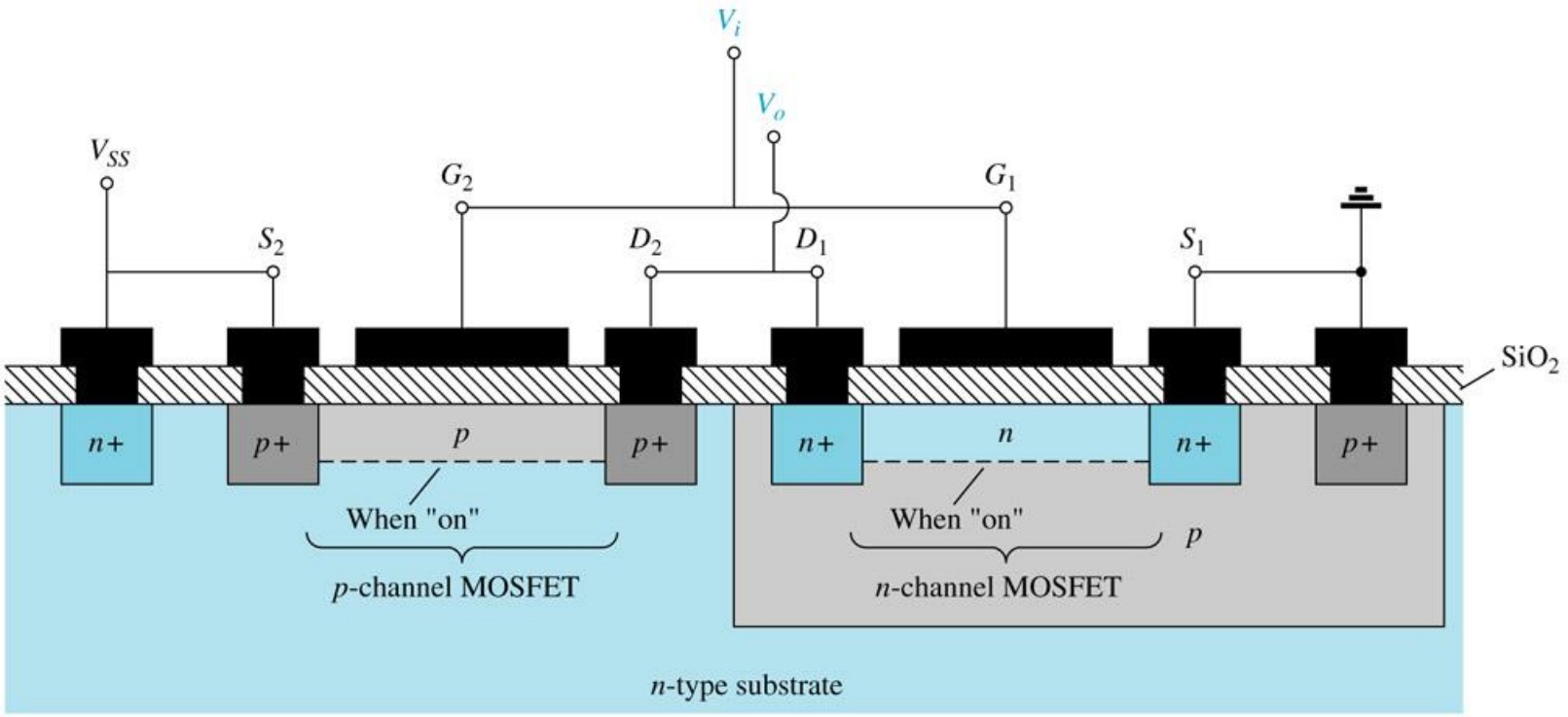
Interfaces de E/S



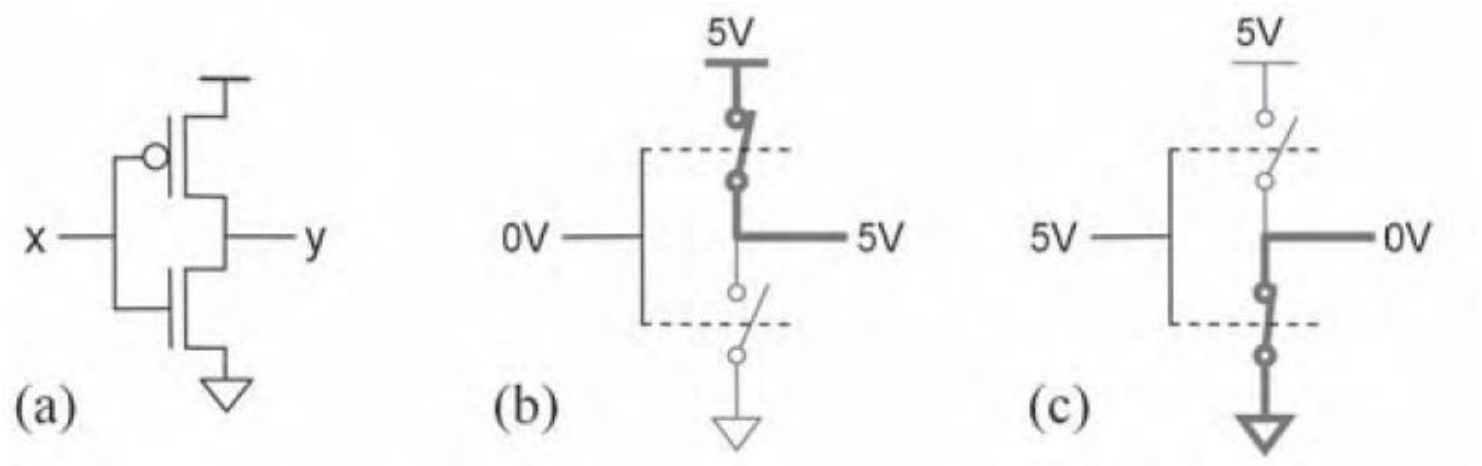
Resumo

- Nível de abstração: HW
- Portas lógicas CMOS
- Níveis de tensão TTL, CMOS
- Diagrama temporal
- Dreno/Coletor aberto
- Consumo de energia CMOS
- Fan-in & Fan-out

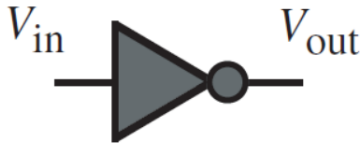
Complementary MOS



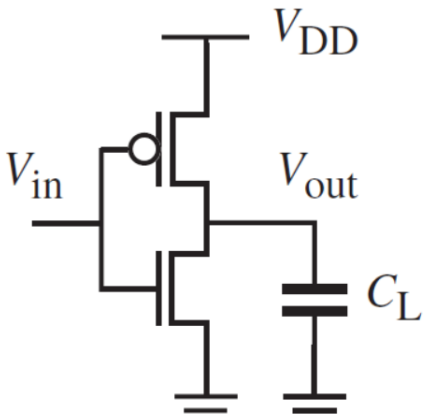
Portas lógicas CMOS – Inversor



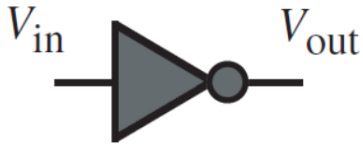
Portas lógicas CMOS – Inversor



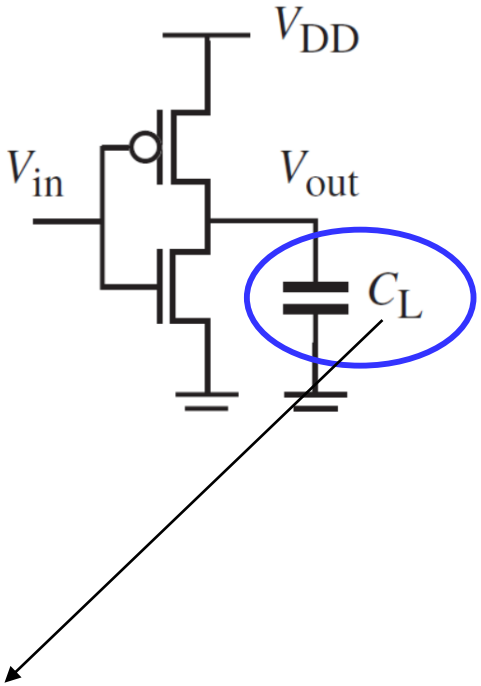
V_{in}	V_{out}
0	1
1	0



Portas lógicas CMOS – Inversor

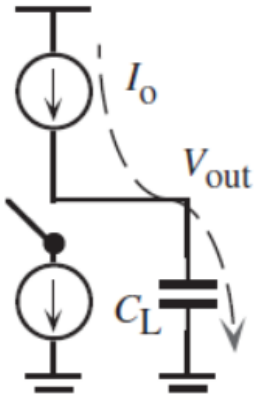


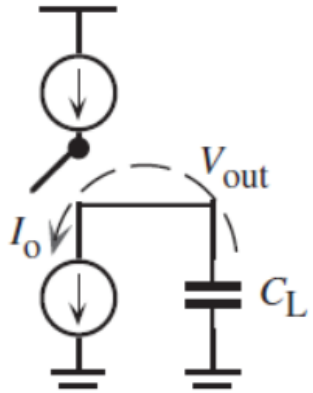
V_{in}	V_{out}
0	1
1	0

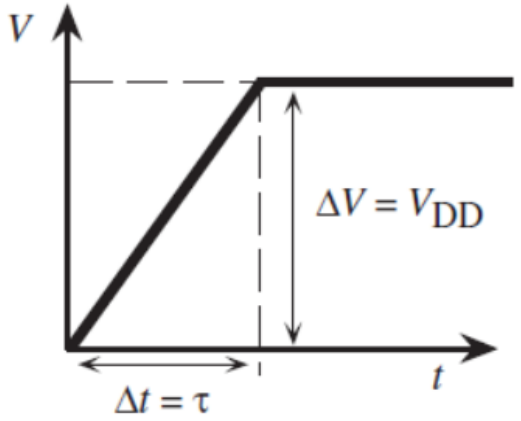


Capacitância de Carga
(entrada de outra porta CMOS)

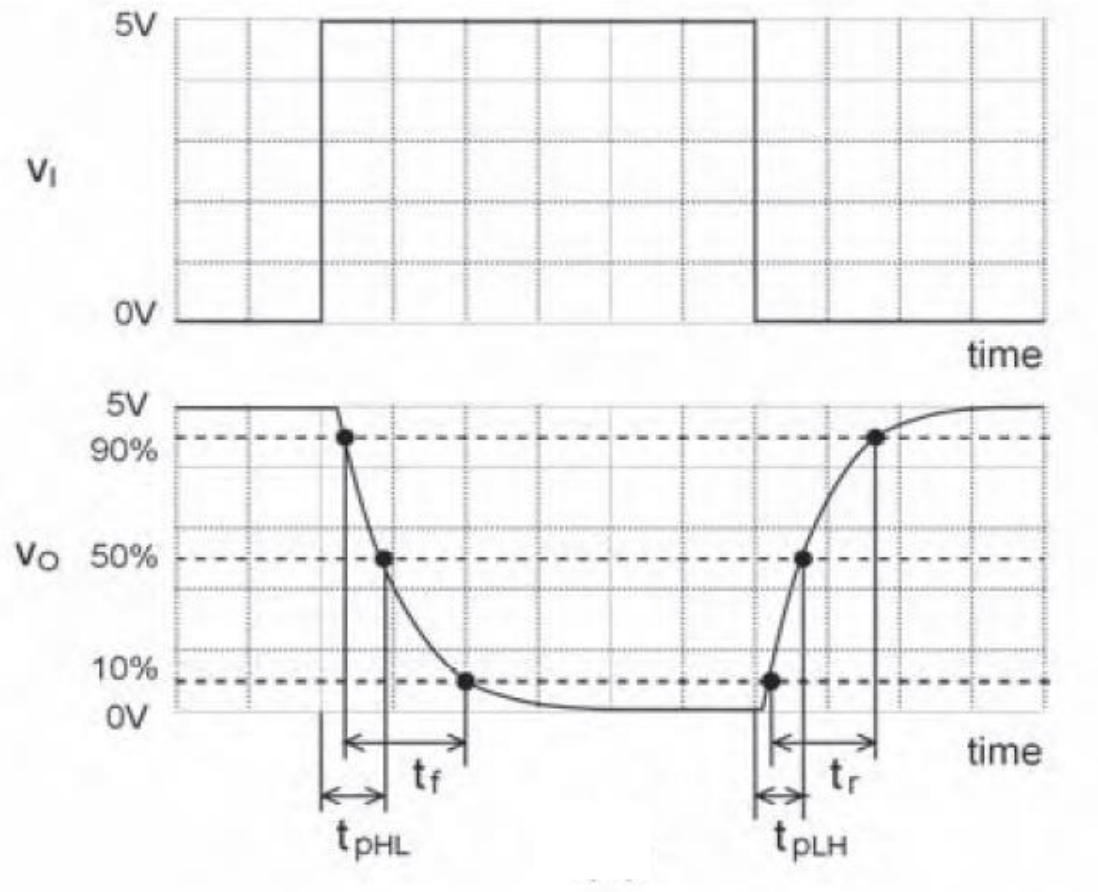
Portas lógicas CMOS – Inversor



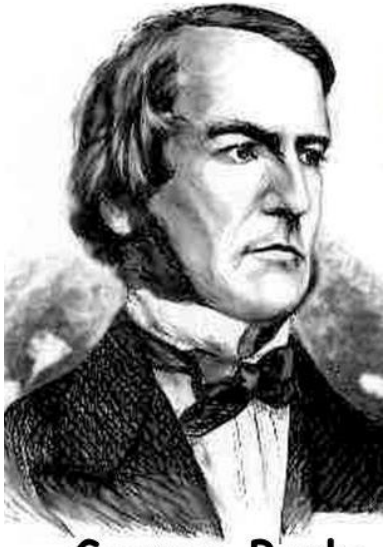




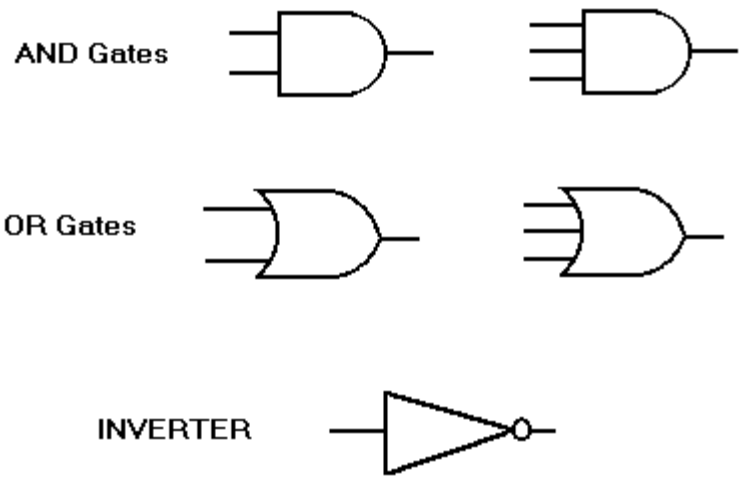
Portas lógicas CMOS – Inversor

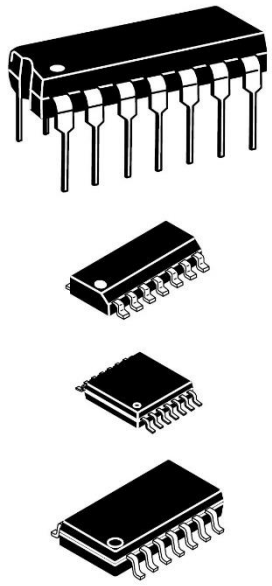


Portas lógicas CMOS

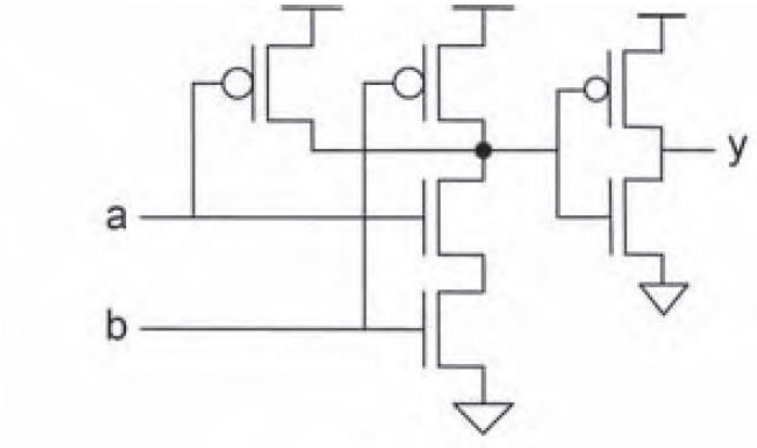


George Boole,
(1815-1864)

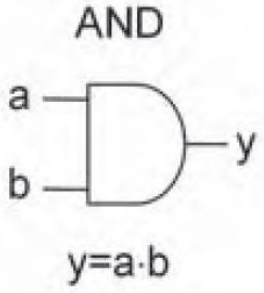




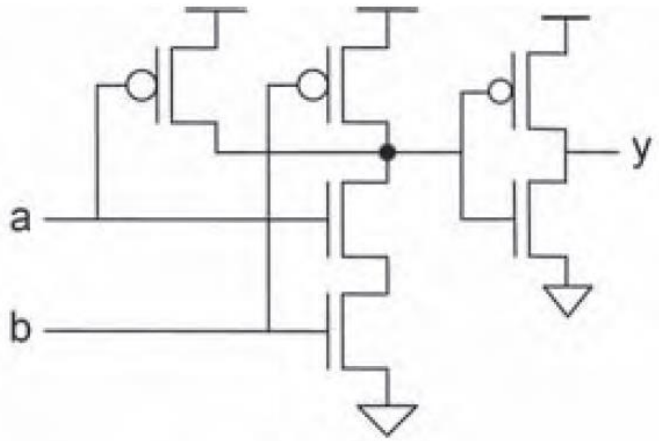
Portas lógicas CMOS – ???



Portas lógicas CMOS – AND



a b	y
0 0	0
0 1	0
1 0	0
1 1	1



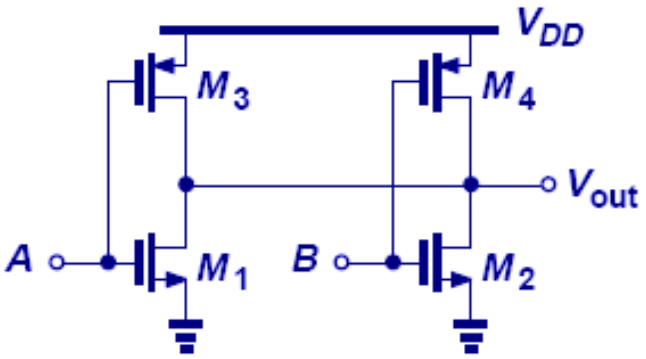
Portas lógicas CMOS

Conceito de ligação complementar dos MOSFETs

ANTENÇÃO

Conceito de ligação complementar dos MOSFETs

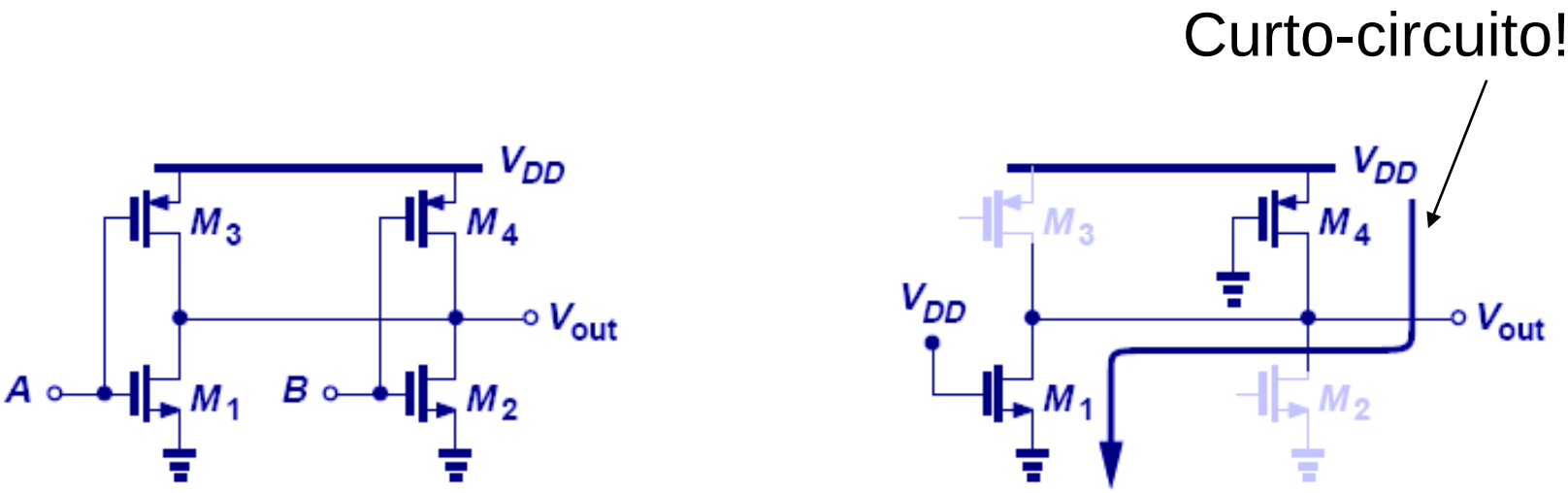
Exemplo:



ANTENÇÃO

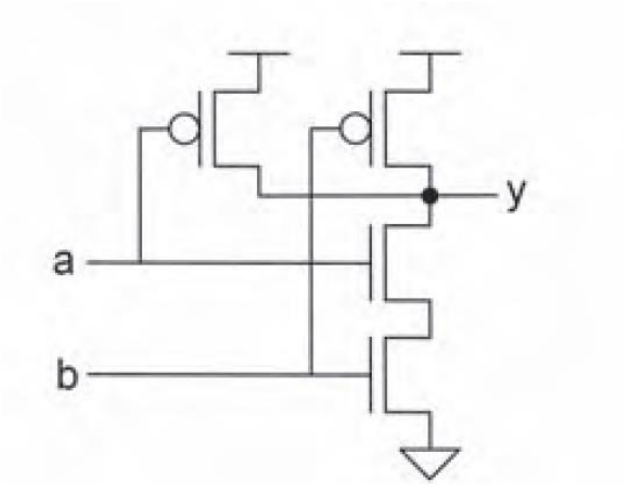
Conceito de ligação complementar dos MOSFETs

Exemplo:



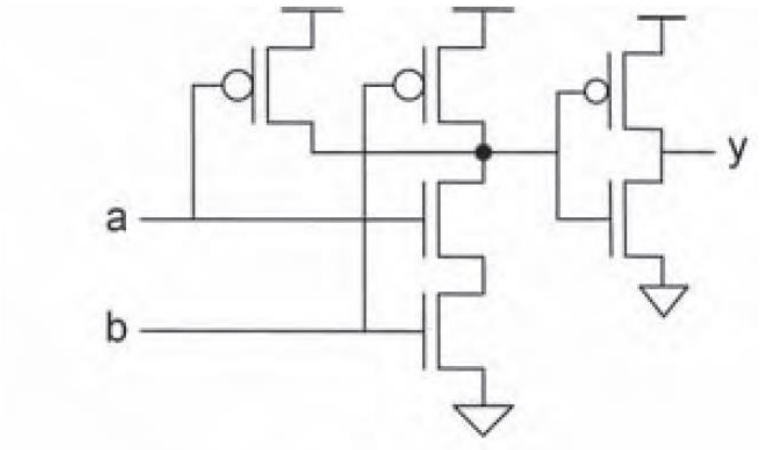
NÃO funciona como uma porta lógica!

Portas lógicas CMOS – ???

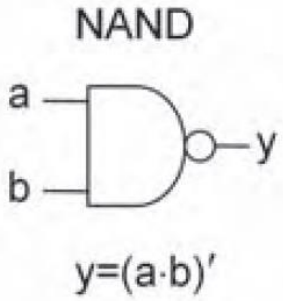


Dica!!

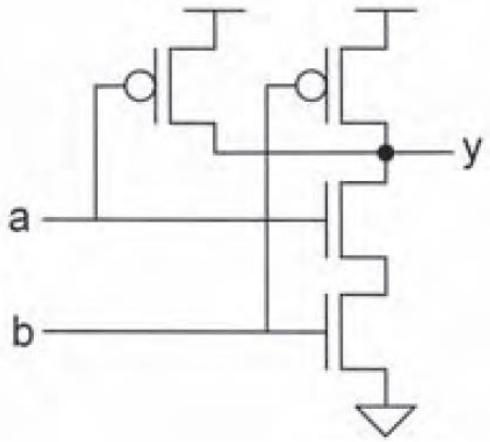
AND =>



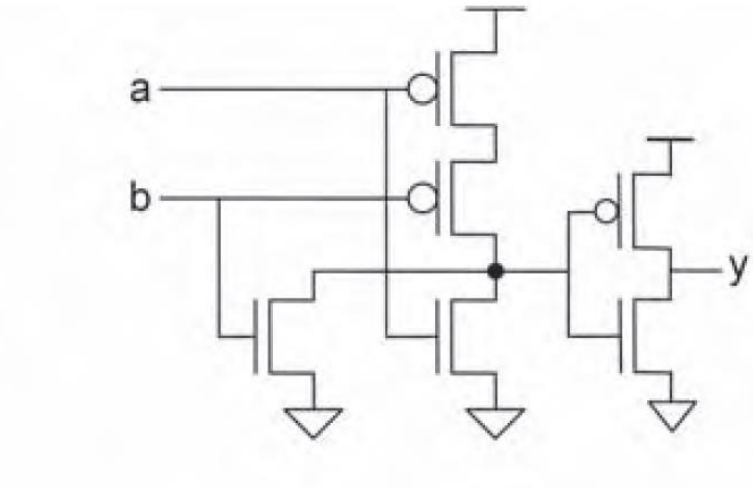
Portas lógicas CMOS – NAND



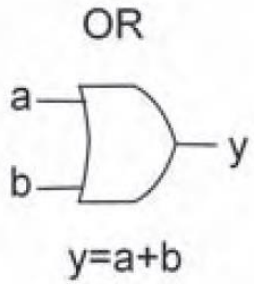
a b	y
0 0	1
0 1	1
1 0	1
1 1	0



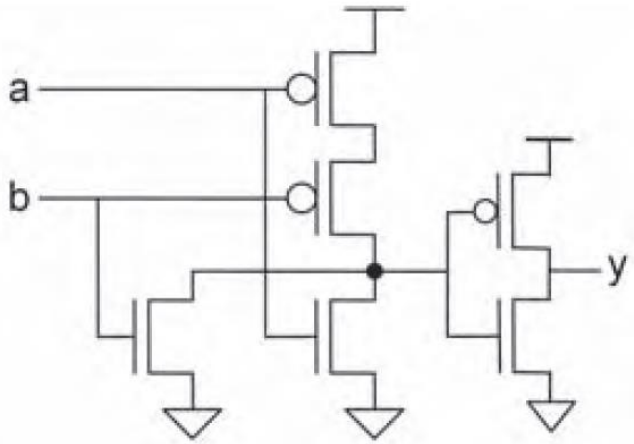
Portas lógicas CMOS – ???



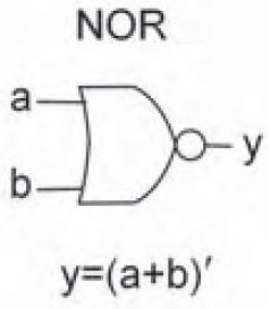
Portas lógicas CMOS – OR



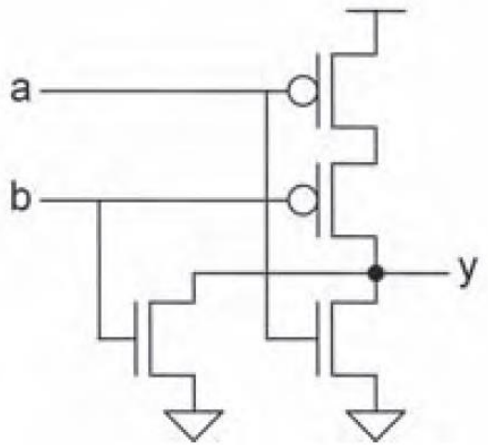
a b	y
0 0	0
0 1	1
1 0	1
1 1	1



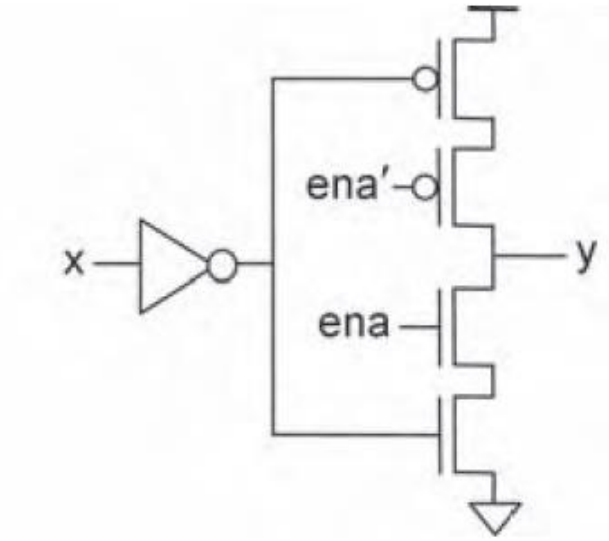
Portas lógicas CMOS – NOR



a b	y
0 0	1
0 1	0
1 0	0
1 1	0

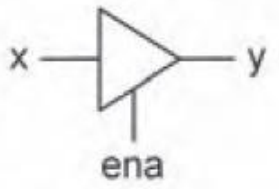


Buffer Tri-state



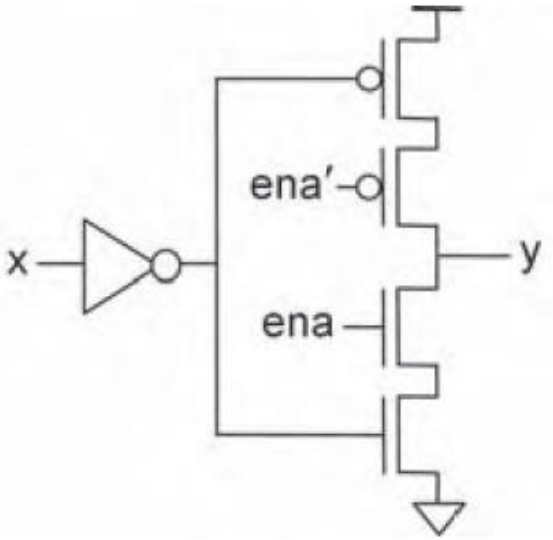
Buffer Tri-state

Tri-state buffer

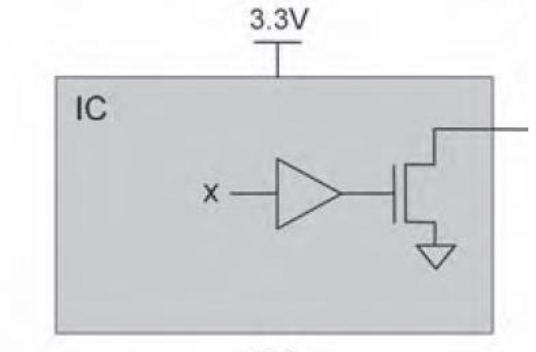


$y = ena' \cdot Z + ena \cdot x$

ena	y
0	Z
1	x

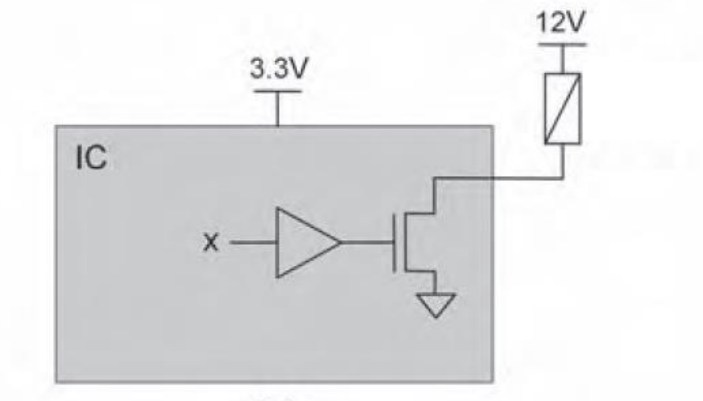


Saída Dreno Aberto – *Open Drain*



Saída Dreno Aberto – *Open Drain*

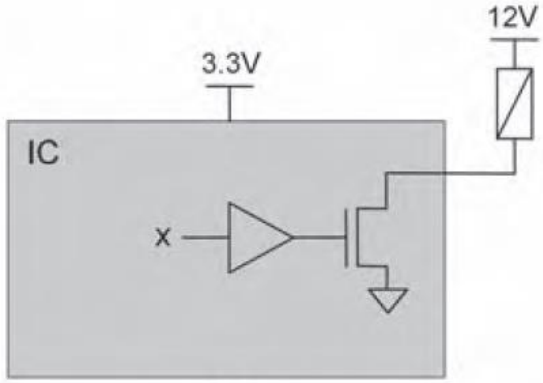
Resistor Pull-up



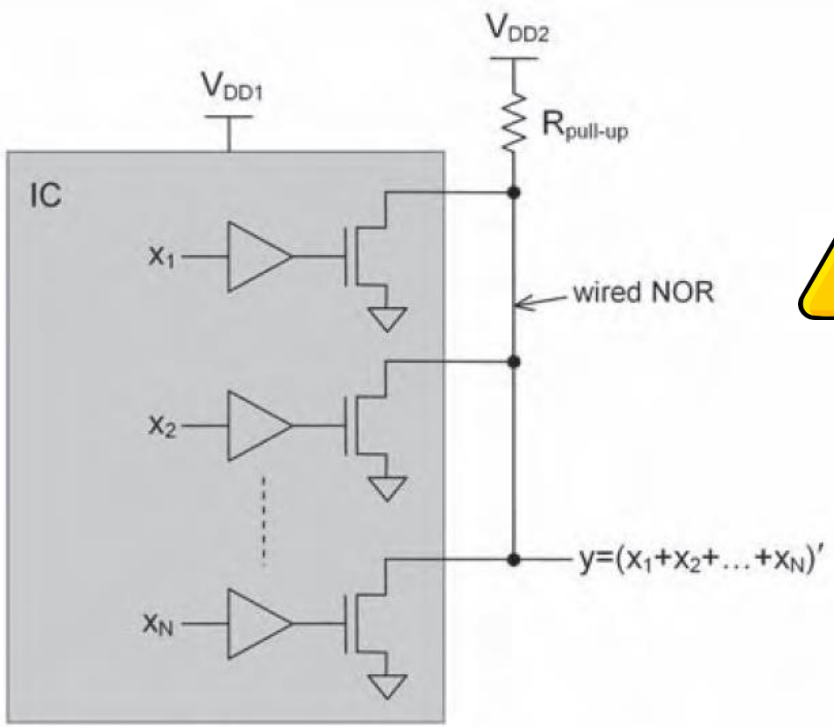
Saída Dreno Aberto – *Open Drain*

Saída invertida
(em relação a x)

Resistor Pull-up

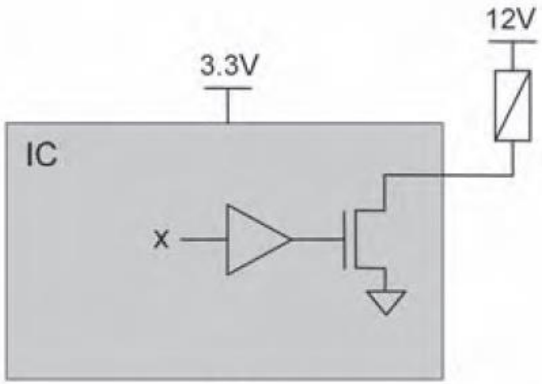


Saída Dreno Aberto – *Open Drain "wired NOR"*

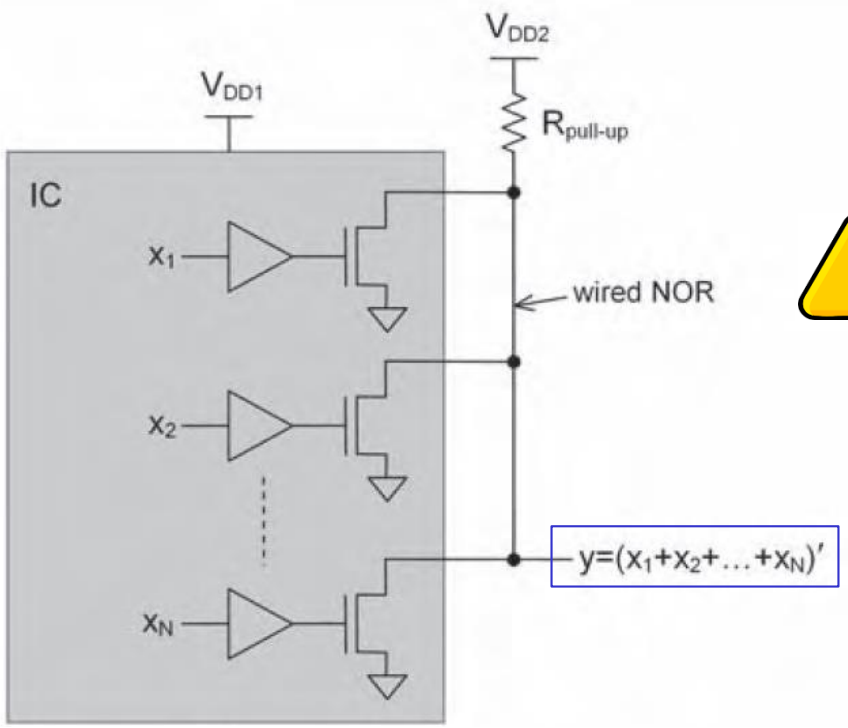


Saída invertida
(em relação a x)

Resistor Pull-up

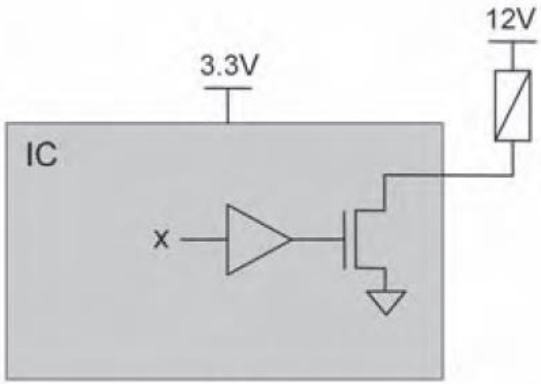


Saída Dreno Aberto – *Open Drain "wired NOR"*



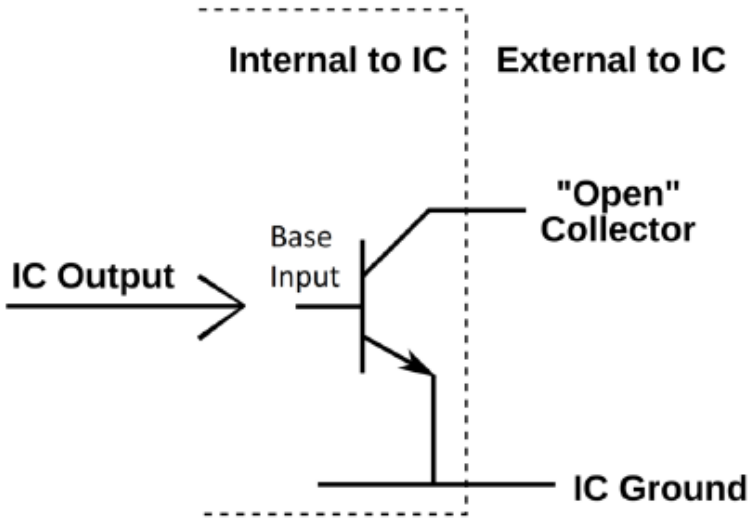
Saída invertida
(em relação a x)

Resistor Pull-up

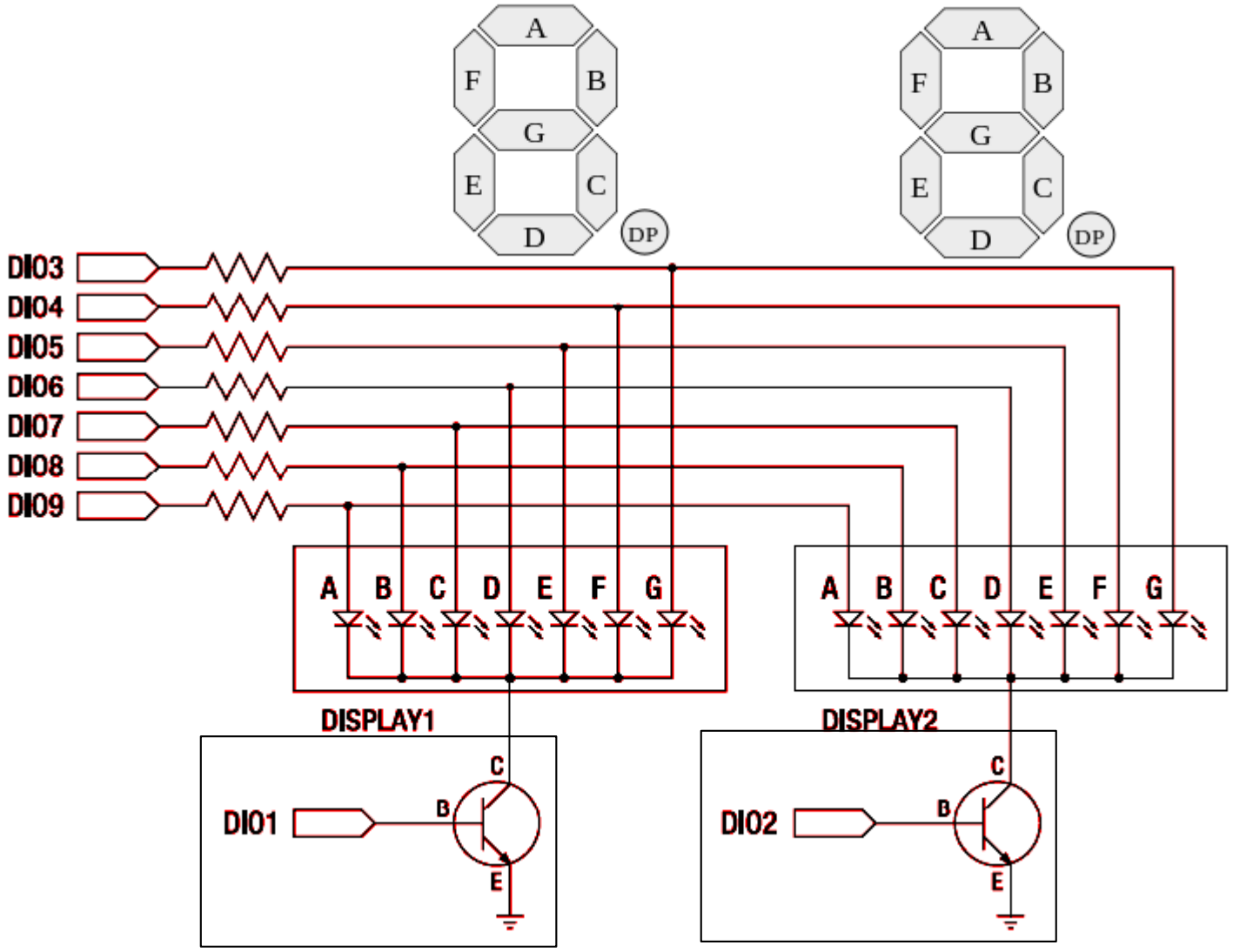


- Wired NOR
- Wired AND
- Múltiplas sinalizações (por ex.: interrupções – ver coletor aberto)

Existe também o Coletor Aberto

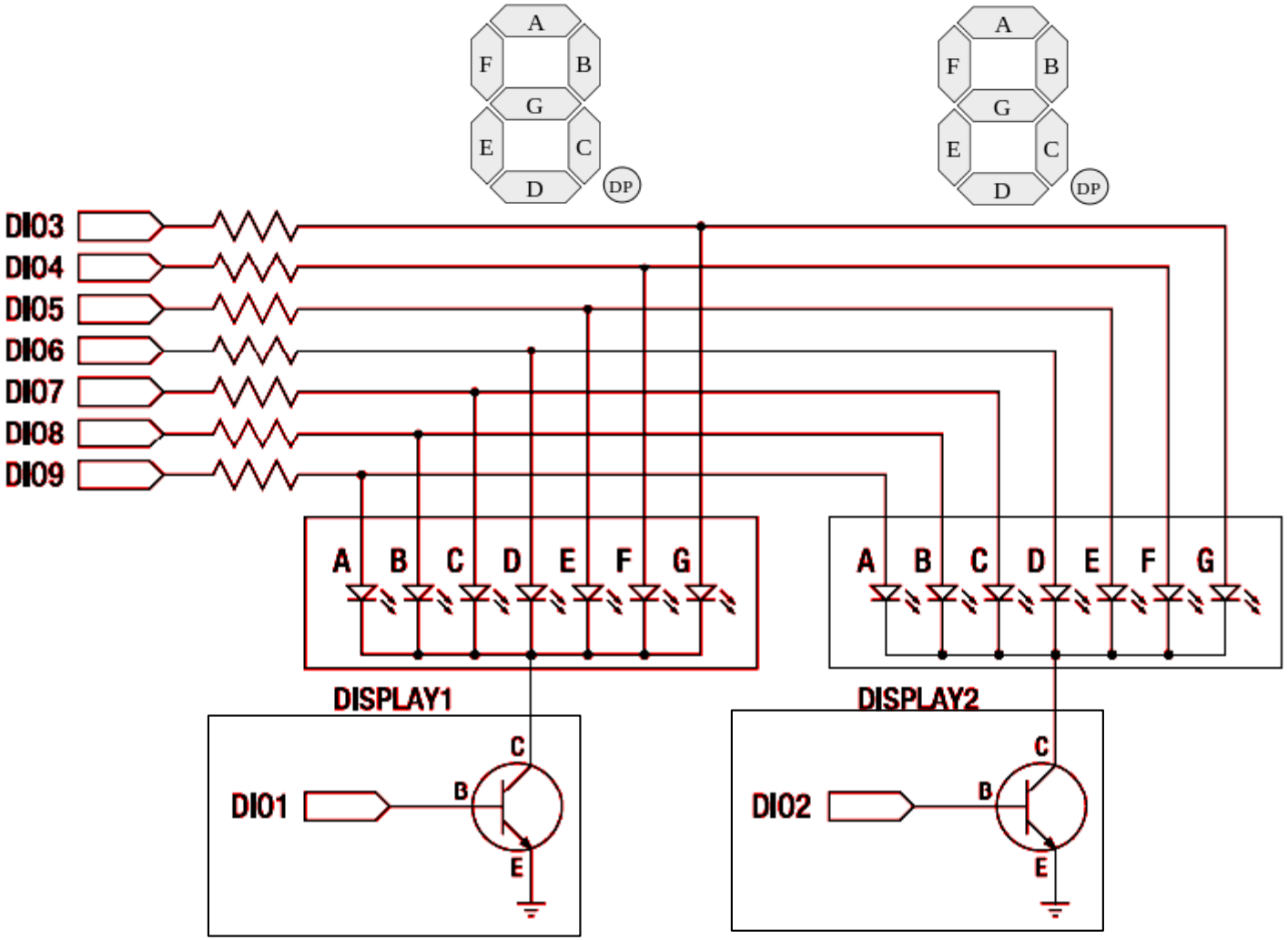


Ex.: Coletor Aberto – Habilitar SSD



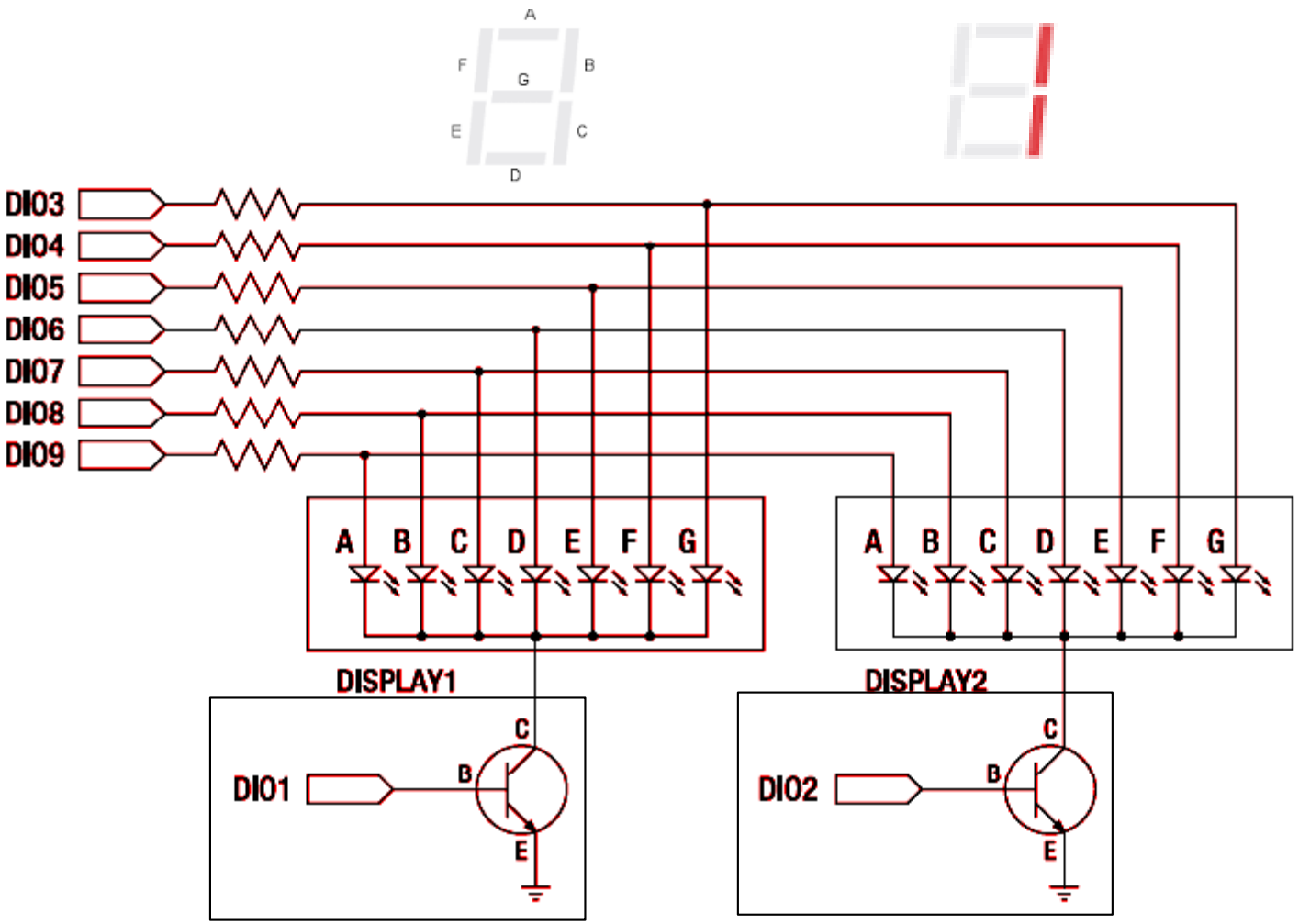
O que exibem os displays?

Di01 = 0
Di02 = 1
Di03 = 0
Di04 = 0
Di05 = 0
Di06 = 0
Di07 = 1
Di08 = 1
Di09 = 0

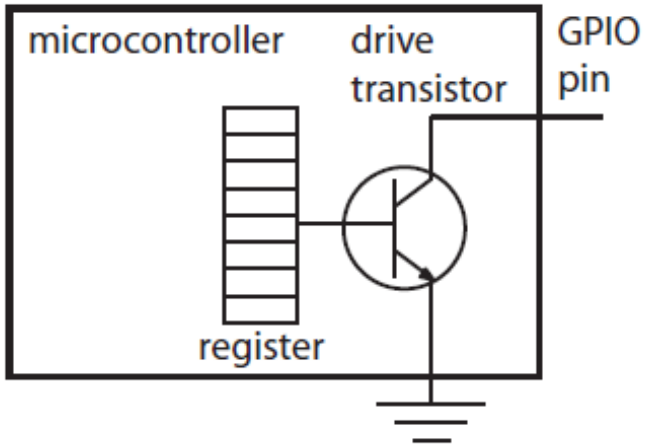


O que exibem os displays?

Di01 = 0
Di02 = 1
Di03 = 0
Di04 = 0
Di05 = 0
Di06 = 0
Di07 = 1
Di08 = 1
Di09 = 0

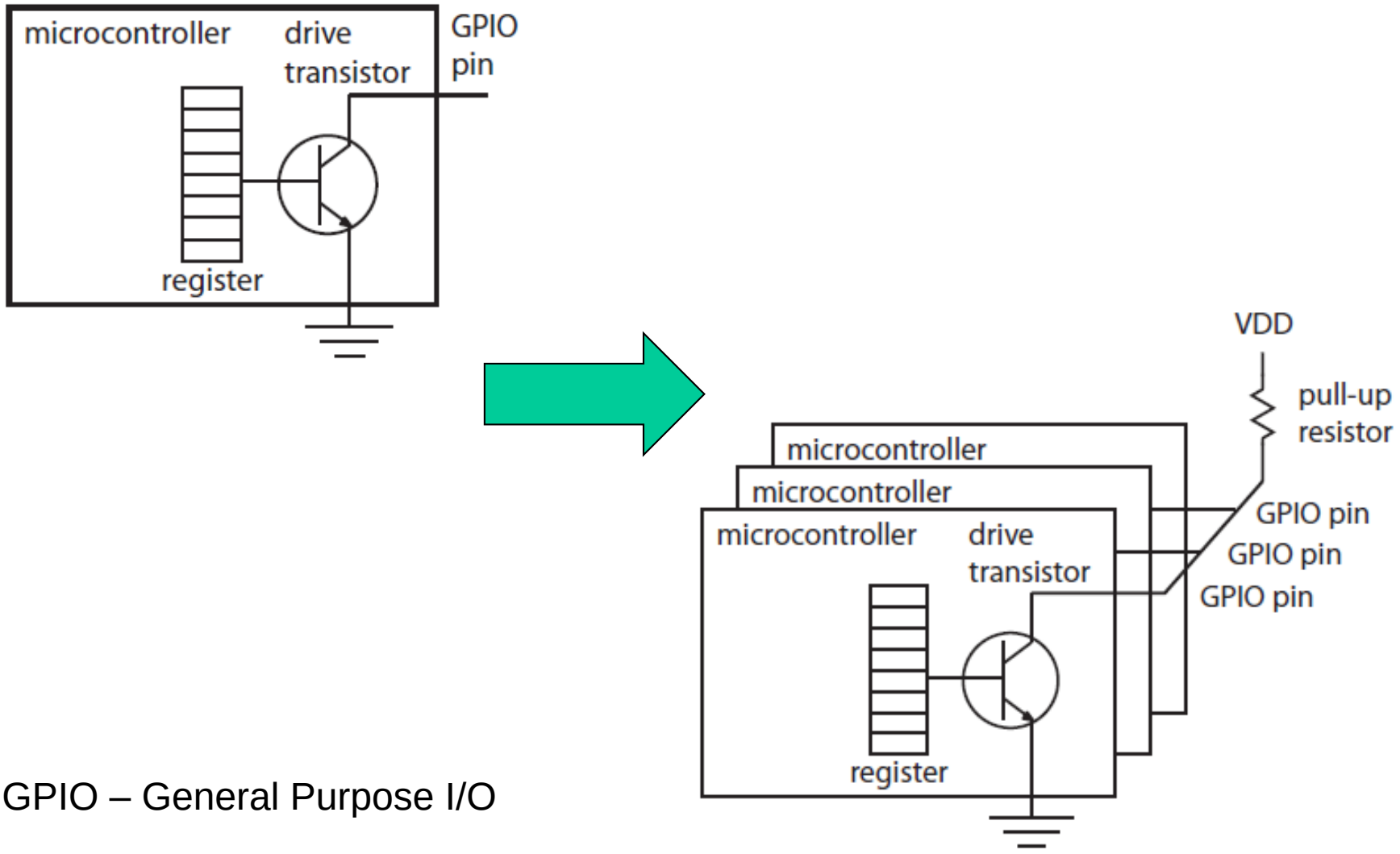


Ex.: Coletor Aberto – Conexão a linha compartilhada



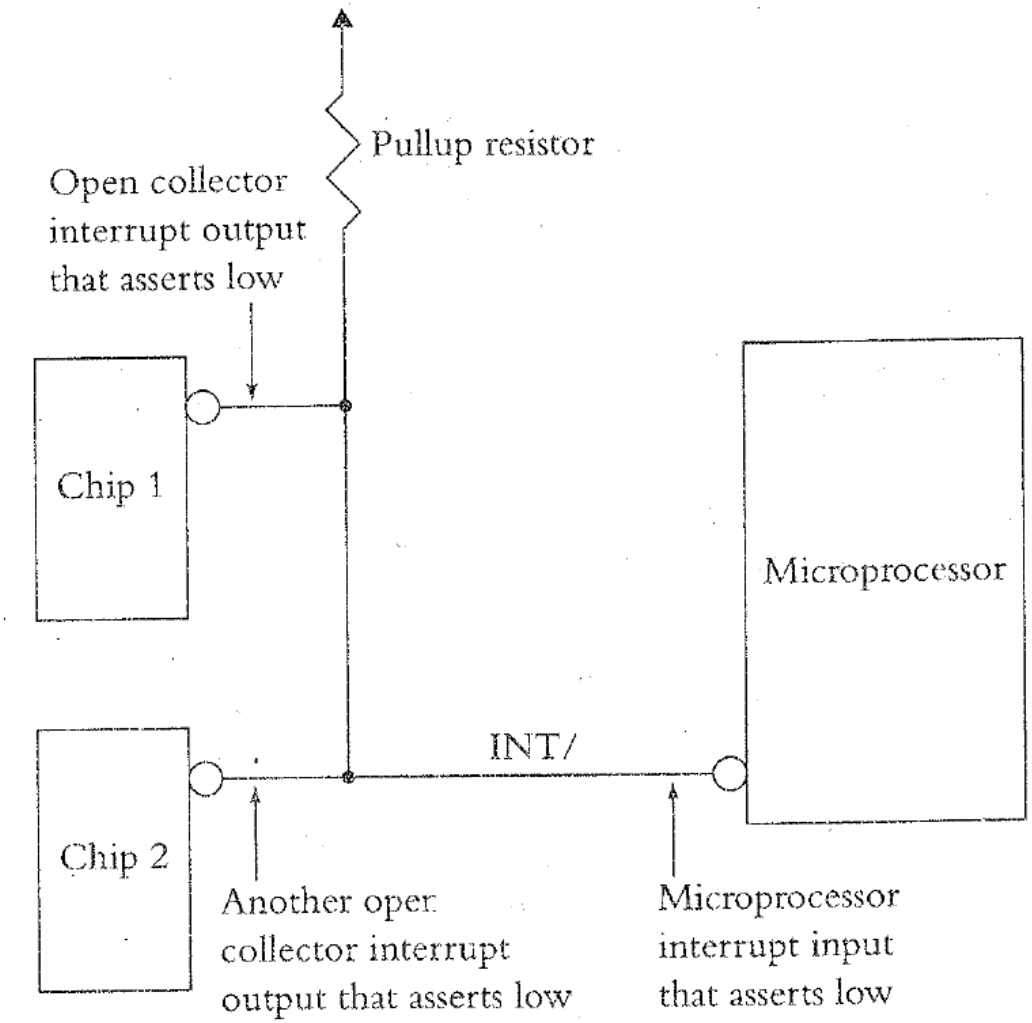
GPIO – General Purpose I/O

Ex.: Coletor Aberto – Conexão a linha compartilhada



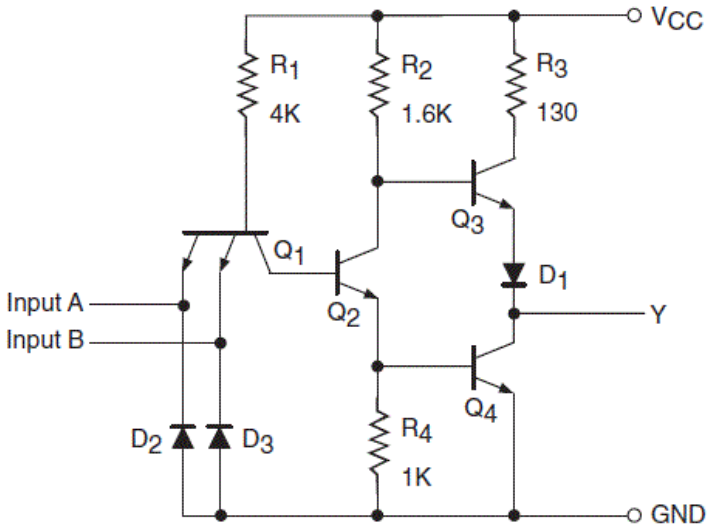
GPIO – General Purpose I/O

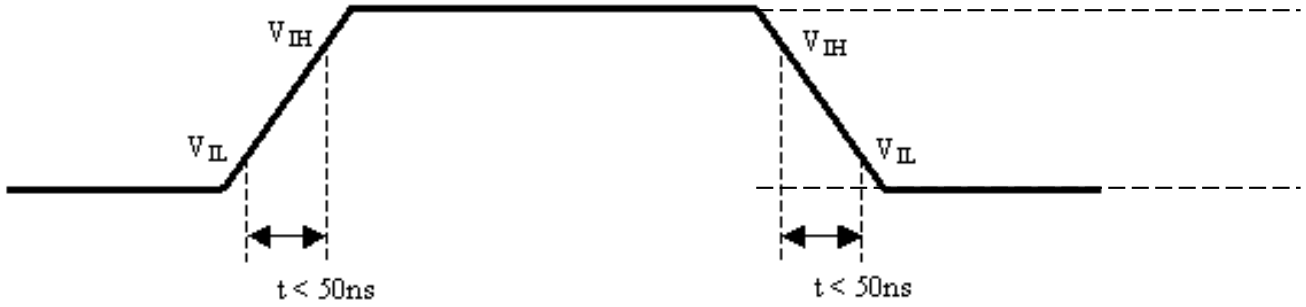
Ex.: Coletor Aberto – linhas de interrupção compartilhadas

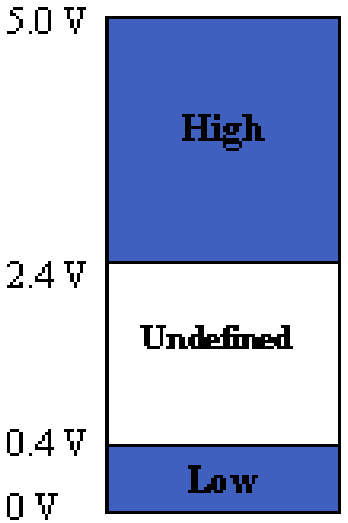


Níveis de tensão x Níveis lógico

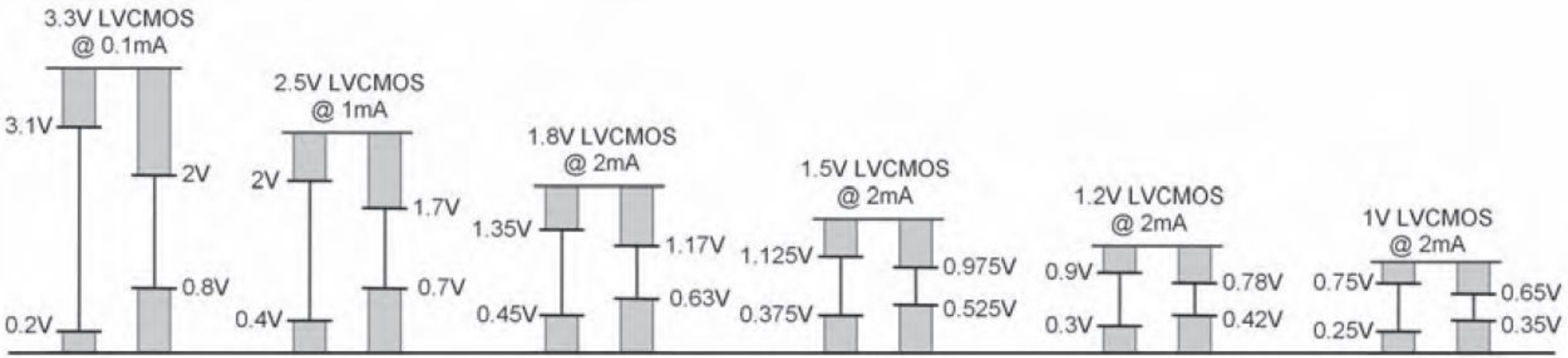
Níveis de tensão x Níveis lógico - TTL





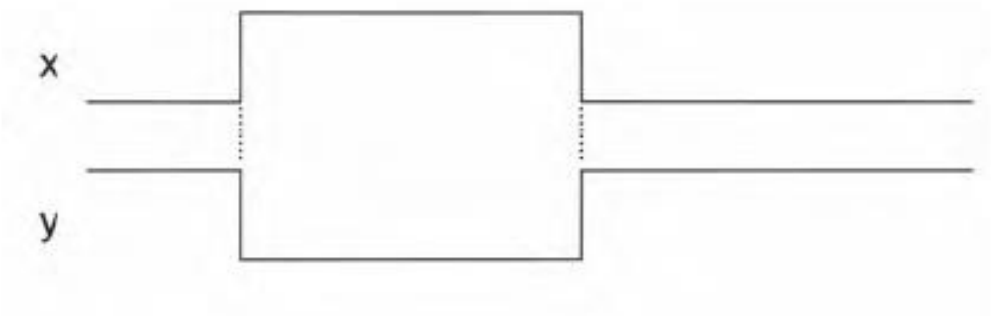


Níveis de tensão x Níveis lógico - CMOS



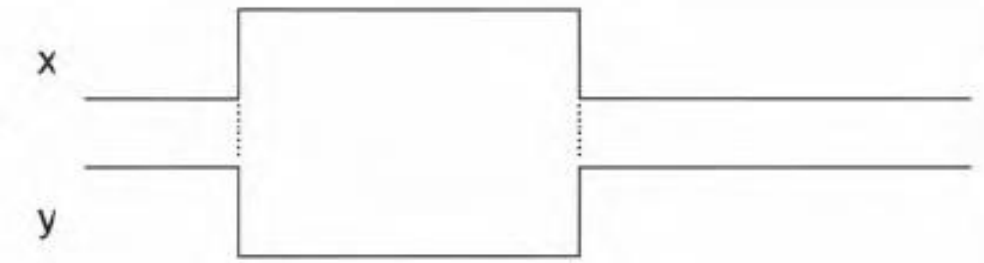
Diagramas temporais

1 – Ideal

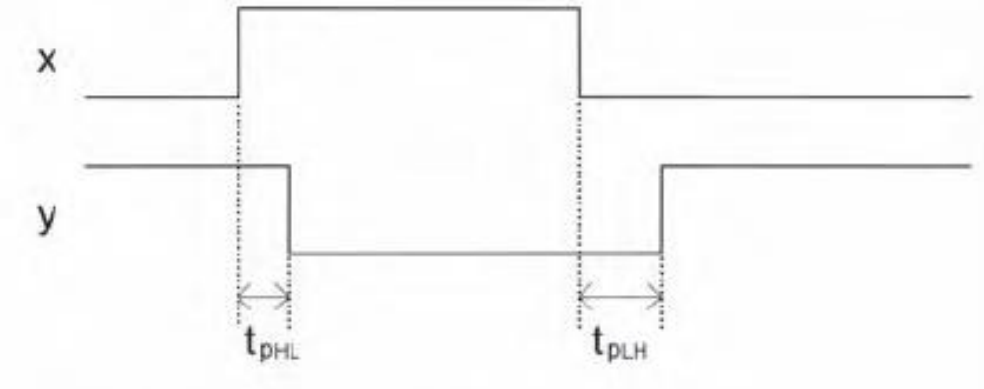


Diagramas temporais

1 – Ideal

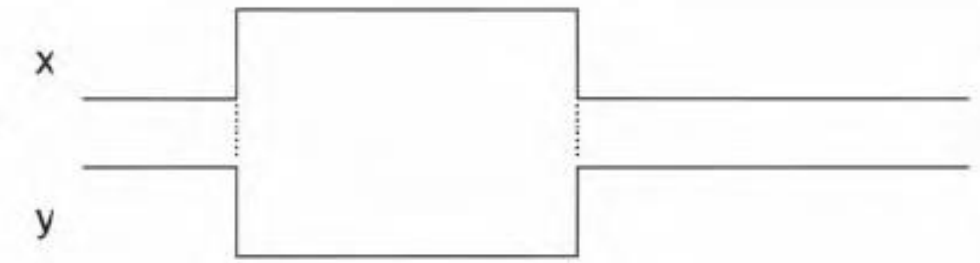


2 – Atraso

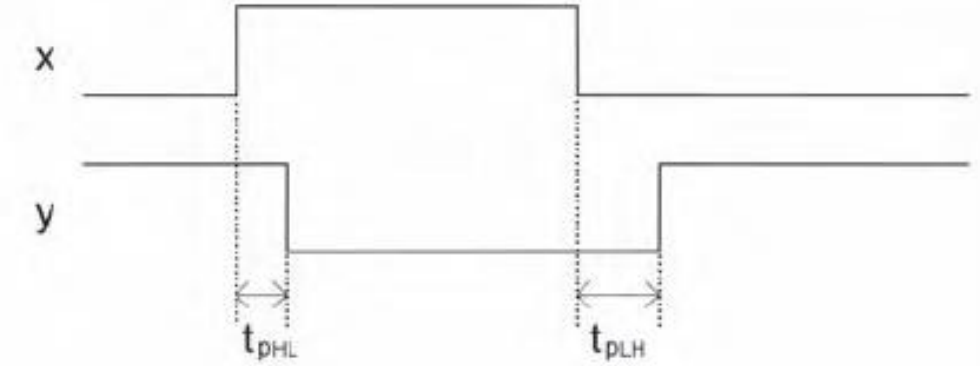


Diagramas temporais

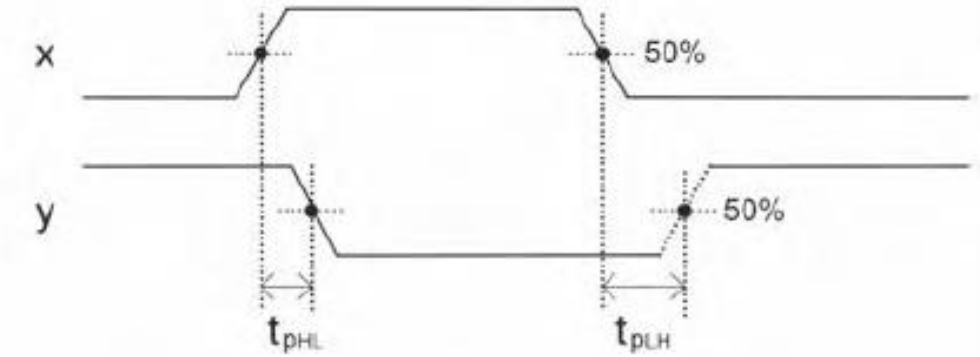
1 – Ideal



2 – Atraso



3 – *Slew Rate*



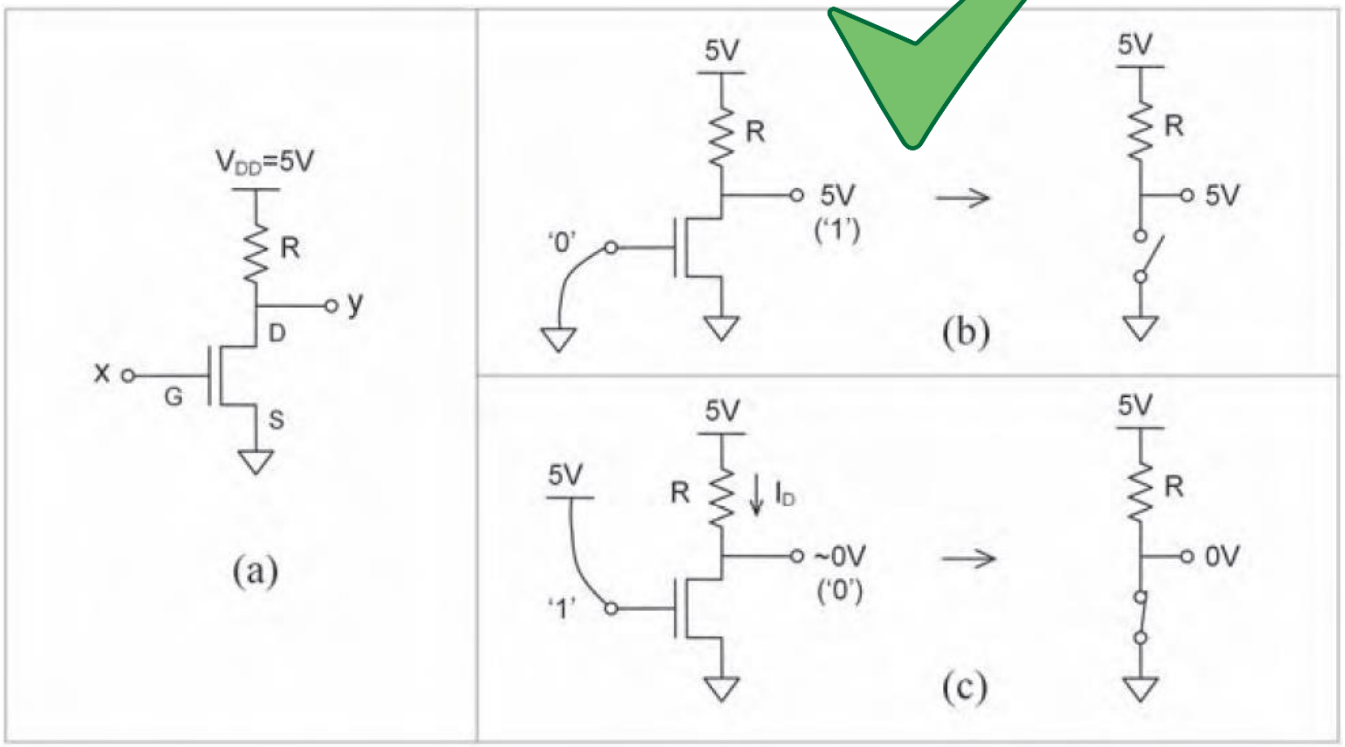
Consumo de Energia

Consumo de energia

$$P_T = P_{static} + P_{dynamic}$$

Consumo de energia - MOSFET

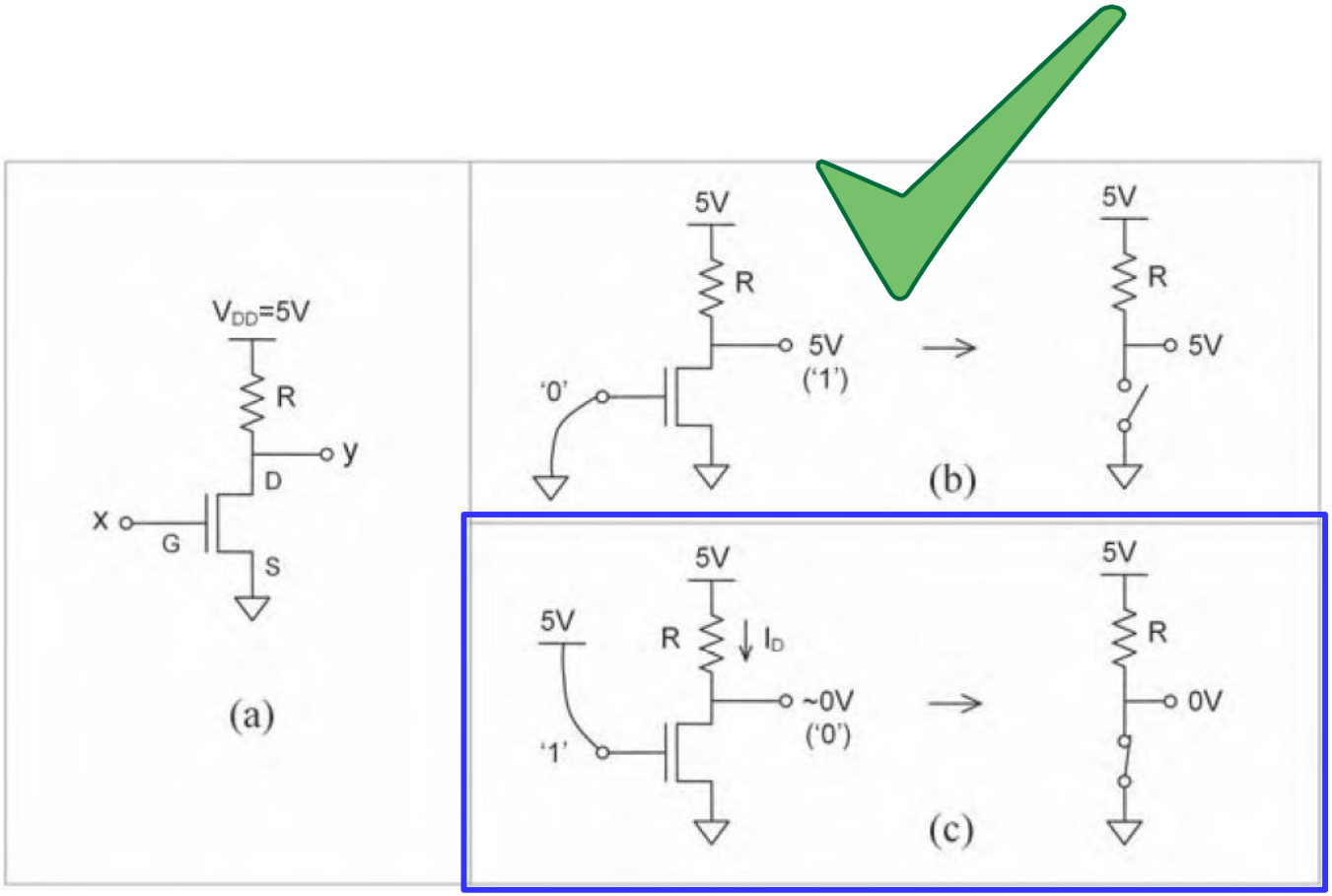
$$P_T = P_{static} + P_{dynamic}$$



P = 0 W

Consumo de energia - MOSFET

$$P_T = P_{static} + P_{dynamic}$$

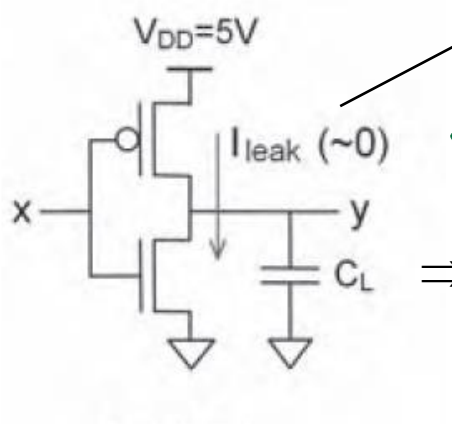


P = 0 W

P = V_{DD} x I_D

Consumo de energia - CMOS

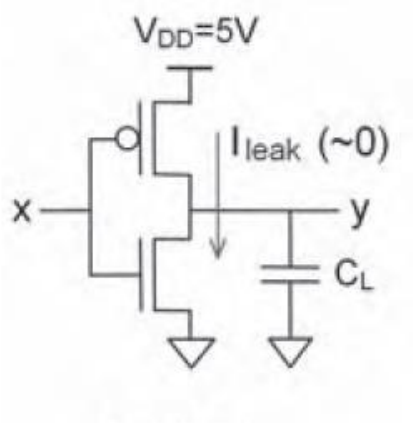
$$P_T = P_{static} + P_{dynamic}$$

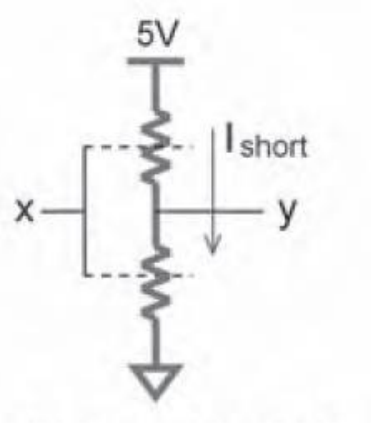


⇒ Capacitância equivalente do circuito de saída

1 – Idle

Consumo de energia - CMOS



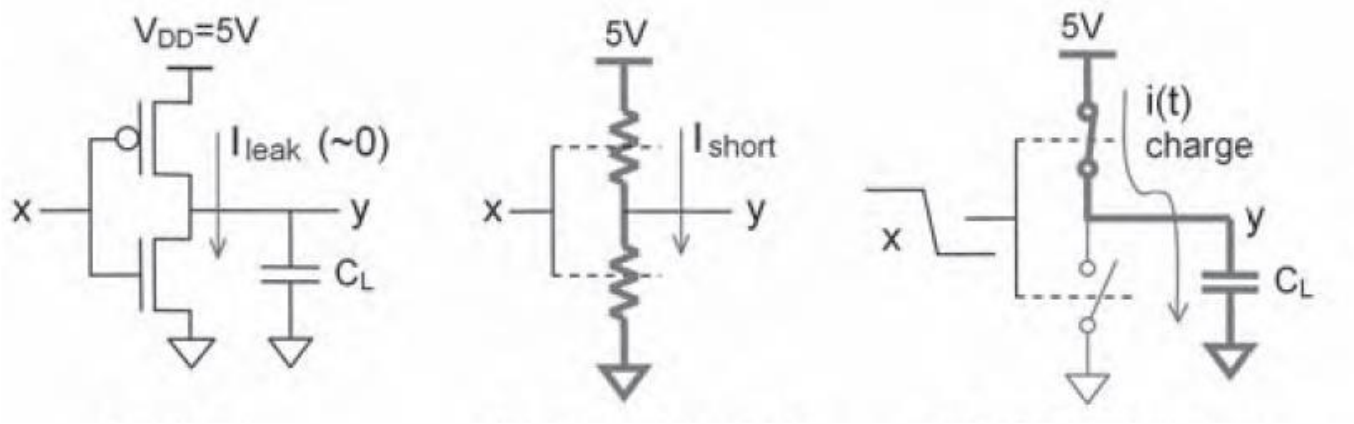


$$P_{short} = \frac{1}{T}\int_0^T V_{DD} \times I_{short}$$

1 – Idle

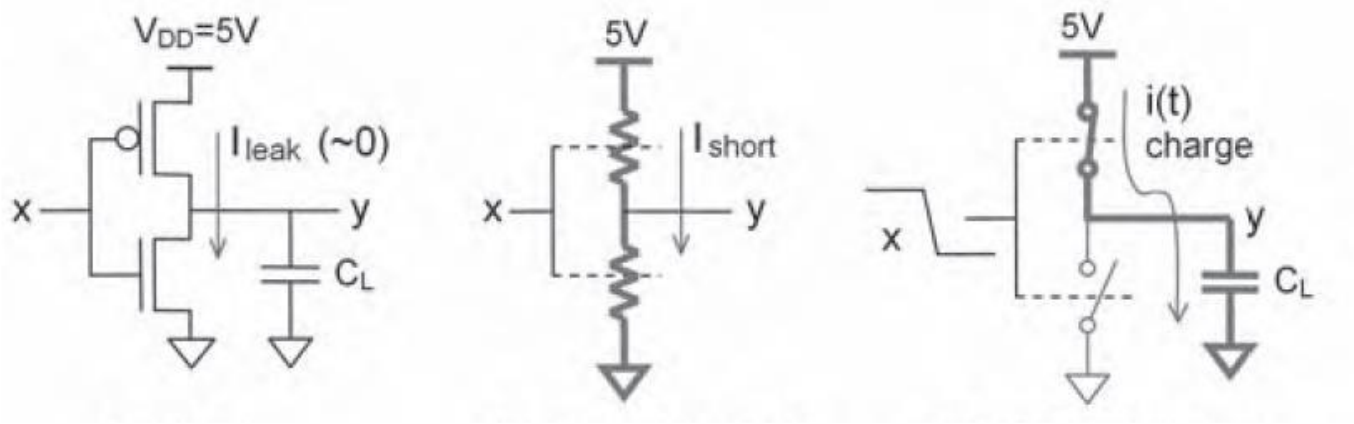
2 – (Des)ligando

Consumo de energia - CMOS



1 – Idle 2 – (Des)ligando 3 – Carga do capacitor

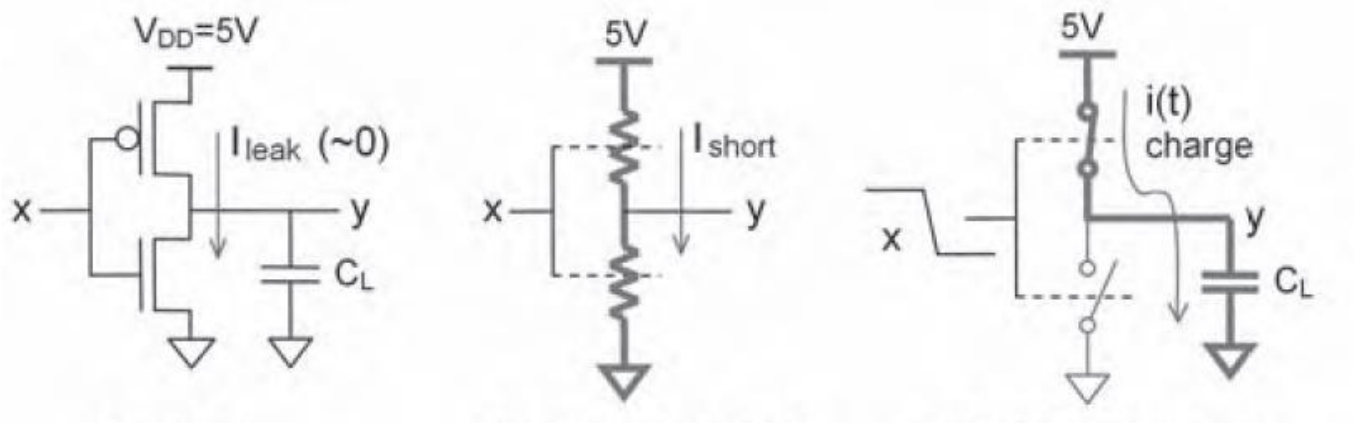
Consumo de energia - CMOS



1 – Idle 2 – (Des)ligando 3 – Carga do capacitor

$$P_{dynamic} = P_{short} + P_{cap}$$

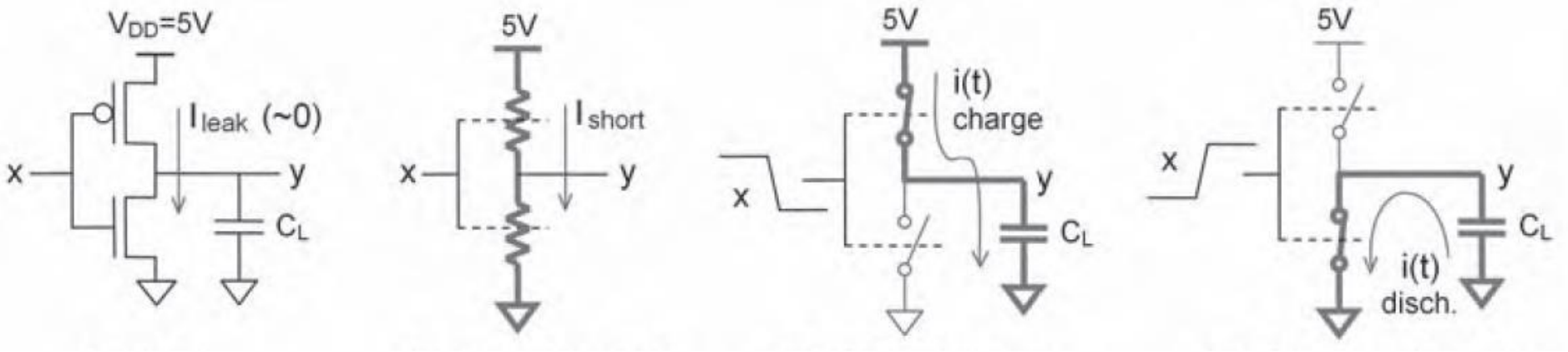
Consumo de energia - CMOS



1 – Idle 2 – (Des)ligando 3 – Carga do capacitor

$$P_{cap} = \frac{1}{T}\int_0^T v(t)i(t)dt = \frac{1}{T}\int_0^T V_{DD}i(t)dt = \frac{V_{DD}}{T}\int_0^T i(t)dt = \frac{V_{DD}}{T}\cdot C_L V_{DD} = C_L V_{DD}^2 f$$

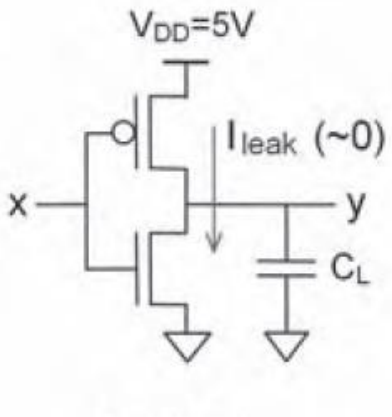
Consumo de energia - CMOS

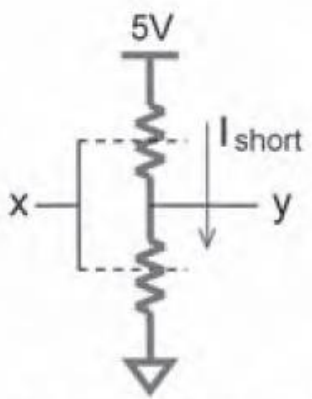


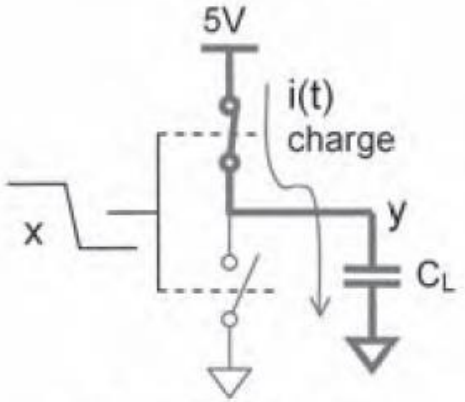
1 – Idle 2 – (Des)ligando 3 – Carga do capacitor 4 – Descarga

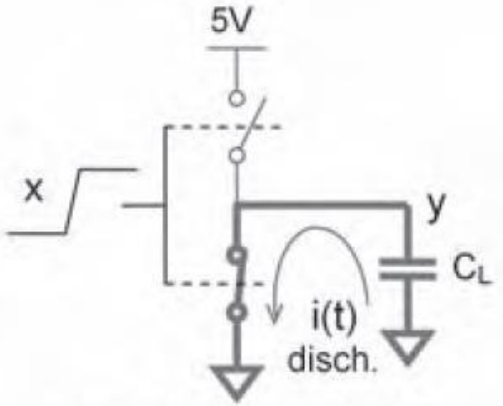
$$P_{cap} = 0$$

Consumo de energia - CMOS





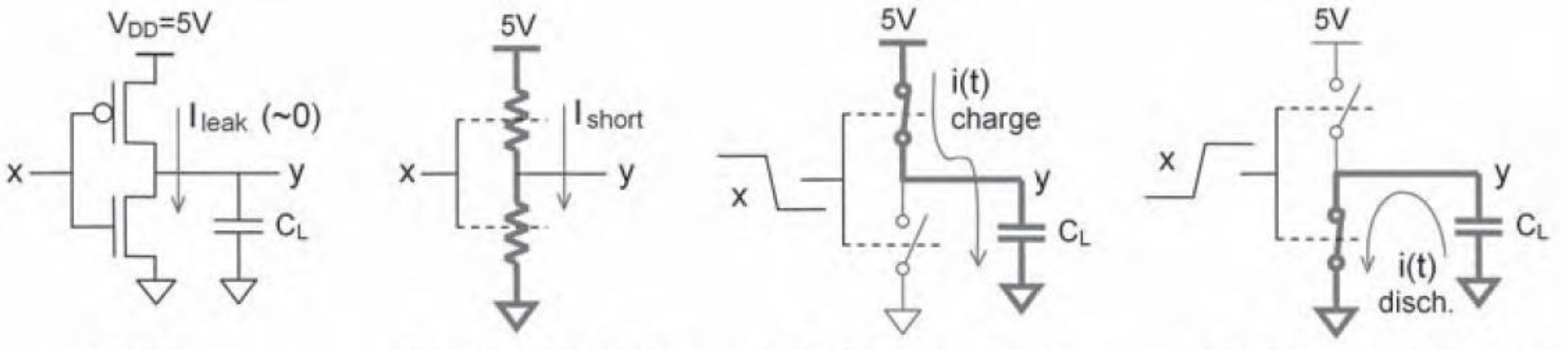




1 – Idle 2 – (Des)ligando 3 – Carga do capacitor 4 – Descarga

$$P_{dynamic} = P_{short} + P_{cap}$$

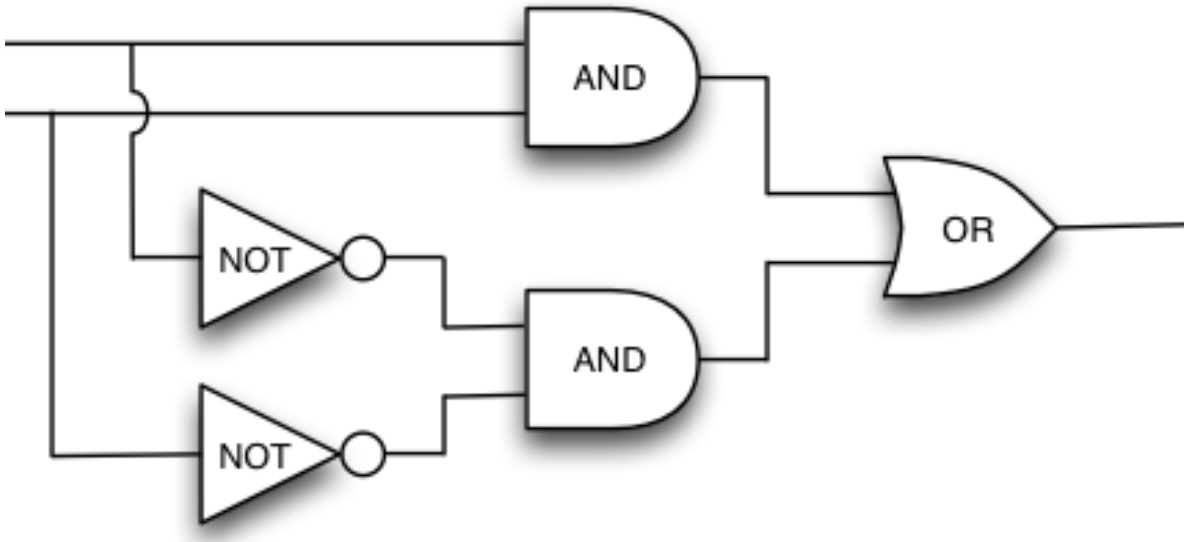
Consumo de energia - CMOS



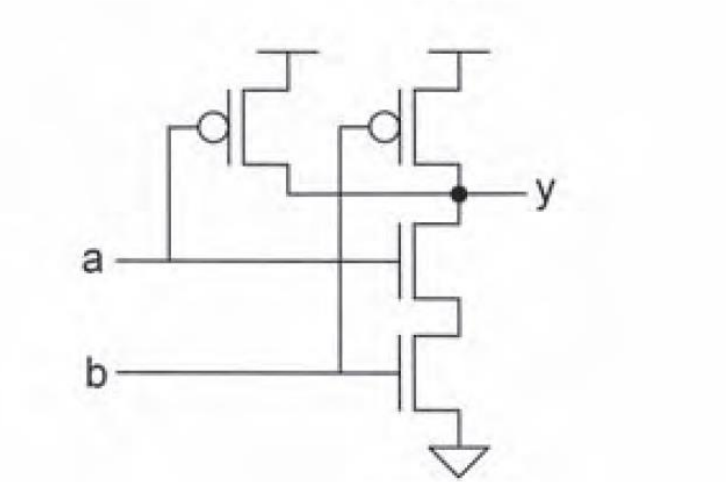
1 – Idle 2 – (Des)ligando 3 – Carga do capacitor 4 – Descarga

$$P_{dynamic} = C_{Leq} V_{DD}^2 f$$

Fan-in & Fan-out

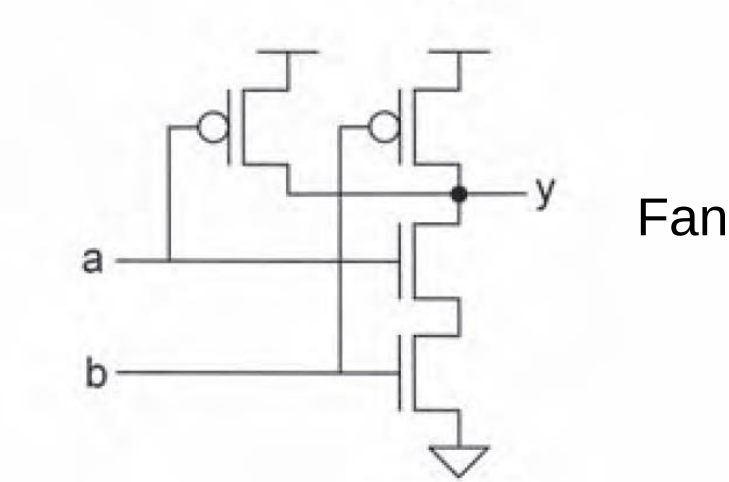


Fan-in



Número de entradas de uma porta lógica.

Fan-in

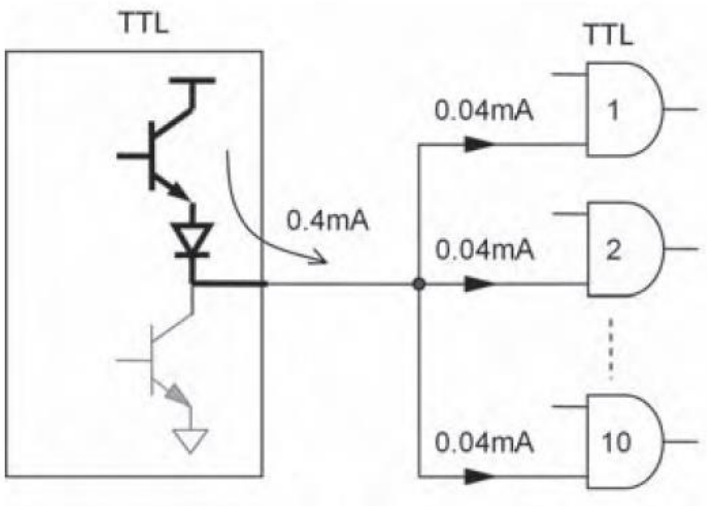


Fan-in = 2

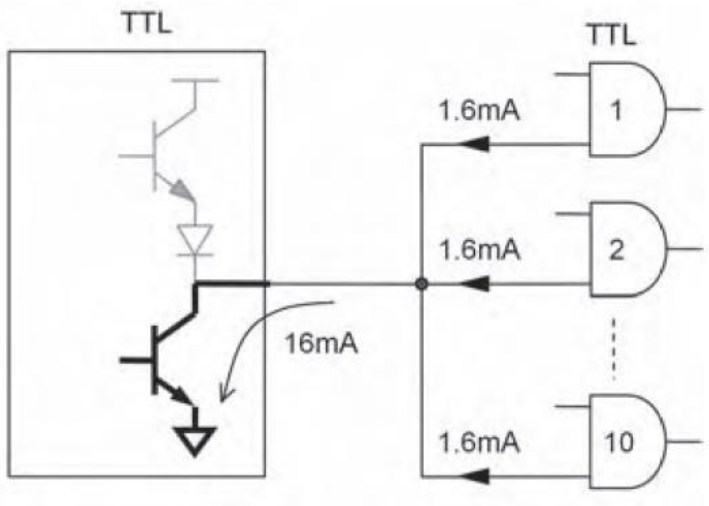
Número de entradas de uma porta lógica.

Fan-out

“ON”

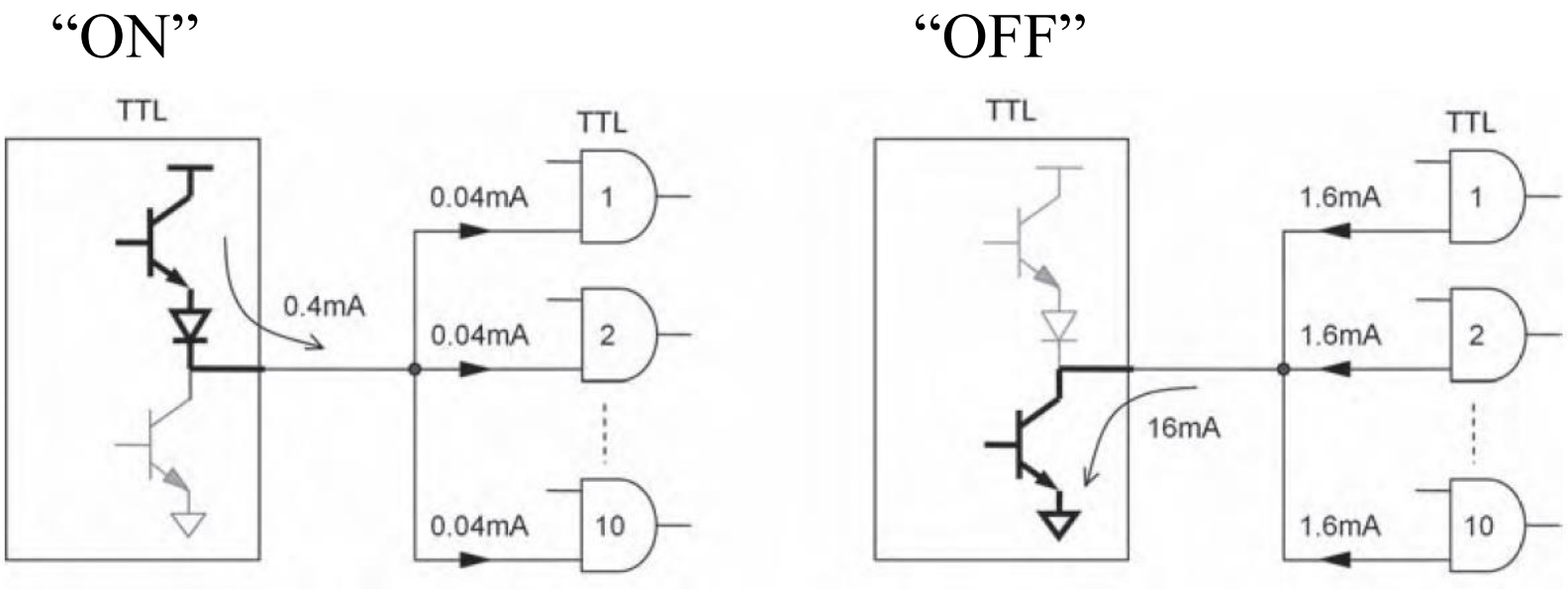


“OFF”



Número de entradas que uma saída de porta lógica suporta.

Fan-out

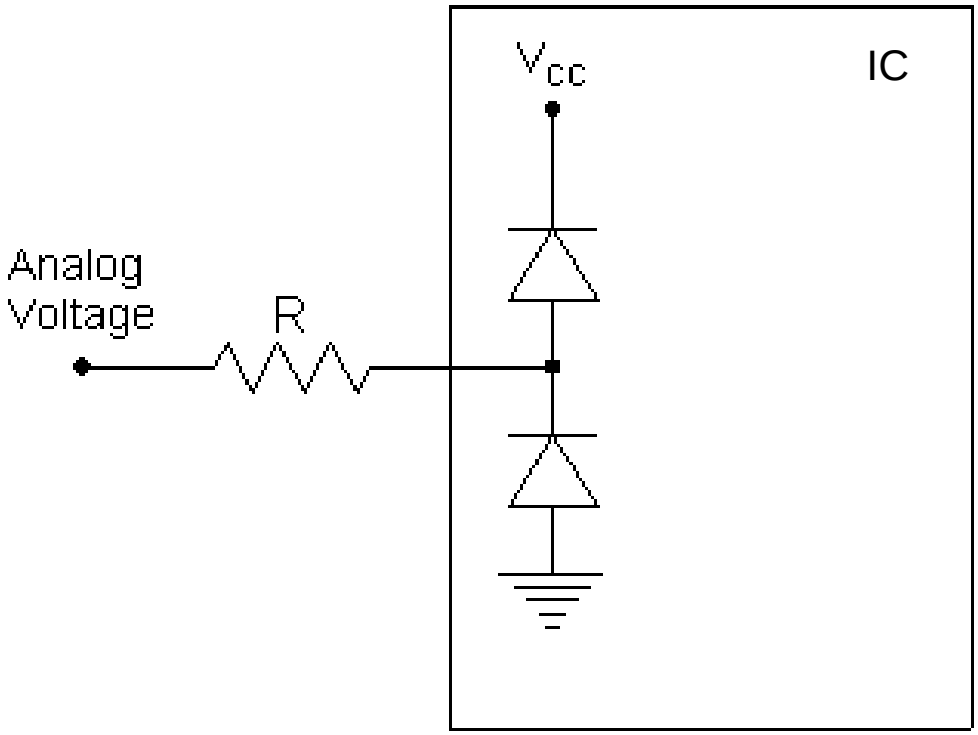


Número de entradas que uma saída de porta lógica suporta.

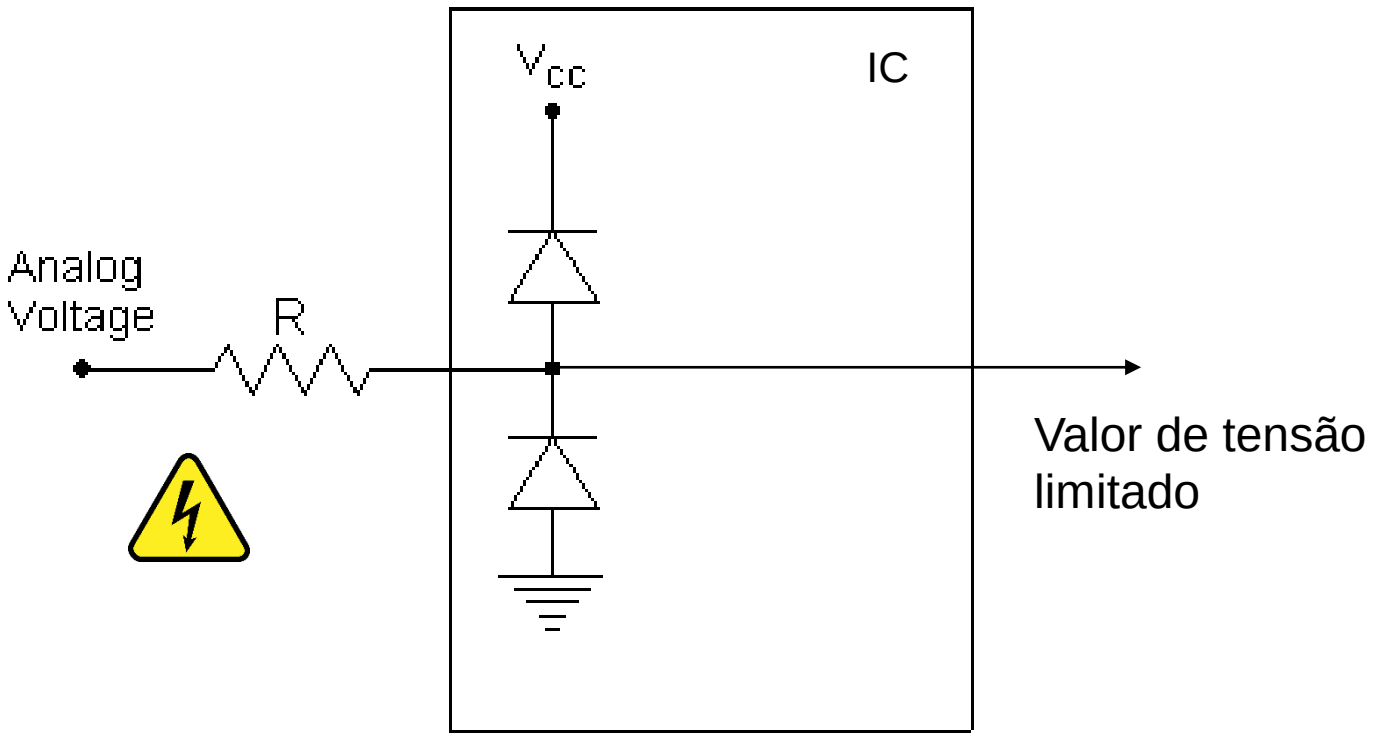
Fan-out = 10

IMPORTANTE: Proteção de E/S !!!

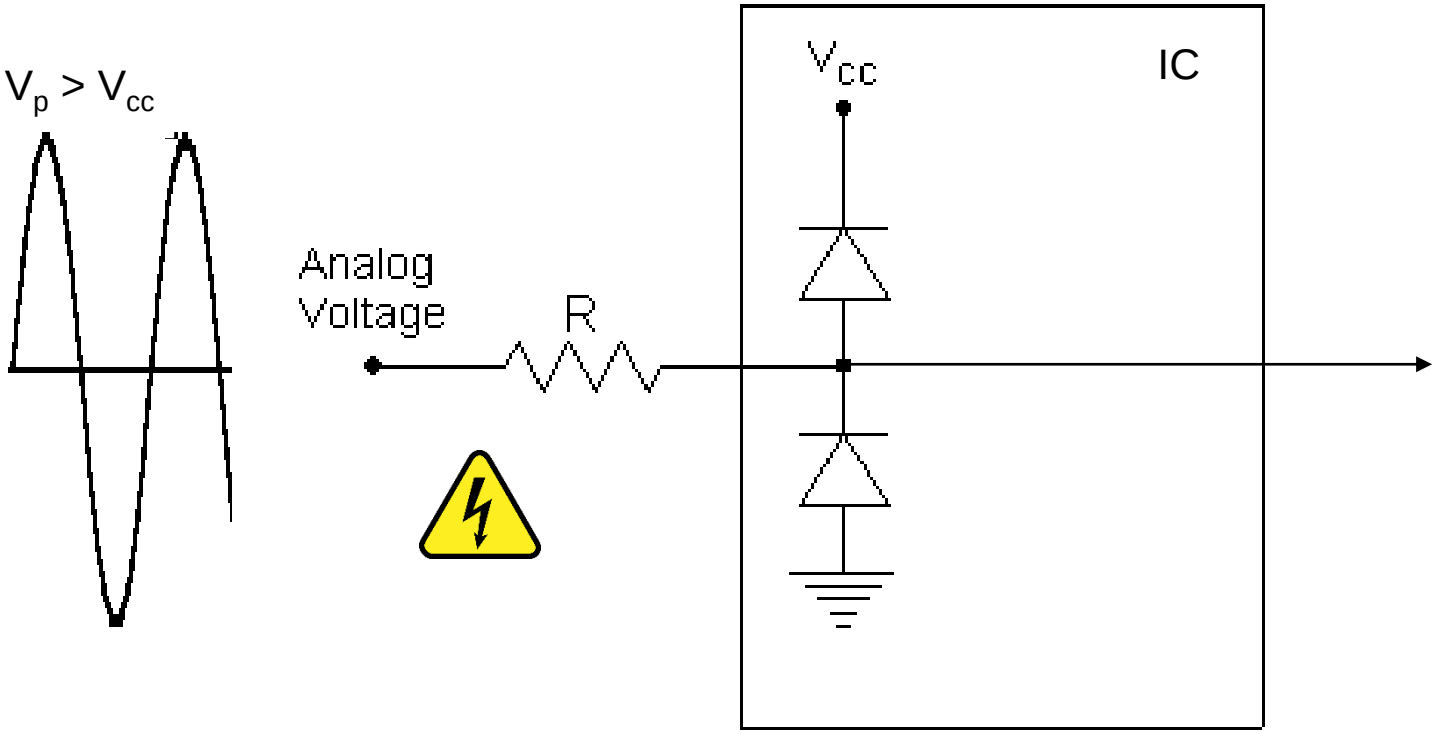
Proteção de E/S com Diodos



Proteção de E/S com Diodos



Proteção de E/S com Diodos



Proteção de E/S com Diodos