Chapter 6: Coincidence Detection Electronics

Experiments in quantum optics utilizing entangled photons rely on the coincident detection of two or more photons. Some experiments of this type use combinations of time-to-amplitude converters (TAC) and single-channel analyzers (SCA) to detect coincident signals from the photodetectors[5, 6, 10]. The TAC/SCA combinations cost several thousand dollars. This chapter describes a fast logic circuit which fulfils the coincidence counting requirements and can be built for under $40. The circuit is designed to receive $25ns$ TTL signals and detect coincidences in a $25ns$ window. The output signals are designed to be $250ns$ TTL pulses. The coincidence window is not adjustable, but a similar circuit with a different coincidence window is easy to design. Additionally, the design of this circuit can be extended to detect pairs of coincidences between more than two inputs.

A circuit was built according to this design and tests showed it had a coincidence window of between $18ns$ and $30ns$. The output signals where clear and should be easy to count, with a digital counting card for example. The following sections document the design, construction, and performance of the coincidence circuit.

6.1 Design

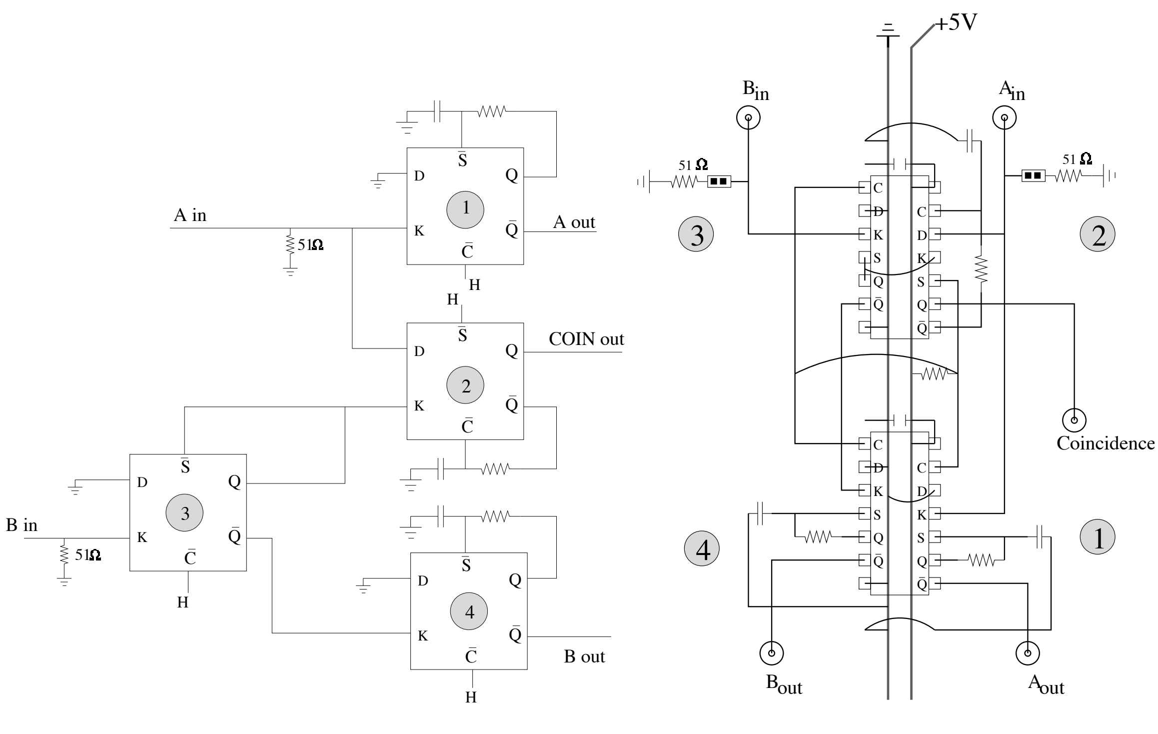
The design for this circuit was published in 2002 by Dehlinger and Mitchell[7]. The only changes from their design to the one described here are two capacitors added for power stability[41]. A schematic is shown in Fig. 6.1(a). The circuit consists of two 74ACT74 dual D-type positive edge-triggered flip-flops, or 4 flip-flops total. Input pulses terminate into a 50Ω load as required by the photodetectors.

Chips 1 and 4 simply relay a pulse received on K to $\overline{Q}$. The duration of the pulse from $\overline{Q}$ depends on the time constant of the RC combination between Q and $\overline{S}$, which for the resistor and capacitor chosen is $1k\Omega \cdot 220pF = 220ns$. This pulse duration should be easy to count with a computer data acquisition card.

Chip 3 in the circuit delays the signal at B_{in} for the time needed to clock and reset, typically $13ns$, with a minimum of $6.5ns$ and maximum of $19.5ns$[42]. In the case of coincident input, the signal from A_{in} sets D on chip 2 to HIGH before the rising pulse from the delayed B_{in} triggers the circuit. From the truth table (Table 6.1) it is clear that this combination will issue HIGH on Q, the coincidence output. The RC reset on chip 2 determines the length of the coincidence signal as in chips 1 and 4. Coincidence detection can only occur while A_{in} is HIGH, so the coincidence window for the $25ns$ input pulses is $25ns$.

Inputs				**Outputs**	
$\overline{\mathrm{S}}_D$	$\overline{\mathrm{C}}_D$	K	D	Q	$\overline{\mathrm{Q}}$
L	H	x	x	H	L
H	L	x	x	L	H
L	L	x	x	H	H
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	x	Q_0	$\overline{\mathrm{Q}}_0$

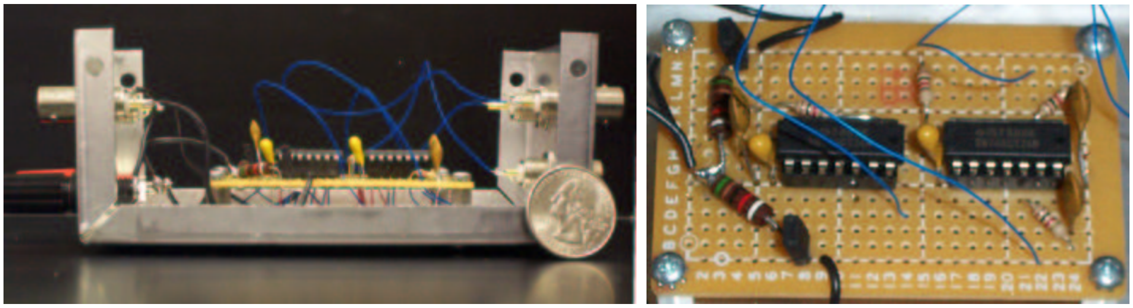
Table 6.1: The truth table for each half of a 74ACT74 logic chip. H, L, $\uparrow$, and x correspond to TTL HIGH, LOW, rising, and immaterial voltages, respectively[42].



(a) A schematic diagram of the coincidence detection circuit. Each square is half a 74ACT74 logic chip. H indicates TTL high, $+5V$.

(b) Diagram of the circuit layout as constructed, including jumpers and additional capacitors across the bus.

Figure 6.1: Two schematic diagrams of the coincidence detection circuit. All capacitors are 220pF except the two across the bus. All resistors are 1kΩ except the two labeled 51Ω.



(a) Side view. (b) Close up.

Figure 6.2: Pictures of the coincidence circuit.

6.2 Construction

The layout of the circuit is shown in Fig. 6.1(b) as assembled on a perforated circuit board with components on top and solder and wiring underneath. Each hole of the board is surrounded by a copper pad to which solder adheres easily. All components are listed in Table 6.2.

The central bus provides stable power and ground to the whole circuit. It was made by soldering two segments of 22 gauge wire to each pad in adjacent rows. By only stripping the portion of the wire to be soldered the wire on the top side remained covered.

The two 14 pin sockets were placed to straddle the bus, and were soldered at each pad. The sockets allow for easy replacement of the logic chips, should it be necessary. A $22\mu F$ capacitor was placed across the bus next to the power pin of each chip to increase power stability. A $1\text{k}\Omega$ was placed between the bus and the connection point for TTL HIGH for chip protection.

Twenty-two gauge wire was chosen for A_{in} and B_{in}, but that choice was unimportant. All remaining wires are 30 gauge because the interconnection soldering is tight and would be difficult to manage with large wire. The wires for the output signals were threaded back up through the board so that any strain is put on the sheathed portion of the wire instead of the connections.

The 51Ω terminations on the inputs are the necessary load required by the photodetectors, but are inhibitory during testing of the circuit. They were joined to the inputs through jumpers so that the terminations can be disconnected by removing the jumper caps.

The completed circuit is mounted inside a metal box to provide electromagnetic shielding and mounts for BNC and banana jacks. The input and output signals travel on BNC cables and the power comes through banana jacks. The connecter holes were drilled with a drill press and drill bit sizes $\frac{25}{64}$ and $\frac{5}{16}$ for the BNC and banana jacks, respectively. It was easy to solder wires into the BNC jacks. However, solder did not bond well to the banana jack posts or to the box. In order to avoid the

Item	Qt.	$/item
51Ω resistor	2	< 1
1kΩ resistor	4	< 1
220pF capacitor	3	< 1
22μF @16Vdc capacitor	2	< 1
14-pin socket	2	< 1
74ACT74 logic chip	2	< 1
Jumper pins	2	< 1
Project box	1	3
Perforated circuit board	1	2
Banana jack panel mount	2	1
BNC panel mount	5	1
22 gauge solid wire		
30 gauge solid wire		
	Total	< 40

Table 6.2: Materials used to build the coincidence circuit.

need to solder the bus ground to both a banana post and the box, it would be better to use a special grounding banana jack. Fig. 6.2 shows pictures of the completed circuit.

The following are useful notes for anyone attempting to create a similar circuit.

- It is difficult to strip 30 gauge wire without a wire stripper.

- The stripped portions of any gauge wire are much weaker than the protected portions. The sheath should be kept wherever possible and stripped portions should be bent as little as possible to avoid breaking.

- The 30 gauge wire is easier to solder and more robust if it is inserted into the perf board hole than if it is laid sideways on the board.

- Some of the connections between pins of the socket and the bus can be made without wire, just by connecting the blobs of solder.

- Although some of the components in this circuit were not trimmed short enough to rest on the board, such trimming is a good idea in general since it prevents possible undue strain on the copper pads underneath.

- A special grounding banana jack (instead of insulated) is recommended for the ground connection, to remove the need to solder to both the banana post and the box.

6.3 Performance

The circuit was tested with a HP 8111A 20MHz function generator and an oscilloscope. The function generator can supply a signal which mimics the 25ns TTL signal from a photodetector we expect as input. The function generator is built for 50Ω signal termination. The oscilloscope was able to display the signals on the circuit inputs and outputs, but ringing made it necessary to use a scope probe, with its shielding connected to the circuit's ground.

When the signal from the function generator was connected to A_{in}, A_{out} showed a 250ns pulse, while B_{out} and Coin$_{out}$ remained flat. Connecting the signal to B_{in} produced a 250ns pulse at B_{out}, while A_{out} and Coin$_{out}$ remained flat. When the function generator signal was connected to A_{in} and B_{in} at the same time it was necessary to disconnect a 50Ω termination by removing a jumper, so that the 50Ω load on the function generated was maintained. In this situation, with signal input at both A_{in} and B_{in}, all three outputs showed 250ns pulses.

To make sure that sufficiently separated signals on A_{in} and B_{in} are resolved as not coincident, part of the signal from the function generator was subjected to the propagation delay of a 7408 2-input positive AND gate. The propagation delay for that chip is typically 9ns according to the datasheet. When one input received the signal from the function generator and the other input received the signal delayed through 2 AND gates, there was no coincidence detected. However a delay of 1 AND gate was not enough to prevent coincidence detection. This is direct evidence that the circuit has a coincidence window of between 18ns (signal 9ns away on either side are coincident) and 36ns (signal 18ns away on either side are not). This fits our expectation that the window is 25ns, the length of the signal at A_{in}.

6.4 Summary

The circuit described in this chapter detects coincidences for 25ns 50Ω terminated TTL pulses with a coincidence window of 18ns to 36ns. This is ideal for quantum optics experiments which rely on coincident detection of photons using photodetectors such as the SPCM from Perkin-Elmer. The circuit can be constructed easily and for less than $40, and can be tested using a function generator and oscilloscope. As an end note, this circuit can be easily extended to accommodate three or more input signals, as shown in Fig. 6.3. Quantum optics experiments with a gating detector and two signal detectors are common and would use this extended circuit.

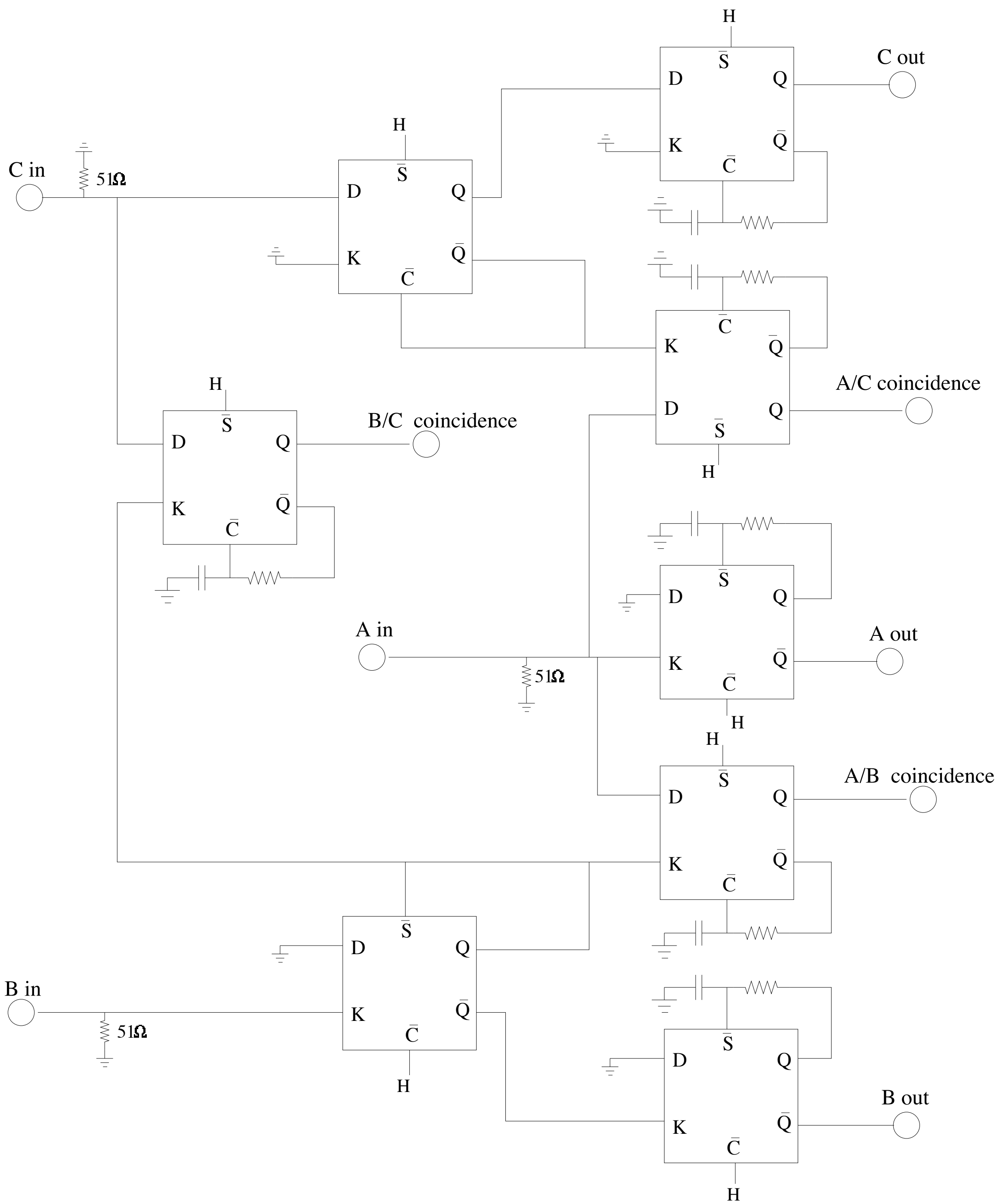


Figure 6.3: The coincidence circuit extended to detect coincidences between pairs of any three inputs.

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