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CORNET TRUSTED-IOT ANNUAL MEETING

16 / 11 / 2023

LOW-POWER FPGA-SOC-BASED SECURE MOBILE ROBOT ARCHITECTURE

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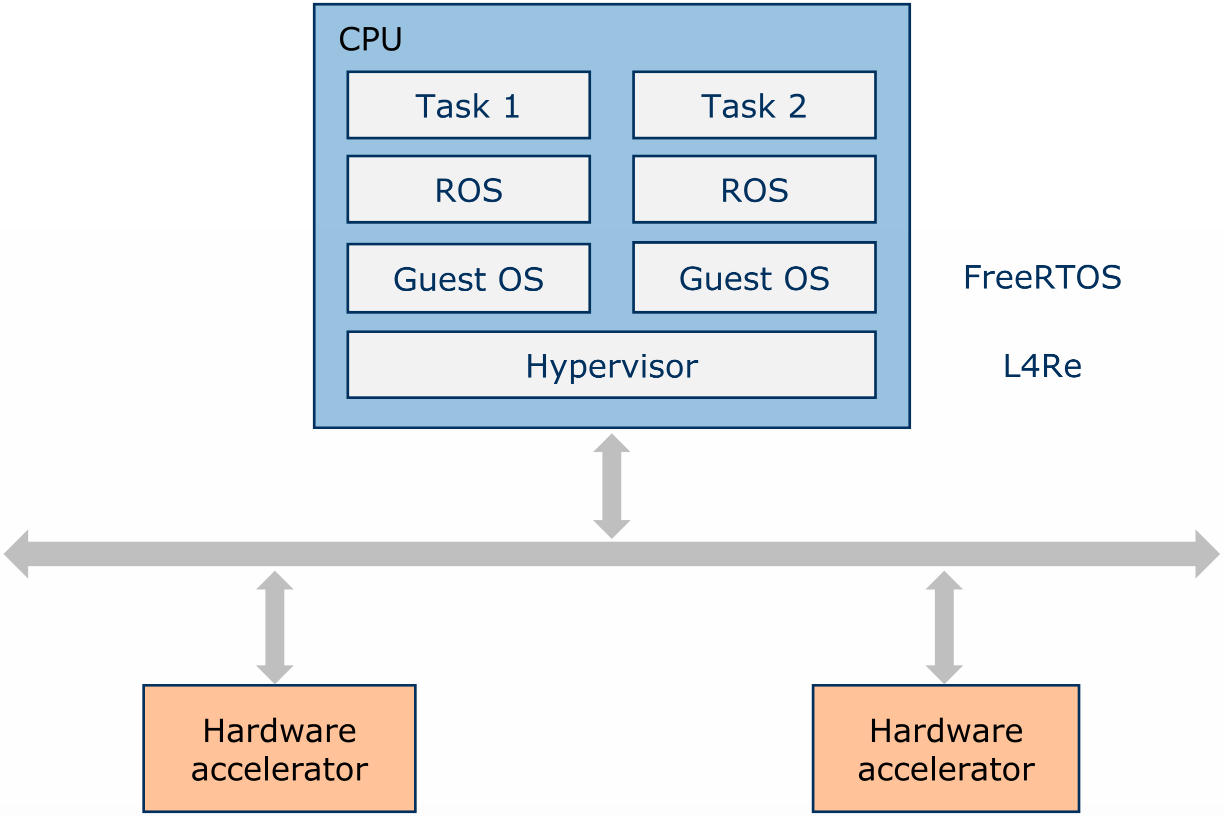
PROTECTION OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE

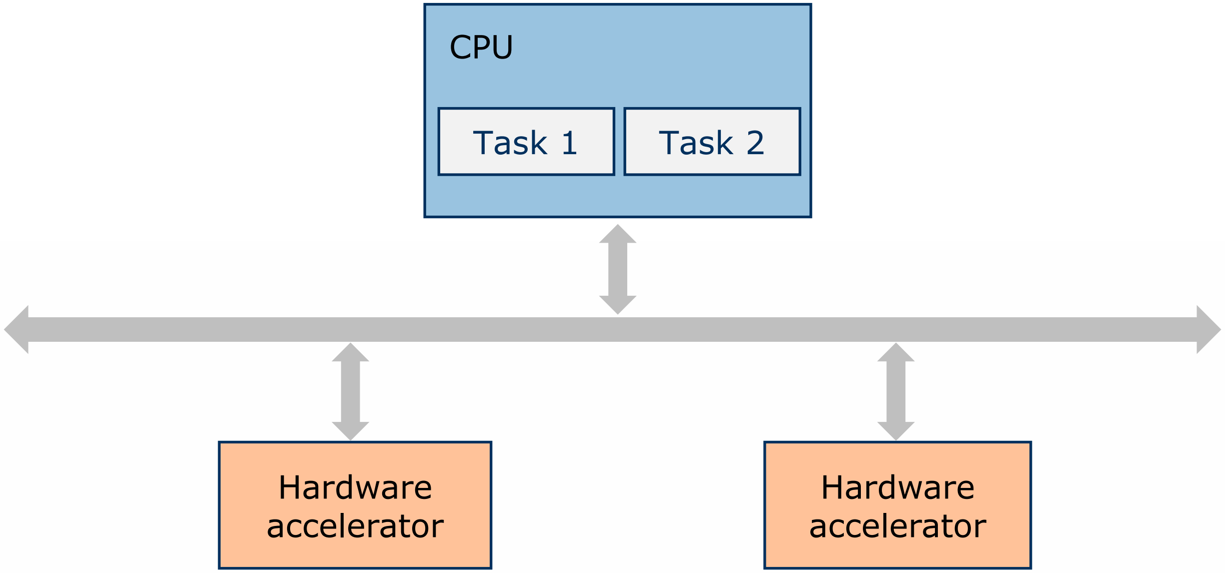


FreeRTOS

L4Re

PROTECTION OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE



AXI4-Stream (DMA):

- virtual memory
- DMA space ✓

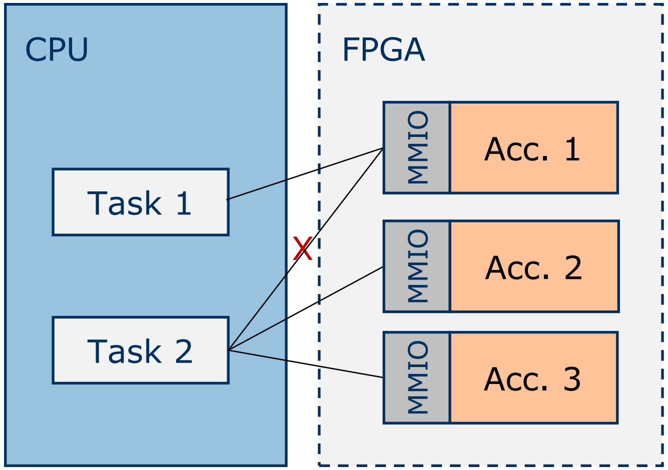
AXI4-Lite / Full (MMIO):

- direct access only with fixed assignment
- flexibility via hypervisor

MOTIVATION

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE

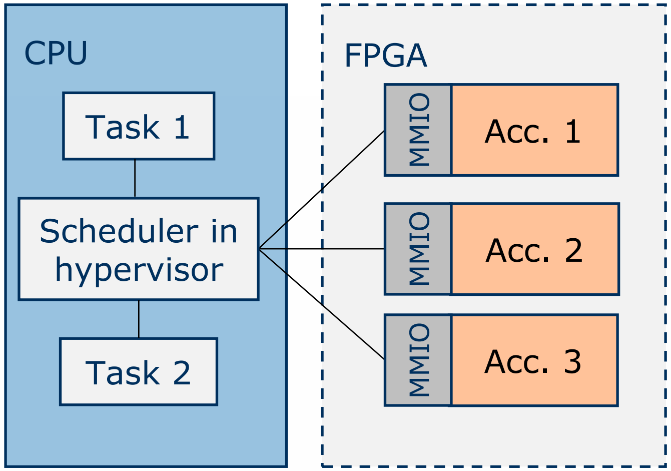
1. Fixed assignment:



Disadvantage:

- No flexibility
- No scalability

2. Access via software scheduler:

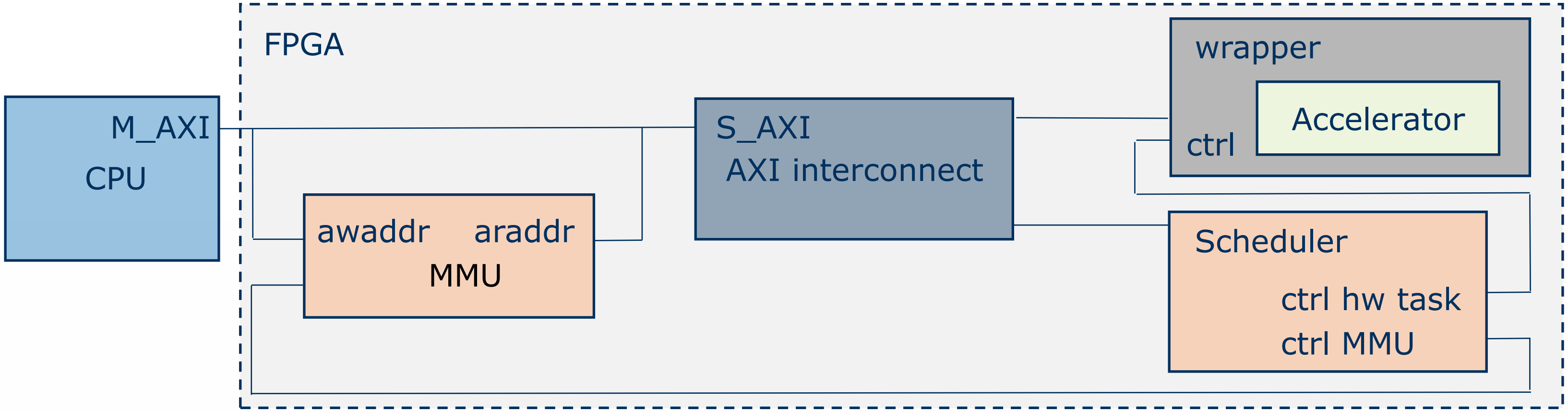


Disadvantage:

- Latency

MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE



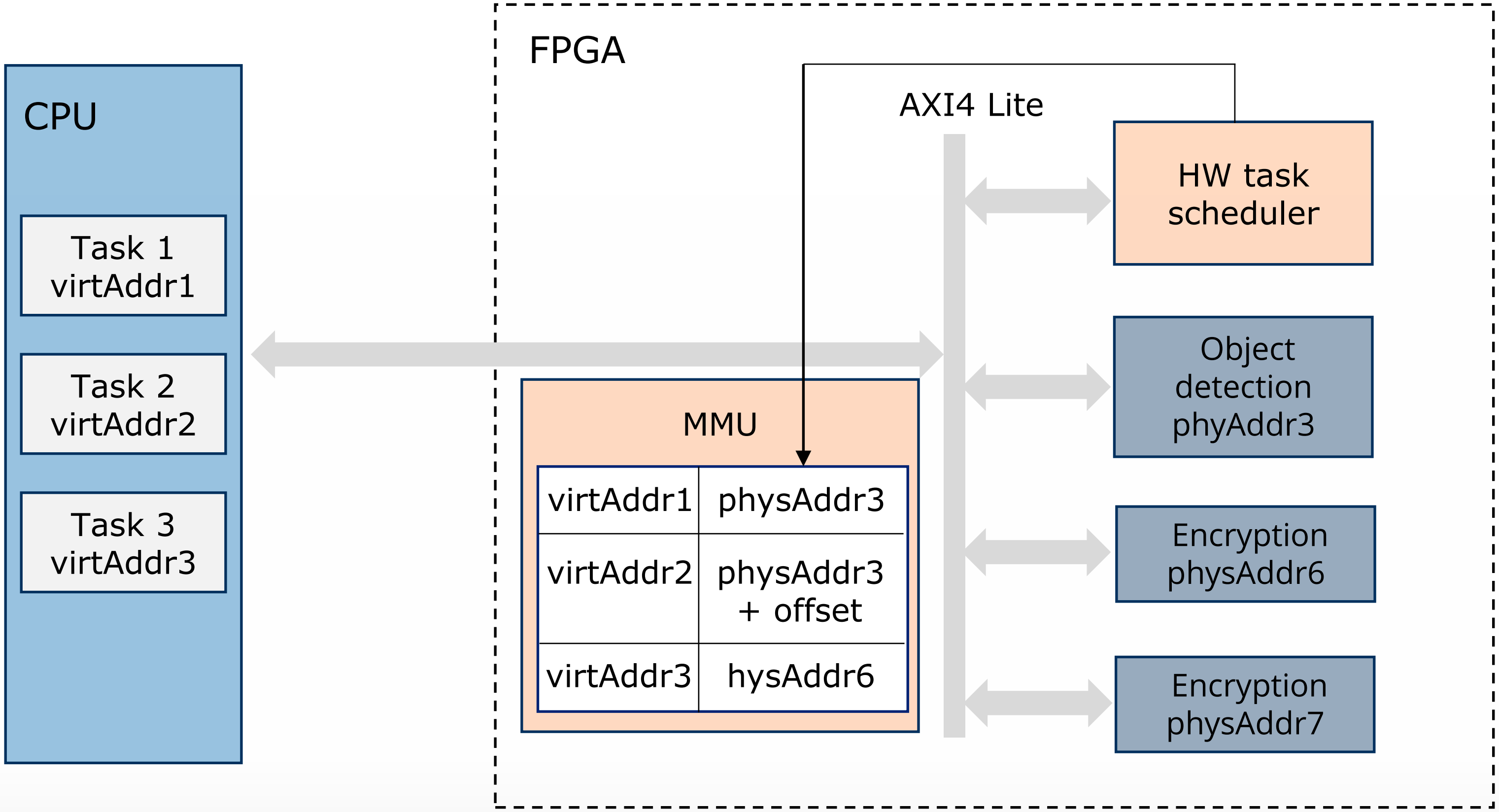
Custom MMU

Scheduler
- Vitis HLS
- Input: accelerator type, priority
- Chooses accelerator and updates the translation table

Priority queue for each accelerator

MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

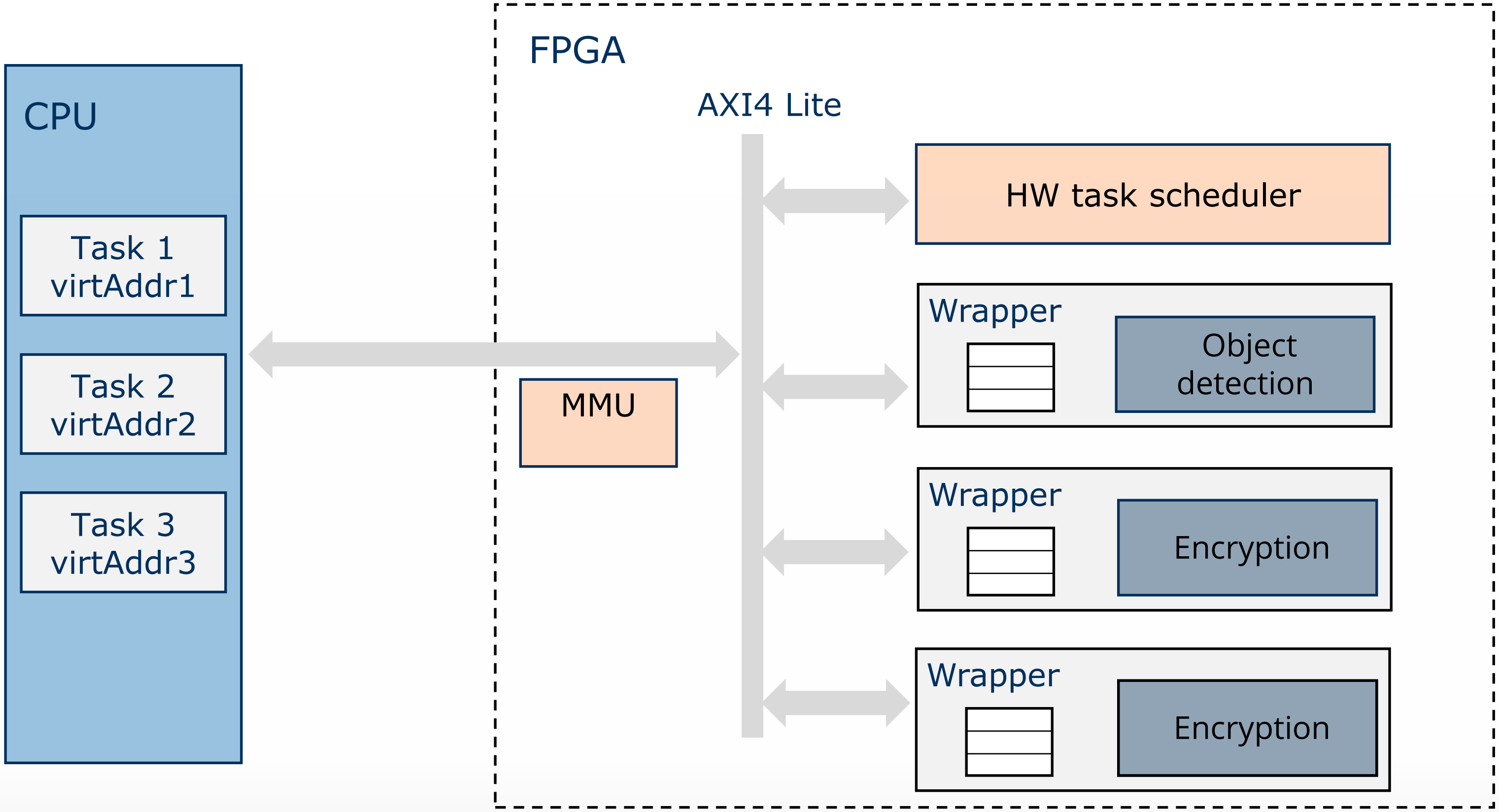
FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE



virtAddr1	physAddr3
virtAddr2	physAddr3 + offset
virtAddr3	hysAddr6

MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE



MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE

l4rec.io

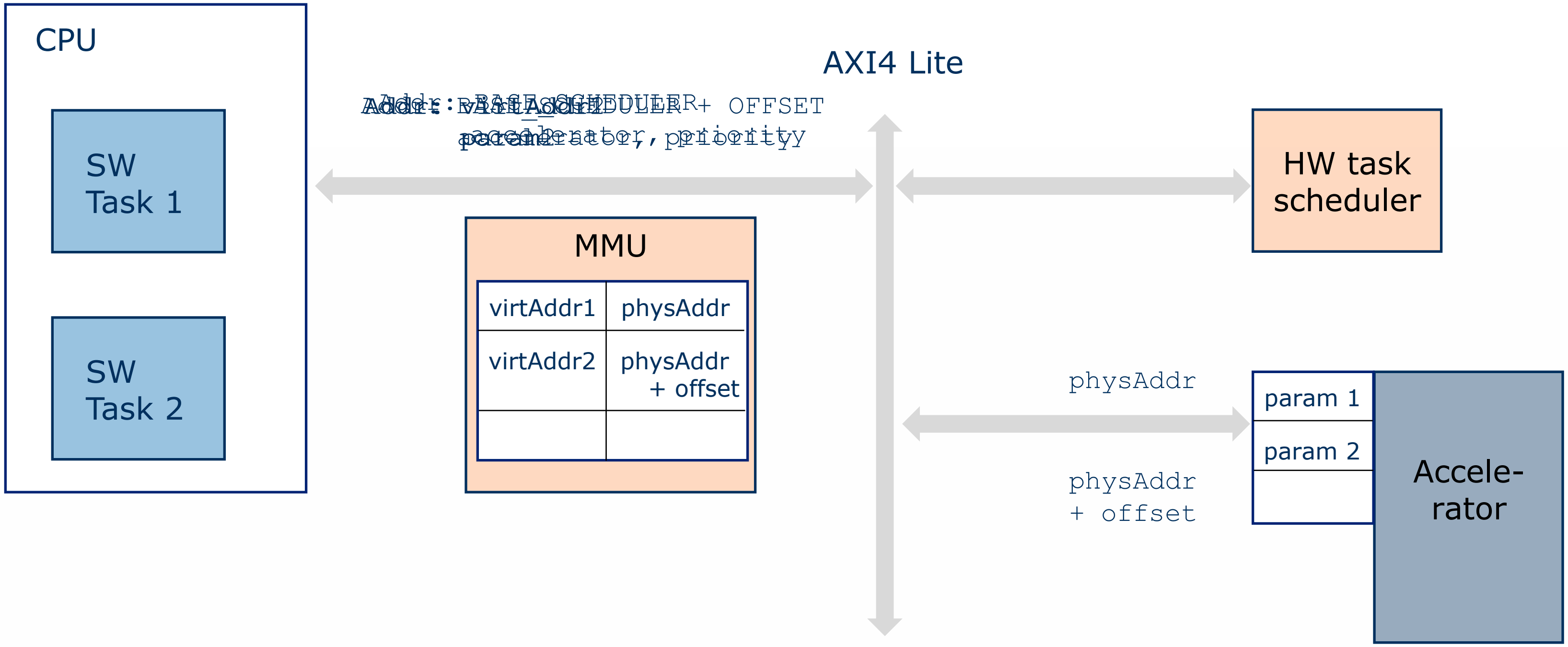
```
Io.hw.add_devices(function()
       hw_scheduler = Io.Hw.Device(function()
              Resource.regs = Io.Res.mmio(0xA0000000, 0xFFFFFFFF)
              Resource.irq1 = Io.Res.irq(IRQ_NUMBER);
                            …
       end);

       task1 = Io.Hw.Device(function()
              Resource.regs = Io.Res.mmio(BASE_SCHEDULER, BASE_SCHEDULER + OFFSET)
              Resource.regs = Io.Res.mmio(BASE_VIRT1, HIGH_VIRT1)
       end);

       task2 = Io.Hw.Device(function()
              Resource.regs = Io.Res.mmio(BASE_SCHEDULER + OFFSET,
                                          BASE_SCHEDULER + 2 * OFFSET)
              Resource.regs = Io.Res.mmio(BASE_VIRT2, HIGH_VIRT2)
       end);
       …
End)
```

MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE



MEMORY-MAPPED ACCESS OF HARDWARE ACCELERATORS

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE

Advantages

- Prevention of unauthorized access
- Shared usage of hardware accelerators
- Preservation of priorities
- Latency reduction compared to a software approach

Disadvantage

- Overhead → to be evaluated, still work in progress

Future work

- Virtualization of interrupts

STUDENT PARTICIPATION

FOR FPGA-SOC-BASED MOBILE ROBOT ARCHITECTURE

Student work (NES project work):

- Isaac Sanchez: Hardware Task Scheduler with Access Control
- Xinyu Liu: Exploration of Security Threats Mitigation using Micro ROS and L4Re

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QUESTIONS

REMARKS

DISCUSSION

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