



# Trusted IoT - User group meeting June 9th, 2023

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## WP2: Exploration, Specification & Requirements study

KU Leuven will have a deeper look into the requirements that come with a <u>unmanned aerial vehicle</u> (drone). Typically there are <u>multiple devices</u> that each serve a specific function. Some components are standalone hardware units and do not have any processor system. Other components are to be vetted so they can be mapped on multiple RISC-V processors. Subsequently an exploration must be done of <u>existing</u>, <u>open-source implementations of RISC-V</u>. As new implementations are regularly made available, choosing the most appropriate implementation for the targeted use case will also be a part in this WP.



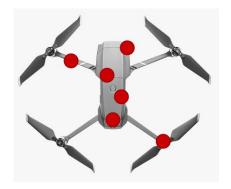




Within Trusted IoT - KU Leuven is working on Multi-Core RISC-V platforms

The industrial Use Case will focus on drones, operated by multiple RISC-V cores.

Multiple, isolated microprocessors will be centralised on a single FPGA



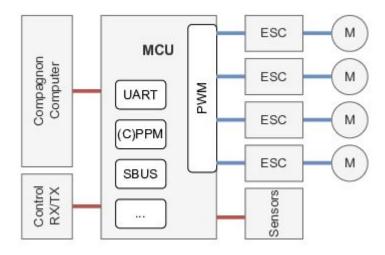




Within Trusted IoT - KU Leuven is working on Multi-Core RISC-V platforms

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Three different RISC-V implementations will be used



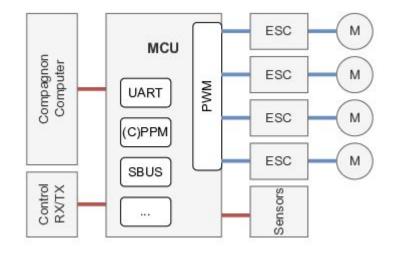


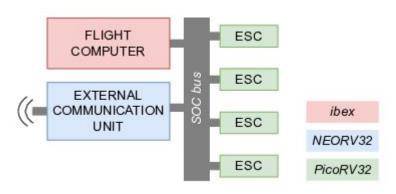


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Three different RISC-V implementations will be used









#### Three different RISC-V implementations will be used

#### ibex

- source: https://github.com/lowRISC/ibex
- intended use: MCU / Flight computer
- **licence**: Apache License Version 2.0
- HDL: SystemVerilog

#### NEORV32

- **source**: <a href="https://github.com/stnolting/neorv32">https://github.com/stnolting/neorv32</a>
- intended use: Commlicence: 3-clause BSD
- HDL: Verilog

#### PicoRV32

- source: <a href="https://github.com/YosysHQ/picorv32">https://github.com/YosysHQ/picorv32</a>
- intended use: ESC
- licence: ISC
- HDL: VHDL



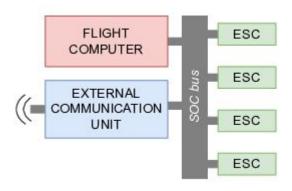
PicoRV32 - A Size-Optimized RISC-V CPU





#### Three different RISC-V implementations will be used

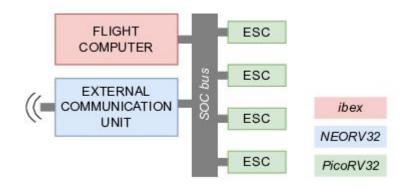
		ibex	NEORV32	PicoRV32
		Apache License 2.0	BSD 3-clause	ISC
cannot	Hold Liable	X	х	Х
	Use Trademark	X	X	
must	Include copyright	X	X	Х
	Include license	X	X	X
	State changes	X		
	Include notice	X		
can	Commercial use	X	X	X
	Modify	X	Х	X
	Distribute	X	X	X
	Place warranty	X	X	
	Private use	X		
	Use patent claims	X		
	Sublicense	X		





#### Benefits:

- improved inter-component communication
  - choice of protocols
  - throughput
  - security (authentication & confidentiality)
- compatibility with COTS
- (remote) attestation of ALL components



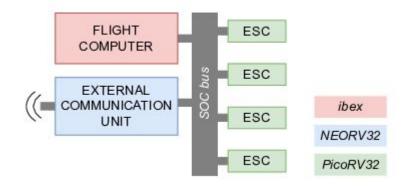






#### Finished

• final report is available on the website







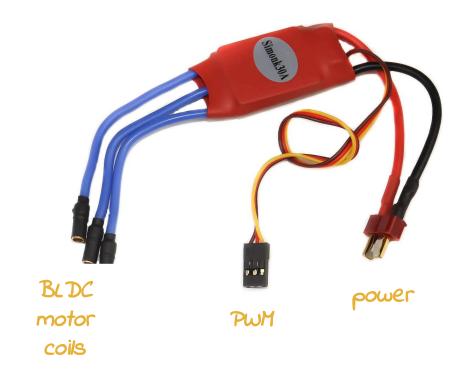
## WP3: Platform-specific security solutions

T 3.3 (KU Leuven) <u>Multi-Core RISC-V</u> platforms. RISC-V is an open standard that implements the principle of a Reduced Instruction Set Computer (RISC), which comes down to the actual processor on which a system is running. A RISC-V core can be adjusted and/or extended to better fit the application it is hosting. With the fact that more and more different 'processors' are available comes the need to have some form of interaction. This, however, could pose a threat. As the weakest component could succumb to attackers, it might infect other components as well. <u>Having multiple cores should have a mechanism that they keep an eye on each other.</u> A typical approach is to provide some <u>trusted hardware</u> to each entity (processor) so they are equipped for overcoming this challenge. Having a reconfigurable processor makes this feasible. The results of the examining and comparing the state-of-the-art techniques and implementations and holding them against the established requirements (as done in WP2) will <u>set out the lines for a proof-of-concept implementation</u>. This will then be translated to suit the needs for the target use-case in WP4.





Started with ESC





There is a processor in the ESC that:

- receives PWM
- transmits coil-steering pattern to the BLDC
- a small <u>microcontroller</u> manages

There is "quite some" power electronics

We want to get around using the microcontroller

(and we're stuck with the power electronics)

(curse you, back EMF)



RISC-V®

Started with ESC



Drone BLDCs are bought

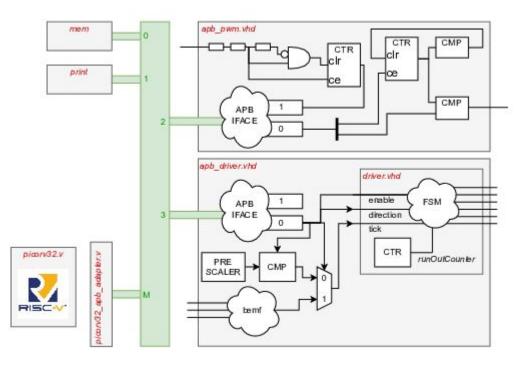
Power electronics has been made

A(n extremely) simple SOC replaces the microcontroller





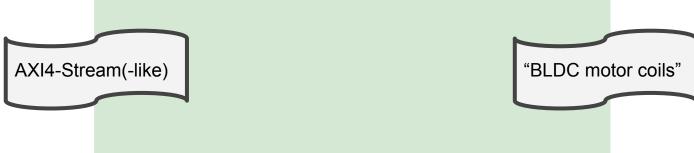
Started with ESC



Drone BLDCs are bought

Power electronics has been made

A(n extremely simple) SOC replaces the microcontroller





# RISC-V®

Started with COMM



There is a processor in the COMM that:

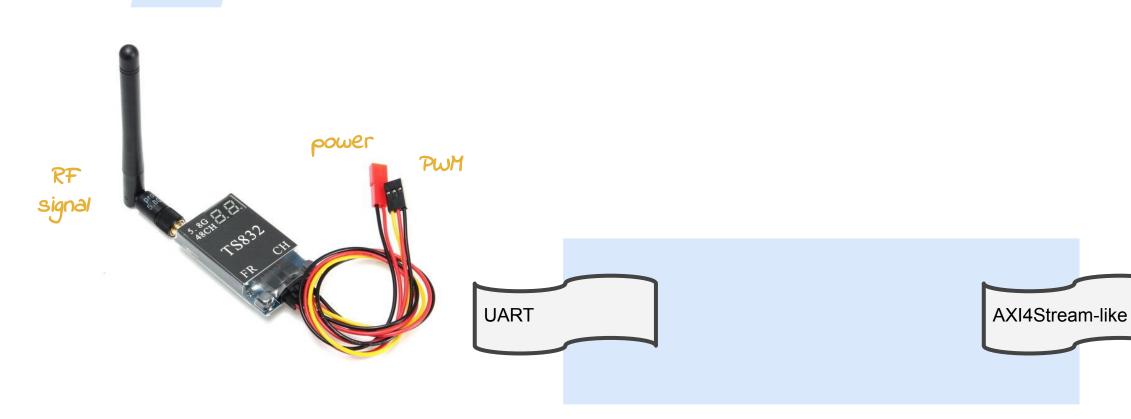
- sends and receives RF signals
- transmits and receives instructions over PWM
  - o can be PWM
  - o can be (C)PPM
  - o can be SBUS
- a small <u>microcontroller</u> manages

We want to get around using the microcontroller

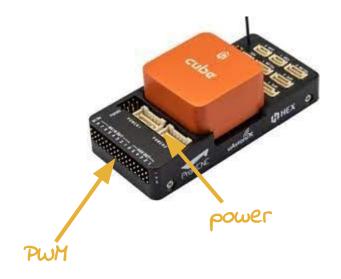




Started with COMM



**NOT** started with **FC** (yet)





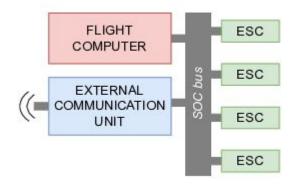
We want to get around using the microcontroller





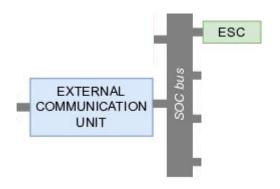


#### Targeted implementation





#### Current state of implementation



This implementation replaces/represents the "main application"



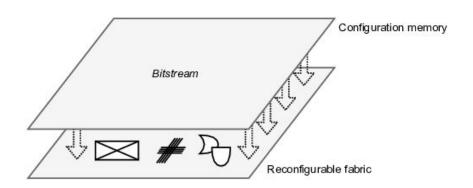




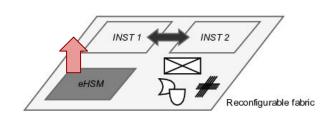
The main application needs to be attested

Because the main hackable components are on the FPGA, attestation of the entire FPGA is required.

Secure communication through LWC winner: ASCON

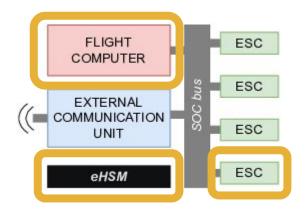


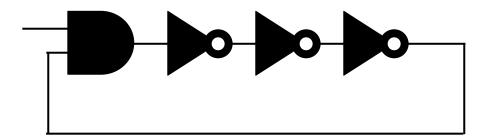












We aim for minimal refactoring to protect industries already available solutions

Different designs of different companies are present on the same chip

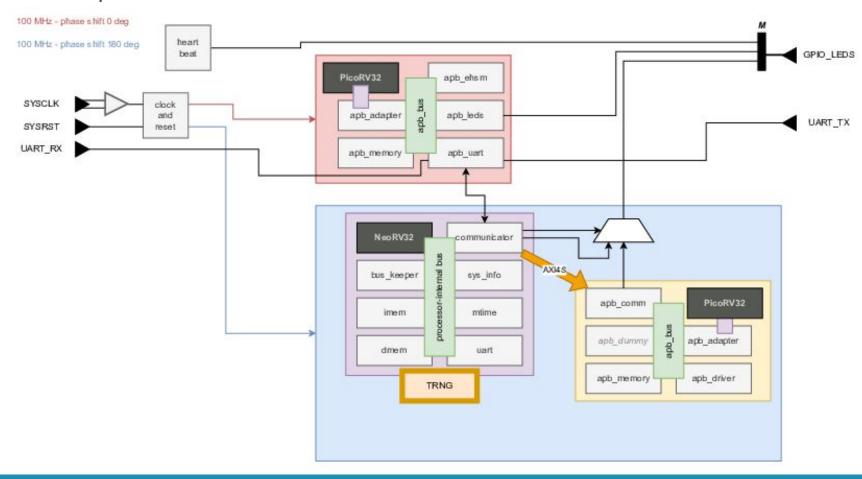
Multi-tenancy

Protection against SCA: active fence





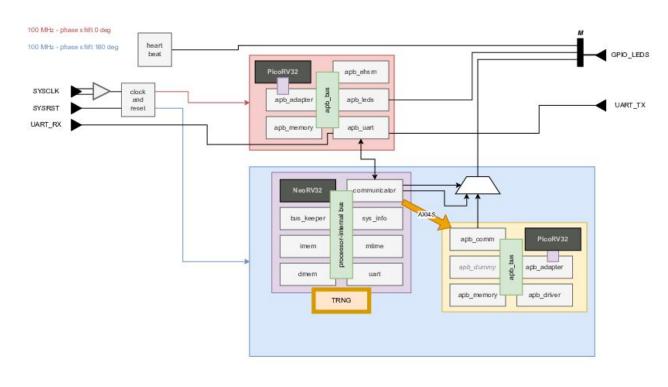
#### Current state of implementation







#### Current state of implementation



We want to get around using the microcontroller

Different clock domains for eHSM and application

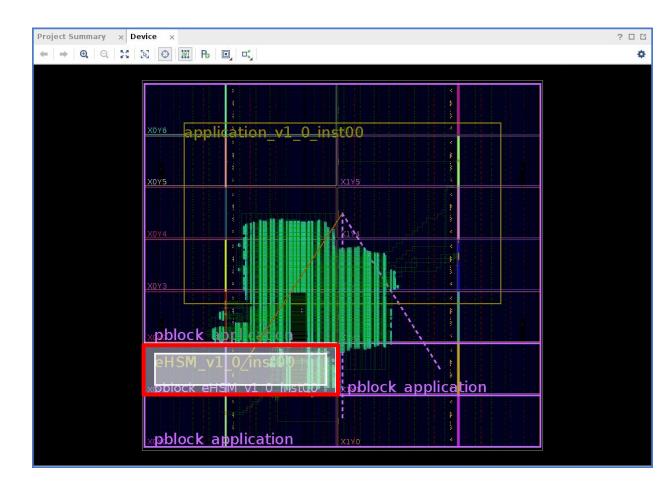
Shared UART (for now)

TRNG is aimed to be dual use:

- as TRNG
- as fence



- 3 out of 4 RISC-V implementations have been tested standalone:
  - eHSM
  - · ESC
  - communication
- a merge was madepartitioned implementationactive fence
- due to practicality reasons:
  only 1 shared UART for all
  (ideally: 1 for eHSM, 1 for application)







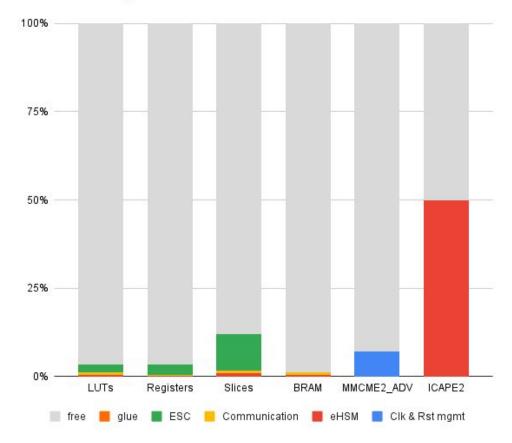


#### Resource usage

- · NO FC
- **ONE** single ESC
- NO encryption
- communication only over (shared) UART

		Slices	Regs	BRAM
Application		1'198	2'788	9
	comm	635	1'867	7
	ESC	566	1'329	2
eHSM		606	1'524	5
Total (avail)		75'900	607'200	1'020

#### Resource usage

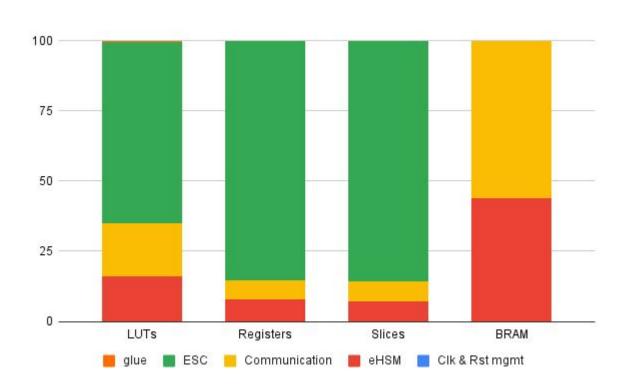




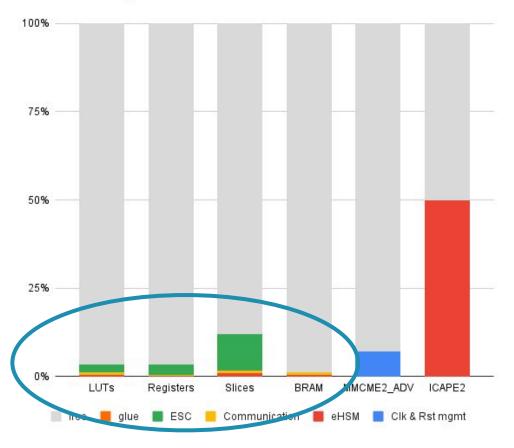




#### Resource usage

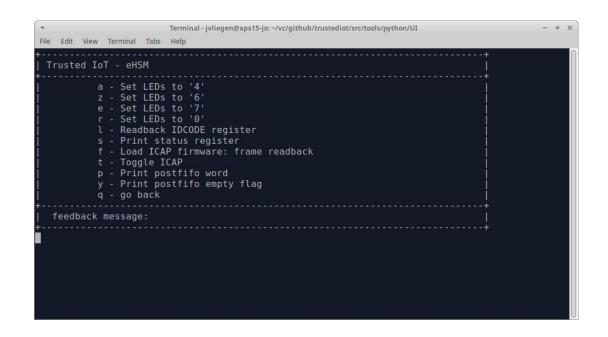


#### Resource usage









first UI with eHSM up-and-running

readback capabilities are currently being tested



## Trusted IoT - demonstrator

#### Working (to certain extend)

- Application
  - single BLDC spins
  - · communication is alive
- eHSM
  - implemented crypto is finished but needs to be merged
  - ICAP readback provides IDCODE

#### Still needs attention

- Application
  - adding the FC
  - making a small PCB for power electronics
  - repeat motor 3 more times
- eHSM
  - •













# thank you!!





