

KICK-OFF CORNET TRUSTED-IOT

02 / 12 / 2022

AGENDA

10h00-10h20: Project summary + introduction of members

10h20-10h40: Introduction to embedded security

10h40-10h50: Use cases and technology (VUB)

10h50-11h10: RISC V

11h10-11h20: Use cases and technology (KULeuven)

11h20-11h35: Funding opportunities (Vlaio) and next TETRA call

11h35-11h45: Round table

11h45-12h30: Networking reception

SUMMARY

VUB	Environmental monitoring	Heterogeneous embedded architectures
KULeuven	Drones	Multi-core RISC-V
BTU	Industry 4.0	Coarse grained reconfigurable architectures (CGRAs)
TUD	Mobile robots	Ultra low-powered (FPGAs)
GFAI	Cooperative robots	Heterogeneous system solutions

VUB – INDI - RAPTOOLS

TEAM



Abdellah Touhafi



Bruno Da Silva



Laurent Segers



An Braeken

- **Reconfigurable architectures**
- **Wireless sensor networks**
- **Environmental monitoring**
- **Security**

Use case : Environmental monitoring

- Single sensors:
 - Humidity
 - Temperature
 - Air quality...
- Arrays of sensors
 - Audio
 - Video



Technology

- Low end platforms



- Middle to high end platforms



Nele Mentens



Md. Masoom
Rabbani



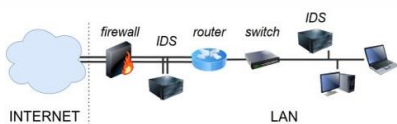
Jo Vliegen

Research group of KU Leuven

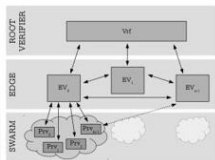
Faculty of Engineering Technology,
campus Diepenbeek, Limburg, Belgium

Algorithm - hardware co-design

- High-speed network security

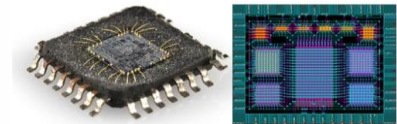


- low-cost & low-energy crypto and trusted computing

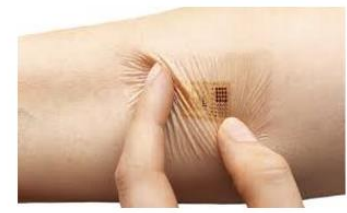


Hardware - technology co-design

Si-CMOS technologies



Emerging technologies



- Focused on multi-core RISC-V platforms
 - Attestation
- Use case: Drones 4.4
 - substitute every processor with a RISC-V, on a single FPGA



Diana Groehringer



Sergio Pertuz



Domain-Specific Computer Architectures

- Processors
- Accelerators
- Network-on-Chip
- Memory

Hardware/Software Co-Design

- Modeling (e.g. UML)
- HW/SW Codesign of applications or middleware (ROS, RTOS)
- High Level Synthesis

Runtime Reconfigurable Systems

- Virtualization
- Self-adaptation
- Dynamic and Partial Reconfiguration

Programming Methods and Tools

- Design Space Exploration
- Application Partitioning and Mapping
- LLVM
- Processing-in-Memory

Platform

- **Ultra low-powered FPGAs:**
 - Potential IoT security criticalities for FPGA-based mobile robots.
 - Robot controller architectures focusing on hardware accelerators for machine learning, image recognition, compression, and security systems.



Use Case

- **FPGA-based mobile robots**
 - Design a generic and flexible platform based on ultra-low powered FPGA technology for studying and prototyping a complete unified robot navigation system.

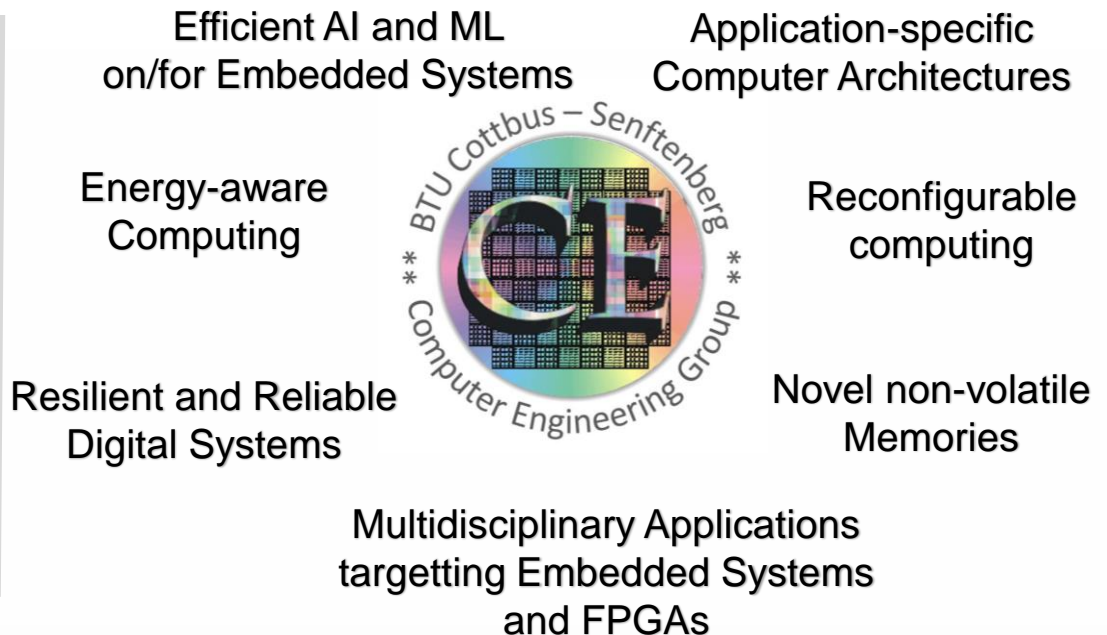


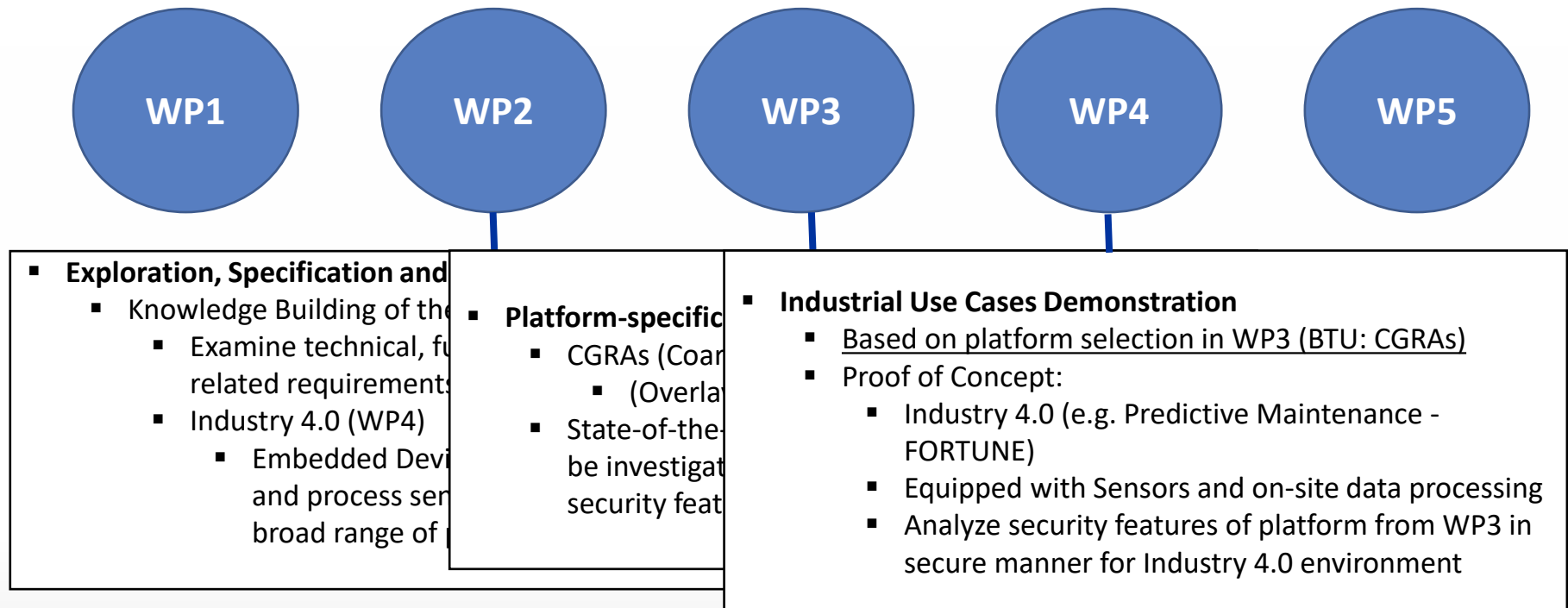
BREMEN TU (BTU)

TEAM

▪ Chair of Computer Engineering

- **Led by: Dr.-Ing. Marc Reichenbach**
- *Prof. Dr.-Ing. habil. Michael Hübner (currently Vice President BTU)*
- *Group of 15+ Phd Research Assistants*
- *Contributing and Collabrating to/with Research Projects from German Research Foundation (DFG), Non-profit Organizations and EU based Research Organizations*





- Project Leader:
 - **Immanuel Rettig**
 - Scrum Master:
 - Nina Bakalova
 - Head of Development:
 - Ben Drost
 - Development:
 - Miriam Schneider
 - Students:
 - Leonardo Maben
 - Orhan Stephan
 - Consultants:
 - Ben Hohnhäuser
 - Stephan Brodkorb
- Develop a system that:
 - Has a safe communication
 - Is fully scalable
 - Is plug&play
 - Use Case could be:
 - Communication and cooperation between multiple robots
 - Communication between multiple image processing units



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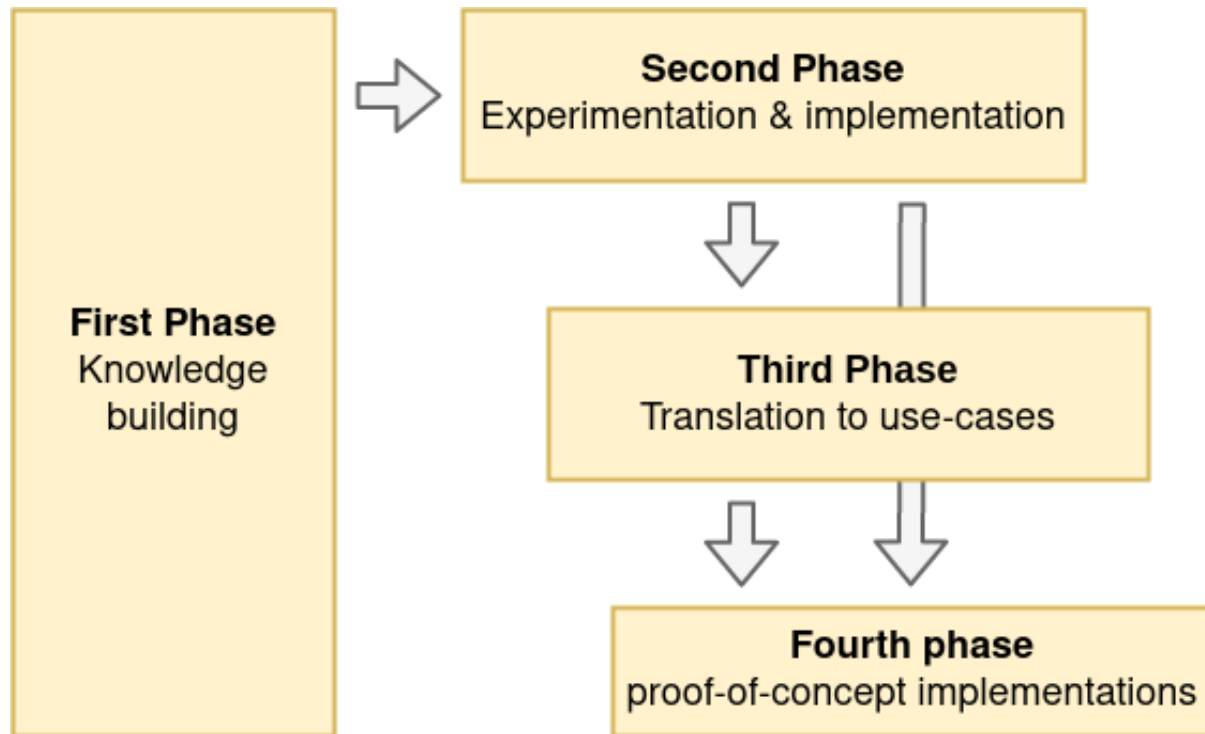
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PROJECT STRUCTURE



FINAL REMARKS

Input welcome: use case, internships,...

Contact to

- VUB: an.braeken@vub.be
- KU Leuven: Jo.vliegen@kuleuven.be

More info available on

https://jvliegen.github.io/trusted_iot_website