KU LEUVEN

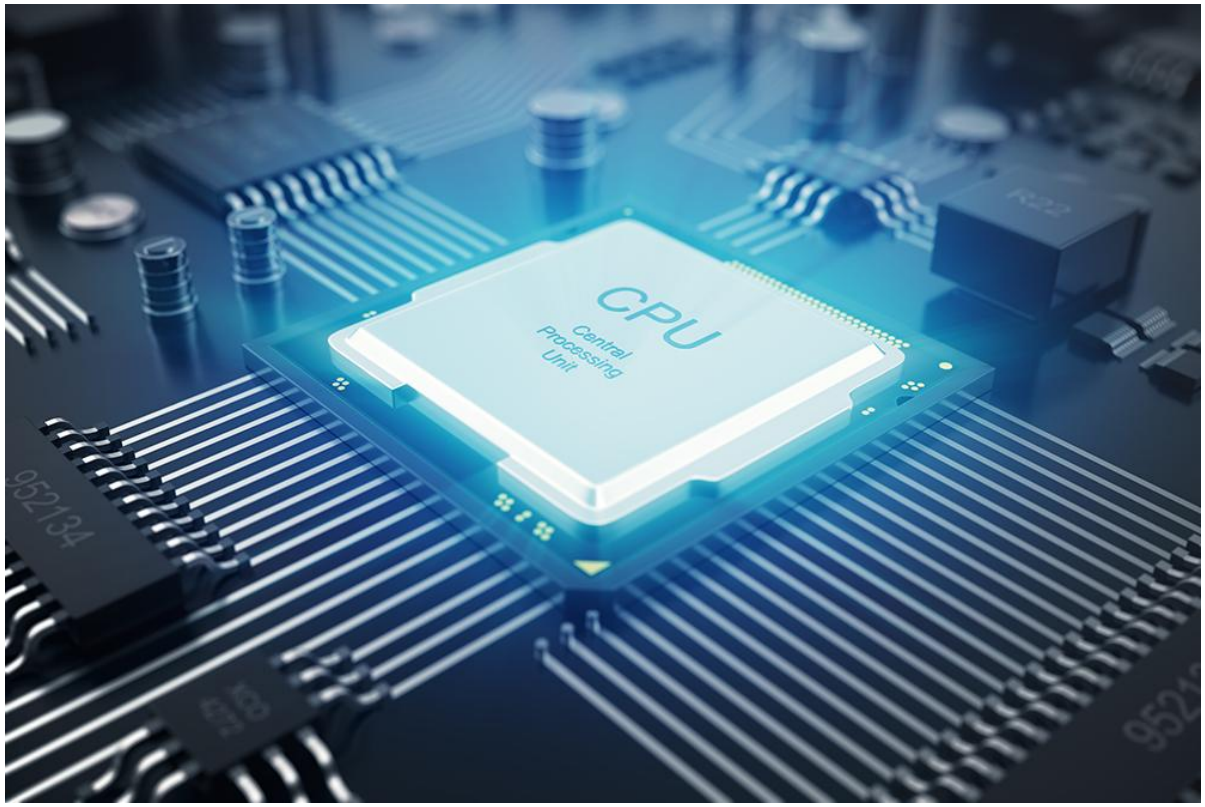
RISC-V

Trusted IoT - Kick-off meeting

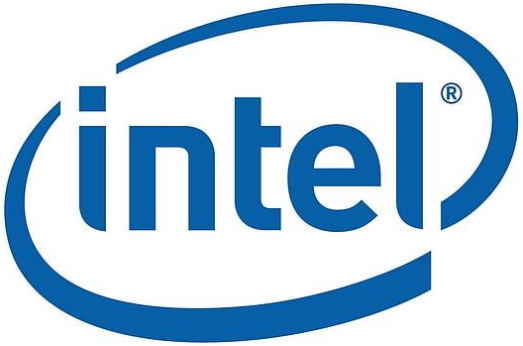
December 2nd, 2022

Processor

Processors are “all over the place”

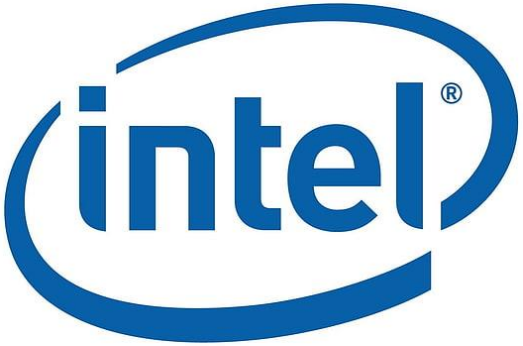


Processor



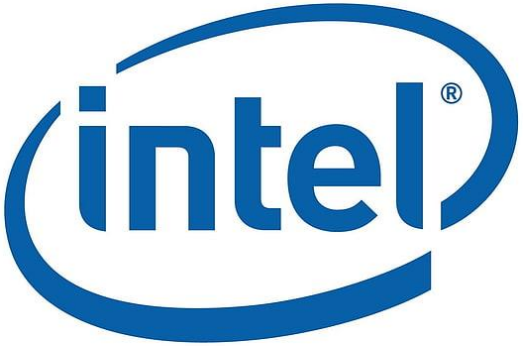
Rule of thumb: if it doesn't have Intel or AMD in the name, it's most likely an ARM

Processor



Architecture	ia32 x86-64	ARMv1 … ARMv9-A

Processor



CISC

Complex instruction set computer

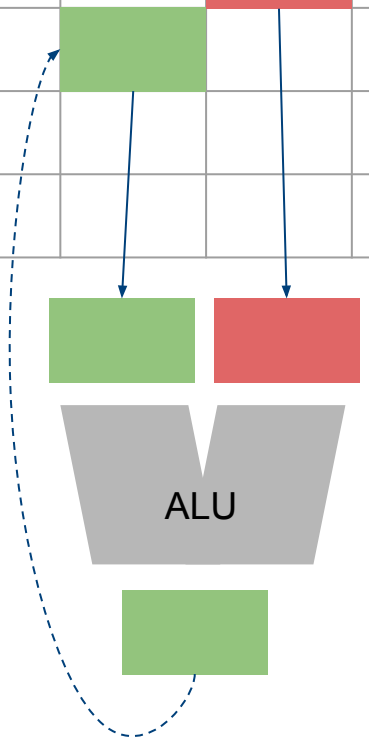
RISC

Reduce instruction set computer

Processor

Memory

	1	2	3	4
A				
B				
C				
D				
E				



example instruction

Operation

<u>In human language:</u>

Add the value at C2 to that of B3 and store the result in C2

Processor

Memory

	1	2	3	4
A				
B				
C				
D				
E				

example instruction

Operation

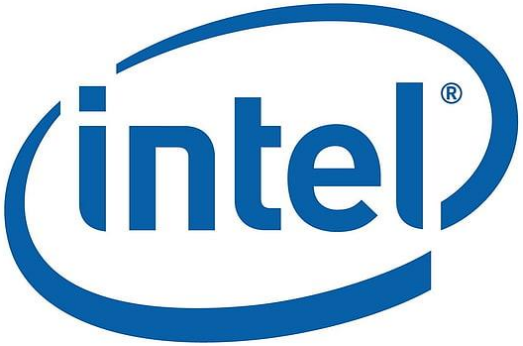
In human language:

Add the value at C2 to that of B3 and store the result in C2

In CISC:
ADD C2, B3

In RISC:
LD R1, C2
LD R2, B3
ADD R1, R2
ST C2, R1

Processor



CISC

Complex instruction set computer

not open
not royalty free

RISC

Reduce instruction set computer

open
not royalty free

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RISC-V

RISC-V:

- **open** source Instruction Set Architecture (ISA)

ISA	Base+Ext	Compact Code	Quad FP	Address 32-bit	Address 64-bit	Address 128-bit	Software GCC	Software LLVM	Software Linux	Software QEMU
SPARC V8			✓	✓			✓	✓	✓	✓
OpenRISC				✓	✓		✓	✓	✓	✓
RISC-V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

source: https://www2.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-146.pdf

RISC-V

RISC-V:

- **open** source Instruction Set Architecture (ISA)
- since 2010
- developed at University of California, Berkeley
- license and royalty free
- latest version

ISA Specification

The specifications shown below represent the current, ratified releases. Work is being done on GitHub.

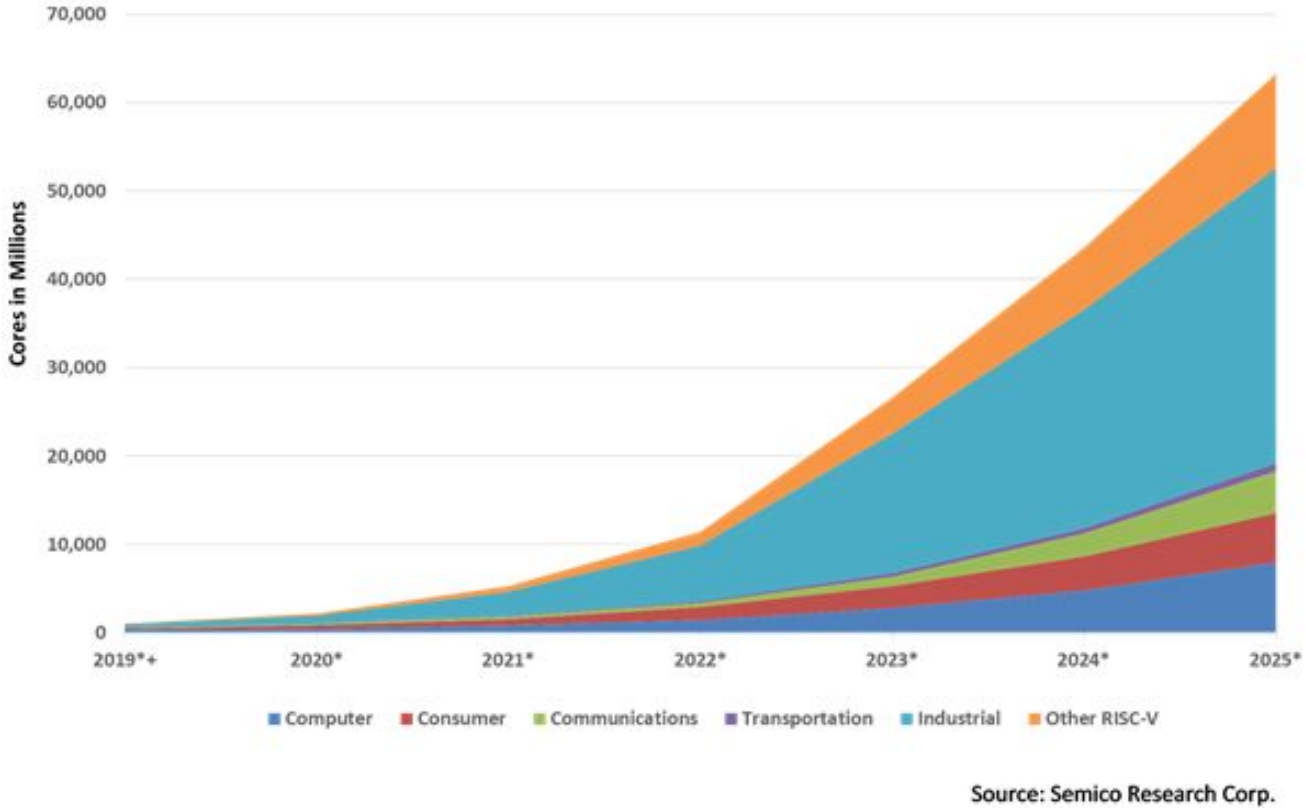
- Volume 1, Unprivileged Spec v. 20191213 [PDF]
- Volume 2, Privileged Spec v. 20211203 [PDF]
- Recently ratified, but not yet integrated, extension specifications

Past ratified releases include the term "ratified" in the release tag.

source: https://riscv.org/technical/specifications/

RISC-V

Semico forecasts strong growth for RISC-V, predicting the market will consume 62.4 billion RISC-V CPU cores by 2025.



Source: Semico Research Corp.

RISC-V

The ISA is built in a modular way:

- Base:
  - RV32I: Base Integer Instruction Set

- Instruction set Extensions
  - M: Standard Extension for Integer Multiplication and Division
  - A: Standard Extension for Atomic Instructions
  - B: Standard Extension for Bit Manipulation
  - …

RISC

The ISA

- Bas
  -
- Ins
  -
  -
  -

Division

Name	Description	Version	Status[b]	Instruction count
Base				
RVWMO	Weak Memory Ordering	2.0	Ratified	
RV32I	Base Integer Instruction Set, 32-bit	2.1	Ratified	40
RV32E	Base Integer Instruction Set (embedded), 32-bit, 16 registers	1.9	Open	40
RV64I	Base Integer Instruction Set, 64-bit	2.1	Ratified	15
RV128I	Base Integer Instruction Set, 128-bit	1.7	Open	15
Extension				
M	Standard Extension for Integer Multiplication and Division	2.0	Ratified	8 (RV32) 13 (RV64)
A	Standard Extension for Atomic Instructions	2.1	Ratified	11 (RV32) 22 (RV64)
F	Standard Extension for Single-Precision Floating-Point	2.2	Ratified	26 (RV32) 30 (RV64)
D	Standard Extension for Double-Precision Floating-Point	2.2	Ratified	26 (RV32) 32 (RV64)
Zicsr	Control and Status Register (CSR)	2.0	Ratified	6
Zifencei	Instruction-Fetch Fence	2.0	Ratified	1
G	Shorthand for the IMAFDZicsr_Zifencei base and extensions	—	—	
Q	Standard Extension for Quad-Precision Floating-Point	2.2	Ratified	28 (RV32) 32 (RV64)
L	Standard Extension for Decimal Floating-Point	0.0	Open	
C	Standard Extension for Compressed Instructions	2.0	Ratified	40
B	Standard Extension for Bit Manipulation	1.0	Ratified	43[28]
J	Standard Extension for Dynamically Translated Languages	0.0	Open	
T	Standard Extension for Transactional Memory	0.0	Open	
P	Standard Extension for Packed-SIMD Instructions	0.9.10	Open	
V	Standard Extension for Vector Operations	1.0	Frozen	187[29]
K	Standard Extension for Scalar Cryptography	1.0.1	Ratified	49
N	Standard Extension for User-Level Interrupts	1.1	Open	3
H	Standard Extension for Hypervisor	1.0	Ratified	15
S	Standard Extension for Supervisor-level Instructions	1.12	Ratified	4
Zam	Misaligned Atomics	0.1	Open	
Ztso	Total Store Ordering	0.1	Frozen	

RISC-V

The default architecture is **unprivileged**.

ISA Specification

The specifications shown below represent the current, ratified releases. Work is being done on GitHub.

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- Volume 2, Privileged Spec v. 20211203 [PDF]
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The **Privileged specification** covers all aspects of RISC-V systems beyond the unprivileged ISA, including privileged instructions as well as additional functionality required for running operating systems and attaching external devices.

RISC-V

… in short … it's all about the ISA **specification**

and it's **NOT** a processor

artist: Andrea Piacquadio
source: https://www.pexels.com/photo/a-man-in-red-shirt-covering-his-face-3760043/

RISC-V

Luckily, there is "*the Internet*"

People have taken the **specification** and have made an **implementation**.

"*Some*" implementations are **open source**.

This opens up the gates to a new maze:

The magical world of open source licenses

RISC-V

Mozilla Public License 2.0

Common Development and Distribution License

Luckily, there is "*the Internet*"

P…he **specifi…** …ac… an **implementation**.

GNU General Public License (GPL)

Apache License v2.0

"*Some* implementations are **op…**

This opens up the ga…

MIT license

YouTube Terms of Service

The magical world of (open source) licenses

BSD license

BSD 2-cl… license

…D 3-clause …license

Common Development and Distribution License

https://github.com/riscvarchive/riscv-cores-list/blob/master/README.md

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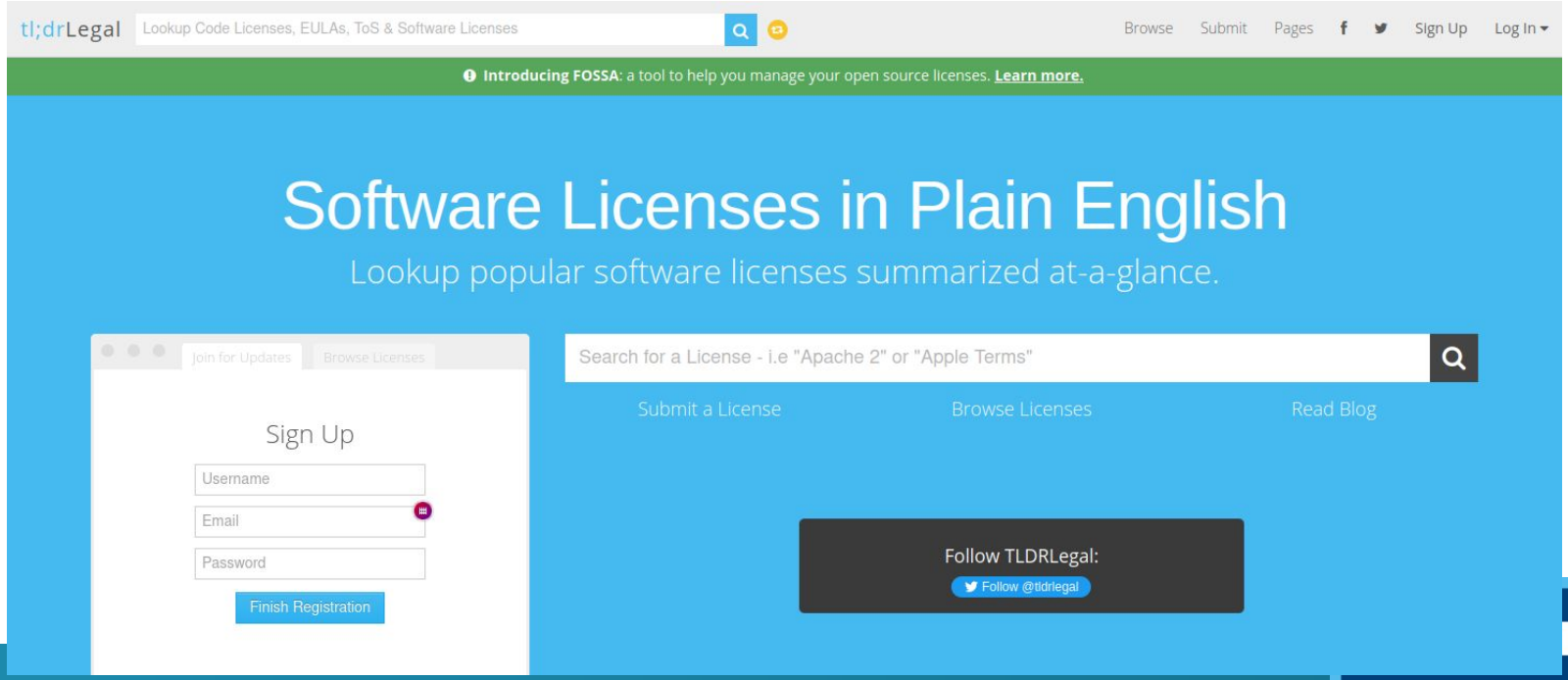
RISC-V

Open source licenses typically makes you think of software

Most of the available RISC-V implementation use an open software license.

A website that might come in handy: https://tldrlegal.com/



RISC-V

for example:

Apache License 2.0 (Apache-2.0)

Track in FOSSA

Code License managed by kevin, submitted 9 years ago. #Open Source #OSI-Approved #Permissive

Summary | Fulltext | Changesets

861844

Quick Summary

Edit

You can do what you like with the software, as long as you include the required notices. This permissive license contains a patent license from the contributors of the code.

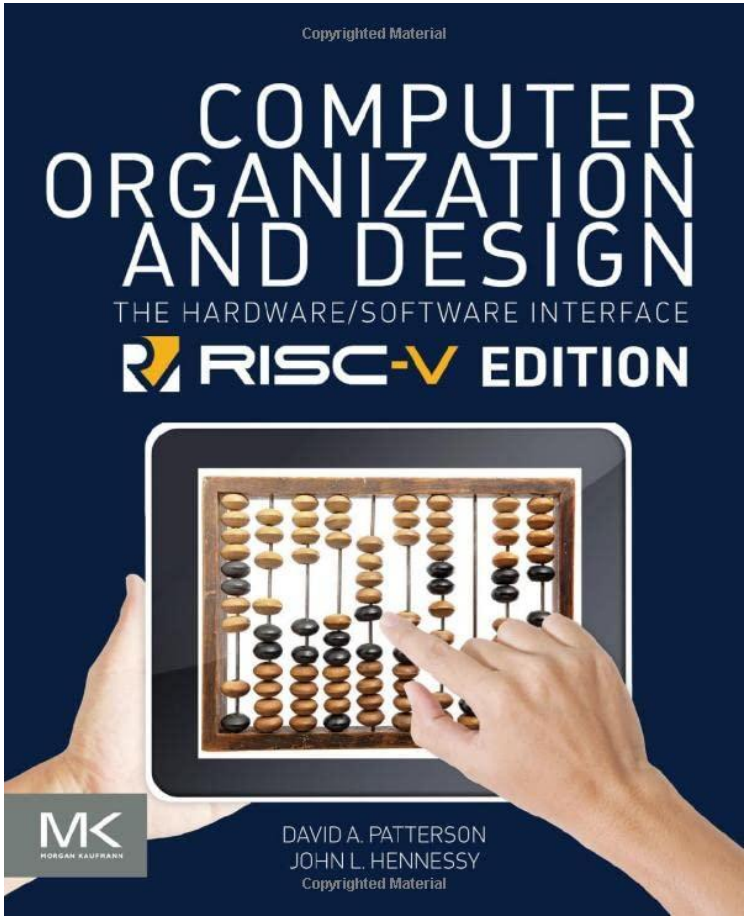
Can	Cannot	Must
Commercial Use	Hold Liable	Include Copyright
Modify	Use Trademark	Include License
Distribute		State Changes
Sublicense		Include Notice
Private Use		
Use Patent Claims		
Place Warranty		

Disclaimer: This is only a short summary of the Full Text. No information on TLDRLegal is legal advice.

RISC-V

Nice book with insights into the ISA

by D. Patterson and J. Hennessy

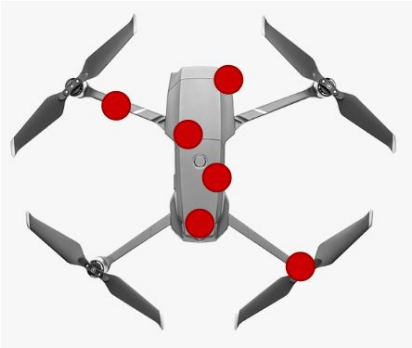


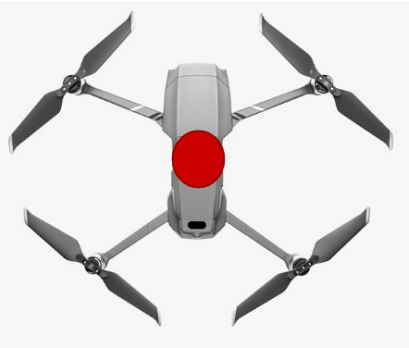
RISC-V

Within Trusted IoT - KU Leuven will work on Multi-Core RISC-V platforms

The industrial Use Case will focus on drones, operated by multiple RISC-V cores.

Multiple, isolated microprocessors will be **centralised** on a single **FPGA**





KU LEUVEN

RISC-V

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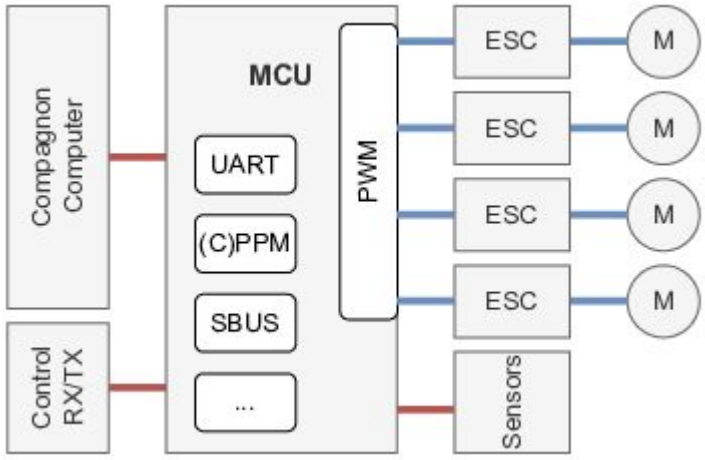
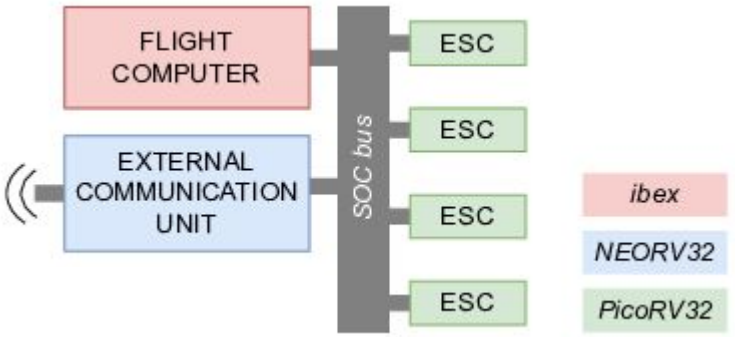
Three different RISC-V implementations will be used





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RISC-V

Three different RISC-V implementations will be used

ibex

- **source**: https://github.com/lowRISC/ibex
- **intended use**: MCU / Flight computer
- **licence**: Apache License Version 2.0
- **HDL**: SystemVerilog

NEORV32

- **source**: https://github.com/stnolting/neorv32
- **intended use**: Comm
- **licence**: 3-clause BSD
- **HDL**: Verilog

PicoRV32

- **source**: https://github.com/YosysHQ/picorv32
- **intended use**: ESC
- **licence**: ISC
- **HDL**: VHDL

RISC-V

Three different RISC-V implementations will be used

		PicoRV32	*NEORV32*	*ibex*
		ISC	***BSD 3-clause***	***Apache License 2.0***
CANNOT	Hold Liable	x	x	x
	Use Trademark		x	x
MUST	Include copyright	x	x	x
	Include licence	x	x	x
	State changes			x
	Include notice			x
CAN	Commercial use	x	x	x
	Modify	x	x	x
	Distribute	x	x	x
	Place warranty		x	x
	Private Use			x
	Use patent claims			x
	Sublicense			x

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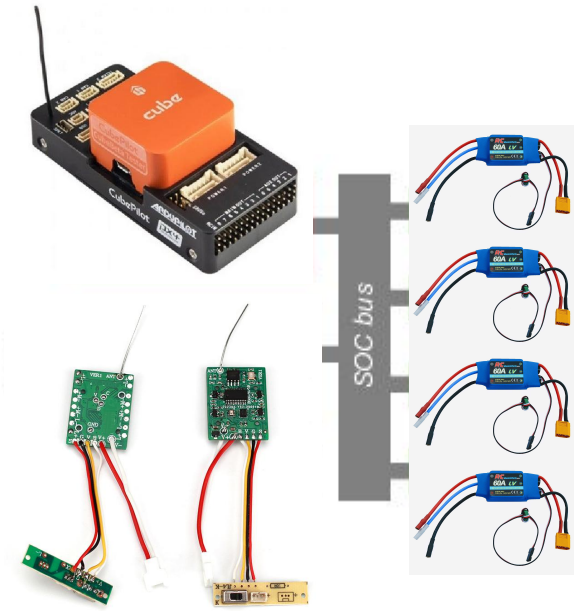
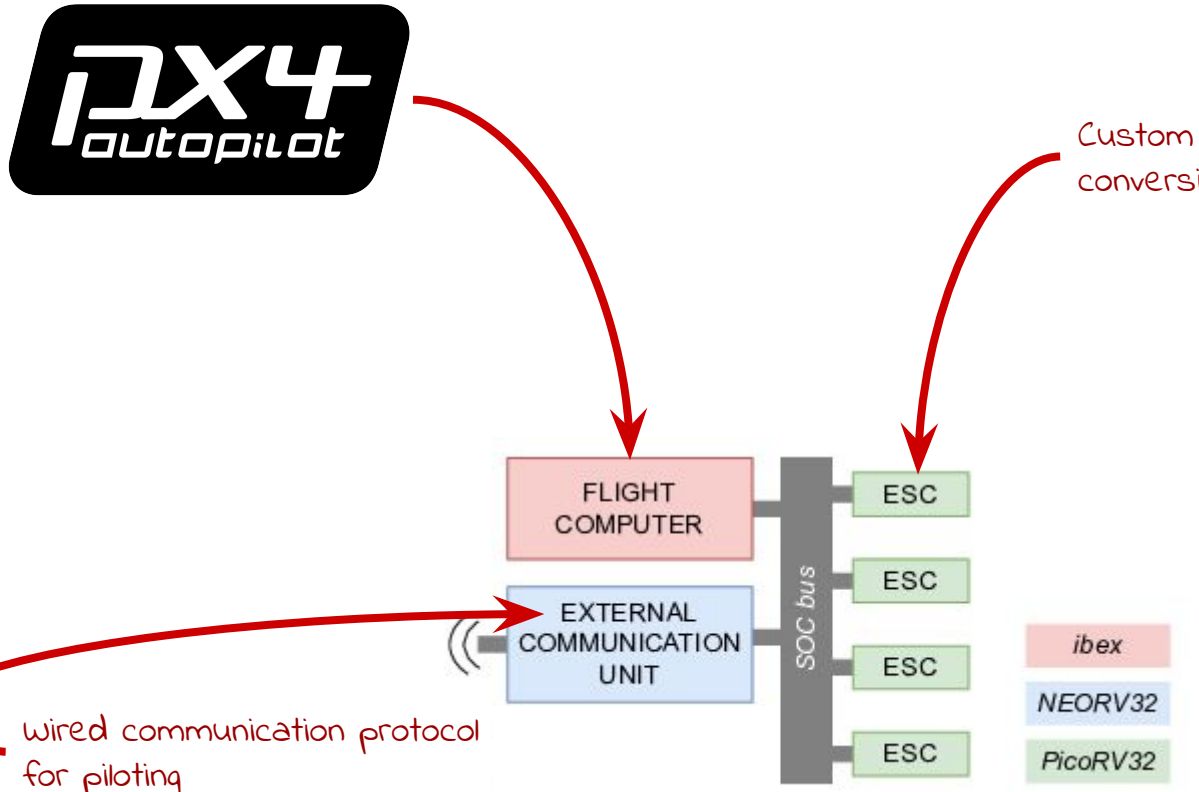
RISC-V



RISC-V

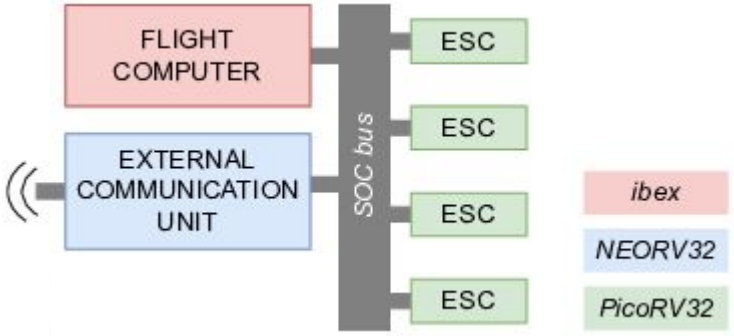

PX4 autopilot
Custom firmware for PWM conversion to 3-phase BLDC
FLIGHT COMPUTER
EXTERNAL COMMUNICATION UNIT
SOC bus
ESC
ESC
ESC
ESC
ibex
NEORV32
PicoRV32
wired communication protocol for piloting
= placeholder for "other" components

RISC-V

Benefits:

- improved inter-component communication
  - choice of protocols
  - throughput
  - security (authentication & confidentiality)
- compatibility with COTS
- (remote) attestation of ALL components

Cryptographic primitives for offloading



Readback of FPGA configuration is required

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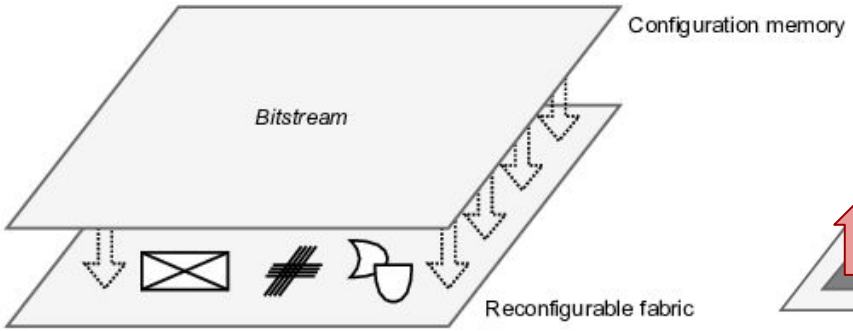
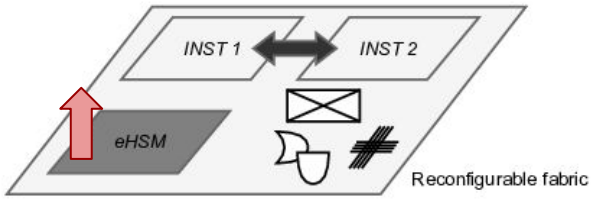
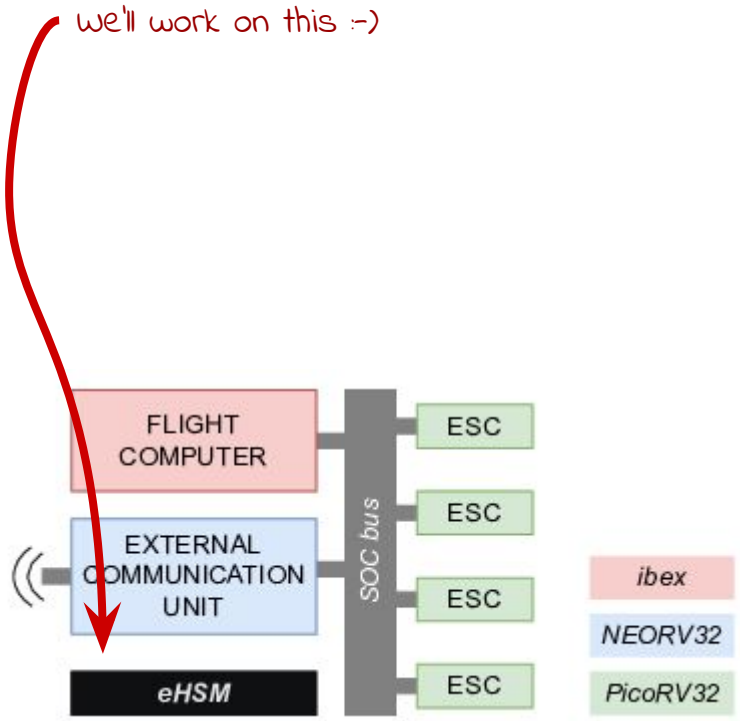




RISC-V


we'll work on this :-)
FLIGHT COMPUTER
EXTERNAL COMMUNICATION UNIT
eHSM
SOC bus
ESC
ESC
ESC
ESC
ibex
NEORV32
PicoRV32

Questions?

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Thank you