CSE433 embedded systems

#Project2

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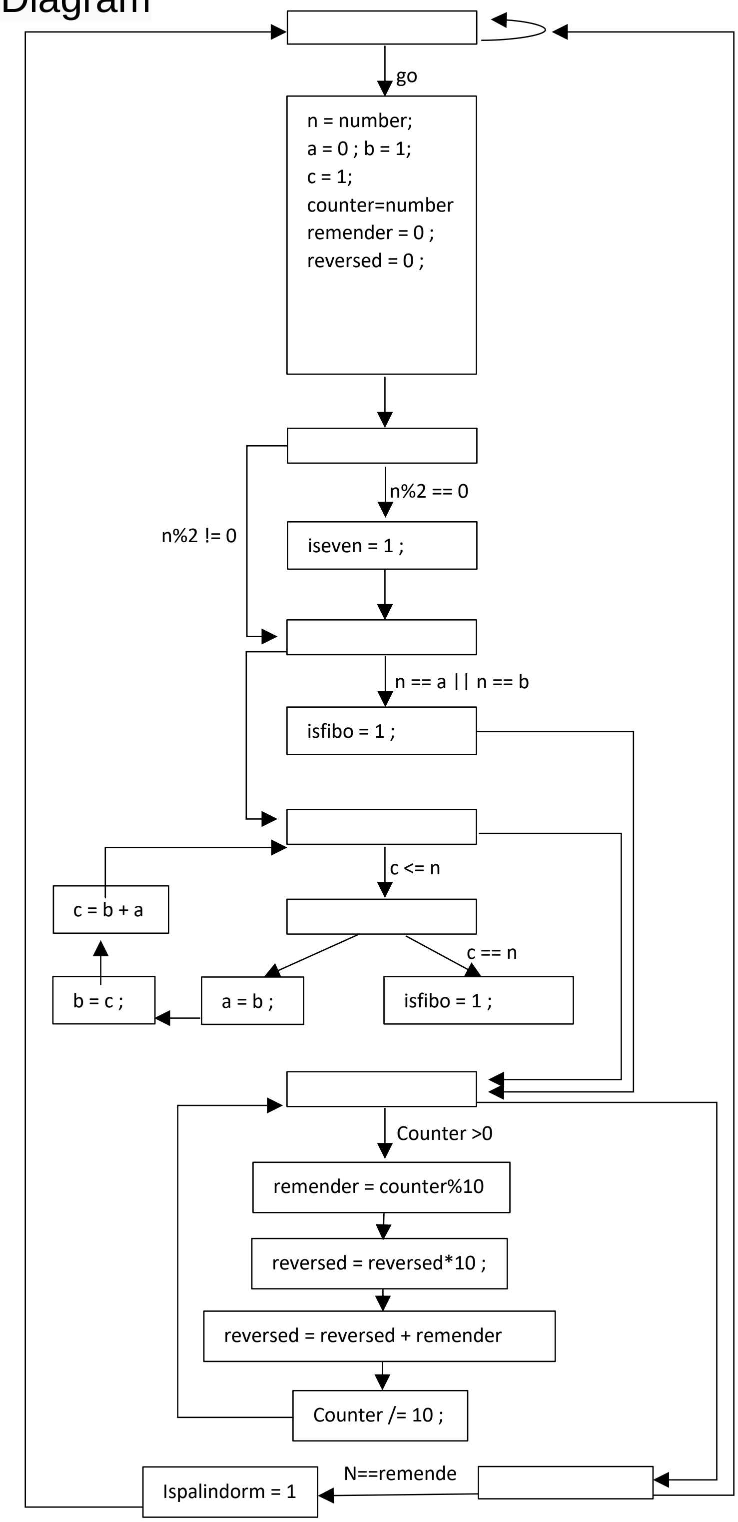
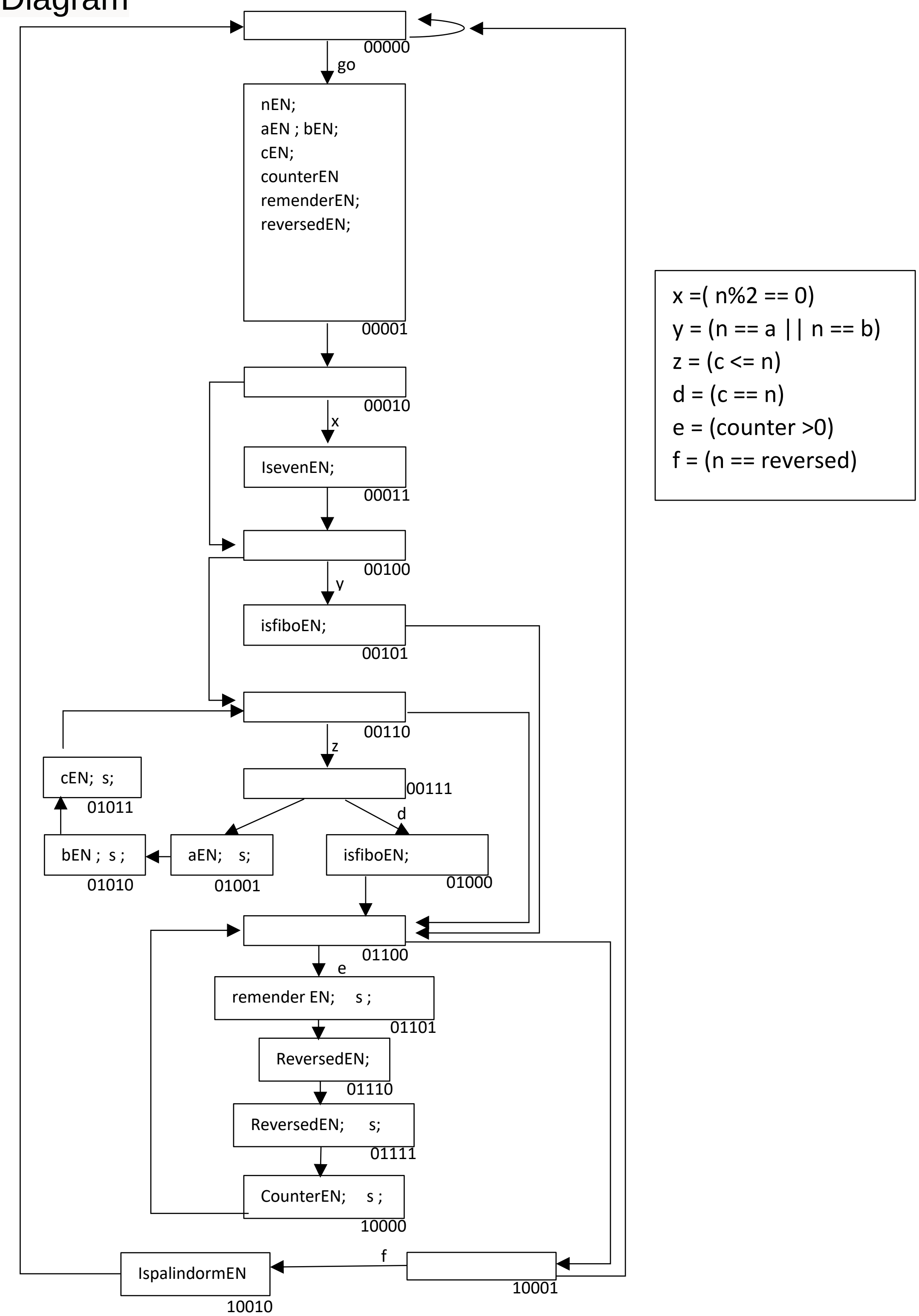
C code:

```c
int n = 34;
int a = 0;
int b = 1;
int iseven = 0 ;
int isfibo = 0 ;
int ispalindorm = 0 ;
int c = a+b;
int counter = n ;
int remender ;
int reversed  = 0 ;
if(n % 2 == 0){
    iseven = 1 ;
}

if (n==a || n==b){
    isfibo = 1;
}else{
    while(c<=n){
        if(c == n){
            isfibo = 1;
            break;
        }
        a = b;
        b = c;
        c = a + b;
    }
}
while(counter > 0){
    remender = counter%10;
    reversed = reversed*10 + remender;
    counter /= 10 ;
}
if(n == reversed){
    ispalindorm = 1;
}


printf("is even %d\n",iseven);
printf("is fibo %d\n",isfibo);
printf("is palindorm %d\n",ispalindorm);
```

FSM / State Diagram



FSM / State Diagram



Truth table

	P_state	reset	go	x	y	z	d	e	f	N_state
	xxxxx	1	x	x	x	x	x	x	x	00000
State0	00000	0	0	x	x	x	x	x	x	00000
	00000	0	1	x	x	x	x	x	x	00001
State1	00001	0	x	x	x	x	x	x	x	00010
State2	00010	0	x	1	x	x	x	x	x	00011
	00010	0	x	0	x	x	x	x	x	00100
State3	00011	0	x	x	x	x	x	x	x	00100
State4	00100	0	x	x	1	x	x	x	x	00101
	00100	0	x	x	0	x	x	x	x	00110
State5	00101	0	x	x	x	x	x	x	x	01100
State6	00110	0	x	x	x	1	x	x	x	00111
	00110	0	x	x	x	0	x	x	x	01100
State7	00111	0	x	x	x	x	1	x	x	01000
	00111	0	x	x	x	x	0	x	x	01001
State8	01000	0	x	x	x	x	x	x	x	01100
State9	01001	0	x	x	x	x	x	x	x	01010
State10	01010	0	x	x	x	x	x	x	x	01011
State11	01011	0	x	x	x	x	x	x	x	00110
State12	01100	0	x	x	x	x	x	1	x	01101
	01100	0	x	x	x	x	x	0	x	10001
State13	01101	0	x	x	x	x	x	x	x	01110
State14	01110	0	x	x	x	x	x	x	x	01111
State15	01111	0	x	x	x	x	x	x	x	10000
State16	10000	0	x	x	x	x	x	x	x	01100
State17	10001	0	x	x	x	x	x	x	1	10010
	10001	0	x	x	x	x	x	x	0	00000
State18	10010	x	x	x	x	x	x	x	x	00000

n0 = (state0 * go)+ (state2 * x) + (state4 * y) + (state6 * z) + (state7 * !d) + (state10) + (state12) +(state14)

n1 = (state1)+ (state2 * x) + (state4 * !y) + (state6 * z) + (state9) + (state10) + (state11) +(state12) + (state13) + (state14) +(state17*f)

n2 = (state2 *!x)+ (state3) + (state4) + (state5) + (state6) + (state8) + (state11) +(state12*e) + (state13) + (state14) +(state16)

n3 = (state5)+ (state6*!z) + (state7) + (state8) + (state9) + (state10) + (state12*e) + (state13) + (state14) +(state16)

n4 = (state15)+ (state17*f)

nEN = state1

aEN = state1 + state9

bEN = state1 + state10

cEN = state1 + state11

isevenEN = state3

isfiboEN = state8 + state5

ispalindormEN = state18

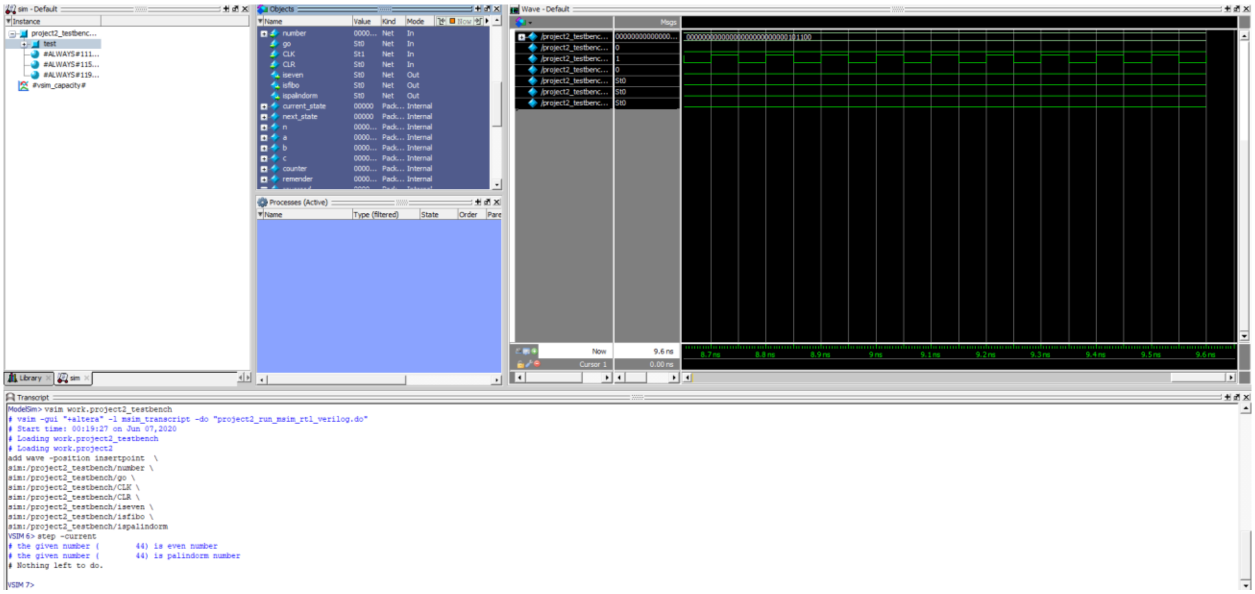
counterEN = state1 + state16

remenderEN = state1 + state13

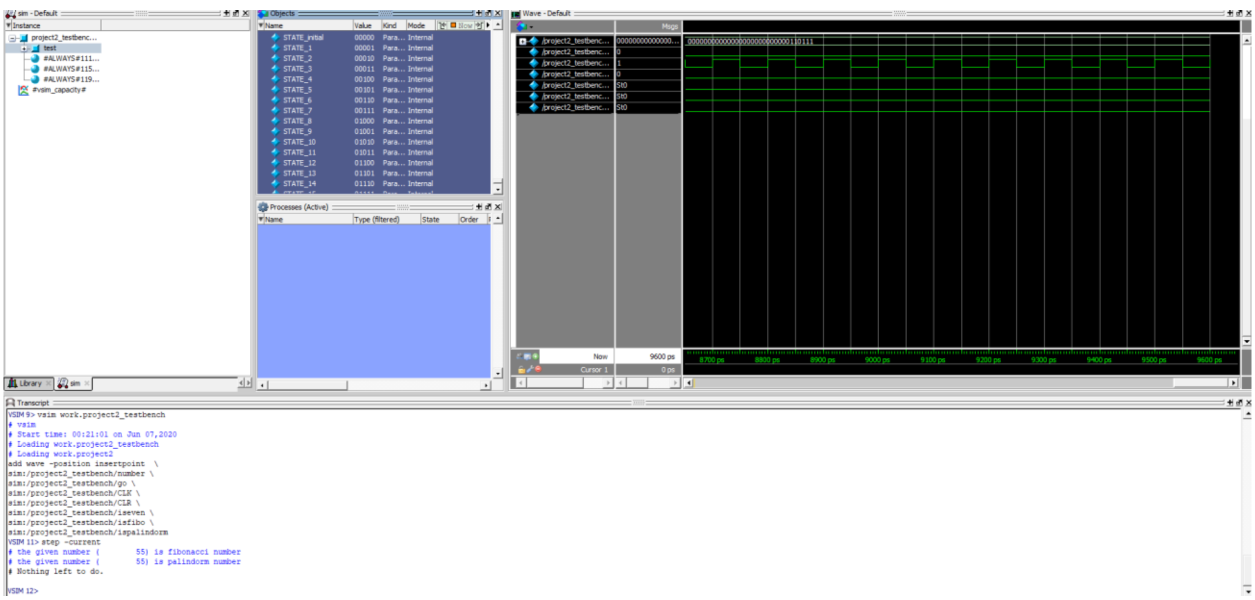
reversedEN = state1 + state14 + state15

s = state10 + state9 + state13 + state11 + state15 + state15

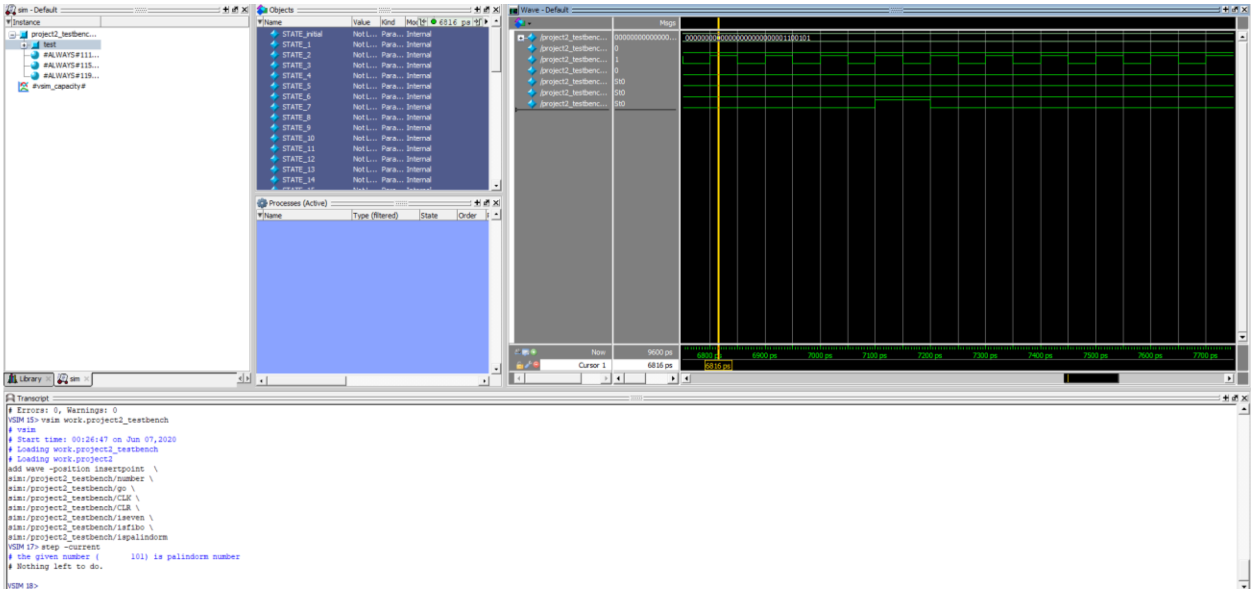
results :

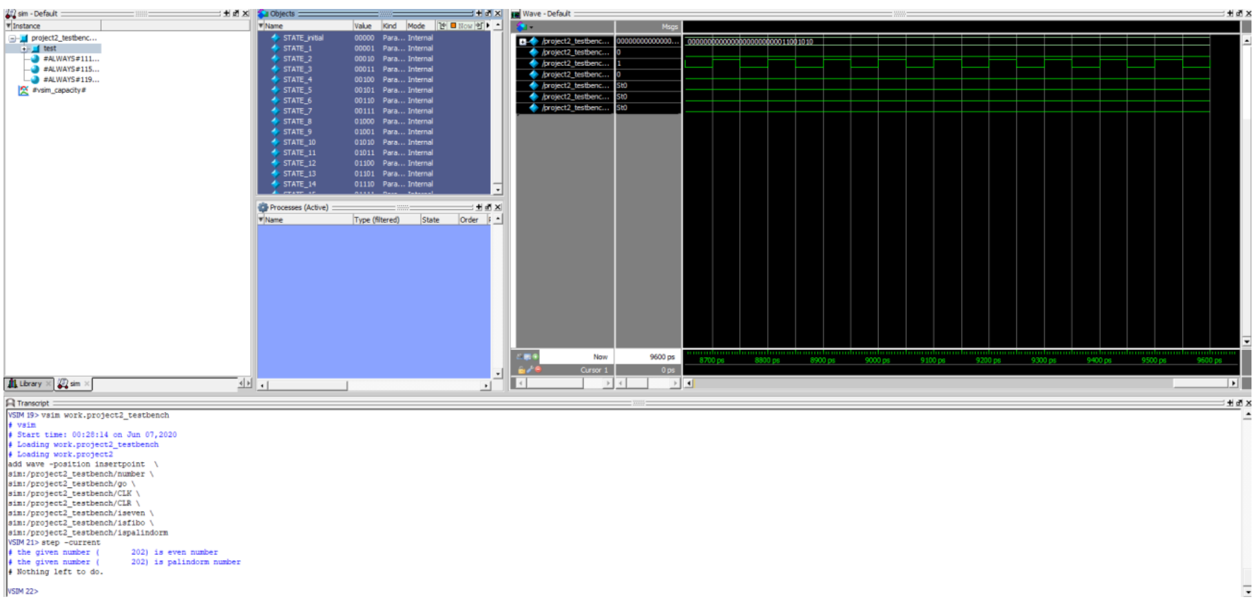


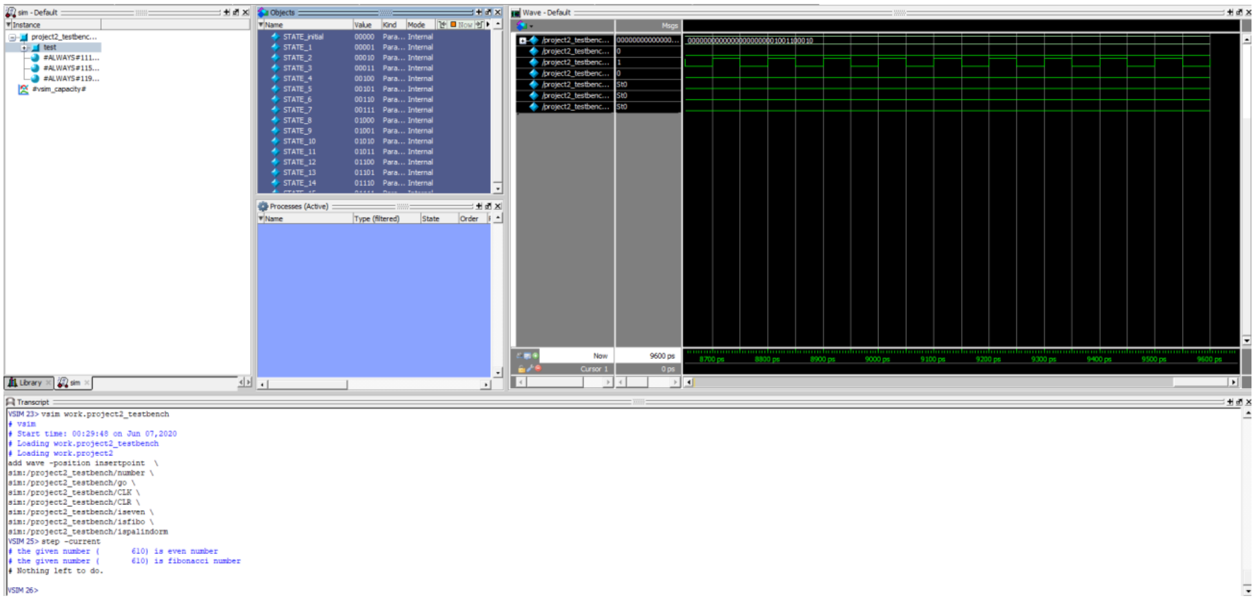
Transcript
ModelSim> vsim work.project2_testbench
vsim -gui "+altera" -l msim_transcript -do "project2_run_msim_rtl_verilog.do"
Start time: 00:19:27 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 6> step -current
the given number (44) is even number
the given number (44) is palindorm number
Nothing left to do.
VSIM 7>

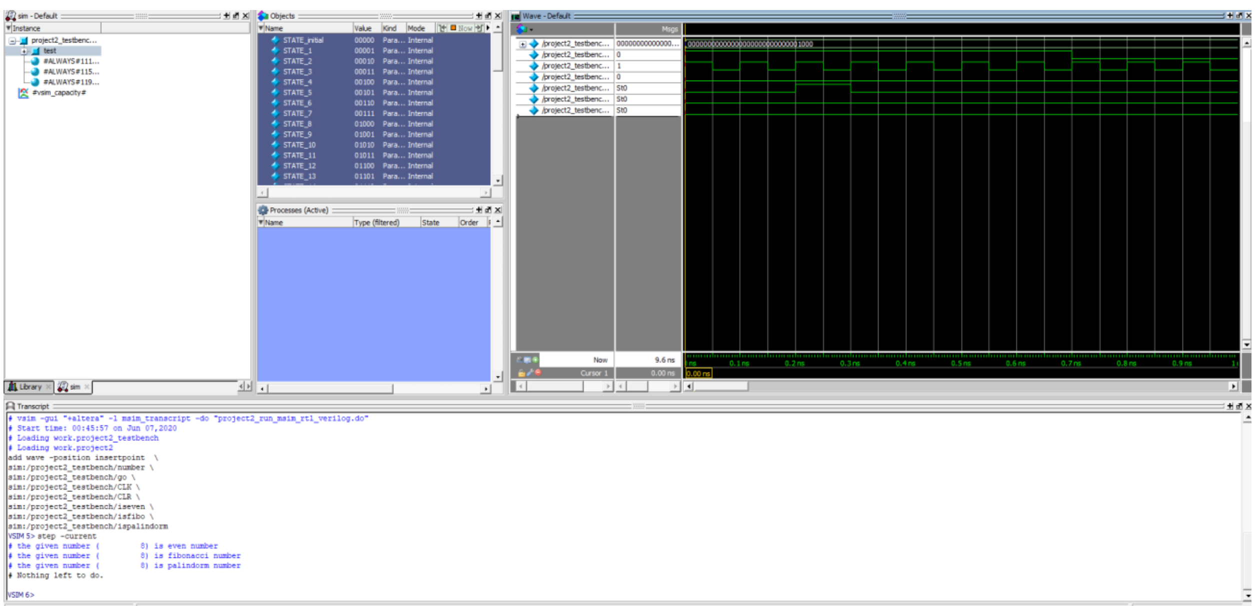


Transcript
VSIM 9> vsim work.project2_testbench
vsim
Start time: 00:21:01 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 11> step -current
the given number (55) is fibonacci number
the given number (55) is palindorm number
Nothing left to do.
VSIM 12>


sim - Default
Objects
Wave - Default
Transcript
Errors: 0, Warnings: 0
VSIM 15> vsim work.project2_testbench
vsim
Start time: 00:26:47 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 17> step -current
the given number (101) is palindorm number
Nothing left to do.
VSIM 18>


sim - Default
Objects
Wave - Default
Transcript
VSIM 19> vsim work.project2_testbench
vsim
Start time: 00:28:14 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 21> step -current
the given number (202) is even number
the given number (202) is palindorm number
Nothing left to do.
VSIM 22>


VSIM 23> vsim work.project2_testbench
vsim
Start time: 00:29:48 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 25> step -current
the given number (610) is even number
the given number (610) is fibonacci number
Nothing left to do.
VSIM 26>


vsim -gui "+altera" -l msim_transcript -do "project2_run_msim_rtl_verilog.do"
Start time: 00:45:57 on Jun 07,2020
Loading work.project2_testbench
Loading work.project2
add wave -position insertpoint \
sim:/project2_testbench/number \
sim:/project2_testbench/go \
sim:/project2_testbench/CLK \
sim:/project2_testbench/CLR \
sim:/project2_testbench/iseven \
sim:/project2_testbench/isfibo \
sim:/project2_testbench/ispalindorm
VSIM 5> step -current
the given number (8) is even number
the given number (8) is fibonacci number
the given number (8) is palindorm number
Nothing left to do.
VSIM 6>