SH69P26

OTP 6K 4-Bit Micro-controller

Features

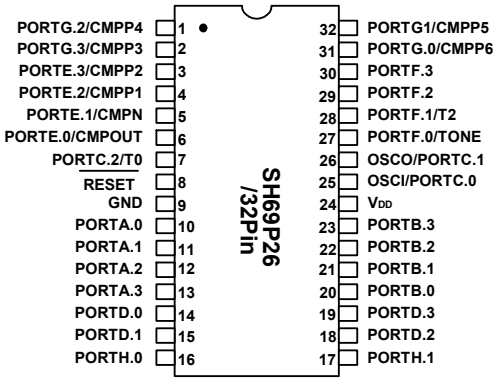
- SH6610D-based single-chip 4-bit micro-controller
- OTPROM: 6k X 16 bits
- RAM: 389 X 4 bits
  - 69 System control register
  - 320 Data memory
- Operation voltage:
  - f_{OSC} = 30kHz - 4MHz, V_{DD} = 2.4V - 5.5V
  - f_{OSC} = 4MHz - 8MHz, V_{DD} = 4.5V - 5.5V
- 29 CMOS bi-directional I/O pins
- 8-level stack (including interrupts)
- Two 8-bit auto re-loaded timer/counter, one can switch to external clock source
- Warm-up timer
- Built-in pull-high for I/O port
- Powerful interrupt sources:
  - Timer0 interrupt
  - Timer1 interrupt
  - Timer2 interrupt
  - External interrupts: PORTF (Falling edge), CMPOUT
- Oscillator (code option)
  - Crystal oscillator: 32.768kHz, 400kHz - 8MHz
  - Ceramic resonator: 400kHz - 8MHz
  - External RC oscillator: 400kHz - 8MHz
  - Internal RC oscillator: 2MHz, 4MHz, 6MHz
  - External clock: 30kHz - 8MHz
- Instruction cycle time (4/f_{OSC})
- Two low power operation modes: HALT and STOP
- Reset:
  - Built-in watchdog timer (code option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR)
- Two-level Low Voltage Reset (LVR) (code option)
- One 16-bit timer/counter for pulse measurement
- LED numeric display drive capability on PORTA, PORTB, PORTD and PORTH [1:0]
- Built-in one comparator
- Read ROM Table function
- 2 channels Tone generator
- Internal reliable reset circuit
- OTP type/code protection
- 28-pin SKINNY/28-pin SOP/32-pin DIP package

General Description

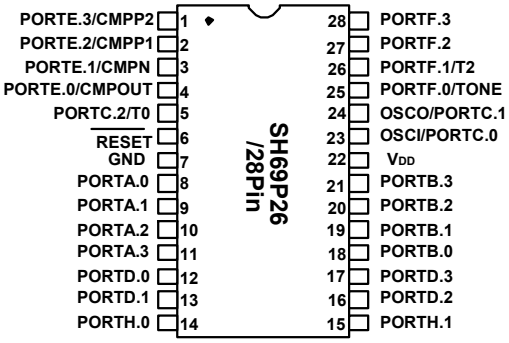
The SH69P26 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, 6K words of OTPROM, 389 nibbles of RAM, two 8-bit timer/counter and one 16-bit timer/counter, comparator, two channel tone generators, on-chip oscillator clock circuitry, on-chip watchdog timer, low voltage reset function. The SH69P26 is suitable for microwave oven application.

Pin Configuration

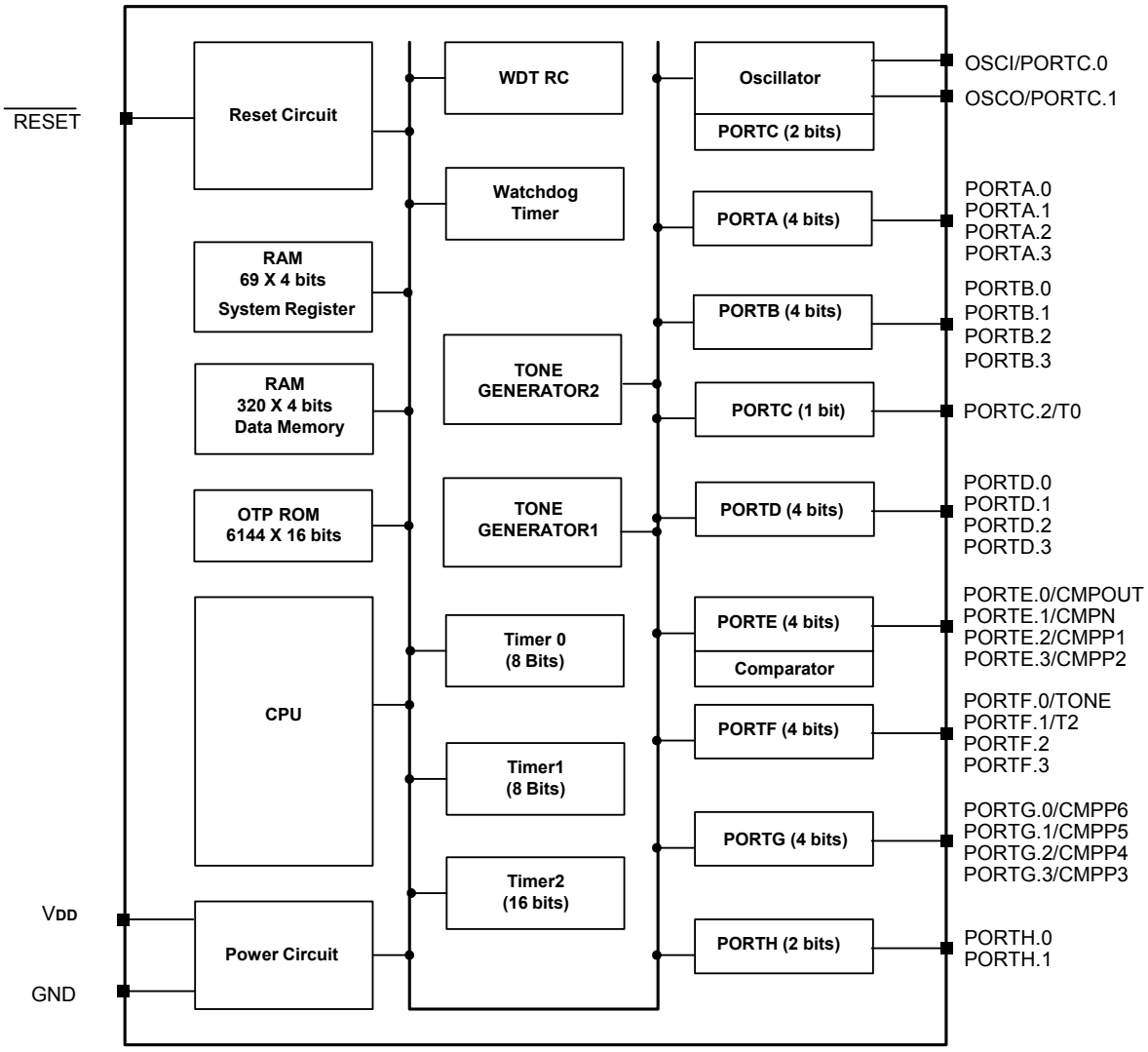
(32-Lead DIP Package)



(28-Lead SKINNY/SOP Package)



Block Diagram



Pin Description

Pin No.		Designation	I/O	Description
32-pin DIP	28-pin SKINNY/SOP			
1	-	PORTG.2 /CMPP4	I/O I	Bi-directional I/O port Shared with Comparator positive input 4
2	-	PORTG.3 /CMPP3	I/O I	Bi-directional I/O port Shared with Comparator positive input 3
3	1	PORTE.3 /CMPP2	I/O I	Bi-directional I/O port Shared with Comparator positive input 2
4	2	PORTE.2 /CMPP1	I/O I	Bi-directional I/O port Shared with Comparator positive input 1
5	3	PORTE.1 /CMPN	I/O I	Bi-directional I/O port Shared with Comparator negative input
6	4	PORTE.0 /CMPOUT	I/O O	Bi-directional I/O port Shared with Comparator output
7	5	PORTC.2 /T0	I/O I	Bi-directional I/O port Shared with Timer0 external clock input
8	6	$\overline{\text{RESET}}$ /PORTC3	I I/O	Reset pin input (low active) Bi-directional I/O port (open-drain output)
9	7	GND	P	Ground pin
10	8	PORTA.0	I/O	Bi-directional I/O port
11	9	PORTA.1	I/O	Bi-directional I/O port
12	10	PORTA.2	I/O	Bi-directional I/O port
13	11	PORTA.3	I/O	Bi-directional I/O port
14	12	PORTD.0	I/O	Bi-directional I/O port
15	13	PORTD.1	I/O	Bi-directional I/O port
16	14	PORTH.0	I/O	Bi-directional I/O port
17	15	PORTH.1	I/O	Bi-directional I/O port
18	16	PORTD.2	I/O	Bi-directional I/O port
19	17	PORTD.3	I/O	Bi-directional I/O port
20	18	PORTB.0	I/O	Bi-directional I/O port
21	19	PORTB.1	I/O	Bi-directional I/O port
22	20	PORTB.2	I/O	Bi-directional I/O port
23	21	PORTB.3	I/O	Bi-directional I/O port
24	22	V_{DD}	P	Power supply pin
25	23	OSCI /PORTC.0	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator. Shared with bi-directional I/O port in the internal RC oscillator code option

Pin Description (continued)

Pin No.		Designation	I/O	Description
32-pin DIP	28-pin SKINNY/SOP			
26	24	OSCO /PORTC.1	O I/O	Oscillator output pin, connect to crystal/ceramic oscillator Shared with bi-directional I/O port in the RC oscillator code option
27	25	PORTF.0 /TONE	I/O I O	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with TONE generator output
28	26	PORTF.1 /T2	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with Timer2 external clock input
29	27	PORTF.2	I/O I	Bi-directional I/O port Vector port interrupt. (falling edge active)
30	28	PORTF.3	I/O I	Bi-directional I/O port Vector port interrupt. (falling edge active)
31	-	PORTG.0 /CMPP6	I/O I	Bi-directional I/O port Shared with Comparator positive input6
32	-	PORTG.1 /CMPP5	I/O I	Bi-directional I/O port Shared with Comparator positive input5

OTP Programming Pin Description (OTP Program Mode)

Pin No.		Symbol	I/O	Sharing	Description
32-pin DIP	28-pin SKINNY/SOP				
24	22	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
8	6	V_{PP}	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
9	7	GND	P	GND	Ground
25	23	SCK	I	OSCI	Programming Clock input pin
10	8	SDA	I/O	PORTA.0	Programming Data pin

Function Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter cans only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
System register and I/O: $000 - $02F, $380 - $394
Data memory: $030 - $16F

2.2. Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	IET0	IET1	IET2	IEP	R/W	Interrupt enable flags
$01	IRQT0	IRQT1	IRQT2	IRQP	R/W	Interrupt request flags
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register Bit3: T0 signal source
$03	T0E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register Bit3: T0 signal edge
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble

Configuration of System Register (continued)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	CMPE	CMPSO	CMPSN	CMPEN	R/W	Comparator control register
$14	CMPGO	CMPSP2	CMPSP1	CMPSP0	R/W	Comparator status register
$15	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Set Timer2 mode Bit2: Select directive edge active enable Bit3: Set Timer2 function start
$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$19	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1A	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1B	PFCR.3	PFCR.3	PFCR.1	PFCR.0	R/W	PORTF input/output control
$1C	LVR	T2E	T2SC	-	R/W	Bit1: Select external signal source for Timer2 Bit2: Timer2 external signal source edge Bit3: Low Voltage Reset flag (Read and Write 0 only)
$1D	-	-	-	-	-	Reserved
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
$1F	-	-	-	BNK0	R/W	Bit0: Bank register for ROM
$20	PGCR.3	PGCR.2	PGCR.1	PGCR.0	R/W	PORTG input/output control In 28 pin mode, All bits of this RAM are reserved, Always keep it to “1” in the User’s program. Refer to I/O notice
$21	-	-	PHCR.1	PHCR.0	R/W	PORTH input/output control
$22	PG.3	PG.2	PG.1	PG.0	R/W	PORTG In 28 pin mode, All bits of this RAM are reserved, Always keep it to “0” in the User’s program. Refer to I/O notice
$23	-	-	PH.1	PH.0	R/W	PORTH
$24	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull high control
$25	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull high control
$26	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull high control
$27	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull high control
$28	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull high control
$29	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull high control

Configuration of System Register (continued)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$2A	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull high control
$2B	-	-	PPHCR.1	PPHCR.0	R/W	PORTH pull high control
$2C	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble
$2D	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Tone generator 1 volume high nibble TG1EN: Tone generator 1 enable
$2E	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble
$2F	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM data table address/data register
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2 load/counter register (low nibble)
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load/counter register (middle_L nibble)
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load/counter register (middle_H nibble)
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load/counter register (high nibble)
$388	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble
$389	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble
$38A	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble
$38B	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble
$38C	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble
$38D	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble
$38E	-	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 prescaler register
$38F	- CNF2	- CNF1	- CNF0	CMPOD -	R R/W	CMPOD: Comparator Output data CNF2-0: Select comparator input channel
$390	PFIEN.3	PFIEN.2	PFIEN.1	PFIEN.0	R/W	PORTF interrupt enable flags
$391	-	-	-	-	-	Reserved
$392	PFIF.3	PFIF.2	PFIF.1	PFIF.0	R/W	PORTF interrupt request flags
$393	-	-	-	-	-	Reserved
$394	-	-	CMPIF	CMPIE	R/W	Bit0: CMP output interrupt enable flag Bit1: CMP output interrupt request flag

3. ROM

The ROM can address 6144 X 16 bits of program area from $000 to $17FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to Timer0 interrupt service routine
$002	JMP*	Jump to Timer1 interrupt service routine
$003	JMP*	Jump to Timer2 interrupt service routine
$004	JMP*	Jump to PORTF or CMP service routine

*JMP instruction can be replaced by any instruction.

3.2. ROM Data Read Table (RDT)

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 13-bit write-only PC address load register (RDT.12 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble), then after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into $380 will start the data read-out action).

3.3. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The Bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to the lower 2K of ROM space (BANK.0). The upper 2K of the CPU addressing space maps to one of the two banks (BNK.0 = $00 - $01) of the upper 4K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space	
	BNK = $00	BNK = $01
$000 - $7FF	$0000 - $07FF (BANK 0)	$0000 - $07FF (BANK 0)
$800 - $FFF	$0800-$0FFF (BANK 1)	$1000 - $17FF (BANK 2)

4. Initial State

4.1. System Register State:

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset/Low Voltage Reset
$00	IET0	IET1	IET2	IEP	0000	0000
$01	IRQT0	IRQT1	IRQT2	IRQP	0000	0000
$02	T0S	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T0E	T1M.2	T1M.1	T1M.0	0000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	-	PC.2	PC.1	PC.0	-000	-000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	CMPE	CMPSO	CMPSN	CMPEN	0000	uuuu
$14	CMPGO	CMPSP2	CMPSP1	CMPSP0	0000	0uuu
$15	T2GO	DEC	TM2S1	TM2S0	0000	0uuu
$16	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$18	-	PCCR.2	PCCR.1	PCCR.0	-000	-000
$19	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1A	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1B	PFCR.3	PFCR.2	PFCR.1	PFCR.0	0000	0000
$1C	LVR	T2E	T2SC	-	000-	*uu-
$1D	-	-	-	-	----	----
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	#000
$1F	-	-	-	BNK0	---0	---0
$20	PGCR.3	PGCR.2	PGCR.1	PGCR.0	0000	0000
$21	-	-	PHCR.1	PHCR.0	--00	--00
$22	PG.3	PG.2	PG.1	PG.0	0000	0000
$23	-	-	PH.1	PH.0	--00	--00
$24	PPACR.3	PPACR.2	PPACR.1	PPACR.0	0000	0000
$25	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	0000	0000
$26	-	PPCCR.2	PPCCR.1	PPCCR.0	-000	-000
$27	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	0000	0000
$28	PPECR.3	PPECR.2	PPECR.1	PPECR.0	0000	0000

System Register State: (continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset/Low Voltage Reset
$29	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	0000	0000
$2A	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	0000	0000
$2B	-	-	PPHCR.1	PPHCR.0	--00	--00
$2C	TV1.3	TV1.2	TV1.1	TV1.0	xxxx	uuuu
$2D	TG1EN	TV1.6	TV1.5	TV1.4	xxxx	uuuu
$2E	TV2.3	TV2.2	TV2.1	TV2.0	xxxx	uuuu
$2F	TG2EN	TV2.6	TV2.5	TV2.4	xxxx	uuuu
$380	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$381	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$382	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$383	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$384	T2D.3	T2D.2	T2D.1	T2D.0	xxxx	xxxx
$385	T2D.7	T2D.6	T2D.5	T2D.4	xxxx	xxxx
$386	T2D.11	T2D.10	T2D.9	T2D.8	xxxx	xxxx
$387	T2D.15	T2D.14	T2D.13	T2D.12	xxxx	xxxx
$388	TG1.3	TG1.2	TG1.1	TG1.0	xxxx	uuuu
$389	TG1.7	TG1.6	TG1.5	TG1.4	xxxx	uuuu
$38A	TG1.11	TG1.10	TG1.9	TG1.8	xxxx	uuuu
$38B	TG2.3	TG2.2	TG2.1	TG2.0	xxxx	uuuu
$38C	TG2.7	TG2.6	TG2.5	TG2.4	xxxx	uuuu
$38D	TG2.11	TG2.10	TG2.9	TG2.8	xxxx	uuuu
$38E	-	T2SC.2	T2SC.1	T2SC.0	-000	-uuu
$38F	- CNF2	- CNF1	- CNF0	CMPOD -	0000	uuu0
$390	PFIEN.3	PFIEN.2	PFIEN.1	PFIEN.0	0000	0000
$391	-	-	-	-	----	----
$392	PFIF.3	PFIF.2	PFIF.1	PFIF.0	0000	0000
$393	-	-	-	-	----	----
$394	-	-	CMPIF	CMPIE	--00	--00

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

***, #: For the detail information, refer to the following table:**

Symbol	WDT reset	LVR reset	WDT reset & LVR reset	Power-on reset/Pin reset
*	0	1	1	0
#	1	0	1	0

4.2. Others Initial State:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

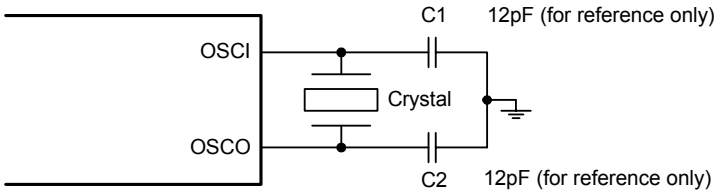
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = f**osc**/4.

5.1. Instruction Cycle Time:

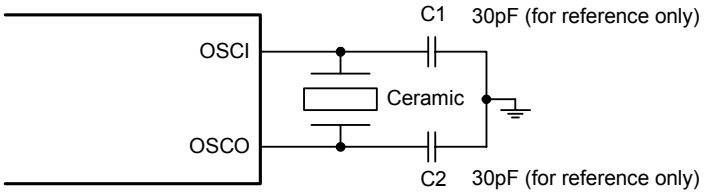
(1) 4/32.768kHz (≈ 122.1μs) for 32.768kHz oscillator.
(2) 4/8MHz (= 0.5μs) for 8MHz oscillator.

5.2. Oscillator Type

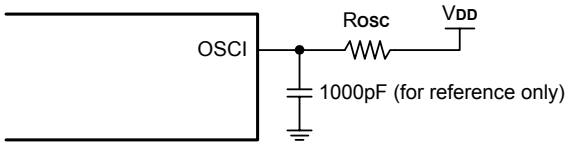
(1) Crystal oscillator: 32.768kHz or 400kHz - 8MHz



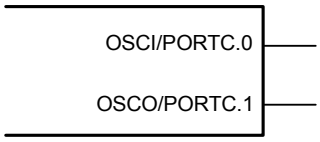
(2) Ceramic resonator: 400kHz - 8MHz



(3) RC oscillator: 400kHz - 8MHz

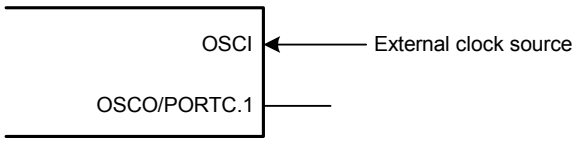


External R**osc** RC



Internal R**osc** RC (f**osc** = 2MHz or 4MHz or 6MHz)

(4) External input clock: 30kHz - 8MHz



Note:

- If the RC oscillator or the external input clock is selected, OSCO pin is used as the I/O port (PORTC.1).
- If the internal RC oscillator is selected, OSCO pin is used as the I/O port (PORTC.1) as well as OSCI pin is used as the PORTC.0.

Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
455kHz	47 - 100pF	47 - 100pF	ZT 455E	JingBo Electronic Shenzhen
3.58MHz	-	-	ZT 3.58M*	JingBo Electronic Shenzhen
4MHz	-	-	ZT 4M*	JingBo Electronic Shenzhen

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3 X 8)	KDS
4MHz	8 - 15pF	8 - 15pF	49S-4.000M-F16E	JingBo Electronic Shenzhen
8MHz	8 - 15pF	8 - 15pF	49S-8.000M-F16E	JingBo Electronic Shenzhen

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures

6. I/O Ports

The MCU provides 29 bi-directional I/O ports. The PORT data put in register $08 - $0D, $22 - $23. The PORT control register ($16 - $21) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by the value of the corresponding bit in the pull-high control register ($24 - $2B), independently.

- When the port is selected as an input port, write "1" to the relevant bit in the port pull-high control register ($24 - $2B) could turn on the pull-high resistor and write "0" could turn off the pull-high resistor.
- When the port is selected as output port, the pull-high resistor will be turned off automatically, regardless the value of the corresponding bit in the port pull-high control register ($24 - $2B).
- When PORTF is selected as the digital input direction, they can active port interrupt by falling edge (if port interrupt is enabled).

System Register $08 - $0D, $22 - $23: Port Data Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF
$22	PG.3	PG.2	PG.1	PG.0	R/W	PORTG
$23	-	-	PH.1	PH.0	R/W	PORTH

Note: In 28 pin mode, All bits of the $22 RAM are reserved, Always keep it to "0" in the User's program.

System Register Port $16 - $1B, $20 - $21: Port Control Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$19	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1A	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1B	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control
$20	PGCR.3	PGCR.2	PGCR.1	PGCR.0	R/W	PORTG input/output control
$21	-	-	PHCR.1	PHCR.0	R/W	PORTH input/output control

Note: In 28 pin mode, All bits of the $20 RAM are reserved, Always keep it to "1" in the User's program.

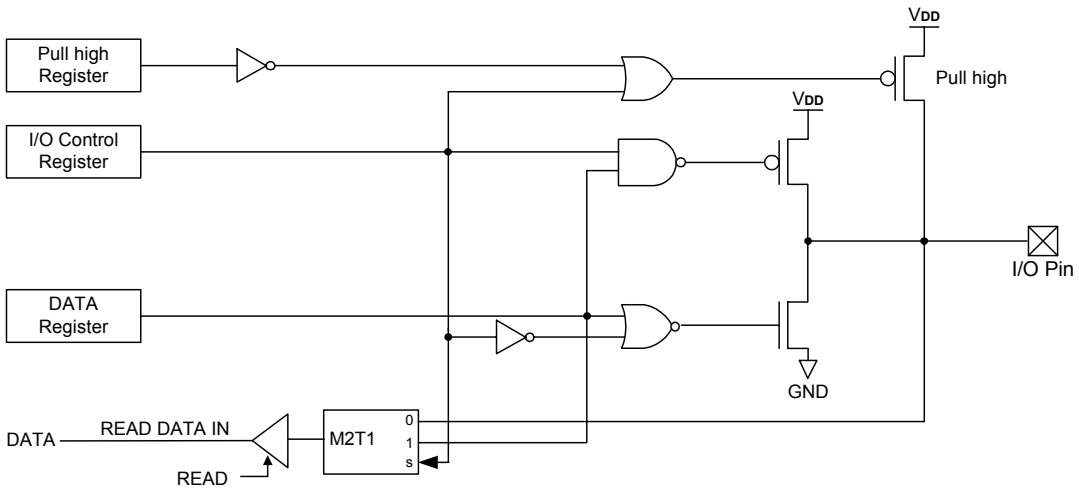
PA (/B/C/D/E/F/G/H) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

System Register $24 - $2B: Port Pull-high Control Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$24	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull-high control
$25	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull-high control
$26	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull-high control
$27	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull-high control
$28	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull-high control
$29	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull-high control
$2A	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull-high control
$2B	-	-	PPHCR.1	PPHCR.0	R/W	PORTH pull-high control

PPA (/B/C/D/E/F/G/H) CR.n, (n = 0, 1, 2, 3)
0: Disable internal pull-high resistor. (Power on initial)
1: Enable internal pull-high resistor.

Equivalent Circuit for a Single I/O Pin



In SH69P26, each output port contains a latch, which can hold the output data. Writing the port data register (PDR) under the output mode can directly transfer data to the corresponding pad.

All input ports do not have latches, so the external input data should be held externally until the input data is read from outside or reading the port data register (PDR) under the input mode

When a digital I/O port is selected to be an output, the reading of the associated port bit actually represents the value of the output data latch, not the voltage on the pad.

When a digital I/O port is selected to be an input, the reading of the associated port bit represents the status on the corresponding pad.

PORTA, PORTB, PORTD and PORTH have powerful drive ability, and they can drive LED numeric display directly. PORTB, PORTD [3:2], PORTH can source 25mA current. PORTA, PORTD [1:0] can sink 200mA current. For detail information, please reference the application circuit.

- PORTC.2 can be shared with T0 input,
- PORTE.0 can be shared with Comparator Output,
- PORTE.1 can be shared with Comparator negative input,
- PORTE.2 can be shared with Comparator positive input1,
- PORTE.3 can be shared with Comparator positive input2,
- PORTF.0 can be shared with TONE output,
- PORTF.1 can be shared with T2 input,
- PORTG.0 can be shared with Comparator positive input6,
- PORTG.1 can be shared with Comparator positive input5,
- PORTG.2 can be shared with Comparator positive input4,
- PORTG.3 can be shared with Comparator positive input3,
- The OSCI pin can be shared with PORTC.0, if the SH69P26 uses the internal RC oscillator as the system oscillation.
- The OSCO pin can be shared with PORTC.1, if the SH69P26 uses the External clock or the RC oscillator as the system oscillation.
- Reset pin can be share as PORTC.3 (open drain).

Note:

1. PORTA, PORTD [1:0] can sink 200mA current. However only one PORT can be used to sink as large as 200mA current in the same time.
2. If external Reset pin is enabled (PORTC.3 is shared as Reset pin), SH69P26 will provide better performance on Electro Magnetic Compatibility (EMC).

Port Interrupt & CMP Interrupt

The PORTF are used as external port interrupt sources. Since PORTF are bit programmable I/Os, only the voltage transition from V_{DD} to GND applying to the digital input port can generate a external interrupt. The analog input cannot generate any interrupt request. Rising or falling on the comparator output can also generate external interrupt.

The interrupt control flags are mapped on $390, $392and $394 of the system register. They can be accessed or tested by the read or write operation. Those flags are cleared to "0" at the initialization by the chip reset.

Port Interrupts (including comparator output interrupt) can be used to wake up the CPU from the HALT or the STOP mode.

System Register $390: Port Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$390	PFIEN.3	PFIEN.2	PFIEN.1	PFIEN.0	R/W	PORTF interrupt enable flags

PFIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Power on initial)
1: Enable port interrupt.

System Register $392: Port Interrupt Request Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$392	PFIF.3	PFIF.2	PFIF.1	PFIF.0	R/W	PORTF interrupt request flags

PFIF.n, (n = 0, 1, 2, 3)
0: Port interrupt is not presented. (Power on initial)
1: Port interrupt is presented.
Only writing these bits to 0 is available.

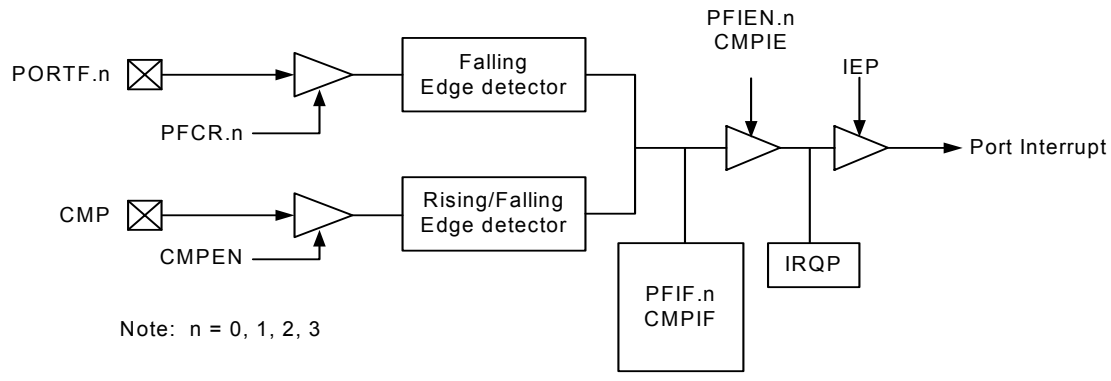
System Register $394: Comparator Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$394	-	-	CMPIF	CMPIE	R/W	Bit0: CMP output interrupt enable flag Bit1: CMP output interrupt request flag

CMPIE
0: CMP output interrupt disable. (Power on initial)
1: CMP output interrupt enable.

CMPIF
0: CMP output interrupt not presented (Power on initial)
1: CMP output interrupt presented
Only writing these bits to 0 is available.

Following is the port interrupt function block-diagram for reference.



Programming Note:

When the Port falling edge is active, any one of I/O input pin transitions from V_{DD} to GND would set PFIF.x to "1". Together, if the PFIEN.x = 1, the port would generate an interrupt request (IRQP = 1).

Port Interrupt can wake the CPU from HALT or STOP mode.

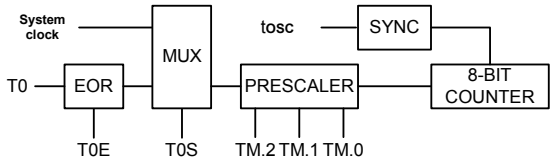
7. Timer

7.1. Timer0/Timer1

The device has three timers: two 8-bit timers (Timer0, Timer1) and one 16-bit timer (Timer2).

The Timer0/Tiemr1 has the following features:
- 8-bit up-counting timer/counter
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer0/Timer1 block diagram.



The Timers provide the following functions:
- Programmable interval timer function.
- Read counter value.

7.1.1. Timer0/Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter. Each of them has both low-order digits and high-order digits. Writing data into the timer load register (T0L, T0H; T1L, T1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

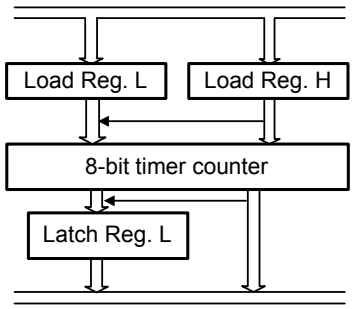
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



7.1.2. Timer0/Timer1 Mode Register

The Timer0/Timer1 can be programmed in several different prescalers by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler overflows output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table 1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1 Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

Table 2 Timer1 Mode Register ($03)

T1M.2	T1M.1	T1M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

7.1.3. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock (System clock/4). The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t**osc**) and low (at least 2 t**osc**). When the prescaler ratio selects /2^0, it is the same as the system clock input.

The requirement is as follows

T0H (T0 high time) $\geq$ 2 * t**osc** + ΔT

T0L (T0 low time) $\geq$ 2 * t**osc** + ΔT ; ΔT = 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value (2^0, 2^1, 2^2, 2^3, 2^5, 2^7, 2^9, 2^{11})

The requirement is:

$$\frac{N * T0}{2} \geq 2 * tosc + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0} = \text{Timer0 period} \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

Timer0 Mode Register: $02

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$02	T0S	-	-	-	R/W	Bit3: T0 signal source
	0	X	X	X	R/W	Shared with PORTC.2, Timer0 source is system clock
	1	X	X	X	R/W	Shared with T0 input, Timer0 source is T0 input clock

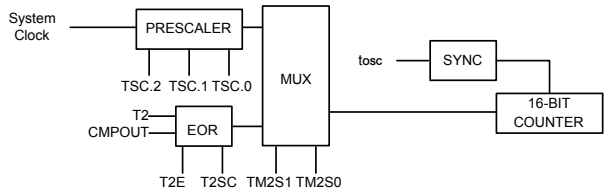
Timer0 Mode Register: $03

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	T0E	-	-	-	R/W	Bit3: T0 signal edge
	0	X	X	X	R/W	Falling edge active
	1	X	X	X	R/W	Rising edge active

7.2. Timer2

Timer2 is a 16-bit timer, and it has the following features:
- 16-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FFFF to $0000.

The following is a simplified Timer2 block diagram.



The Timer2 provides the following functions:
- Programmable interval timer function.
- Read counter value.

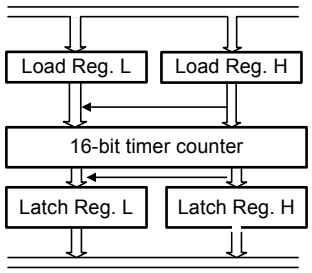
7.2.1. Timer2 Configuration and Operation

Timer2 consists of a 16-bit write-only timer load register (T2DL, T2DML, T2DMH, T2DH) and a 16-bit read-only timer counter. Each of them has low-order digits and high-order digits. Writing data into the timer load register (T2DL, T2DML, T2DMH, T2DH) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FFFF to $0000.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:
Write Operation:
Low nibble first
High nibble to update the counter
Read Operation:
High Nibble first
Low nibble followed.



7.2.2. Timer2 Control Register

The Timer2 can be programmed in several different modes: timer, external event counter, external trigger timer and pulse width measurement.

Timer2 Control Register: $15

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select Bit2: Select directive edge active enable Bit3: Set Timer2 function start
	X	X	0	0	R/W	Timer with internal system clock
	X	X	0	1	R/W	Event counter with external signal source
	X	X	1	0	R/W	Timer with external trigger
	X	X	1	1	R/W	Pulse width measurement
	0	X	X	X	R/W	Timer/counter stops (Read: status; Write: command) (default)
	1	X	X	X	R/W	Timer/counter starts (Read: status; Write: command)

7.2.3. Timer2 External Signal Source (ESS) Select Register

T2 pin input and comparator output (CMPOUT) can be selected as timer2 external signal source (ESS). If T2 pin input is selected as timer2 external signal source, PORTF.1 is shared as T2 pin. Otherwise, PORTF.1 is shared as I/O. Timer2 external signal source can be selected from CMPOUT, while PORTE.0 is shared as CMPOUT.

Timer2 External Signal Source Select Register: $1C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	-	T2E	T2SC	-	R/W	Bit1: Select external signal source for Timer2 Bit2: Timer2 external signal source edge Bit3: Low Voltage Reset flag (Read and Write 0 only)
	X	X	0	X	R/W	External signal source (ESS) is from T2, if T2SC = 0. PORTF.1 is shared as T2
	X	X	1	X	R/W	External signal source (ESS) is from CMPOUT, if T2SC = 1. PORTF.1 is shared as I/O.
	X	0	X	X	R/W	Falling edge is active, if external signal source is selected for timer2
	X	1	X	X	R/W	Rising edge is active, if external signal source is selected for timer2

7.2.4. Timer Mode

In this mode, Timer2 is performed using the internal clock. The contents of the Timer2 counter register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the T2GO (bit3) in the Timer2 control register ($15) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) bit1 (IET2) is set to “1”.

After the T2GO (bit3) in the Timer2 control register ($15) has been set to “1”, writing the Timer2 counter register ($384 - $387) cannot affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($15) has been reset to 0, the revised contents of the Timer2 counter register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

Timer2 Prescaler Register: $38E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38E	-	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 prescaler register
	X	0	0	0	R/W	Timer clock: System clock/2^{11}
	X	0	0	1	R/W	Timer clock: System clock/2^{9}
	X	0	1	0	R/W	Timer clock: System clock/2^{7}
	X	0	1	1	R/W	Timer clock: System clock/2^{5}
	X	1	0	0	R/W	Timer clock: System clock/2^{3}
	X	1	0	1	R/W	Timer clock: System clock/2^{2}
	X	1	1	0	R/W	Timer clock: System clock/2^{1}
	X	1	1	1	R/W	Timer clock: System clock/2^{0}

7.2.5. External Event Counter Mode

In this mode, Timer2 is performed using the external signal source (ESS), which is selected by T2S and T2SC in the Timer2 external signal source select register ($1C). The external events are counted at the edge of ESS. Either the rising or falling edge can be selected with the external trigger controlled by the status of the T2E (bit2) in the Timer2 external signal source select register ($1C). The contents of the Timer2 counter register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the T2GO (bit3) in the Timer2 control register ($15) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000, if the Interrupt enable register ($00) bit1 (IET2) is set to “1”.

After the T2GO (bit3) in the Timer2 control register ($15) has been set to “1”, writing the Timer2 counter register ($384 - $387) cannot affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($15) has been reset to 0, the revised contents of the Timer2 counter register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The external clock source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t**osc**) and low (at least 2 t**osc**). In this mode, the prescaler circuit will not affect the external clock input. That means the input clock will bypass the prescaler circuit, regardless the real value written by programming. So, the limitation is applied for the external clock period (T_E) time described as follows:

$$T_E \text{ (period time)} \geq 4 * t_{osc} + 2 * \Delta T \qquad ; \Delta T = 20ns$$

7.2.6. External Trigger Timer Mode

In this mode, the counting is triggered by an external signal. This trigger is the edge of the ESS input. Either the rising or falling edge can be selected with the external trigger controlled by the status of the T2E (bit2) in the Timer2 external signal source select register ($1C). But the source clock of the up-counter is an internal clock. The contents of the Timer2 counter register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. Only after the T2GO (bit3) in the Timer2 control register ($15) has been set to 1, a proper edge signal on the ESS input can start counting. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) bit1 (IET2) is set to "1". When the Timer2 interrupt is generated the up-counter is HALTed. The up-counter is restarted by the next selected edge of the ESS input.

When DEC (bit2) in the Timer2 control register ($15) is 1, inputting the edge to the reverse direction of the trigger edge selected by the former programming to start counting stops the operating and then re-load contents from the Timer2 counter register ($384 - $387). Inputting a proper constant pulse width can generate interrupts. When DEC (bit2) in the Timer2 control register ($15) is 0, the reverse directive edge input is ignored. The ESS input another active edge before the up-counter overflowing is also ignored.

After the T2GO (bit3) in the Timer2 control register ($15) has been set to "1", writing the Timer2 counter register ($384 - $387) can not affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($15) has been reset to 0, the revised contents of the Timer2 counter register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The ESS input signal must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 1/2 $t_{Timer\ clock}$) and low (at least 1/2 $t_{Timer\ clock}$). In this mode, the real value of the Timer clock is selected by the state in the Timer2 prescaler register. So, the limitation is applied for the external clock period (T_E) time described as follows:

T_E (period time) $\geq 1 * t_{Timer\ clock} + 2 * \Delta T$; $\Delta T = 20ns$

T_E (period time) $\geq (M * t_{OSC}) + 2 * \Delta T$

where M = 2^3, 2^4, 2^5, 2^6, 2^8, 2^{10}, 2^{12} or 2^{14}

Timer2 Control Register: $15 (under the external trigger timer mode)

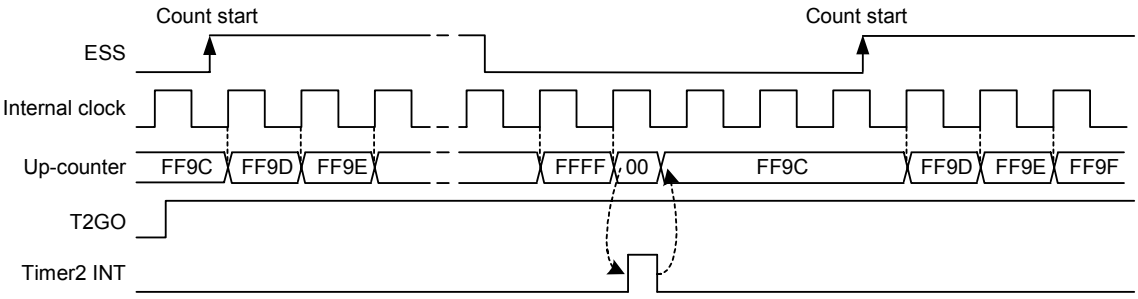
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select
	X	0	X	X	R/W	Bit2: Reverse directive edge input is ignored
	X	1	X	X	R/W	Bit2: Reverse directive edge input reloadsinternal up-counter

Timer2 Prescaler Register: $38E (under the external trigger timer mode and pulse width measurement mode)

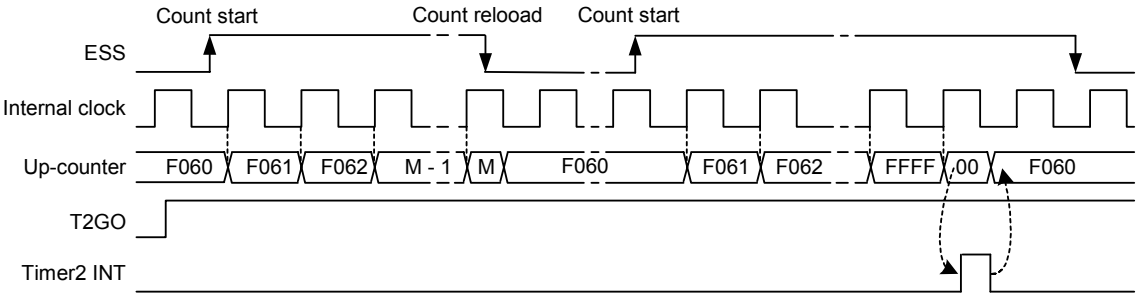
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38E	-	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 prescaler register
	X	0	0	0	R/W	Timer clock: System clock/2^{12}
	X	0	0	1	R/W	Timer clock: System clock/2^{10}
	X	0	1	0	R/W	Timer clock: System clock/2^8
	X	0	1	1	R/W	Timer clock: System clock/2^6
	X	1	0	0	R/W	Timer clock: System clock/2^4
	X	1	0	1	R/W	Timer clock: System clock/2^3
	X	1	1	0	R/W	Timer clock: System clock/2^2
	X	1	1	1	R/W	Timer clock: System clock/2^1

Timer2 Counter Register: $384 - $387

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2 load/counter register low nibble
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load/counter register middle_L nibble
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load/counter register middle_H nibble
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load/counter register high nibble



Trigger Start (DEC = 0)



Trigger Start and Stop (DEC = 1)

7.2.7. Pulse Width Measurement Mode

In this mode, Timer2 is performed using a special function under the timer mode in which counting is started on an edge of pulse waveform, which is from ESS input. It is possible to measure the width of the pulse waveform by reading the up-counter values on state transitions of the pulse. The rising or falling edge of the pulse is selected by setting the T2E (bit2) in the Timer2 External Signal Source Select Register ($1C). But the source clock of the up-counter is an internal clock selected by proper setting the T2SC (bit2-0) in the Timer2 prescaler register ($38E). When the T2GO (bit3) in the Timer2 control register ($15) is set to “1”, the contents of the up-counter must reset to “0000H”, automatically. Then a rising (falling) edge signal of the pulse triggers the up-counter to start counting. At the next falling (rising) edge, the counter value is loaded to the Timer2 counter register ($384 - $387), individually. Simultaneously, the Timer2 interrupt is generated if the Interrupt enable register ($00) bit1 (IET2) is set to 1.

When DEC (bit2) in the Timer2 control register ($15) is 0, the Timer2 is in the one-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 - $387) at first, then will be cleared again and the counter is HALTed. When the next rising edge applies, the up-counter starts counting for another measurement cycle.

When DEC (bit2) in the Timer2 control register ($15) is 1, the Timer2 is in the double-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 - $387) at first, then the counter continues counting. When the next rising edge applies, the Timer2 interrupt request is also generated. At this time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 - $387) again, then the counter must be cleared and can be continued to start counting following measurement cycles.

In this mode, writing the Timer2 counter register ($384 - $387) at any time cannot affect the up-counter operating anymore.

In this mode, the pulse signal must follow certain constraints as in the external trigger timer mode. So, the limitation is applied for the external clock period (TE) time described as follows:

T_E (period time) ≥ 1 * $t_{Timer\ clock}$ + 2 * ΔT ; ΔT = 20ns

T_E (period time) ≥ (M * t_{OSC}) + 2 * ΔT

Where M (prescaler value for Timer2 internal clock) = 2^3, 2^4, 2^5, 2^6, 2^8, 2^{10}, 2^{12}or 2^{14}

But, in order to correctly get the pulse measurement value in programming, a sufficient wait period must be needed for the relevant Timer2 interrupt subroutine program.

So, if DEC (bit2) in the Timer2 control register ($15) is 0, the Timer2 is in the one-edge capture operation. The limitation is applied for the external clock period (TE) time described as follows:

T_E (period time) ≥ 14 * $t_{System\ clock}$

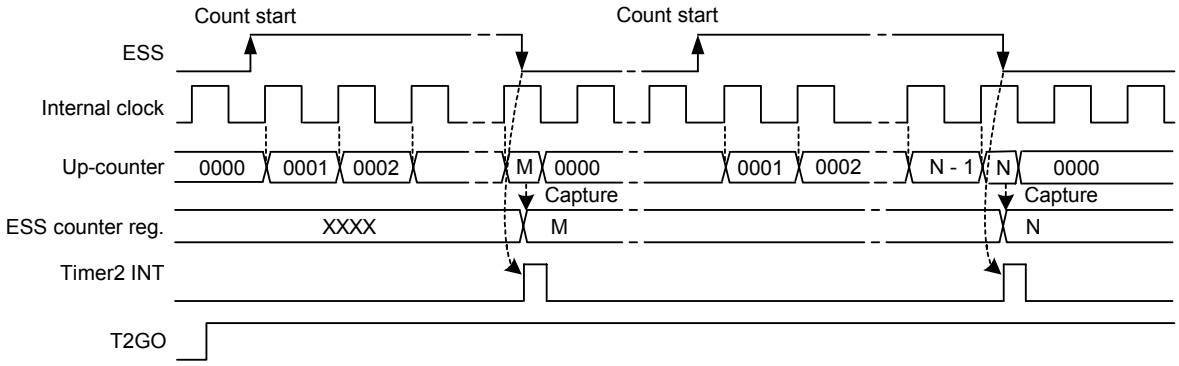
T_E (period time) ≥ 14 * 4 * t_{OSC}

The maximum value of these two equations shown above is valid to the proper application.

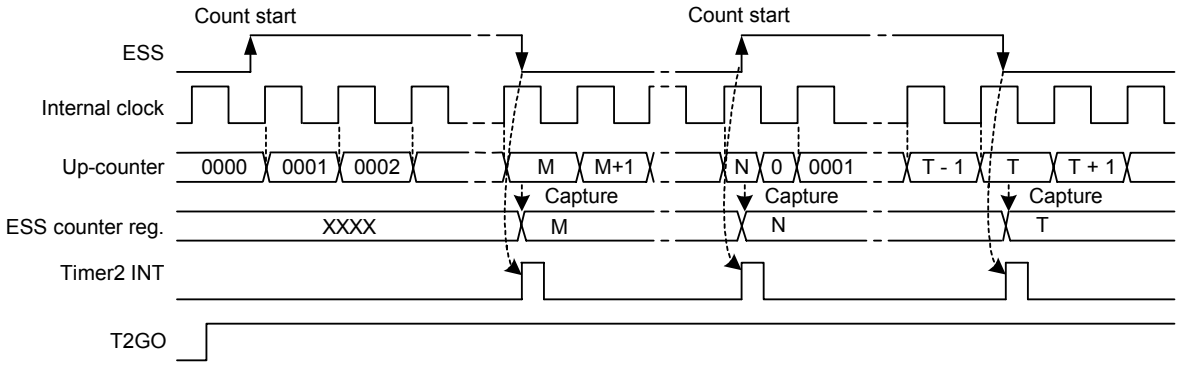
If DEC (bit2) in the Timer2 control register ($15) is 1, the Timer2 is in the double-edge capture operation. The limitation is applied for the ESS input signal high or low level period described as follows:

T_E (high or low level period time) ≥ 14 * $t_{System\ clock}$

T_E (high or low level period time) ≥ 14 * 4 * t_{OSC}



One edge capture (DEC = 0)



Double edge capture (DEC = 1)

Timer2 Control Register: $15 (under the pulse width measurement mode)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select
	X	0	X	X	R/W	Bit2: One edge capture
	X	1	X	X	R/W	Bit2: Double edge capture

8.Interrupt

Four interrupt sources are available on SH69P26:
- Timer0 interrupt
- Timer1 interrupt
- Timer2 interrupt
- External interrupts (including PORTF interrupts, comparator interrupt)

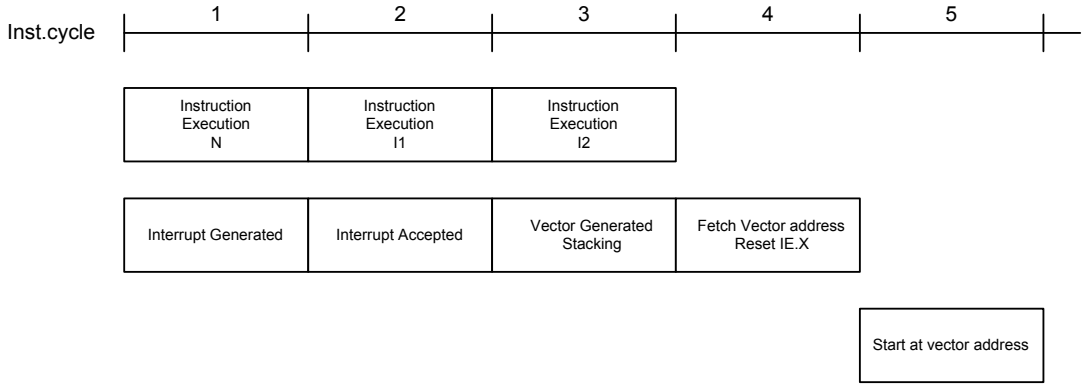
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IET0	IET1	IET2	IEP	R/W	Interrupt enable flags
$01	IRQT0	IRQT1	IRQT2	IRQP	R/W	Interrupt request flags

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into the stack memory and jump to the interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Timer (Timer0, Timer1, Timer2) Interrupt

The input clock of Timer0, Timer1 and Timer2 are based on system clocks or external clock/event T0 input as Timer0 source and ESS input as Timer2 source. The timer overflow from $FF to $00 (from $FFFF to $0000 for Timer2) will generate an internal interrupt request (IRQT0, IRQT1 = 1 or IRQT2 = 1), If the interrupt enable flag is enabled (IET0, IET1 = 1 or IET2 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from the HALT mode.

External Interrupt

Only the digital input port can generate an external interrupt. The analog input cannot generate an interrupt request. Any one of the PORTF input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1).

Rising or falling on the comparator output can also generate external interrupt.

Port Interrupt (including comparator output interrupt) can be used to wake the CPU from HALT or STOP mode.

Port Interrupts by Bit

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$390	PFIEN.3	PFIEN.2	PFIEN.1	PFIEN.0	R/W	PORTF edge to interrupt enable
$392	PFIF.3	PFIF.2	PFIF.1	PFIF.0	R/W	PORTF edge detector flag

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$394	-	-	CMPIF	CMPIE	R/W	Bit0: CMP output interrupt enable flag Bit1: CMP output interrupt request flag

Application Notice:

When the Port falling edge is active, any one of PORTF input pin transitions from V_{DD} to GND would set PFIF.x to “1”. Together, if the PFIEN.x = 1, the port would generate an interrupt request (IRQP = 1).

Port Interrupt can wake the CPU from HALT or STOP mode.

Rising or falling on the comparator output would set CMPIF to “1”. Together, if the CMPIE = 1, the port would generate an interrupt request (IRQP = 1).

Comparator Interrupt can also wake the CPU from HALT or STOP mode.

9. Analog Comparator (CMP)

Comparator includes 1 negative input, 6 positive inputs and 1 output. Each of them can be selected individually by comparator control register (CCR). When CMPEN is set to 1, the comparator enables. PORTE.1 input or internal reference voltage (V_{DD}/2) can be selected as comparator negative input. One or more positive input should be selected. PORTE.0 can be shared as comparator output, if it is necessary. The rising or falling edge (selected by CMPE) will generate a CMP interrupt.

System Register $13: Analog Comparator Control Register (CMPC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	CMPE	CMPSO	CMPSN	CMPEN	R/W	Comparator control register
	X	X	X	1	R/W	Comparator enable
	X	X	X	0	R/W	Comparator disable
	X	X	1	X	R/W	PORTE.1 input is selected as comparator negative input
	X	X	0	X	R/W	Internal reference voltage (V_{DD}/2) is selected as comparator negative input
	X	1	X	X	R/W	PORTE.0 is shared as CMPOUT
	X	0	X	X	R/W	PORTE.0 is shared as I/O
	1	X	X	X	R/W	Comparator output rising edge generate interrupt
	0	X	X	X	R/W	Comparator output falling edge generate interrupt

Comparator Data Register: ($38F)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38F	- CNF2	- CNF1	- CNF0	CMPOD -	R R/W	CMPOD: Comparator output data CNF2-0: Select comparator input channel

At any time, if comparator is operating, CMPOD equals the comparator output.

Comparator Data Register: ($38F)

CNF2	CNF1	CNF0	5	4	3	2	1	0
0	0	0	PORTG.0	PORTG.1	PORTG.2	PORTG.3	PORTE.3	PORTE.2
0	0	1	PORTG.0	PORTG.1	PORTG.2	PORTG.3	PORTE.3	CMPP1
0	1	0	PORTG.0	PORTG.1	PORTG.2	PORTG.3	CMPP2	CMPP1
0	1	1	PORTG.0	PORTG.1	PORTG.2	CMPP3	CMPP2	CMPP1
1	0	0	PORTG.0	PORTG.1	CMPP4	CMPP3	CMPP2	CMPP1
1	0	1	PORTG.0	CMPP5	CMPP4	CMPP3	CMPP2	CMPP1
1	1	0	CMPP6	CMPP5	CMPP4	CMPP3	CMPP2	CMPP1
1	1	1	CMPP6	CMPP5	CMPP4	CMPP3	CMPP2	CMPP1

Comparator Status Register ($14)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	CMPGO	CMPSP2	CMPSP1	CMPSP0	R/W	Comparator Status Register
	X	0	0	0	R/W	Comparator positive input is from CMPP1
	X	0	0	1	R/W	Comparator positive input is from CMPP2
	X	0	1	0	R/W	Comparator positive input is from CMPP3
	X	0	1	1	R/W	Comparator positive input is from CMPP4
	X	1	0	0	R/W	Comparator positive input is from CMPP5
	X	1	0	1	R/W	Comparator positive input is from CMPP6
	X	1	1	0	R/W	Comparator positive input is from CMPP6
	X	1	1	1	R/W	Comparator positive input is from CMPP6
	1	X	X	X	R/W	Comparator output is valid
	0	X	X	X	R/W	Comparator output is invalid, and the output always equal zero

Note:

1. Before enable the comparator, these registers must be set correctly. Forbid connecting analog signal to any digital I/O.
2. When set CMPEN to 1, system will take 3us to setup the comparator, including internal V_{DD}/2. So wait 5us before set CMPGO to 1
3. When set CMPGO to 1, positive input or negative input channel cannot be changed. If it is necessary to change positive input or negative channel, clear CMPGO bit, when the change is finished, set CMPGO to 1 again.

10. Dual Tone

Two Channel Tone is provided. They are the 12-bit pseudo random counter. To reduce power consumption, disable the sound effect generator during both STOP and HALT statuses.

Tone Generator Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble
$389	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble
$38A	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble
$38B	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble
$38C	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble
$38D	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble

Tone Generator Volume Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2C	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble
$2D	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Tone generator 1 volume high nibble TG1EN: Tone generator 1 enable
$2E	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble
$2F	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable

The volume control register has 7 bits used to control the output level of the tone generator.
TGxEN: Tone generator X enable
0: Tone generator X disable (Power on initial) 1: Tone generator X enable
Note: X = 1 or 2

Programming Notice:

Never execute the "HALT" or "STOP" instruction while the Tone Generator is playing.

Music Table 1.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSC = 4MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B2	123.47	4050	02E	123.46	-0.01	**#F5**	739.99	676	D5C	739.64	-0.05
C3	130.81	3822	112	130.82	0.01	**G5**	783.99	638	D82	783.70	-0.04
#C3	138.59	3608	1E8	138.58	-0.01	**#G5**	830.61	602	DA6	830.56	-0.01
D3	146.83	3405	2B3	146.84	0.01	**A5**	880.00	568	DC8	880.28	0.03
#D3	155.56	3214	372	155.57	0.00	**#A5**	932.33	536	DE8	932.84	0.06
E3	164.81	3034	426	164.80	-0.01	**B5**	987.77	506	E06	988.14	0.04
F3	174.61	2863	4D1	174.64	0.02	**C6**	1046.5	478	E22	1046.0	-0.05
#F3	185.00	2703	571	184.98	-0.01	**#C6**	1108.7	451	E3D	1108.7	-0.01
G3	196.00	2551	609	196.00	0.00	**D6**	1174.7	426	E56	1173.7	-0.08
#G3	207.65	2408	698	207.64	-0.01	**#D6**	1244.5	402	E6E	1243.8	-0.06
A3	220.00	2273	71F	219.97	-0.01	**E6**	1318.5	379	E85	1319.3	0.06
#A3	233.08	2145	79F	233.10	0.01	**F6**	1396.9	358	E9A	1396.7	-0.02
B3	246.94	2025	817	246.91	-0.01	**#F6**	1480.0	338	EAE	1479.3	-0.05
C4	261.63	1911	889	261.64	0.01	**G6**	1568.0	319	EC1	1567.4	-0.04
#C4	277.18	1804	8F4	277.16	-0.01	**#G6**	1661.2	301	ED3	1661.1	-0.01
D4	293.66	1703	959	293.60	-0.02	**A6**	1760.0	284	EE4	1760.6	0.03
#D4	311.13	1607	9B9	311.14	0.00	**#A6**	1864.7	268	EF4	1865.7	0.05
E4	329.63	1517	A13	329.60	-0.01	**B6**	1975.5	253	F03	1976.3	0.04
F4	349.23	1432	A68	349.16	-0.02	**C7**	2093.0	239	F11	2092.1	-0.05
#F4	369.99	1351	AB9	370.10	0.03	**#C7**	2217.5	225	F1F	2222.2	0.22
G4	392.00	1276	B04	391.85	-0.04	**D7**	2349.3	213	F2B	2347.4	-0.08
#G4	415.30	1204	B4C	415.28	-0.01	**#D7**	2489.0	201	F37	2487.6	-0.06
A4	440.00	1136	B90	440.14	0.03	**E7**	2637.0	190	F42	2631.6	-0.21
#A4	466.16	1073	BCF	465.98	-0.04	**F7**	2793.8	179	F4D	2793.3	-0.02
B4	493.88	1012	C0C	494.07	0.04	**#F7**	2960.0	169	F57	2958.6	-0.05
C5	523.25	956	C44	523.01	-0.05	**G7**	3136.0	159	F61	3144.7	0.28
#C5	554.37	902	C7A	554.32	-0.01	**#G7**	3322.4	150	F6A	3333.3	0.33
D5	587.33	851	CAD	587.54	0.04	**A7**	3520.0	142	F72	3521.1	0.03
#D5	622.25	804	CDC	621.89	-0.06	**#A7**	3729.3	134	F7A	3731.3	0.05
E5	659.26	758	D0A	659.63	0.06	**B7**	3951.1	127	F81	3937.0	-0.36
F5	698.46	716	D34	698.32	-0.02	**C8**	4186.0	119	F89	4201.7	0.37

Music Table 2.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSC =2MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B1	61.73	4050	2E	61.73	0.00	**C5**	523.25	478	E22	523.01	-0.05
C2	65.10	3840	100	65.10	0.00	**#C5**	554.37	451	E3D	554.32	-0.01
#C2	69.29	3608	1E8	69.29	0.00	**D5**	587.33	426	E56	586.85	-0.08
D2	73.42	3405	2B3	73.42	0.00	**#D5**	622.25	402	E6E	621.89	-0.06
#D2	77.78	3214	372	77.78	0.00	**E5**	659.26	379	E85	659.63	0.06
E2	82.41	3034	426	82.40	-0.01	**F5**	698.46	358	E9A	698.32	-0.02
F2	87.31	2863	4D1	87.32	0.01	**#F5**	739.99	338	EAE	739.64	-0.05
#F2	92.50	2703	571	92.49	-0.01	**G5**	783.99	319	EC1	783.70	-0.04
G2	98.00	2551	609	98.00	0.00	**#G5**	830.61	301	ED3	830.56	-0.01
#G2	103.82	2408	698	103.82	0.00	**A5**	880.00	284	EE4	880.28	0.03
A2	110.00	2273	71F	109.99	-0.01	**#A5**	932.33	268	EF4	932.84	0.06
#A2	116.54	2145	79F	116.55	0.01	**B5**	987.77	253	F03	988.14	0.04
B2	123.47	2025	817	123.46	-0.01	**C6**	1046.5	239	F11	1046.0	-0.05
C3	130.81	1911	889	130.82	0.01	**#C6**	1108.7	225	F1F	1111.1	0.22
#C3	138.59	1804	8F4	138.58	-0.01	**D6**	1174.7	213	F2B	1173.7	-0.08
D3	146.83	1703	959	146.80	-0.02	**#D6**	1244.5	201	F37	1243.8	-0.06
#D3	155.56	1607	9B9	155.57	0.00	**E6**	1318.5	190	F42	1315.8	-0.21
E3	164.81	1517	A13	164.80	-0.01	**F6**	1396.9	179	F4D	1396.7	-0.02
F3	174.61	1432	A68	174.58	-0.02	**#F6**	1480.0	169	F57	1479.3	-0.05
#F3	185.00	1351	AB9	185.05	0.03	**G6**	1568.0	159	F61	1572.3	0.28
G3	196.00	1276	B04	195.92	-0.04	**#G6**	1661.2	150	F6A	1666.7	0.33
#G3	207.65	1204	B4C	207.64	-0.01	**A6**	1760.0	142	F72	1760.6	0.03
A3	220.00	1136	B90	220.07	0.03	**#A6**	1864.7	134	F7A	1865.7	0.05
#A3	233.08	1073	BCF	232.99	-0.04	**B6**	1975.5	127	F81	1968.5	-0.36
B3	246.94	1012	C0C	247.04	0.04	**C7**	2093.0	119	F89	2100.8	0.37
C4	261.63	956	C44	261.51	-0.04	**#C7**	2217.5	113	F8F	2212.4	-0.23
#C4	277.18	902	C7A	277.16	-0.01	**D7**	2349.3	106	F96	2358.5	0.39
D4	293.66	851	CAD	293.77	0.04	**#D7**	2489.0	100	F9C	2500.0	0.44
#D4	311.13	804	CDC	310.95	-0.06	**E7**	2637.0	95	FA1	2631.6	-0.21
E4	329.63	758	D0A	329.82	0.06	**F7**	2793.8	89	FA7	2809.0	0.54
F4	349.23	716	D34	349.16	-0.02	**#F7**	2960.0	84	FAC	2976.2	0.55
#F4	369.99	676	D5C	369.82	-0.05	**G7**	3136.0	80	FB0	3125.0	-0.35
G4	392.00	638	D82	391.85	-0.04	**#G7**	3322.4	75	FB5	3333.3	0.33
#G4	415.30	602	DA6	415.28	-0.01	**A7**	3520.0	71	FB9	3521.1	0.03
A4	440.00	568	DC8	440.14	0.03	**#A7**	3729.3	67	FBD	3731.3	0.05
#A4	466.16	536	DE8	466.42	0.06	**B7**	3951.1	63	FC1	3968.3	0.44
B4	493.88	506	E06	494.07	0.04	**C8**	4186.0	60	FC4	4166.7	-0.46

11. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by Code option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

12. Watchdog Timer (WDT)

The watchdog timer is a count-down counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E bit2 - bit0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0	R/W	Watchdog timer-out period = 4096ms
	X	0	0	1	R/W	Watchdog timer-out period = 1024ms
	X	0	1	0	R/W	Watchdog timer-out period = 256ms
	X	0	1	1	R/W	Watchdog timer-out period = 128ms
	X	1	0	0	R/W	Watchdog timer-out period = 64ms
	X	1	0	1	R/W	Watchdog timer-out period = 16ms
	X	1	1	0	R/W	Watchdog timer-out period = 4ms
	X	1	1	1	R/W	Watchdog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer-out period valid for V_{DD} = 5V.

13. HALT and STOP Mode

After the execution of HALT instruction, SH69P26 will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Timer0, Timer1, Timer2, CMP and watchdog timer) will keep status.

After the execution of STOP instruction, SH69P26 will enter the Stop mode. The whole chip (including oscillator) will STOP operating. But watchdog and CMP are still enabled.

In the HALT mode, SH69P26 can be waked up if any interrupt occurs.

In the STOP mode, SH69P26 can be waked up if any port interrupt (including other external sources, such as CMP output interrupt) occurs or watchdog timer overflows (WDT is enabled).

14. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

Power-on Reset, Pin Reset:

Warm-up time interval:

(1) In RC oscillator mode, **fosc** = 32.768kHz - 6MHz, the warm-up counter prescaler divide ratio is 2^{12} (4096).

(2) In Crystal oscillator or Ceramic resonator mode, **fosc** = 32.768kHz - 8MHz, the warm-up counter prescaler divide ratio is 2^{14} (16384).

Wake Up from Stop Mode, WDT Reset & LVR Reset:

Warm-up time interval:

(1) In RC oscillator mode, **fosc** = 32.768kHz - 6MHz, the warm-up counter prescaler is divided by 2^7 (128).

(2) In Crystal oscillator or Ceramic resonator mode, **fosc** = 32.768kHz - 8MHz, the warm-up counter prescaler is divided by 2^{12} (4096).

15. Code Option

OSC:
- 000: External Clock (default)
- 001: Internal RC Oscillator (2MHz)
- 010: Internal RC Oscillator (4MHz)
- 011: Internal RC Oscillator (6MHz)
- 100: External RC Oscillator (400kHz - 8MHz)
- 101: Ceramic Resonator (400kHz - 8MHz)
- 110: Crystal Oscillator (400kHz - 8MHz)
- 111: 32.768kHz Crystal Oscillator

OSC Range:
- 0: 2MHz - 8MHz (default)
- 1: 400kHz - 2MHz

WDT:
- 0: Enable (default)
- 1: Disable

LVR:
- 0: Disable (default)
- 1: Enable

LVR Voltage Range:
- 0: High LVR voltage (default)
- 1: Low LVR voltage

Chip pin Reset*:
- 0 = pin reset function is enabled (Default)
- 1 = pin reset function is disabled

*** Note:**

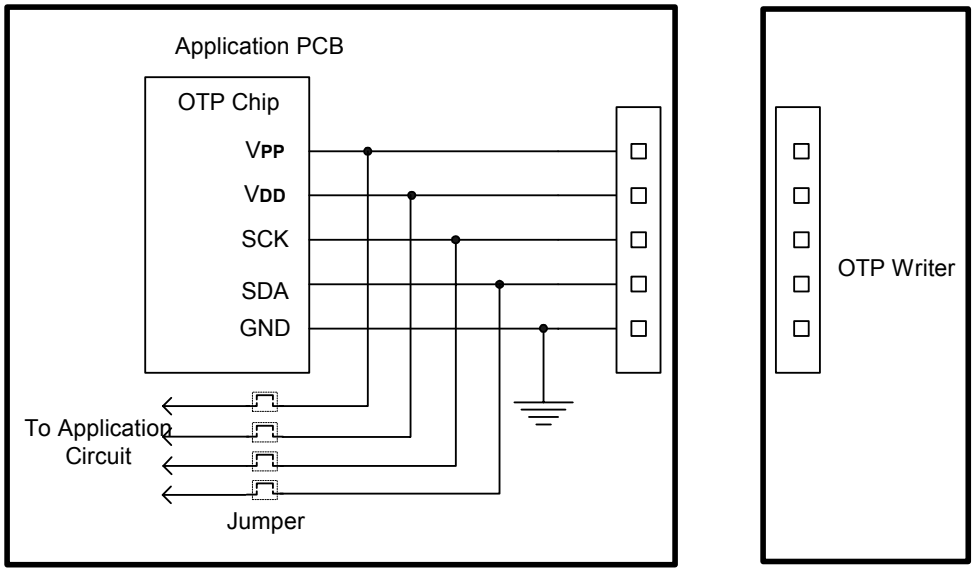
1. Reset pin can be shared as IO.
2. If reset pin is enabled, the EMC quality will be better.

In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.

(2) Connect the programming interface with OTP writer and begin programming.

(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1 Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC[3], AC[0] -> CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- lll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -40℃ to +85℃

Storage Temperature . . . . -55℃ to +125℃

***Comments**

Stresses exceed those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristic (GND = 0V, T_A = 25℃, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	fosc = 8MHz
		2.4	5.0	5.5	V	fosc = 4MHz
Low Voltage Reset voltage1	V_{LVR1}	3.8	-	4.2	V	LVR enable
Low Voltage Reset voltage2	V_{LVR2}	2.3	-	2.7	V	LVR enable
LVR Voltage Pulse Width	t_{LVR}	500	-	-	μs	$V_{DD} \leq V_{LVR}$
Operating Current	I_{OP}	-	1.5	2	mA	fosc = 8MHz All output pins unloaded, execute NOP instruction, (WDT off, LVR off, CMP disable.) V_{DD} = 5.0V
		-	1.0	1.5	mA	fosc = 4MHz All output pins unloaded, execute NOP instruction, (WDT off, LVR off, CMP disable.) V_{DD} = 5.0V
Stand by Current 1 (HALT)	I_{SB1}	-	-	1	mA	fosc = 8MHz, All output pins unloaded (HALT mode), WDT off, LVR off, CMP disable, V_{DD} = 5.0V
Stand by Current 2 (HALT)	I_{SB2}	-	-	0.8	mA	fosc = 4MHz, All output pins unloaded (HALT mode), WDT off, LVR off, CMP disable, V_{DD} = 5.0V
Stand by Current 3 (STOP)	I_{SB3}	-	-	1	μA	All output pins unloaded (STOP mode), WDT off, LVR off, CMP disable, V_{DD} = 5.0V
WDT Current	I_{WDT}	-	-	20	μA	STOP, WDT on, CMP disable, LVR off, V_{DD} = 5.0V

DC Electrical Characteristics (continued1) (GND = 0V, T_A = 25℃, fosc = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Low Voltage	V_{IL1}	GND	-	V_{DD} X0.2	V	I/O Ports, pins tri-state, V_{DD} = 5.0V
Input Low Voltage	V_{IL2}	GND	-	V_{DD} X0.15	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger), V_{DD} = 5.0V
Input High Voltage	V_{IH1}	V_{DD} X0.8	-	V_{DD}	V	I/O Ports, pins tri-state, V_{DD} = 5.0V
Input High Voltage	V_{IH2}	V_{DD} X0.85	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger), V_{DD} = 5.0V
Input Leakage Current	I_{IL}	-1	-	1	μA	I/O ports, GND < V_{IN} < V_{DD}
Pull-high Resistor	R_{PH}	-	30	-	KΩ	Pull-high/Pull-low resistor (V_{DD} = 5.0V)
Output High Voltage	V_{OH1}	V_{DD} - 1.0	-	-	V	I/O ports, I_{OH} = -25mA (PORTB, PORTH, PORTD [3:2])
Output High Voltage	V_{OH2}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -10mA (PORTA, PORTC, PORTD [1:0], PORTE, PORTF, PORTG), V_{DD} = 5.0V
Output Low Voltage	V_{OL1}	-	-	GND + 1.5	V	I/O ports, I_{OL} = 200mA (PORTA, PORTD [1:0]), V_{DD} = 5.0V
Output Low Voltage	V_{OL2}	-	-	GND + 0.6	V	I/O ports, I_{OL} = 20mA (PORTB, PORTH, PORTD [3:2], PORTC, PORTE, PORTF, PORTG), V_{DD} = 5.0V

DC Electrical Characteristics (continued2) (GND = 0V, T_A = 25℃, fosc = 8MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Low Voltage	V_{IL3}	GND	-	V_{DD} X0.2	V	I/O Ports, pins tri-state, V_{DD} = 5.0V
Input High Voltage	V_{IH3}	V_{DD} X0.8	-	V_{DD}	V	I/O Ports, pins tri-state, V_{DD} = 5.0V

AC Electrical Characteristics (V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified.)

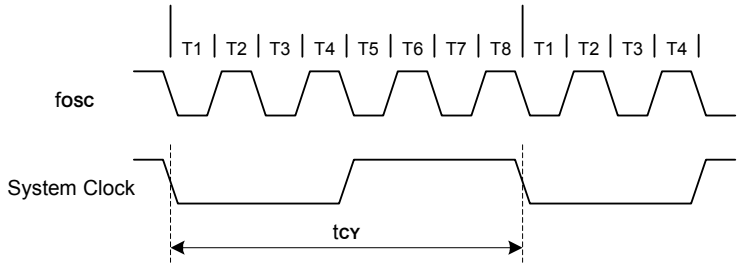
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	t_{CY}	0.5	-	133.4	μs	f_{OSC} = 30KHz - 8MHz
T0/T2 input width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio, V_{DD} = 5.0V
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	V_{DD} = 5.0V
RESET pulse width	t_{RESET}	10	-	-	μs	Low active, V_{DD} = 5.0V
WDT Period	t_{WDT}	1	-	-	ms	V_{DD} = 5.0V
Frequency Variation	|Δf|/f	-	-	15	%	External R_{OSC} Oscillator, Include chip-to-chip variation, V_{DD} = 5V
Frequency Variation	|Δf|/f	-	-	50	%	Internal R_{OSC} Oscillator, f_{OSC} = 2MHz, 4MHz, 6MHz. Include chip-to-chip variation, V_{DD} = 5V

Analog Comparator Electrical Characteristics
(V_{DD} = 4.5V - 5.5V, GND = 0V, T_A = -40°C to +85°C, f_{OSC} = 30kHz - 10MHz, PORTE.1 input is selected as comparator negative input. unless otherwise specified.)

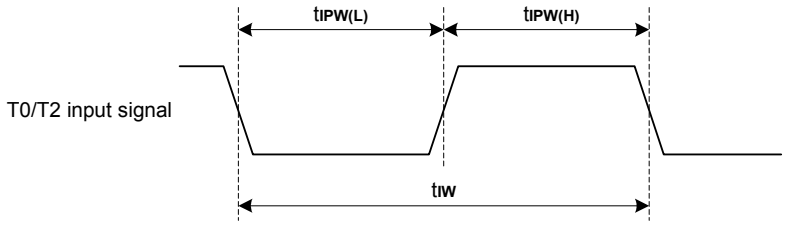
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Offset Voltage comparator inputs	$\|V_{IO}\|$	-	-	10	mV	V_{DD} = 5.0V
Common Mode range comparator inputs	V_{CM}	GND	-	V_{DD} - 1.0	V	V_{DD} = 5.0V
Response time	t_{RES}	-	250	500	ns	V_{DD} = 5.0V
Comparator enable to output valid time	t_{OV}	-	-	10	μs	V_{DD} = 5.0V
Input leakage current	I_{IL}	-	-	10	μA	0 < V_{IN} < V_{DD}

Timing Waveform

(a) System Clock Timing Waveform

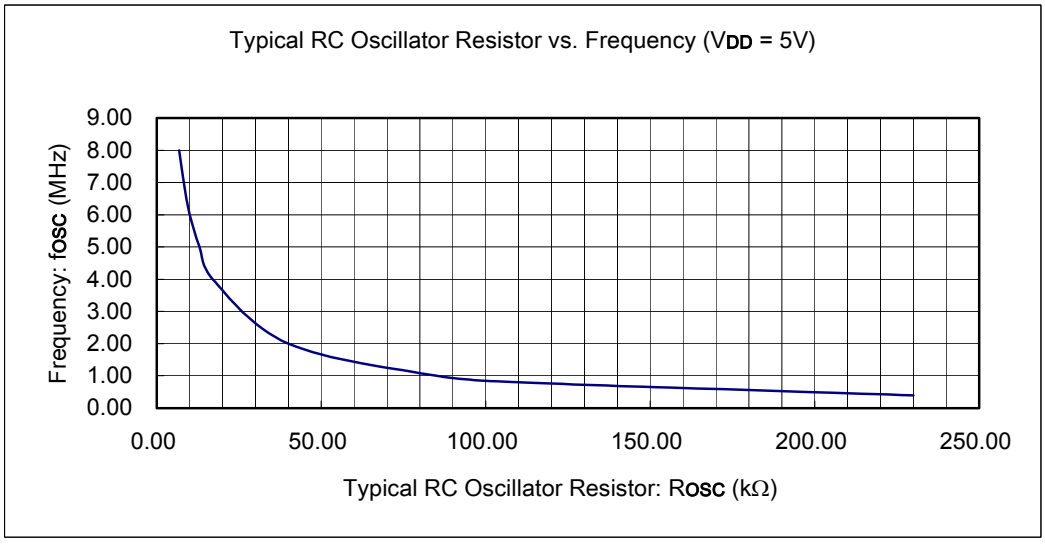


(b) T0/T2 Input Waveform



RC Oscillator Characteristics Graphs (for reference only)

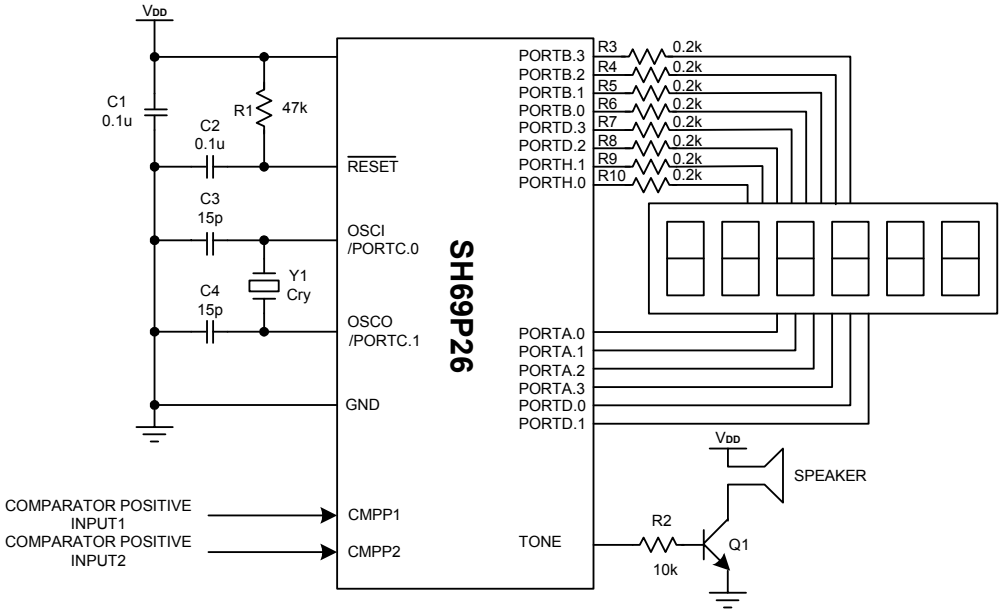
Typical RC Oscillator Resistor vs. Frequency (V_{DD} = 4.5 - 5.5V)



Application Circuit (For Reference Only)

AP:

SH69P26 has powerful drive ability, and it can drive LED directly.
(1) Operating voltage: 5.0V
(2) Oscillator: Crystal resonator 4MHz
(3) PORTA, B, D, H: Output

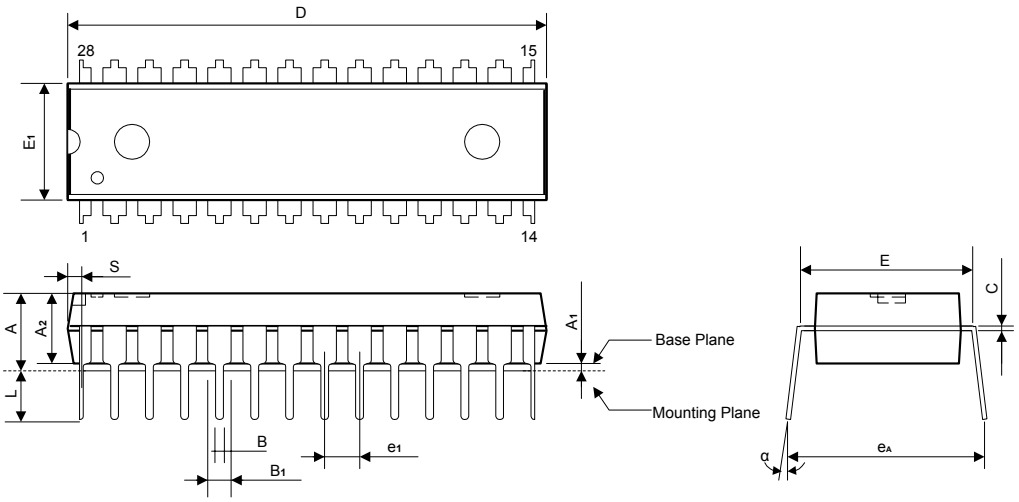


Ordering Information

Part No.	Package
SH69P26K	28L SKINNY
SH69P26M	28L SOP
SH69P26	32L DIP

Package Information

SKINNY 28-pin Outline Dimensions unit: inches/mm

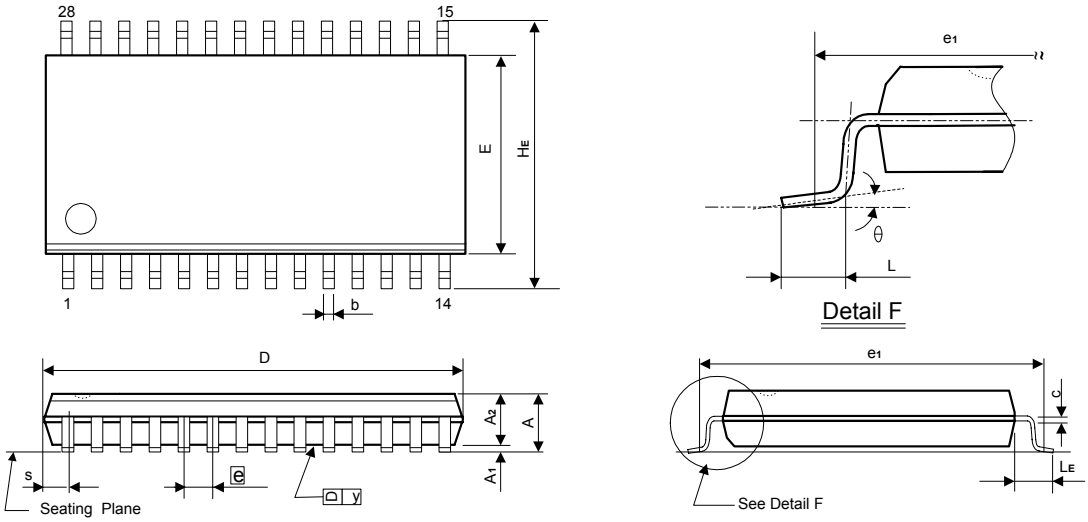


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.005	3.30 ± 0.13
B	0.018+ 0.004 - 0.002	0.46+ 0.10 - 0.05
B_1	0.060+ 0.004 - 0.002	1.52+ 0.10 - 0.05
C	0.010+0.004 -0.002	0.25+ 0.10 - 0.05
D	1.388 Typ. (1.400 Max.)	35.26 Typ. (35.56 Max.)
E	0.310 ± 0.010	7.87 ± 0.25
E_1	0.288 ± 0.005	7.32 ± 0.13
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.350 ± 0.020	8.89 ± 0.51
S	0.055 Max.	1.40 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

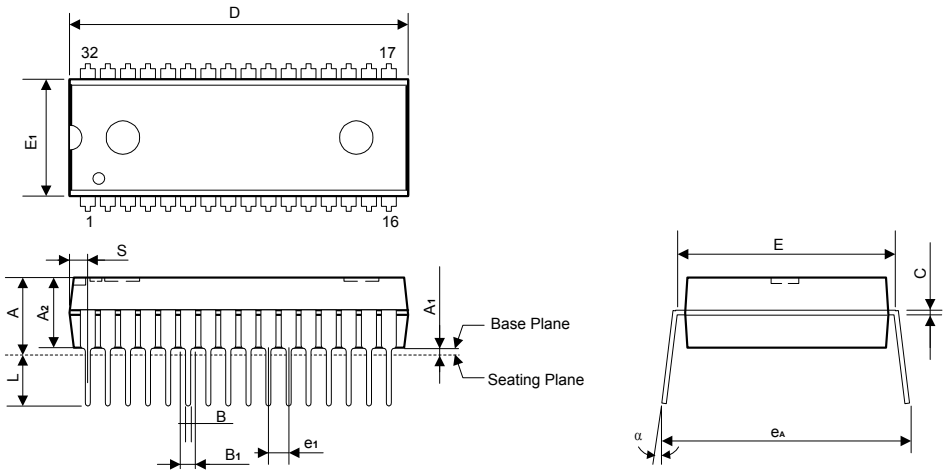
SOP (N.B.) 28L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.093 ± 0.005	2.36 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.705 ± 0.020	17.91 ± 0.51
E	0.291 - 0.299	7.39 - 7.59
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.40 NOM.
H_E	0.394 - 0.417	10.01 - 10.60
L	0.036 ± 0.008	0.91 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.043 Max.	1.09 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

P-DIP 32-pin Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.155 ± 0.010	3.94 ± 0.25
B	0.018 + 0.004 - 0.002	0.46 + 0.10 - 0.05
B_1	0.050 + 0.004 - 0.002	1.27 + 0.10 - 0.05
C	0.010 + 0.004 - 0.002	0.25 + 0.11 - 0.05
D	1.650 Typ. (1.670 Max.)	41.91 Typ. (42.42 Max.)
E	0.600 ± 0.010	15.24 ± 0.25
E_1	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.655 ± 0.035	16.64 ± 0.89
S	0.090 Max.	2.29 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.2	Delete Bonding Diagram, Pad Location and update DC Electrical Characteristic	Feb. 2008
2.1	Package information update	Apr. 2007
2.0	Add reset pin share function (share as IO)	Feb. 2006
1.0	Original	Sep. 2005