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Lab session 022
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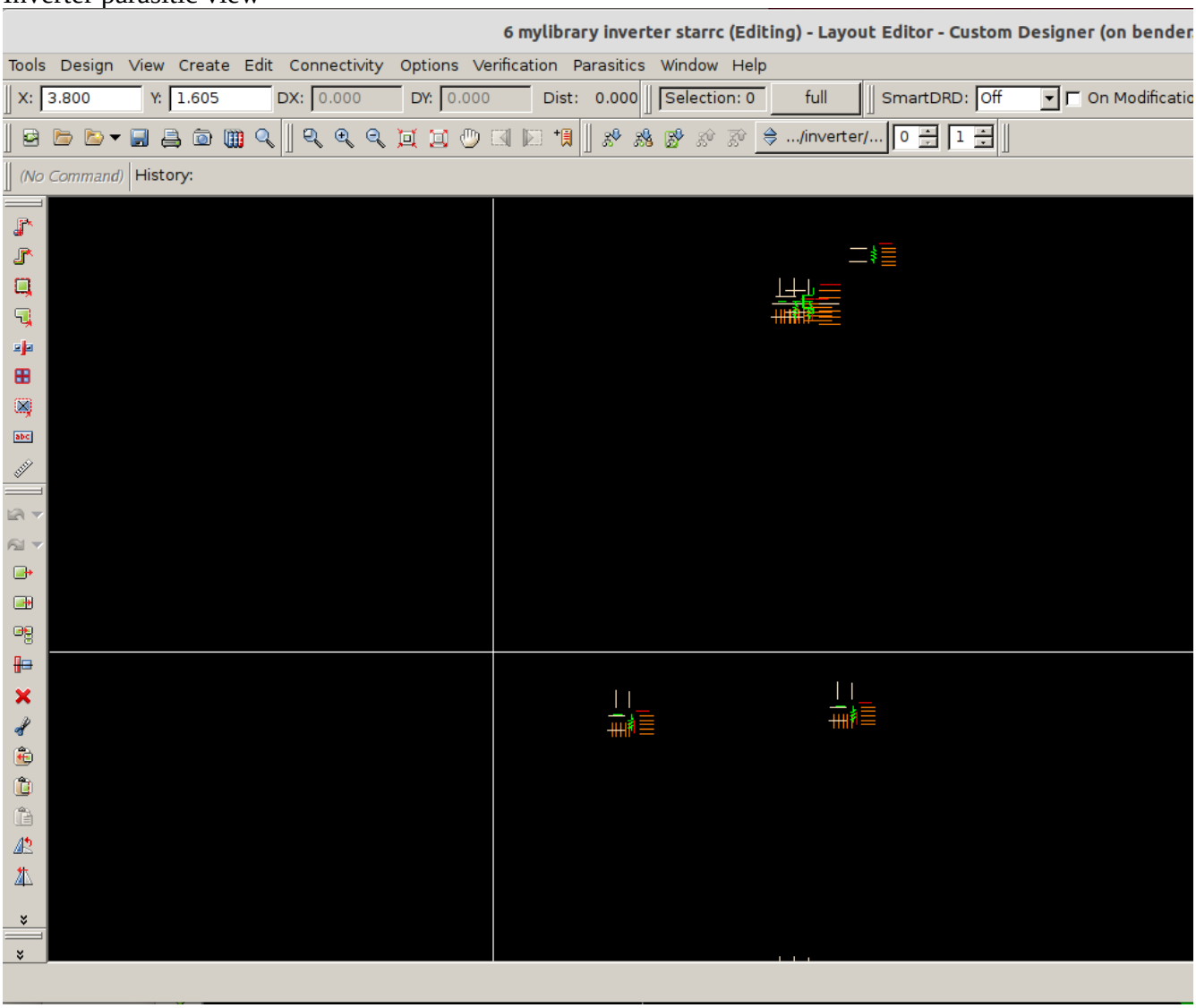
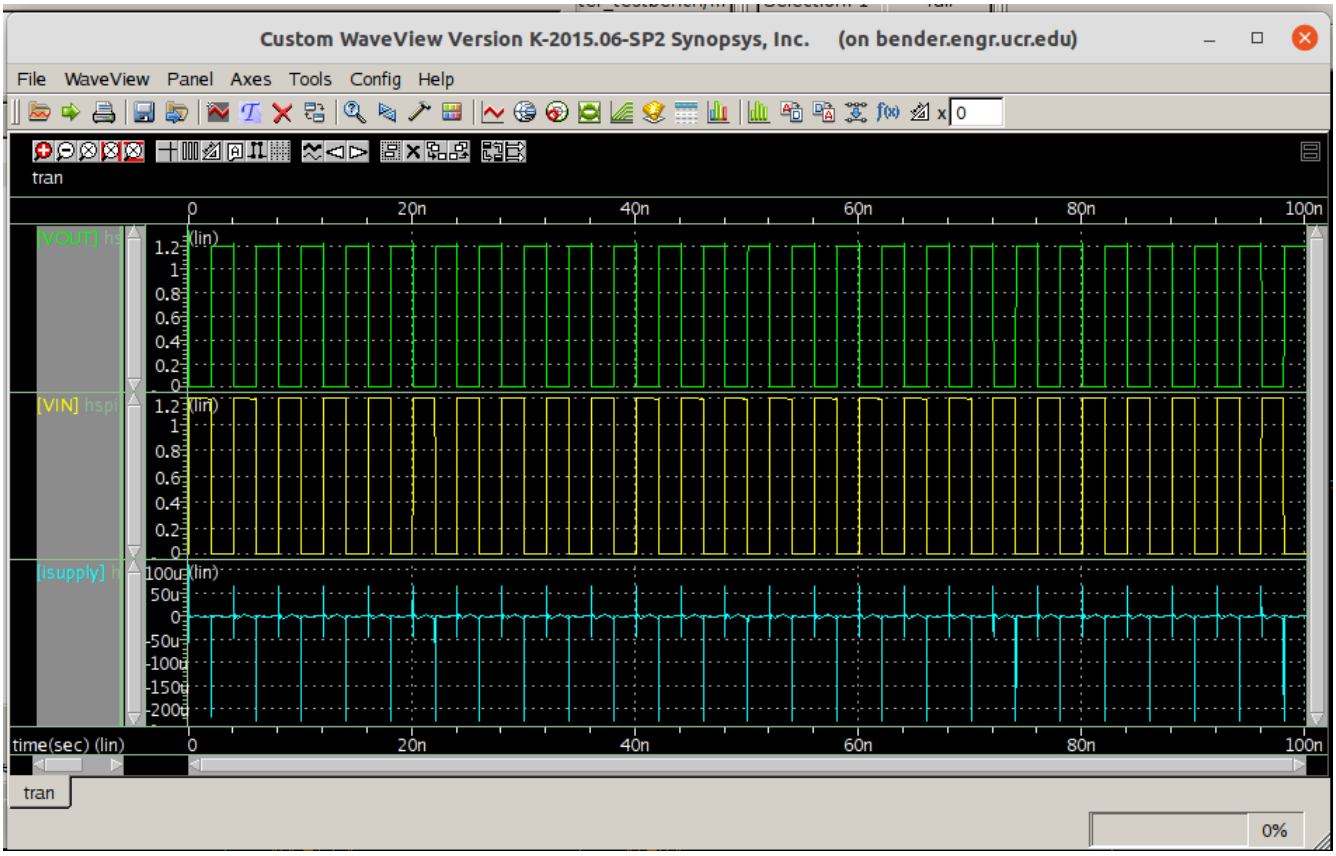
Demo videos: https://drive.google.com/drive/folders/16wwpaxhdH3CktAFFAsVMnSIiQ0Wrul1K?usp=sharing

This lab incorporates all of our previous experience to work on larger scale layouts. This larger scale exposed us to problems which required very careful troubleshooting for the DRC and LVS tests. My work stopped at the 1bit-adder LVS test due to these issues. This lab introduced the concept of parasitic circuits and the tests used to identify them. We created an oscillator from inverters, a 1 bit adder from complex transistor configurations, and a 4 bit adder from the 1 bit adders. We conducted simulations of inputs, DRC, LVS, and LPE tests.

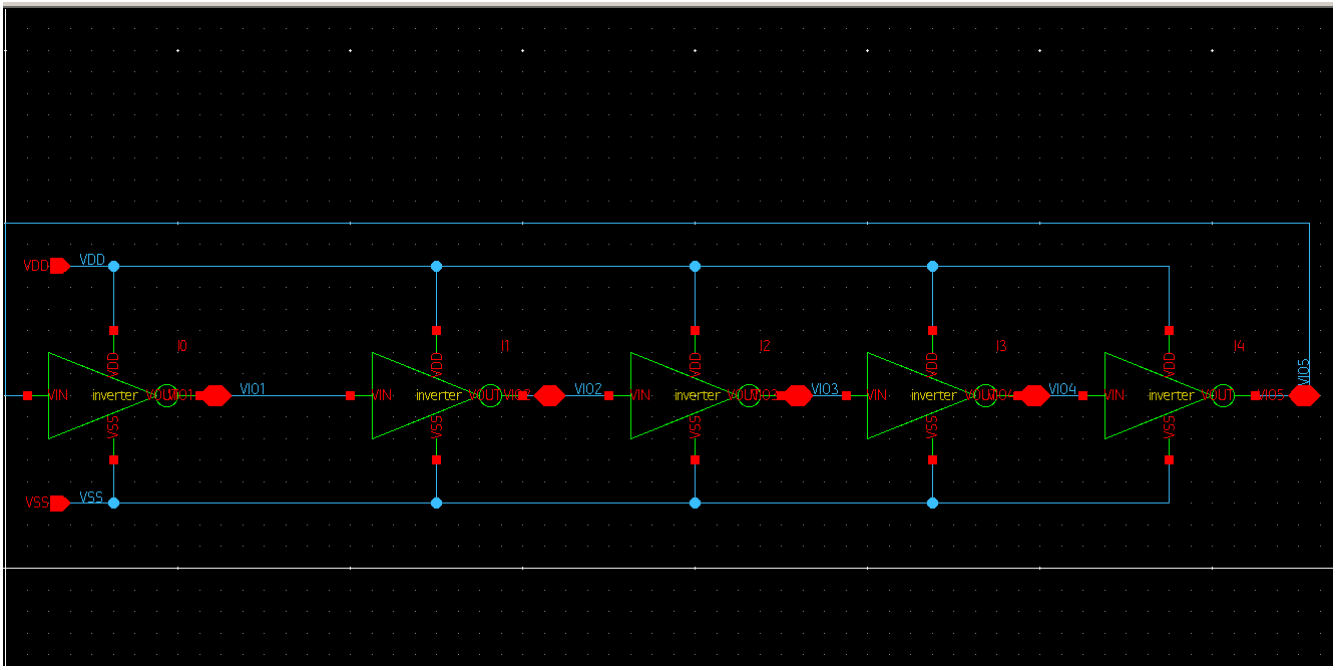
Inverter parasitic view



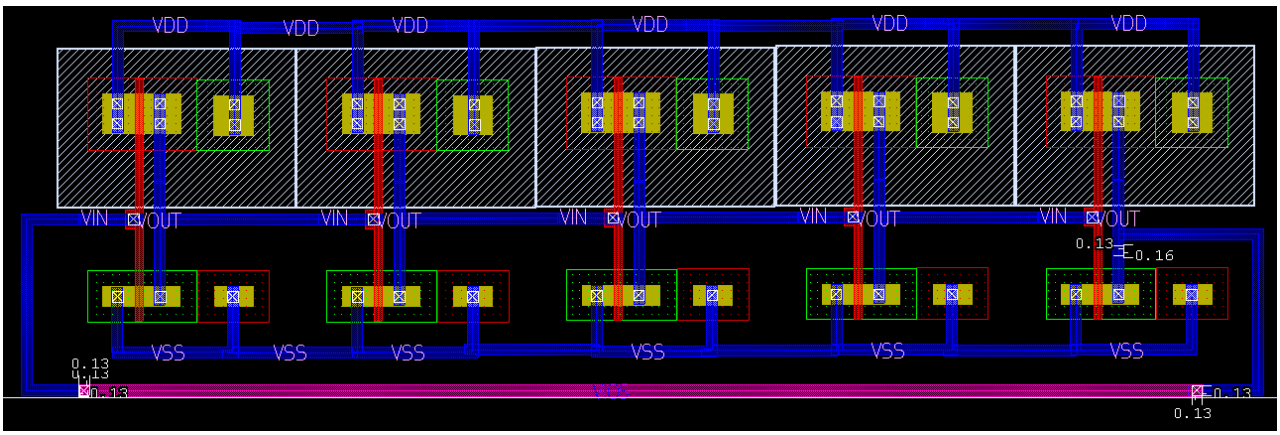
Simulation result



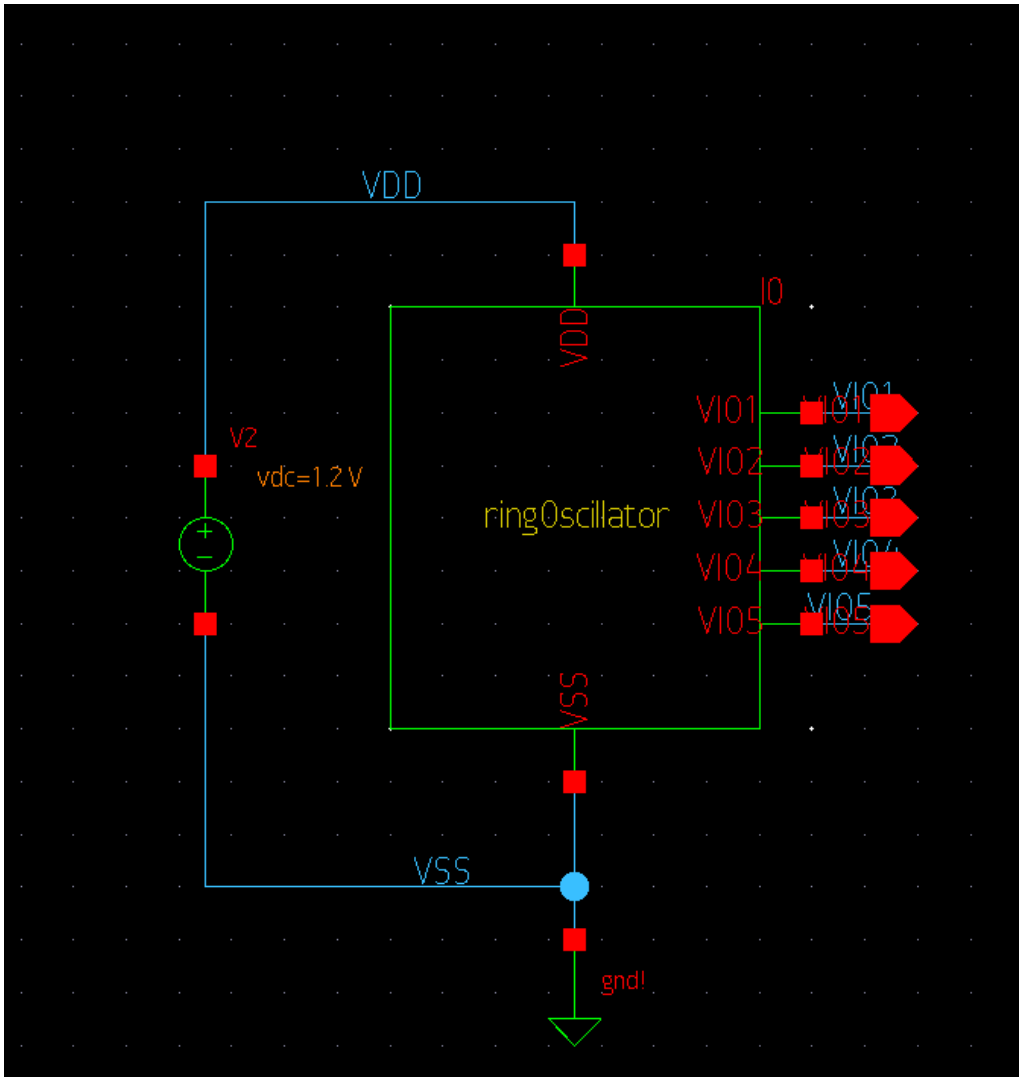
- Your ring oscillator schematic (with hierarchical design)



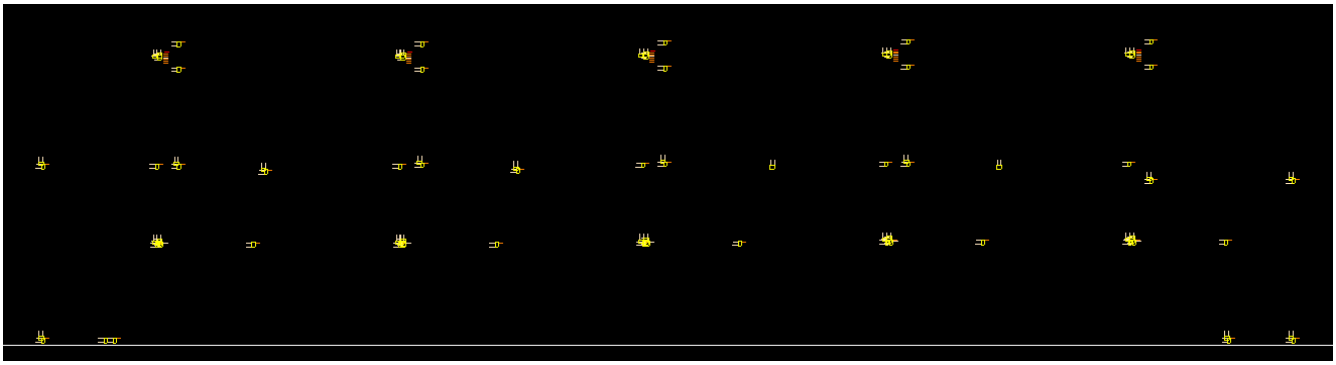
- Your ring oscillator layout

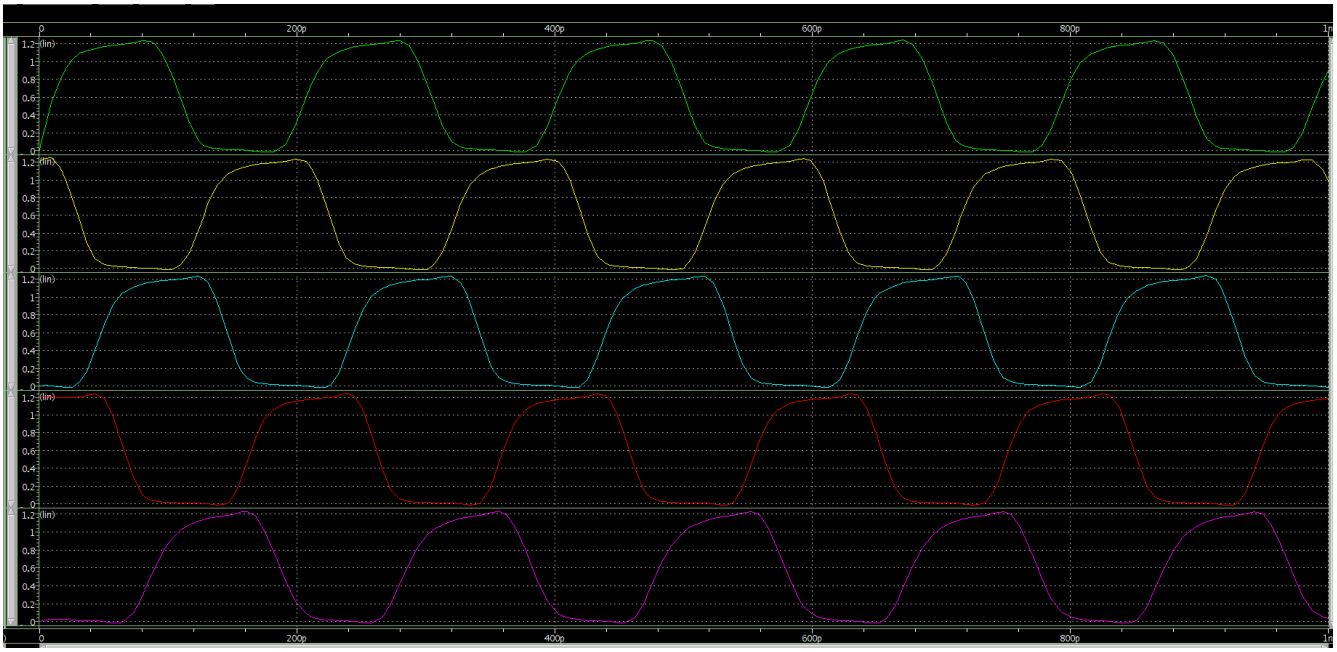


- Your ring oscillator testbench

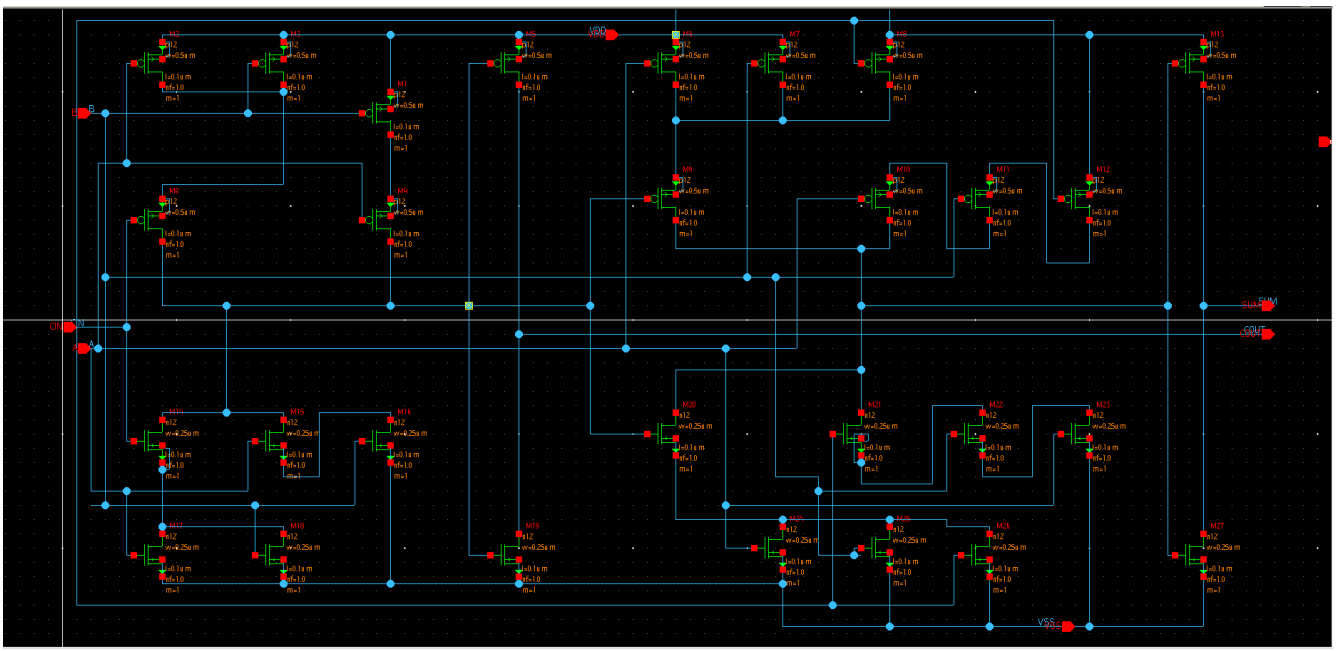


- Your ring oscillator **POST (Layout) SIMULATION** result (with parasitic extraction)



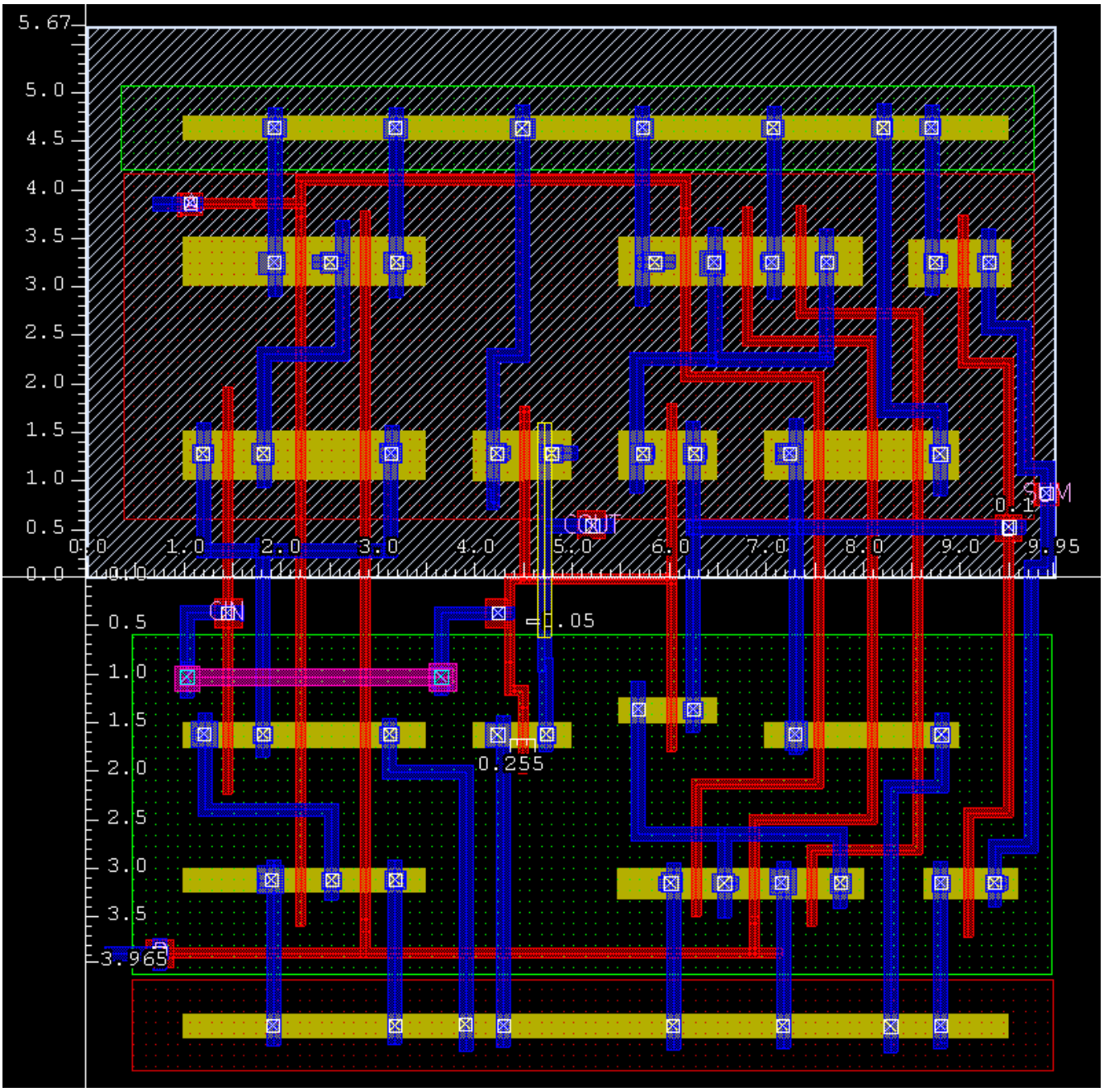

0
200p
400p
600p
800p
1.2 (lin)
1
0.8
0.6
0.4
0.2
0

- Your 1-bit full adder schematic - it must be transistor-level not logic-level

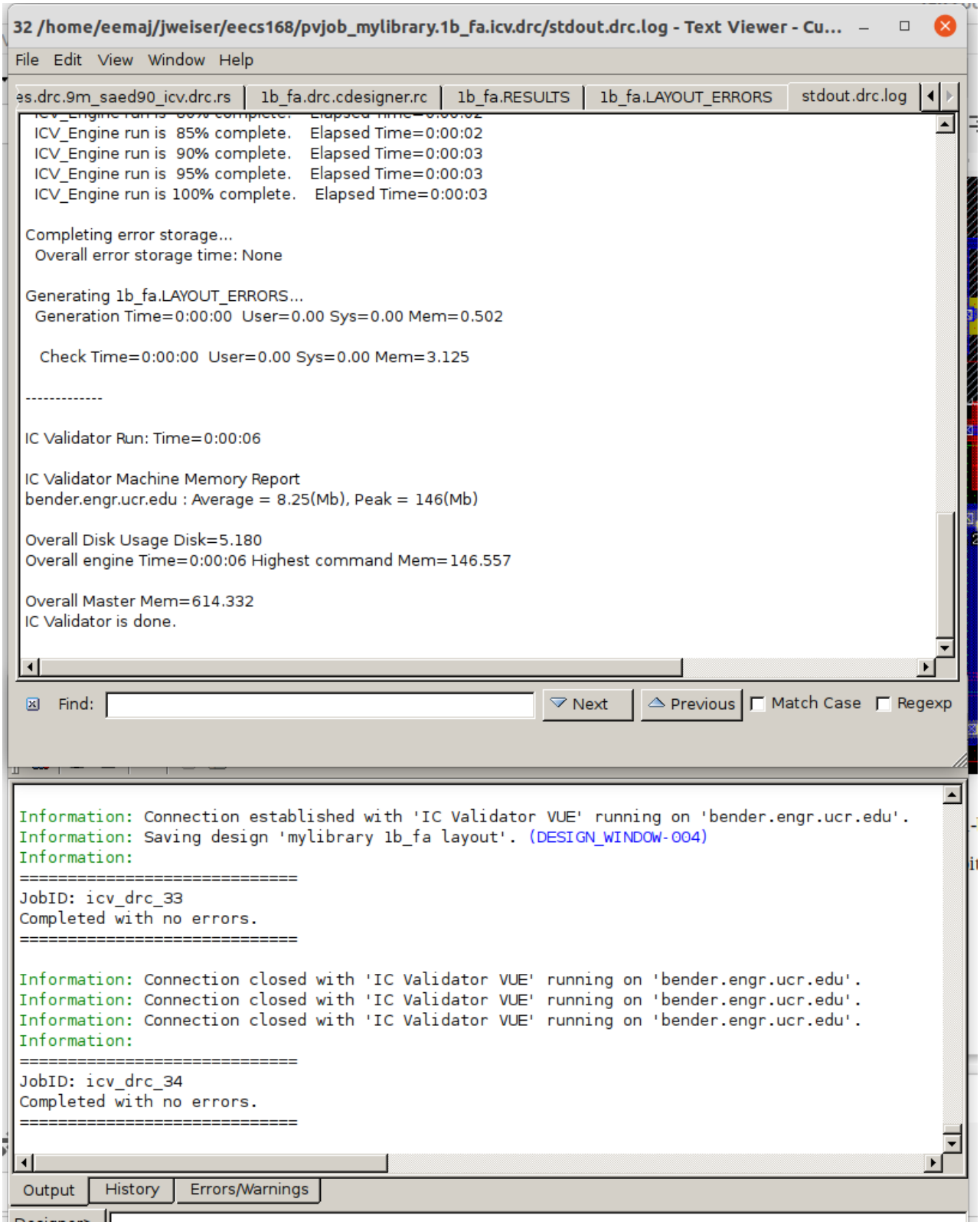


- Your 1-bit full adder simulation
- Your 1-bit full adder stick diagram

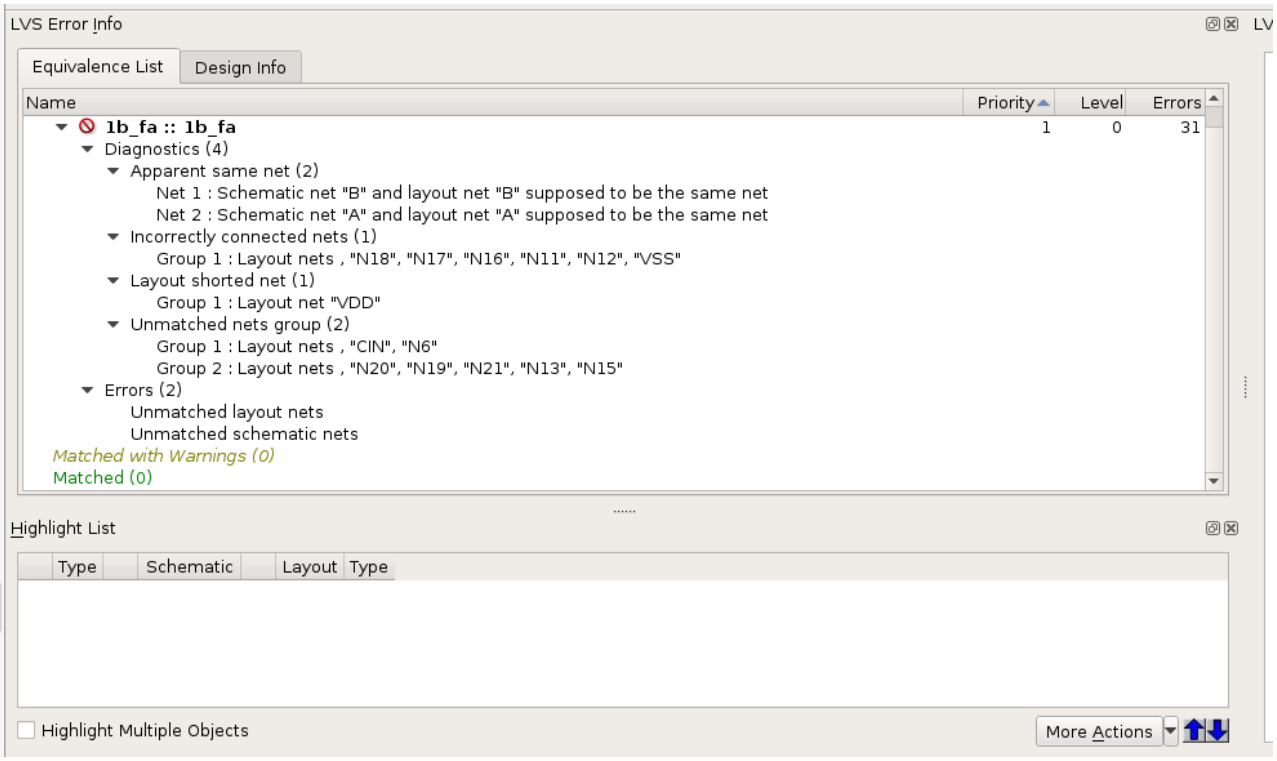
- Your 1-bit full adder layout



- An DRC Result with `CLEAN` for your 1-bit full adder



- An LVS Result with PASS for your 1-bit full adder



The DRC and LVS testing each took about 6-8 hours. The LVS was unresolved. Along the process I learned a lot about

First week: Check off your parasitic extraction and ring oscillator layout and post-simulator

- Second week: Check off your 1-bit full adder layout (DRC, LVS should be okay) and post-simulation
- Third week: Check off your 4-bit full adder layout (DRC, LVS should be okay) and post-simulation
- Fourth week: Extra work time in case you cannot finish within 3 weeks, you should have everything checked off by the end of this week's lab