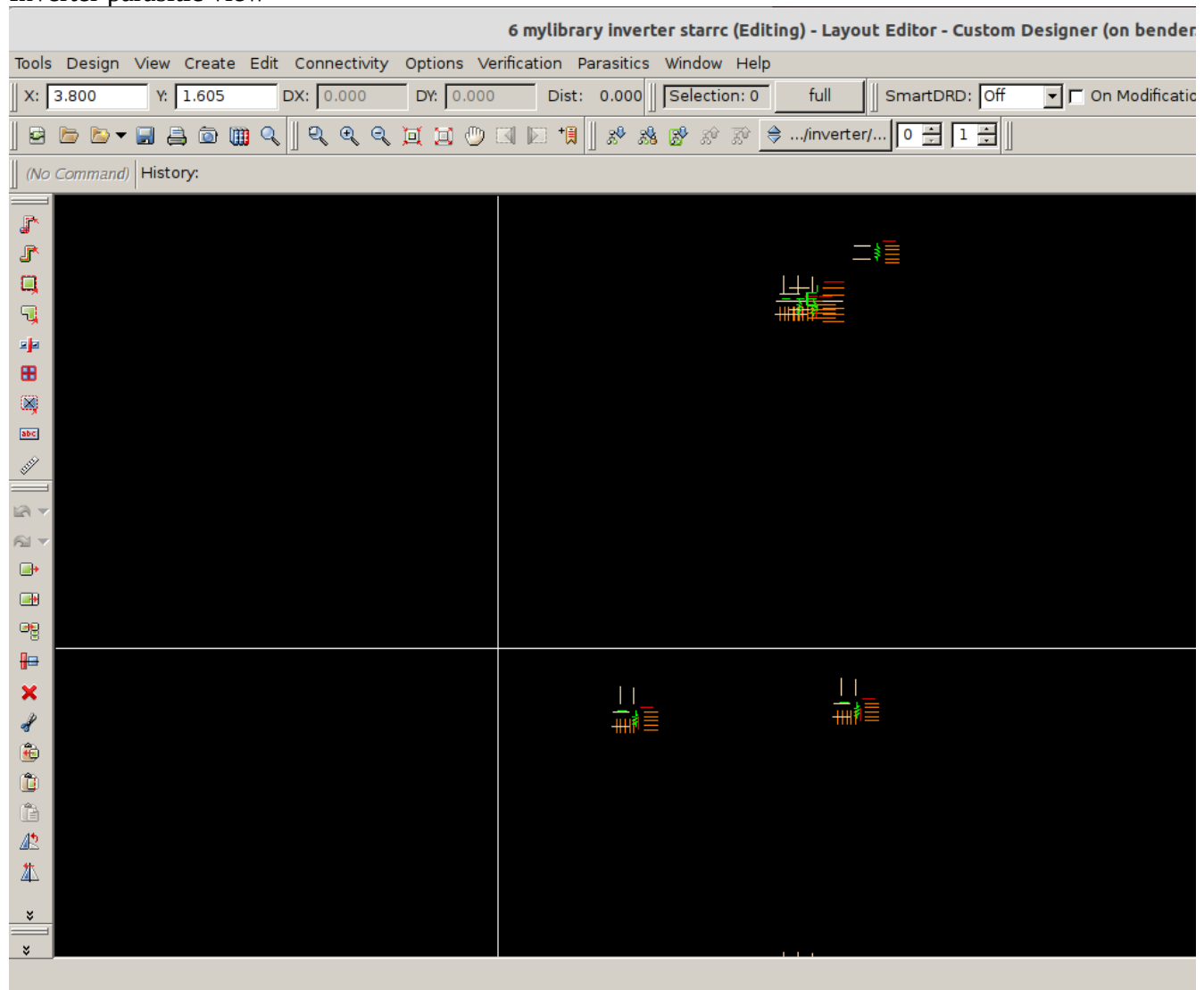


Jason Weiser
SID 62113384
Lab session 022
ENGR ID jweiser
UCR NetID jweis012

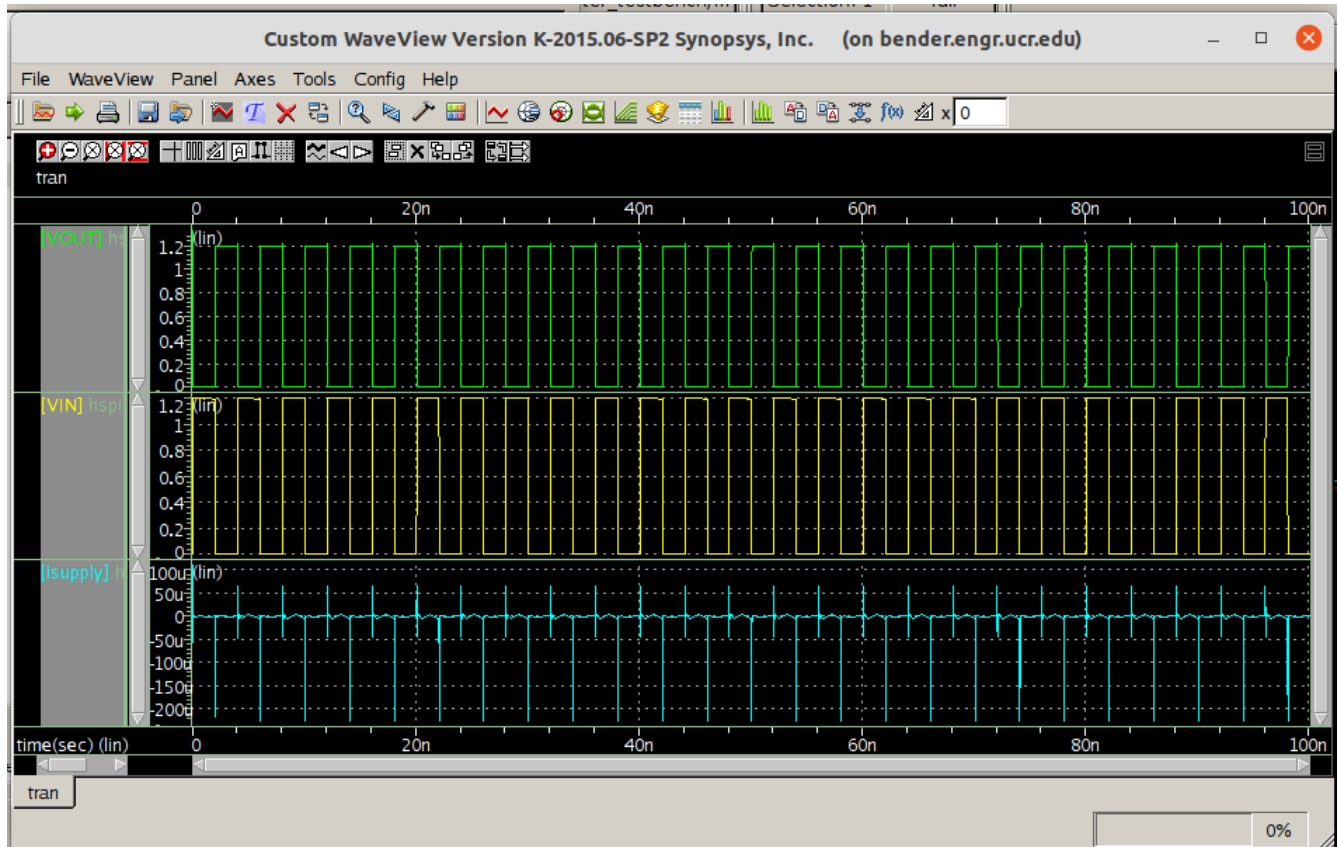
Demo videos: <https://drive.google.com/drive/folders/16wwpaxhdH3CktAFFAsVMnSliQ0Wrul1K?usp=sharing>

This lab incorporates all of our previous experience to work on larger scale layouts. This larger scale exposed us to problems which required very careful troubleshooting for the DRC and LVS tests. My work stopped at the 1bit-adder LVS test due to these issues. This lab introduced the concept of parasitic circuits and the tests used to identify them. We created an oscillator from inverters, a 1 bit adder from complex transistor configurations, and a 4 bit adder from the 1 bit adders. We conducted simulations of inputs, DRC, LVS, and LPE tests.

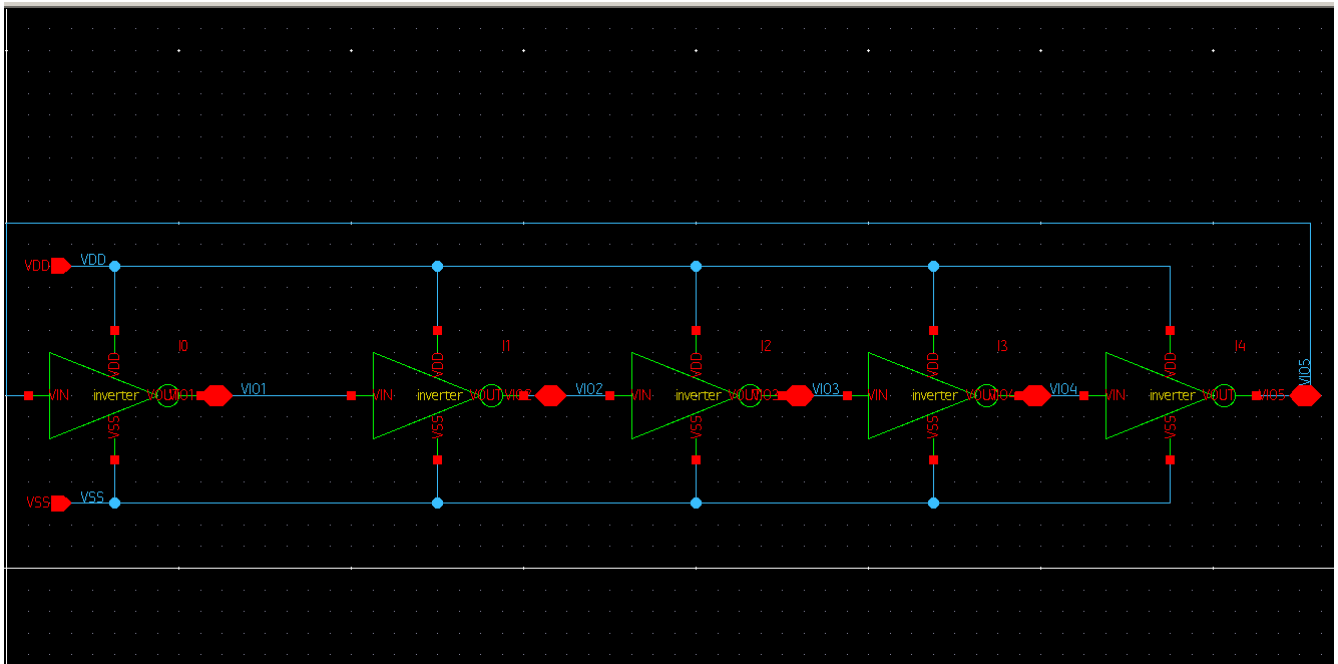
Inverter parasitic view



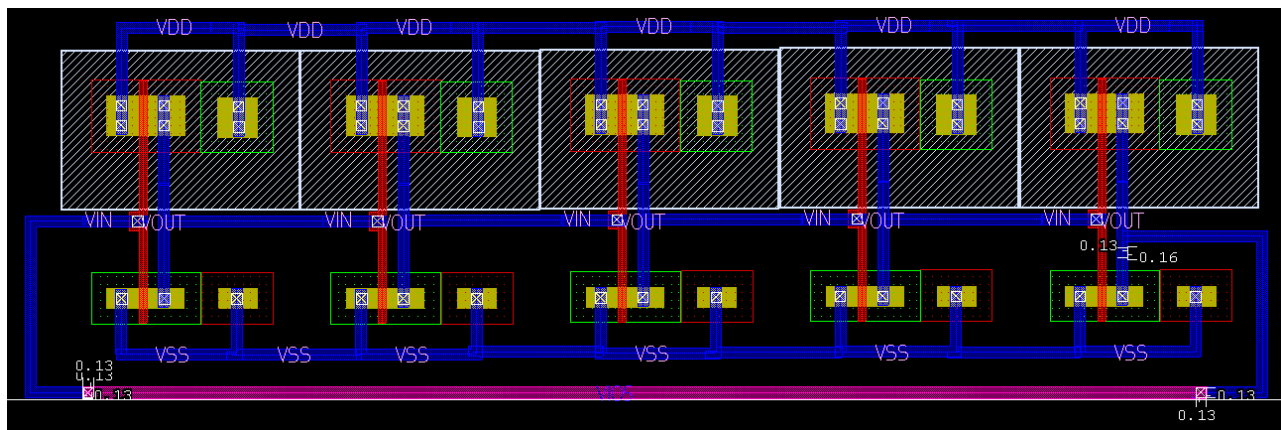
Simulation result



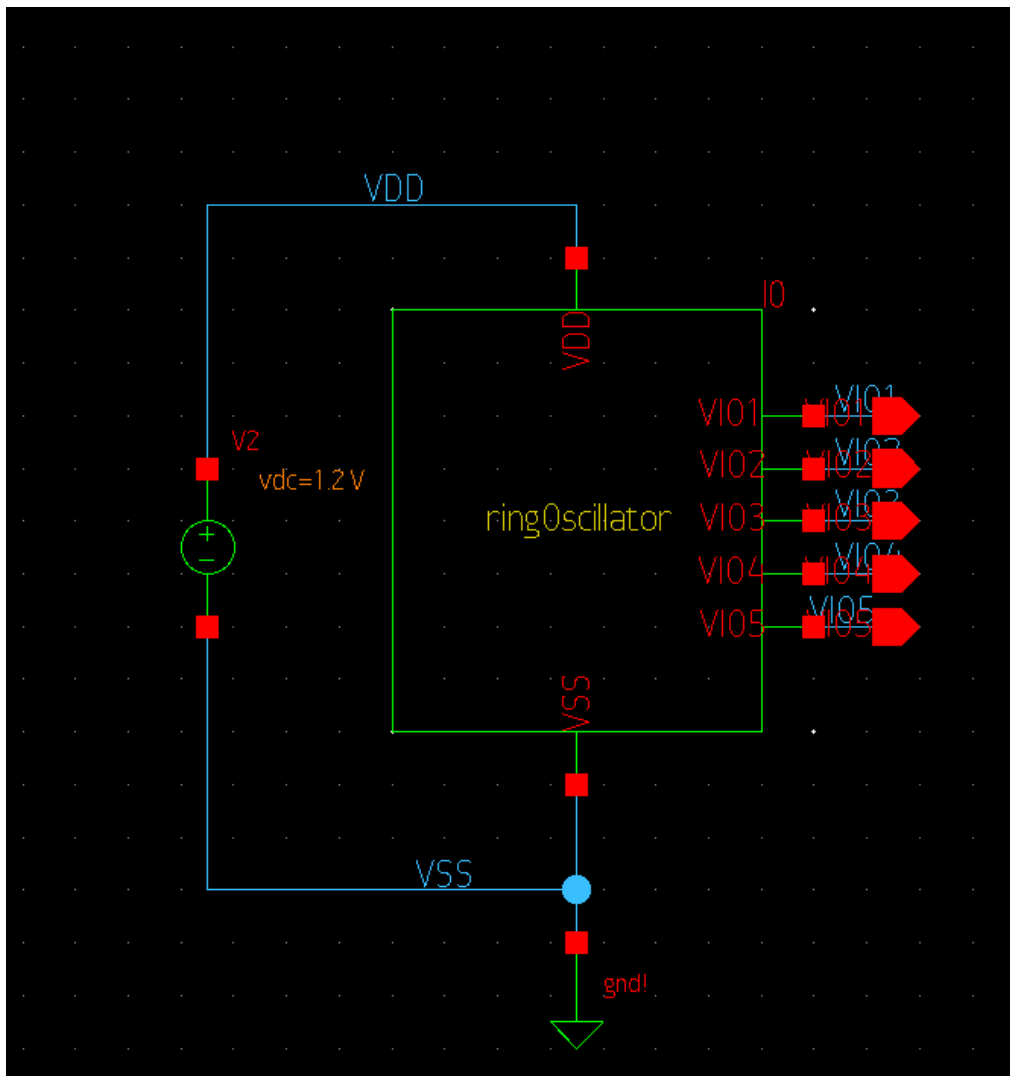
- Your ring oscillator schematic (with hierarchical design)



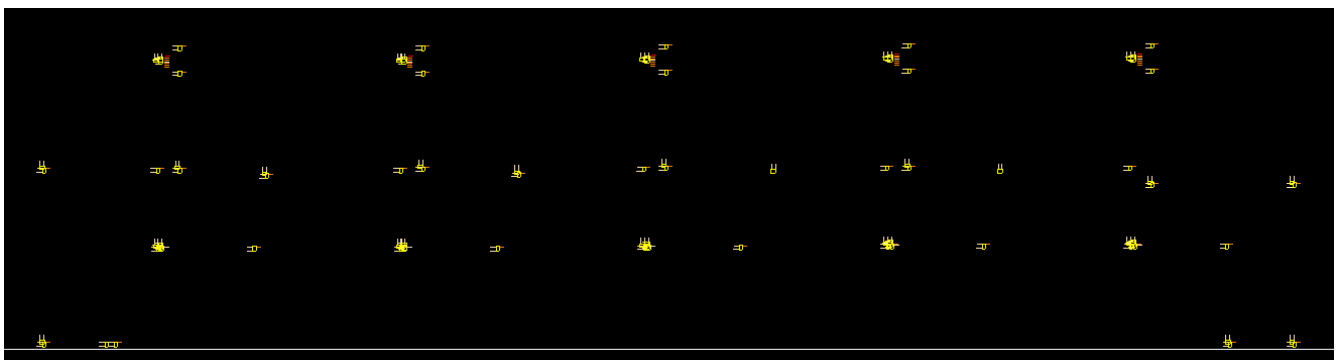
- Your ring oscillator layout

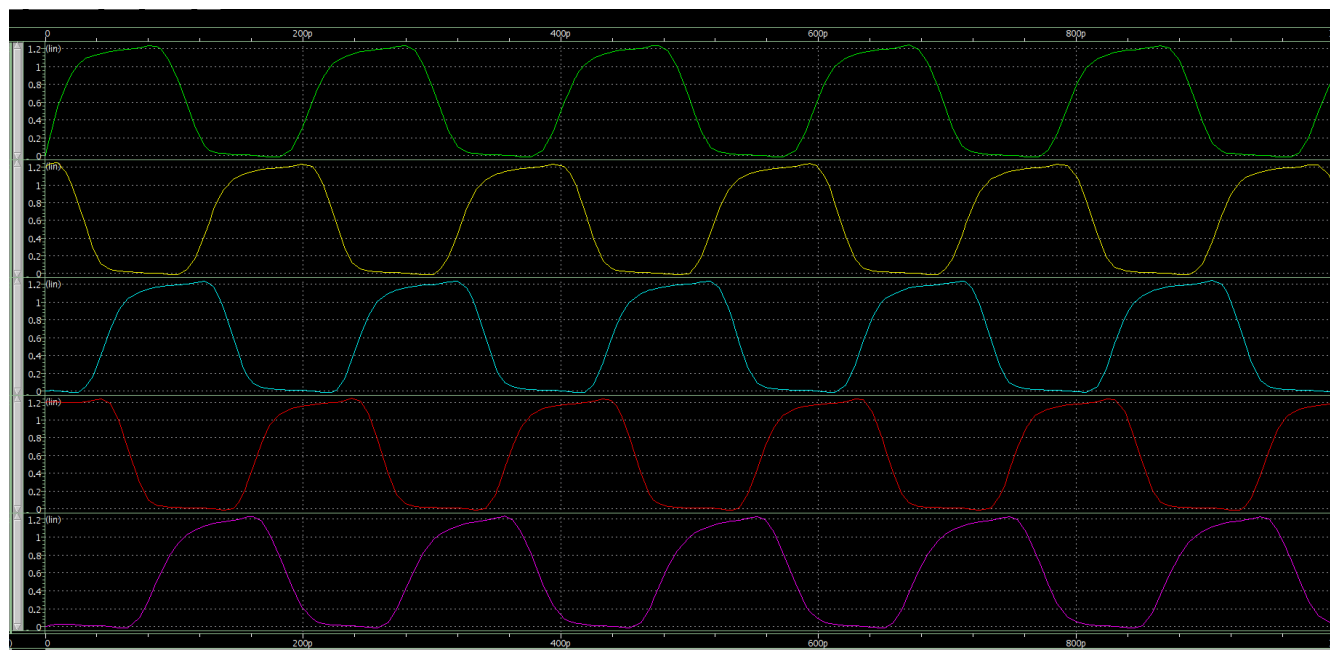


- Your ring oscillator testbench

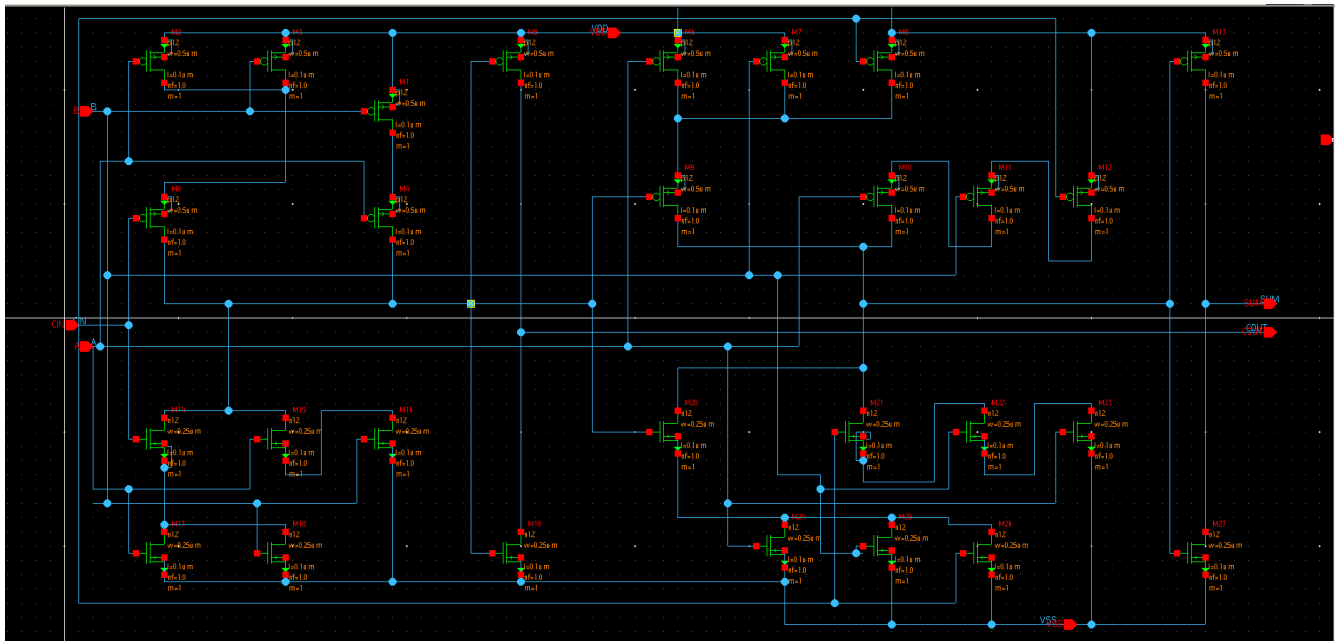


- Your ring oscillator **POST (Layout) SIMULATION** result (with parasitic extraction)



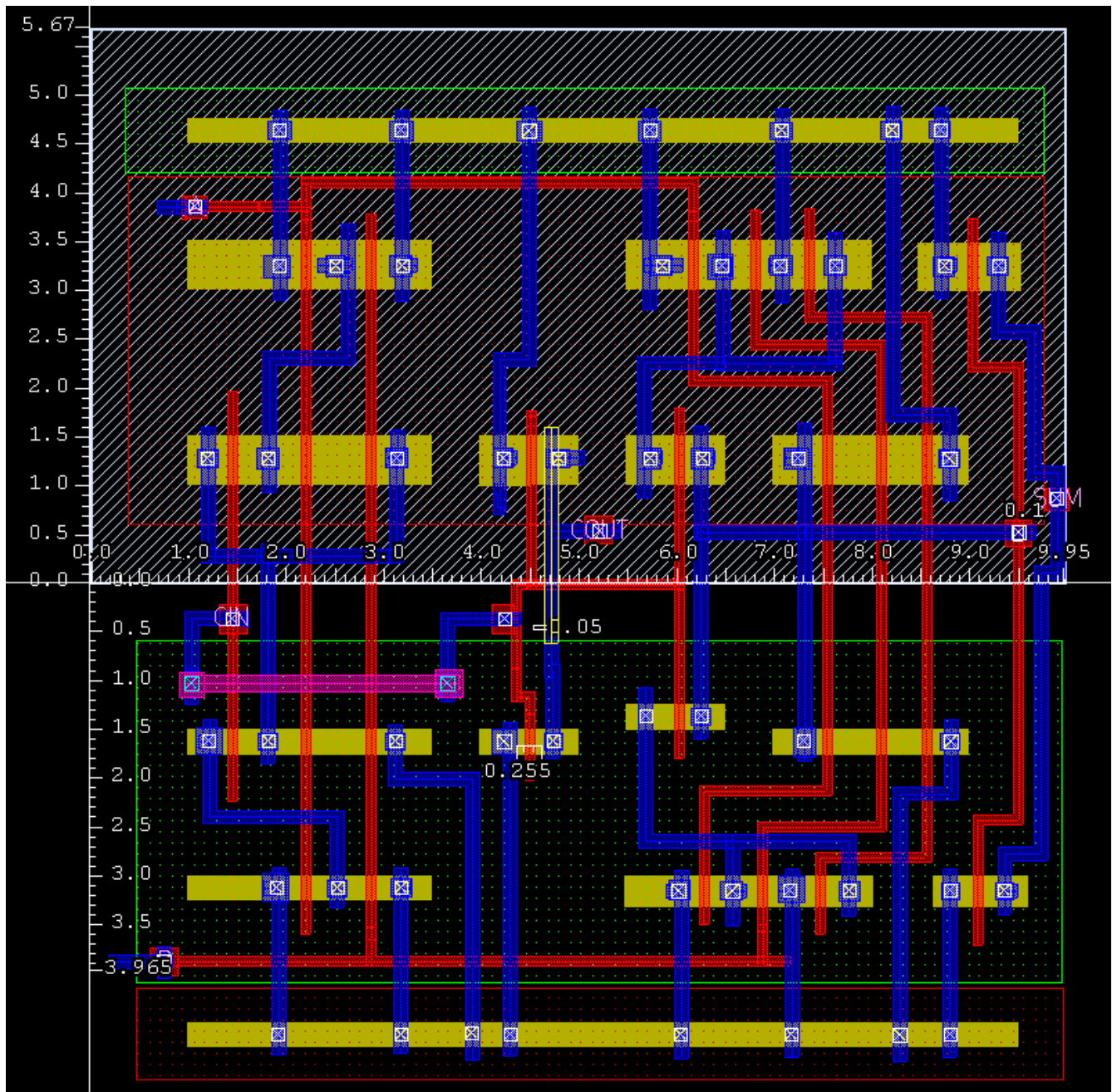


- Your 1-bit full adder schematic - it must be transistor-level not logic-level



- Your 1-bit full adder simulation
- Your 1-bit full adder stick diagram

- Your 1-bit full adder layout



- An DRC Result with CLEAN for your 1-bit full adder

```

32 /home/eemaj/jweiser/eecs168/pvjob_mylibrary.1b_fa.icv.drc/stdout.drc.log - Text Viewer - Cu...
File Edit View Window Help

es.drc.9m_saed90_icv.drc.rs | 1b_fa.drc.cdesigner.rc | 1b_fa.RESULTS | 1b_fa.LAYOUT_ERRORS | stdout.drc.log

ICV_Engine run is 80% complete. Elapsed Time=0:00:02
ICV_Engine run is 85% complete. Elapsed Time=0:00:02
ICV_Engine run is 90% complete. Elapsed Time=0:00:03
ICV_Engine run is 95% complete. Elapsed Time=0:00:03
ICV_Engine run is 100% complete. Elapsed Time=0:00:03

Completing error storage...
Overall error storage time: None

Generating 1b_fa.LAYOUT_ERRORS...
Generation Time=0:00:00 User=0.00 Sys=0.00 Mem=0.502

Check Time=0:00:00 User=0.00 Sys=0.00 Mem=3.125

-----

IC Validator Run: Time=0:00:06

IC Validator Machine Memory Report
bender.engr.ucr.edu : Average = 8.25(Mb), Peak = 146(Mb)

Overall Disk Usage Disk=5.180
Overall engine Time=0:00:06 Highest command Mem=146.557

Overall Master Mem=614.332
IC Validator is done.

Find: [ ] [Next] [Previous] [Match Case] [Regexp]

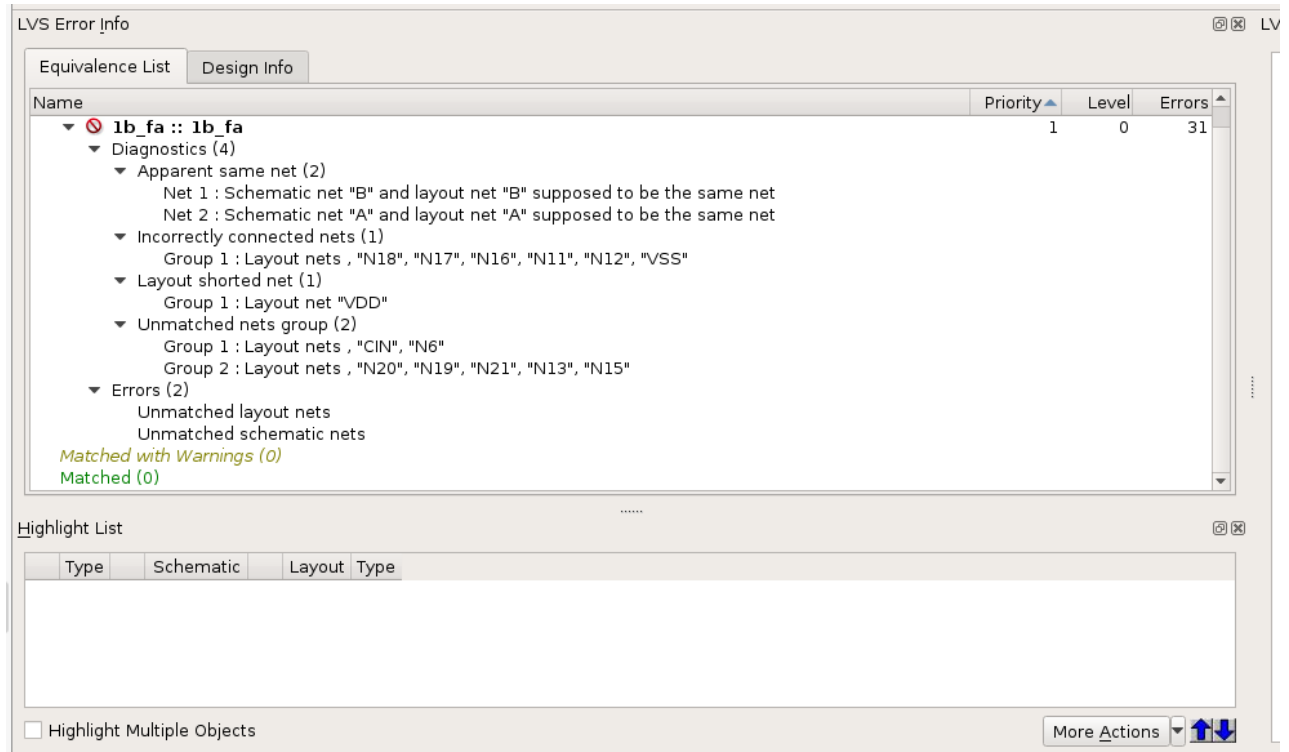
Information: Connection established with 'IC Validator VUE' running on 'bender.engr.ucr.edu'.
Information: Saving design 'mylibrary 1b_fa layout'. (DESIGN_WINDOW-004)
Information:
=====
JobID: icv_drc_33
Completed with no errors.
=====

Information: Connection closed with 'IC Validator VUE' running on 'bender.engr.ucr.edu'.
Information: Connection closed with 'IC Validator VUE' running on 'bender.engr.ucr.edu'.
Information: Connection closed with 'IC Validator VUE' running on 'bender.engr.ucr.edu'.
Information:
=====
JobID: icv_drc_34
Completed with no errors.
=====

Output History Errors/Warnings

```


- An LVS Result with PASS for your 1-bit full adder



The DRC and LVS testing each took about 6-8 hours. The LVS was unresolved. Along the process I learned a lot about

First week: Check off your parasitic extraction and ring oscillator layout and post-simulator

- Second week: Check off your 1-bit full adder layout (DRC, LVS should be okay) and post-simulation
- Third week: Check off your 4-bit full adder layout (DRC, LVS should be okay) and post-simulation
- Fourth week: Extra work time in case you cannot finish within 3 weeks, you should have everything checked off by the end of this week's lab