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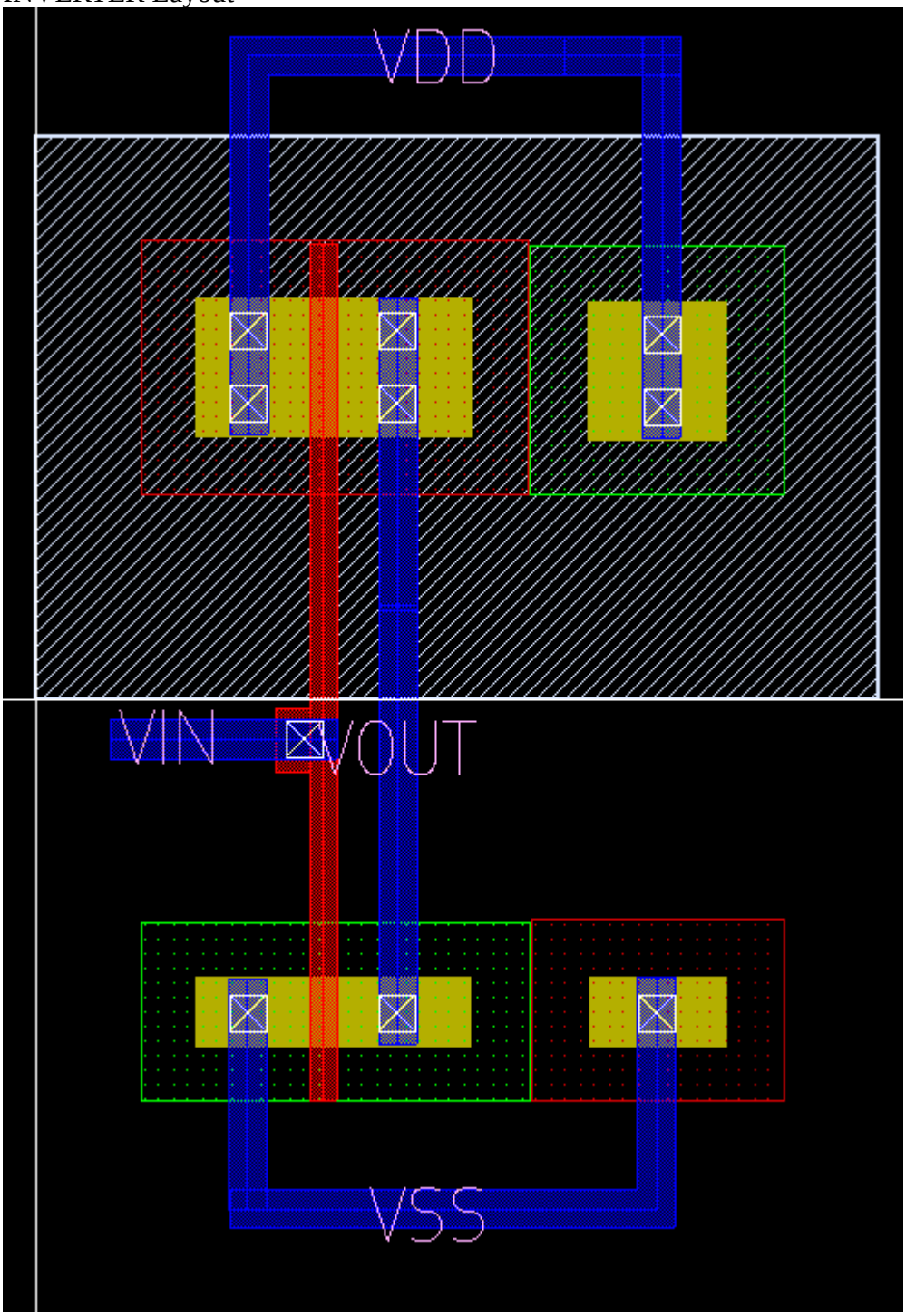
Lab 2

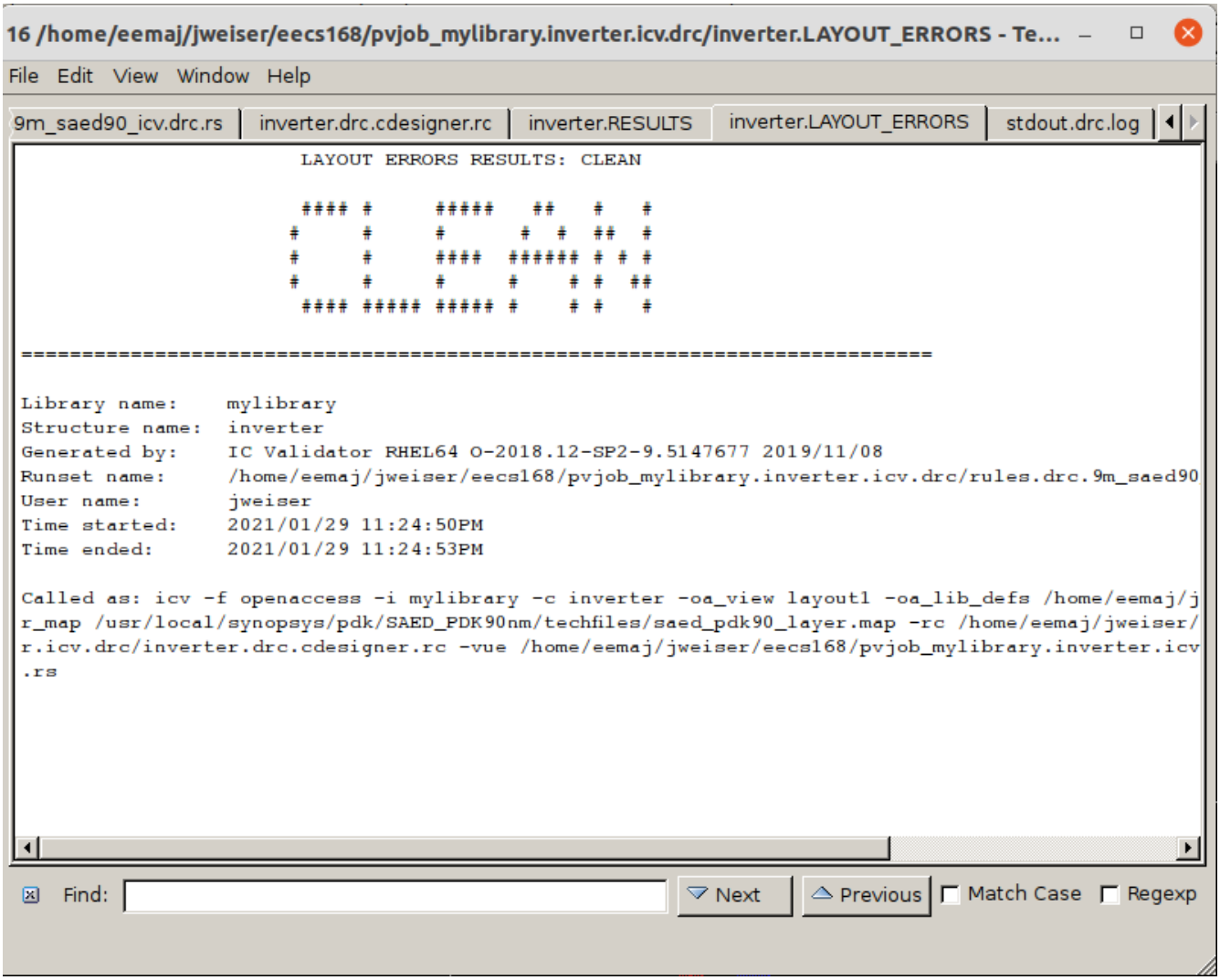
Video Checkoff link:
https://drive.google.com/drive/folders/1Cpb5T16FBCyPfIlKHGQP3RjBh4zqX86X?usp=sharing

Summary:
This lab dealt with creating layouts and running DRC/LVS simulations. We did it with an inverter and a NAND gate. The inverter was left over from Lab 1, but the NAND gate was a new setup. I learned about carefully following each design rule and about how wiring transistors carries over between levels of abstractions. It was also a chance to internalize what low level gates in circuits actually do.

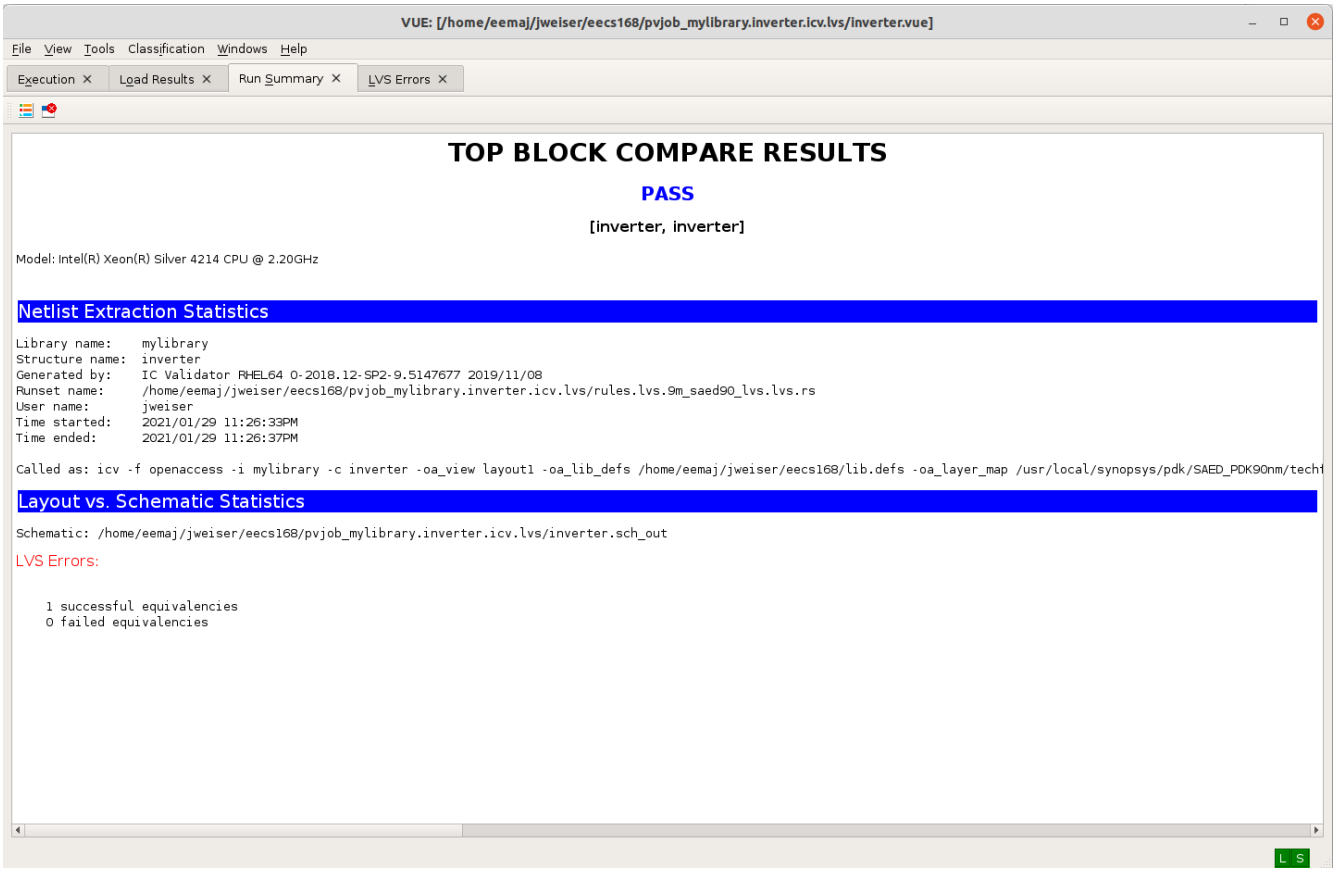
INVERTER Layout



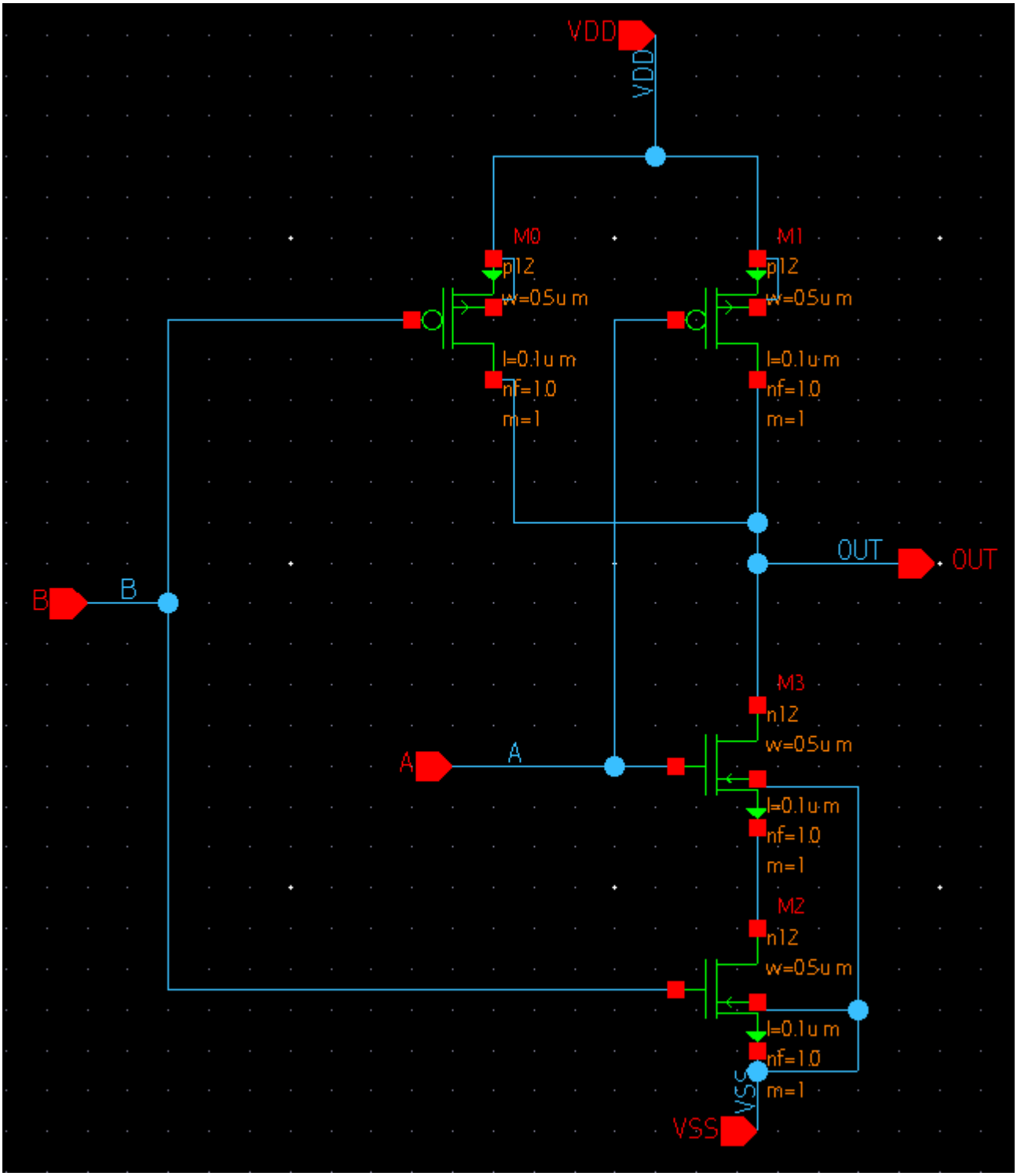
INVERTER DRC



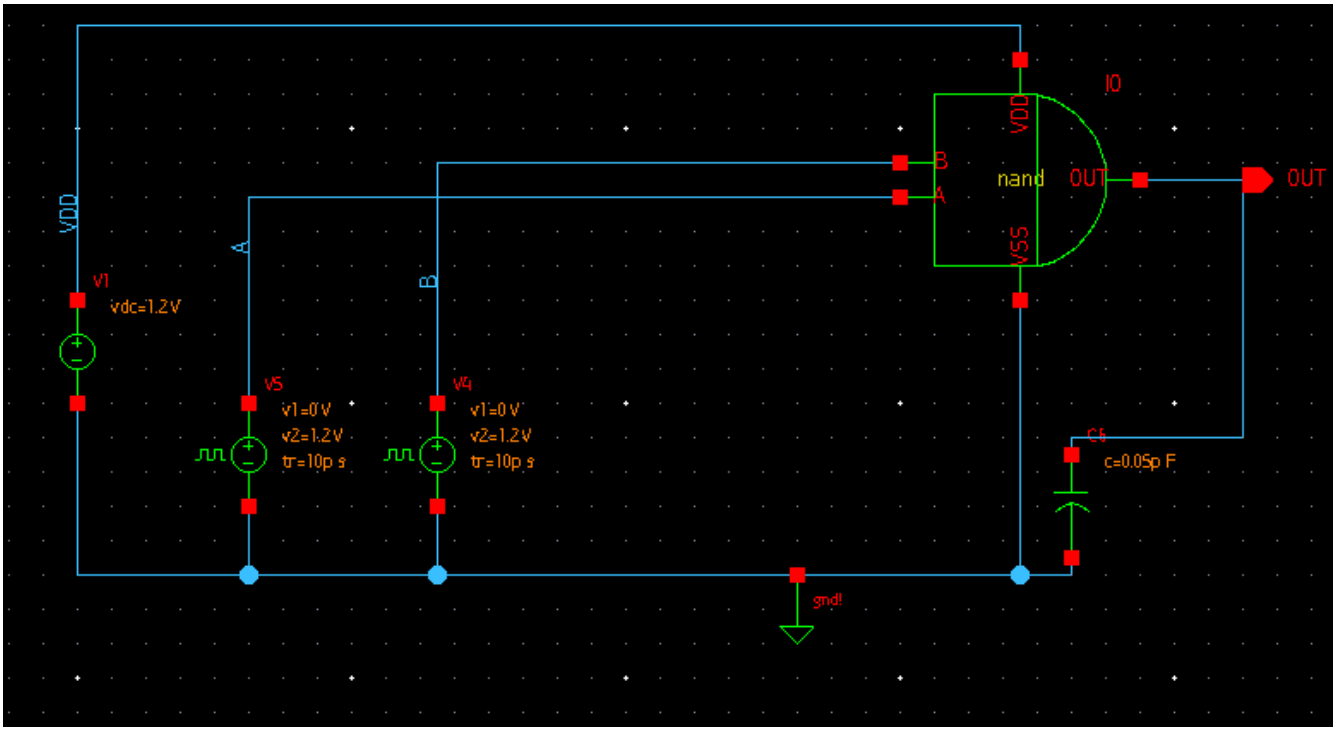
INVERTER LVS


VUE: [/home/eemaj/jweiser/eecs168/pvjob_mylibrary.inverter.icv.lvs/inverter.vue]
File View Tools Classification Windows Help
Execution
Load Results
Run Summary
LVS Errors
TOP BLOCK COMPARE RESULTS
PASS
[inverter, inverter]
Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Netlist Extraction Statistics
Library name: mylibrary
Structure name: inverter
Generated by: IC Validator RHEL64 O-2018.12-SP2-9.5147677 2019/11/08
Runset name: /home/eemaj/jweiser/eecs168/pvjob_mylibrary.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.lvs.rs
User name: jweiser
Time started: 2021/01/29 11:26:33PM
Time ended: 2021/01/29 11:26:37PM
Called as: icv -f openaccess -i mylibrary -c inverter -oa_view layout1 -oa_lib_defs /home/eemaj/jweiser/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDK90nm/techf
Layout vs. Schematic Statistics
Schematic: /home/eemaj/jweiser/eecs168/pvjob_mylibrary.inverter.icv.lvs/inverter.sch_out
LVS Errors:
1 successful equivalencies
0 failed equivalencies
L S

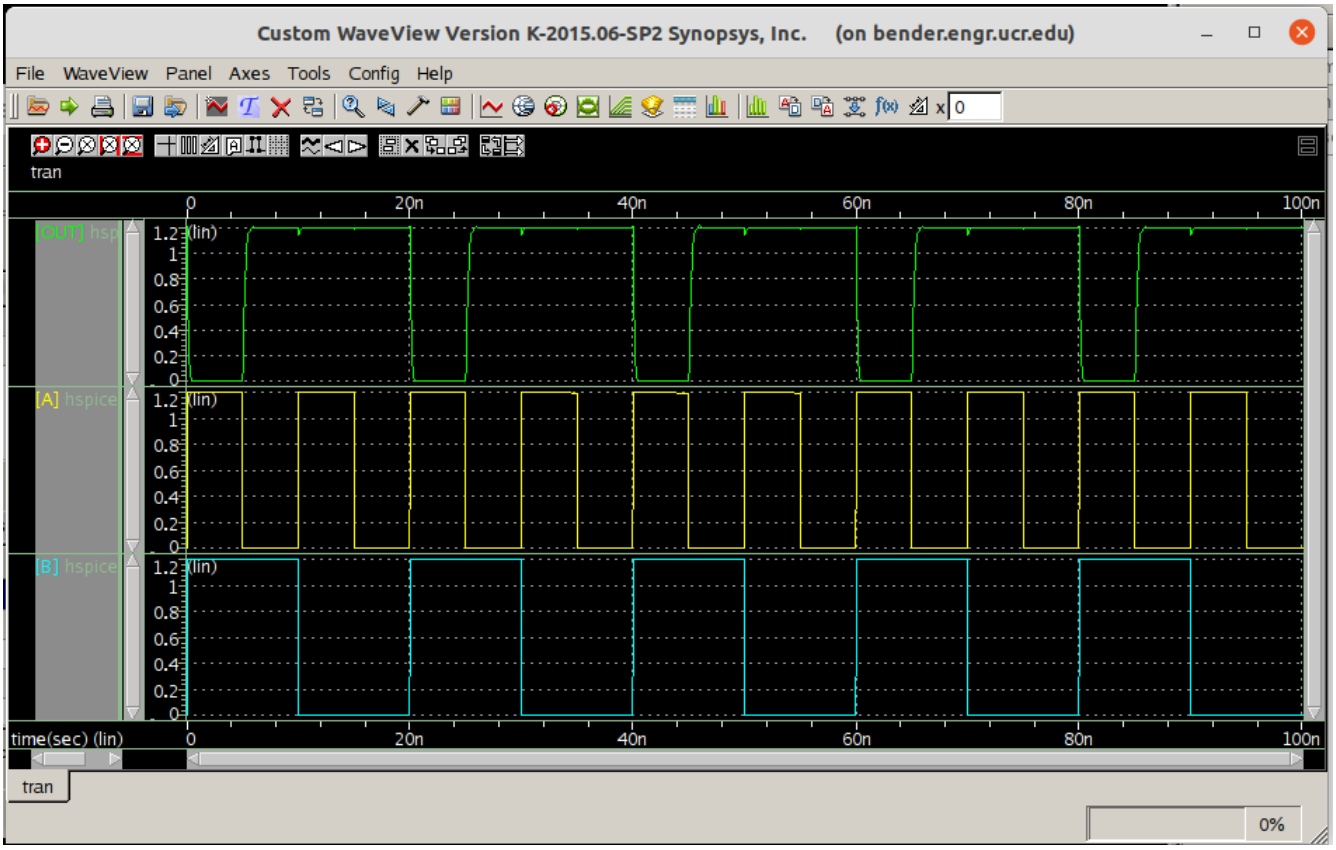
NAND SCHEMATIC



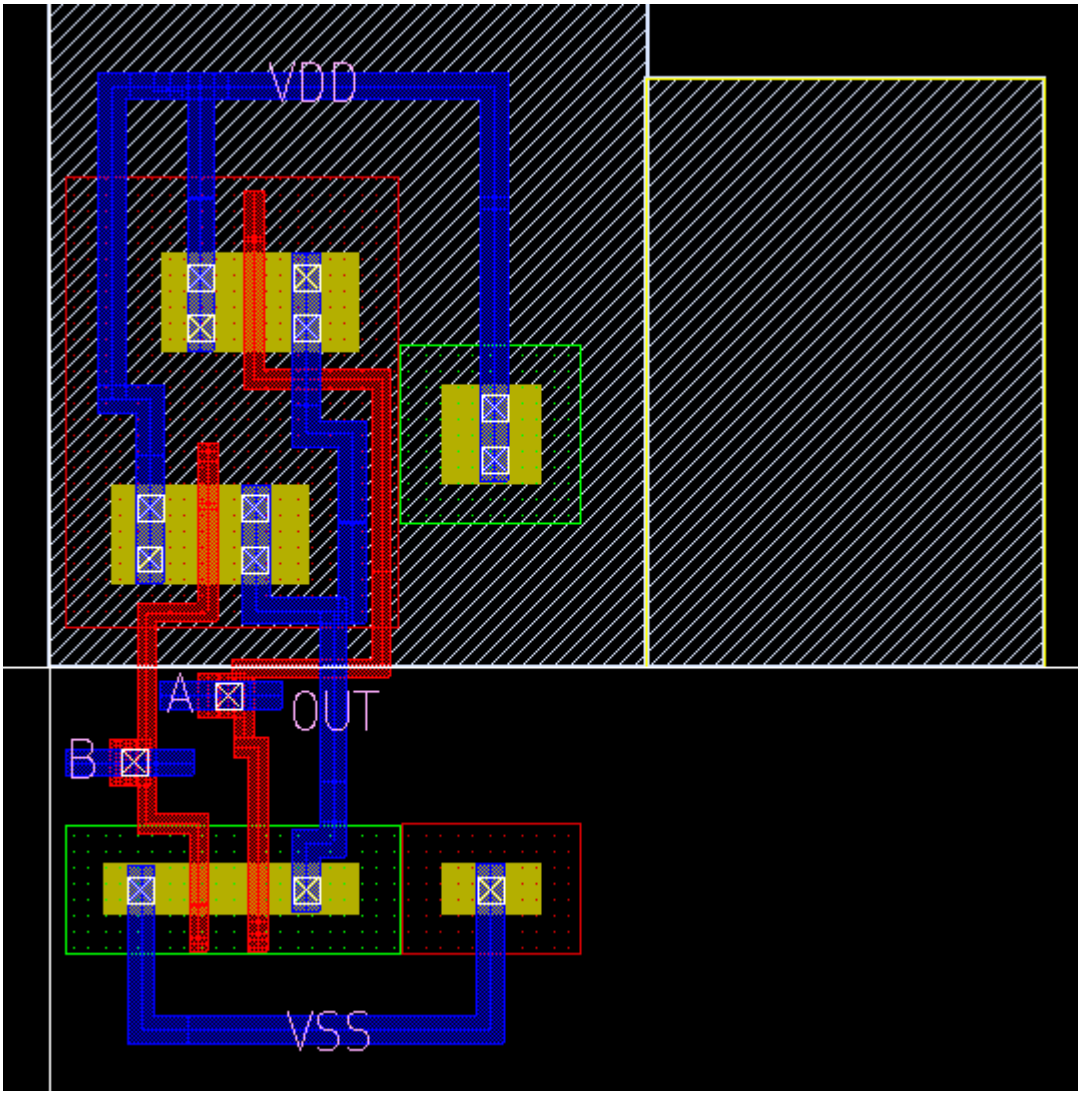
NAND Test Bench Schematic



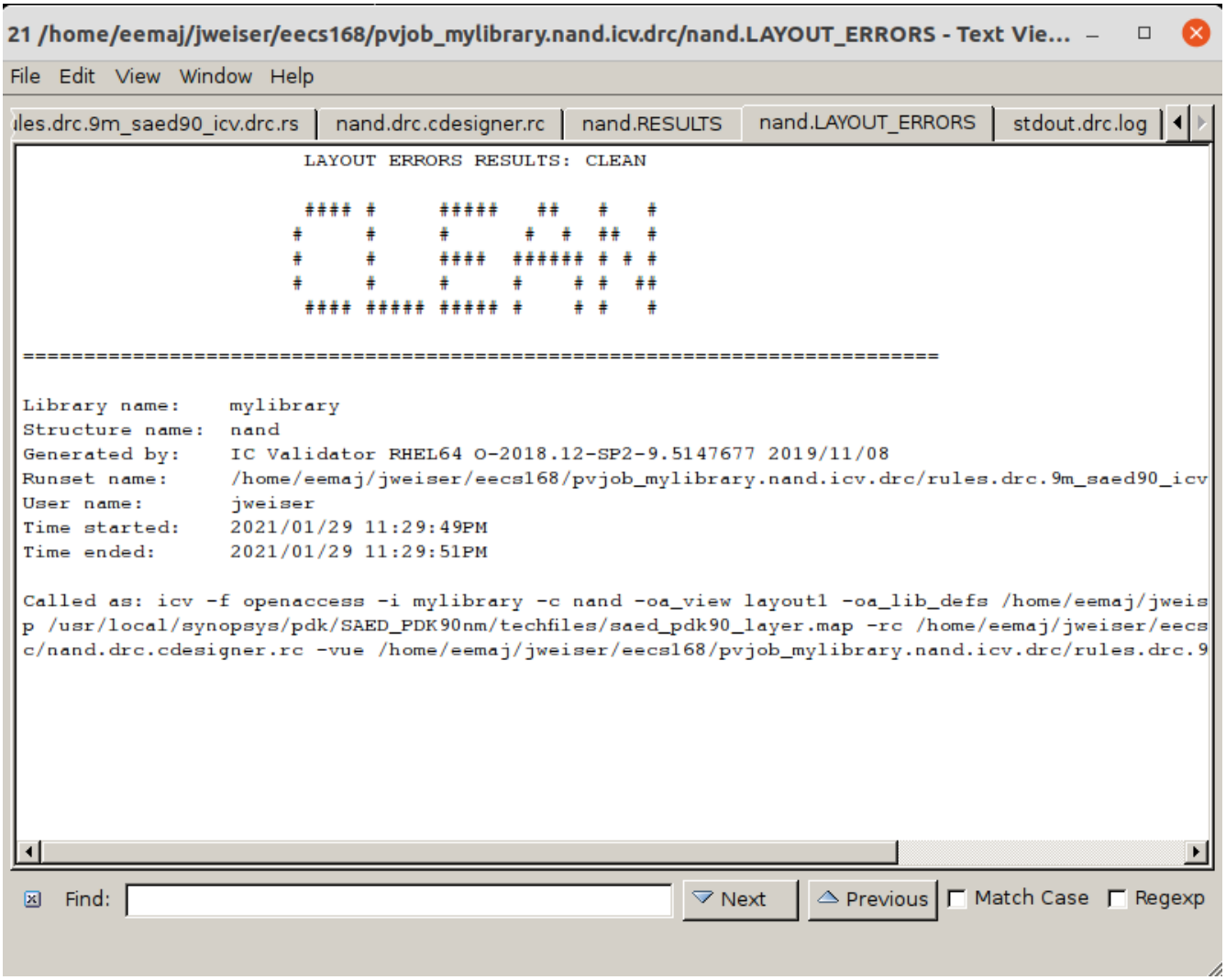
NAND Test Bench Results



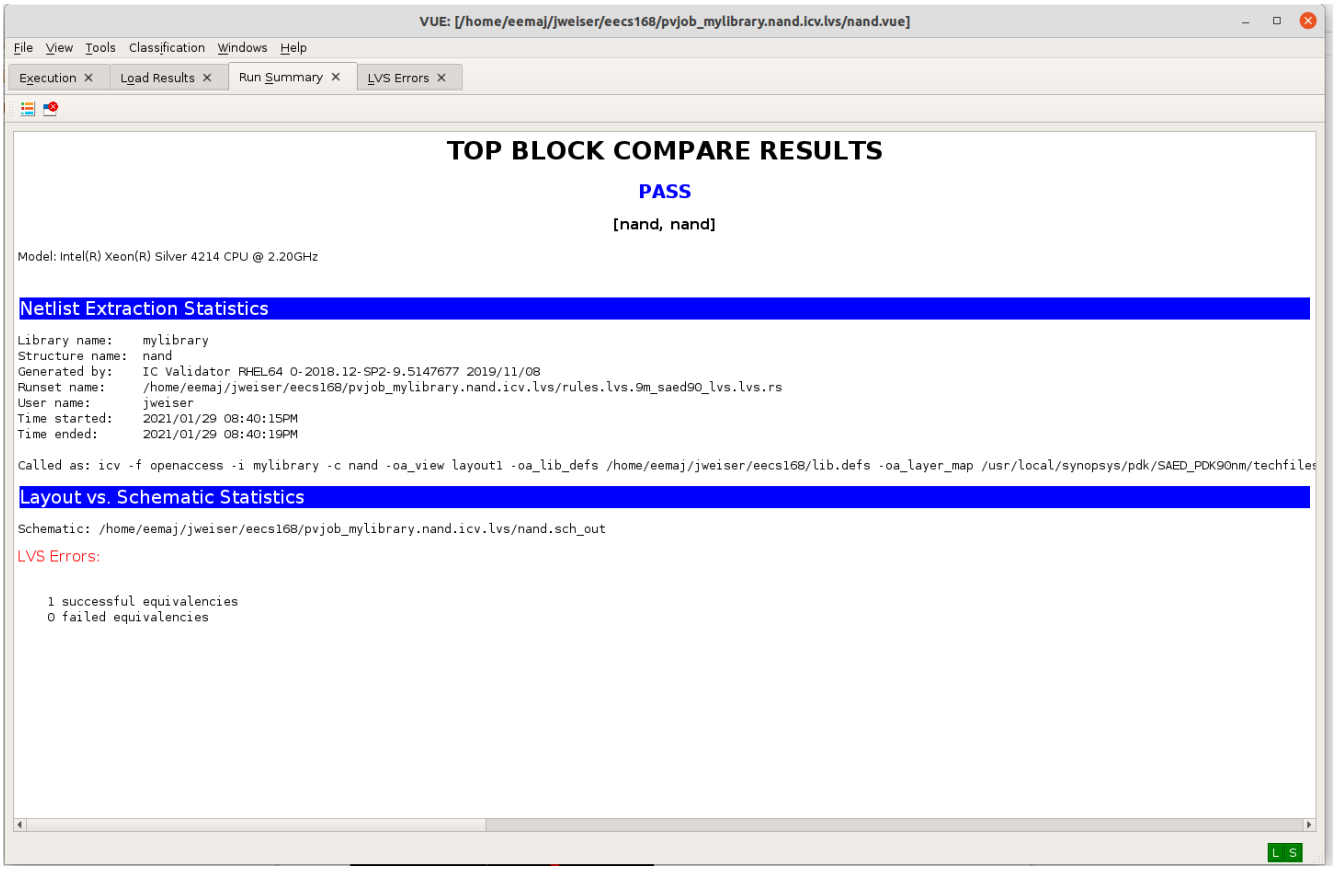
NAND LAYOUT



NAND DRC


21 /home/eemaj/jweiser/eecs168/pvjob_mylibrary.nand.icv.drc/nand.LAYOUT_ERRORS - Text Vie...
File Edit View Window Help
iles.drc.9m_saed90_icv.drc.rs
nand.drc.cdesigner.rc
nand.RESULTS
nand.LAYOUT_ERRORS
stdout.drc.log
LAYOUT ERRORS RESULTS: CLEAN
Library name: mylibrary
Structure name: nand
Generated by: IC Validator RHEL64 O-2018.12-SP2-9.5147677 2019/11/08
Runset name: /home/eemaj/jweiser/eecs168/pvjob_mylibrary.nand.icv.drc/rules.drc.9m_saed90_icv
User name: jweiser
Time started: 2021/01/29 11:29:49PM
Time ended: 2021/01/29 11:29:51PM
Called as: icv -f openaccess -i mylibrary -c nand -oa_view layout1 -oa_lib_defs /home/eemaj/jweis
p /usr/local/synopsys/pdk/SAED_PDK90nm/techfiles/saed_pdk90_layer.map -rc /home/eemaj/jweiser/eecs
c/nand.drc.cdesigner.rc -vue /home/eemaj/jweiser/eecs168/pvjob_mylibrary.nand.icv.drc/rules.drc.9
Find:
Next
Previous
Match Case
Regexp

NAND LVS



Issues:

I had an issue with matching names on the NAND gate because I didn’t share connections on the wires of the bottom 2 gates for the schematic. I had trouble with the NAND test bench parameters. General unfamiliarity and learning was also a challenge.