Integrated Digital Light Sensor with Interrupt

ISL29035

The ISL29035 is an integrated ambient and infrared light-to-digital converter with I²C (SMBus Compatible) Interface. Its advanced self-calibrated photodiode array emulates human eye response with excellent IR rejection. The on-chip ADC is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The Lux range select feature allows users to program the Lux range for optimized counts/Lux.

For ambient light sensing, an internal 16-bit ADC has been designed based upon the charge-balancing technique. The ADC conversion time is nominally 90ms and is user adjustable from 11µs to 90ms, depending on oscillator frequency and ADC resolution. In normal operation, typical current consumption is 57µA. In order to further minimize power consumption, two power-down modes have been provided. If polling is chosen over continuous measurement of light, the auto-power-down function shuts down the whole chip after each ADC conversion for the measurement. The other power-down mode is controlled by software via the I²C interface. The power consumption can be reduced to less than 0.3µA when powered down.

The ISL29035 supports a software brownout condition detection. The device powers up with the brownout bit asserted until the host clears it through the I²C interface.

The ISL29035 supports a software and hardware interrupt that remains asserted until the host clears it through the I²C interface. Function of ADC conversion continues without stopping after interrupt is asserted.

Designed to operate on supplies from 2.25V to 3.63V with an I²C supply from 1.7V to 3.63V, the ISL29035 is specified for operation over the -40°C to +85°C ambient temperature range.

Features

- Resolution . . . . . .16-bits ADC
- Wide dynamic range 1:4,200,000
- Integrated noise reduction 50/60Hz
- Close to human eye response with excellent IR/UV rejection
- Shutdown modes . . . . . .Software and Automatic
- Programmable interrupt threshold with persistence filter
- Supply current (typ) 57µA
- Shutdown current (max) 0.3µA
- I²C (SMB compatible) power supply . . . . . 1.7V to 3.63V
- Sensor power supply . . . . . 2.25V to 3.63V
- Operating temperature range. . . . . -40°C to +85°C
- Small form factor package . . . . . 6 Ld 1.5x1.6x0.75 ODFN

Applications

- Mobile devices: smart phone, PDA, GPS
- Computing devices: notebook PC, MacBook, tablets
- Consumer devices: LCD-TV, digital camera
- Industrial and medical light sensing

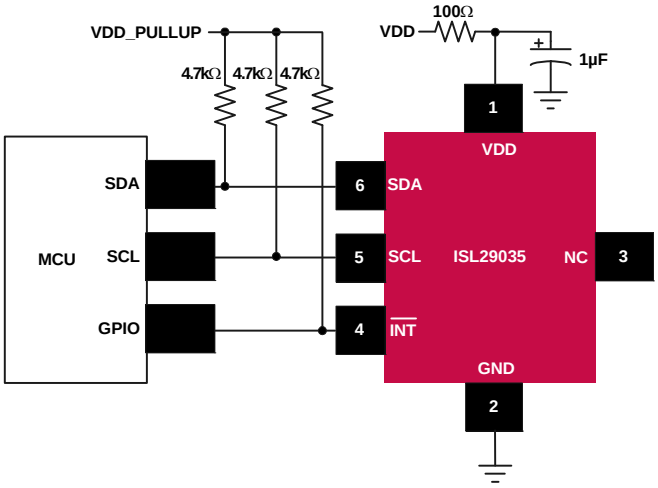


FIGURE 1. ISL29035 TYPICAL APPLICATION DIAGRAM

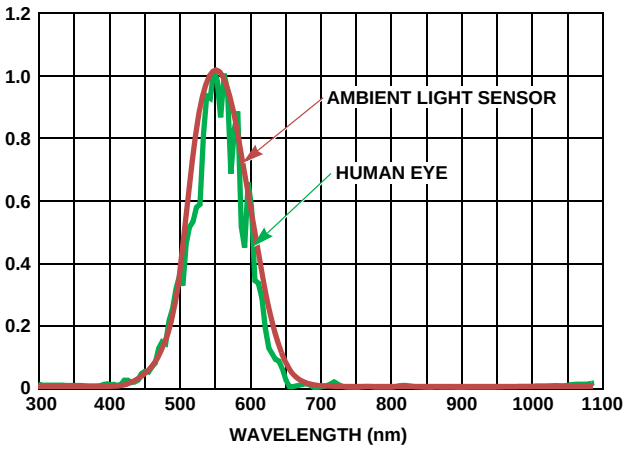
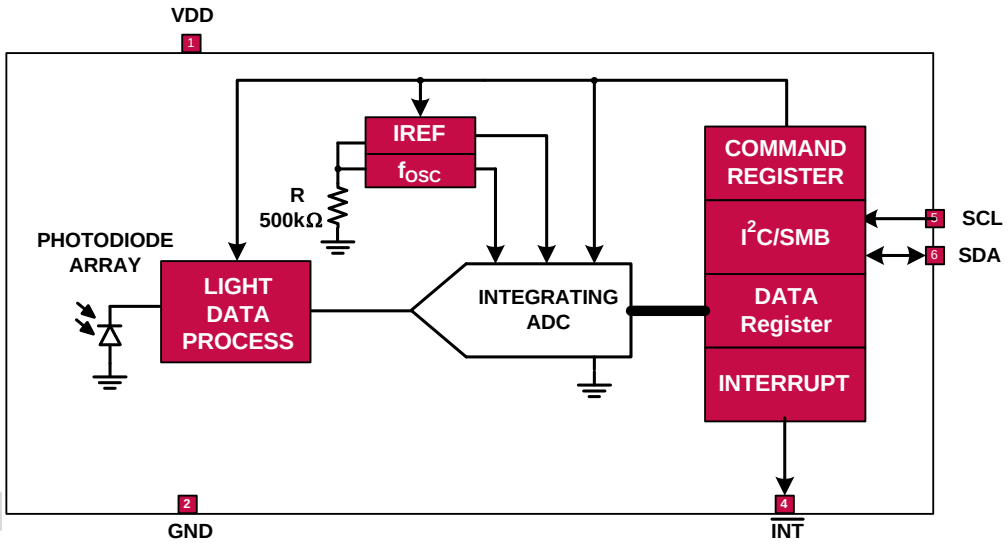


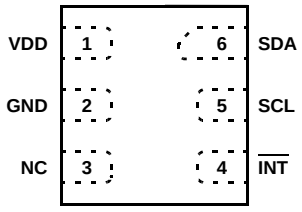
FIGURE 2. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING

Block Diagram



Pin Configuration

ISL29035
(6 LD ODFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VDD	Positive supply
2	GND	Ground pin
3	NC	No Connect
4	$\overline{INT}$	Interrupt pin; LOW for interrupt alarming. $\overline{INT}$ pin is open drain. $\overline{INT}$ remains asserted until the interrupt status bit is reset.
5	SCL	I^2C serial clock
6	SDA	I^2C serial data

Ordering Information

PART NUMBER (Notes 2, 3)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-free)	PKG. DWG. #
ISL29035IROZ-T7 (Note 1)	-40 to +85	6 Ld ODFN	L6.1.5x1.6
ISL29035IROZ-EVALZ	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL please see tech brief TB477.

Absolute Maximum Ratings

VDD to GND ..... +4.0V
I^2C Bus (SCL, SDA) and $\overline{INT}$ Pin Voltage..... -0.2V to 4.0V
I^2C Bus (SCL, SDA) and $\overline{INT}$ Pin Current..... <10mA
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
Human Body Model 3kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
6 Ld ODFN Package (Note 4)	210

Maximum Junction Temperature (TJ_{MAX})..... +90°C
Storage Temperature Range..... -40°C to +100°C
Operating Temperature ..... -40°C to +85°C
b-Free Reflow Profile (*) ..... see TB477
*Peak temperature during solder reflow +235°C max

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{DD}	Power Supply Range		2.25		3.63	V
I_{DD}	Supply Current			57	85	µA
I_{DD1}	Supply Current when Powered Down	Software disabled or auto power-down		0.24	0.51	µA
V_{I^2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V
t_{int}	ADC Integration/Conversion Time	16-bit ADC data		105		ms
F_{I^2C}	I^2C Clock Rate Range			400		kHz
DATA_0	Count Output When Dark	E = 0 Lux, Range 0 (1k Lux)		1	5	Counts
DATA_F	Full Scale ADC Code				65535	Counts
%/Value	Light Source Variation (3σ population)	E = 300 Lux, Cold White LED (Range 1k Lux)		±5		%
ADC_{R0}	Light Count Output with LSB of 0.015 Lux/count	E = 300 Lux, Cold White LED (Note 5), ALS (Range 0 to 1k Lux)		20473		Counts
ADC_{R1}	Light Count Output with LSB of 0.06 Lux/count	E = 300 Lux, Cold White LED (Note 5), ALS (Range 1 to 4k Lux)		5100		Counts
ADC_{R2}	Light Count Output with LSB of 0.24 Lux/count	E = 300 Lux, Cold White LED, ALS (Range 2 to 16k Lux)		1400		Counts
ADC_{R3}	Light Count Output with LSB of 0.96 Lux/count	E = 300 Lux, Cold White LED (Note 5), ALS (Range 3 to 64k Lux)		366		Counts
ADC_IR_{R0}	Infrared Count Output	Range 0 to 1k Lux	1402	1997	2598	
ADC_IR_{R1}	Infrared Count Output	Range 1 to 4k Lux		481		
ADC_IR_{R2}	Infrared Count Output	Range 2 to 16k Lux		148		
ADC_IR_{R3}	Infrared Count Output	Range 3 to 64k Lux		42		
I_{SDA}	SDA Current Sinking Capability		4	5		mA
I_{INT}	$\overline{INT}$ Current Sinking Capability		4	5		mA

NOTES:

5. 550nm green LED is used in production test. The 550nm LED irradiance is calibrated to produce the same DATA count against an illuminance level of 300 Lux Cold White LED.
6. 850nm IR LED is used in production test. The 850nm LED irradiance is calibrated to produce the same DATA_IR count against an illuminance level of 210 Lux sunlight at sea level.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. A illuminant is intended to represent typical, domestic, tungsten-filament lighting. Its CCT is about 2856K.
9. D series of illuminants are constructed to represent natural daylight. D65 is used in lab to represent as noon light to test. Its CCT is 6504K
10. F series of illuminants represent various types of fluorescent lighting. F2 is cool white fluorescent using in lab to test. Its CCT is 4230K

I²C Interface Specifications V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{IL}	SDA and SCL Input Buffer LOW Voltage				0.55	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		1.25			V
V_{Hys} (Note 11)	SDA and SCL Input Buffer Hysteresis			0.05 x V_{DD}		V
V_{OL} (Note 11)	SDA Output Buffer LOW Voltage (open-drain), Sinking 4mA		0	0.06	0.4	V
C_{PIN} (Note 11)	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid				900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission		1300			ns
t_{LOW}	Clock LOW Time		1300			ns
t_{HIGH}	Clock HIGH Time		600			ns
$t_{SU:STA}$	START Condition Setup Time		600			ns
$t_{HD:STA}$	START Condition Hold Time		600			ns
$t_{SU:DAT}$	Input Data Setup Time		100			ns
$t_{HD:DAT}$	Input Data Hold Time		30			ns
$t_{SU:STO}$	STOP Condition Setup Time		600			ns
$t_{HD:STO}$	STOP Condition Hold Time		600			ns
t_{DH}	Output Data Hold Time		0			ns
t_R (Note 11)	SDA and SCL Rise Time		20 + 0.1 x Cb			ns
t_F (Note 11)	SDA and SCL Fall Time		20 + 0.1 x Cb			ns
C_b (Note 13)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip			400	pF
R_{PU} (Note 11)	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ For Cb = 40pF, max is about 15kΩ ~ 20kΩ	1			kΩ

NOTES:

11. Limits should be considered typical and are not production tested.

12. These are I²C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.

13. C_b is the capacitance of the bus in pF.

SDA vs SCL Timing

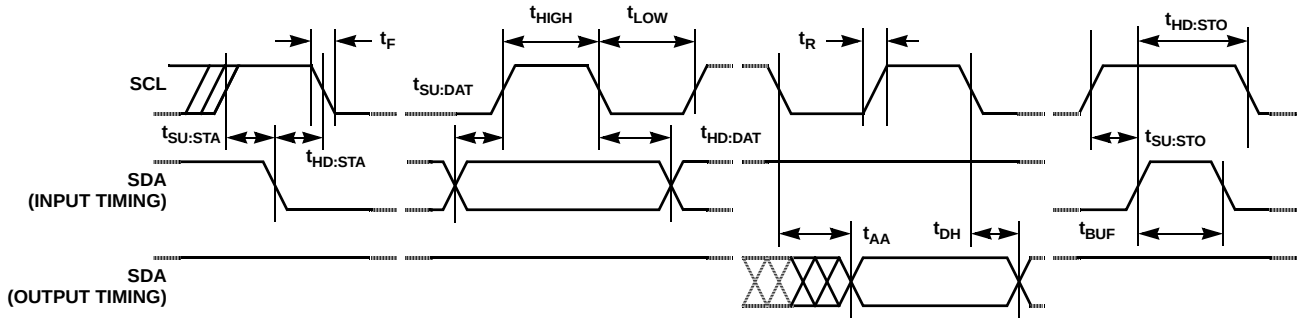


FIGURE 3. I²C BUS TIMING

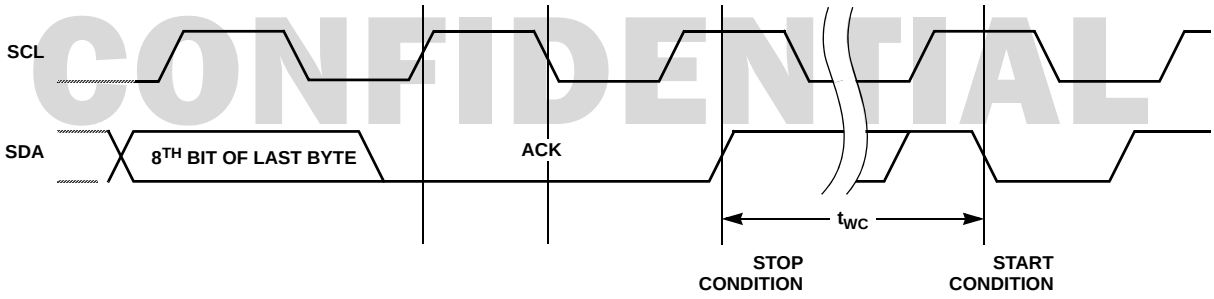


FIGURE 4. I²C WRITE CYCLE TIMING

Typical Performance Curves

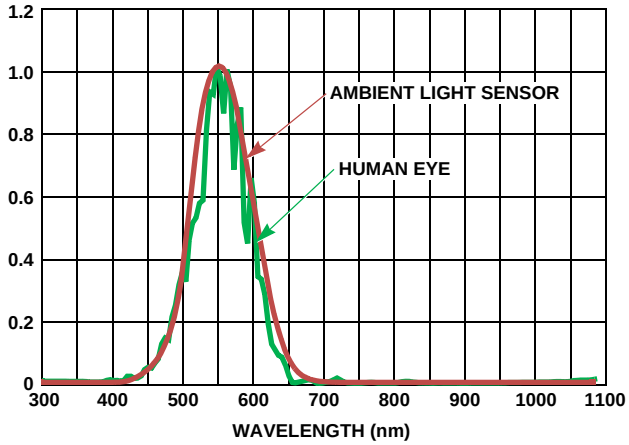


FIGURE 5. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING AND IR SENSING

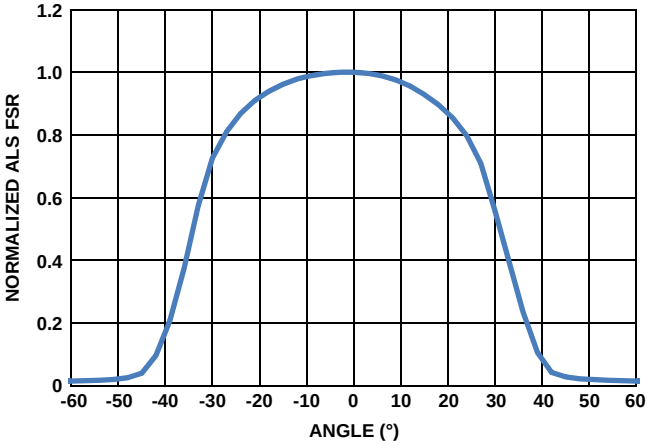


FIGURE 6. NORMALIZED RADIATION PATTERN

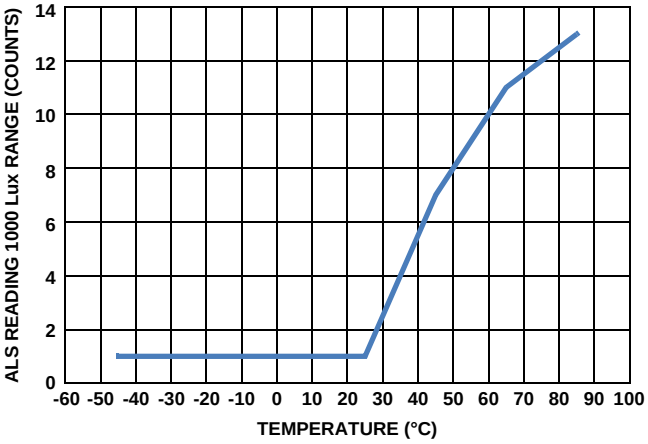


FIGURE 7. TEMPERATURE TEST IN DARK CONDITION

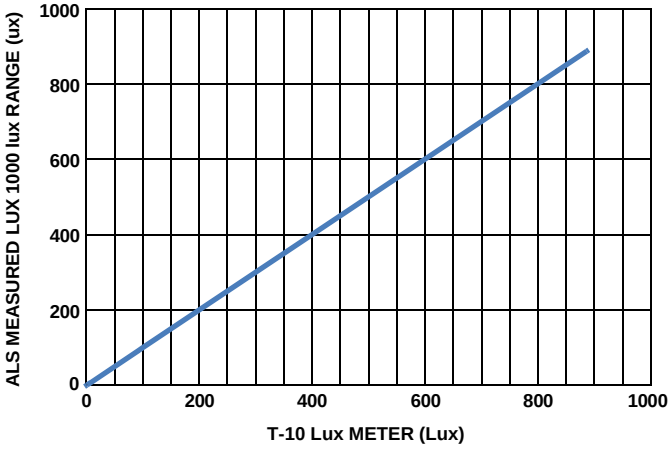


FIGURE 8. ALS TRANSFER FUNCTION UNDER F2 LIGHT SOURCE

Principles of Operation

Photodiodes and ADC

The ISL29035 contains two photodiode arrays, which convert light into current. The spectral response for ambient light sensing and IR sensing is shown in Figure 14 on page 12 in the "Applications" section. After light is converted to current during the light signal process, the current output is converted to digital by a built-in 16-bit Analog-to-Digital Converter (ADC). An I^2C command reads the ambient light or IR intensity in counts.

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously.

The integration time of the built-in ADC is determined by the internal oscillator, and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. A good balancing act of integration time and resolution (depending on the application) is required for optimal results.

The ADC has I^2C programmable range select to dynamically accommodate various lighting conditions. For very dim conditions, the ADC can be configured at its lowest range (Range 1) in the ambient light sensing.

Low-Power Operation

The ISL29035 initial operation is at the power-down mode after a supply voltage is provided. The data registers contain the default value of 0. When the ISL29035 receives an I^2C command to do a one-time measurement from an I^2C master, it will start ADC conversion with light sensing. It will go to the power-down mode automatically after one conversion is finished and keep the conversion data available for the master to fetch anytime afterwards. The ISL29035 will continuously do ADC conversion with light sensing if it receives an I^2C command of continuous measurement. It will continuously update the data registers with the latest conversion data. It will go to the power-down mode after it receives the I^2C command of power-down.

Ambient Light and IR Sensing

There are four operational modes in ISL29035: Programmable ALS once with auto power-down, programmable IR sensing once with auto power-down, programmable continuous ALS sensing and programmable continuous IR sensing. These four modes can be programmed in series to fulfill the application needs. The detailed program configuration is listed in "Command-I Register (Address: 0x00)" on page 10.

When the part is programmed for ambient light sensing, the ambient light with wavelength within the "Ambient Light Sensing" spectral response curve in Figure 14 is converted into current. With ADC, the current is converted to an unsigned n-bit (up to 16 bits) digital output.

When the part is programmed for infrared (IR) sensing, the IR light with wavelength within the "IR Sensing" spectral response curve in Figure 14 is converted into current. With ADC, the current is converted to an unsigned n-bit (up to 16-bits) digital output.

Interrupt Function

The active low interrupt pin is an open drain pull-down configuration. The interrupt pin serves as an alarm or monitoring function to determine whether the ambient light level exceeds the upper threshold or goes below the lower threshold. It should be noted that the function of ADC conversion continues without stopping after interrupt is asserted. If the user needs to read the ADC count that triggers the interrupt, the reading should be done before the data registers are refreshed by the following conversions. The user can also configure the persistency of the interrupt pin. This reduces the possibility of false triggers, such as noise or sudden spikes in ambient light conditions. An unexpected camera flash, for example, can be ignored by setting the persistency to 8 integration cycles.

Serial Interface

The ISL29035 supports the Inter-Integrated Circuit (I^2C) bus data transmission protocol. The I^2C bus is a two-wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I^2C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a "0" and releases it to transmit a "1". The master always initiates the data transfer, only when the bus is not busy, and provides the clock for both transmit and receive operations. The ISL29035 operates as a slave device in all applications. The serial communication over the I^2C interface is conducted by sending the most significant bit (MSB) of each byte of data first.

Start Condition

During data transfer, the SDA line must remain stable while the SCL line is HIGH. All I^2C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH (refer to Figure 11 on page 8). The ISL29035 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (refer to Figure 11). A START condition is ignored during the power-up sequence.

Stop Condition

All I^2C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH (refer to Figure 11). A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before 1 full Data byte + ACK is sent, then the serial communication of the ISL29035 resets itself without performing the read/write. The contents of the array are not affected.

Acknowledge

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (refer to Figure 11). The ISL29035 responds with an ACK after recognition of a START condition

followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL29035 also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation.

Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of the ISL29035 are internally hard-wired as “1000100”. The LSB of the Device Address byte is defined as a read or write (R/$\overline{W}$) bit. When this R/$\overline{W}$ bit is a “1”, a read operation is selected and when “0”, a write operation is selected (refer to Figure 9). The master generates a START condition followed by Device Address byte 1000100x (x as R/$\overline{W}$) and the ISL29035 compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line (refer to Figure 11).

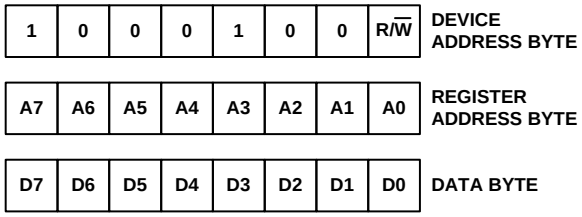


FIGURE 9. DEVICE ADDRESS, REGISTER ADDRESS AND DATA BYTE

Write Operation

BYTE WRITE

In a byte write operation, the ISL29035 requires the Device Address byte, Register Address byte, and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte, and the Data byte, the ISL29035 responds with an acknowledge (ACK). Following the ISL29035 data acknowledge response, the master terminates the transfer by generating a STOP condition. The ISL29035 then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master (refer to Figure 10).

BURST WRITE

The ISL29035 has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ISL29035 responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it “rolls over” and goes back to the first Register Address.

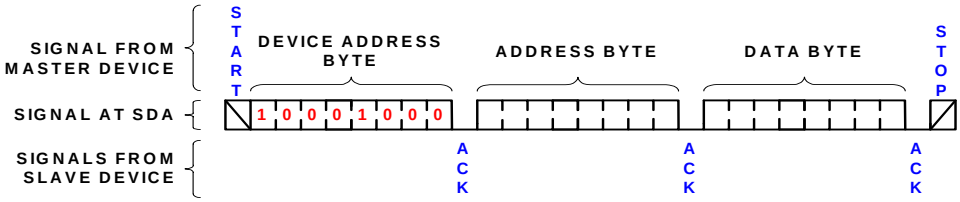


FIGURE 10. BYTE WRITE SEQUENCE

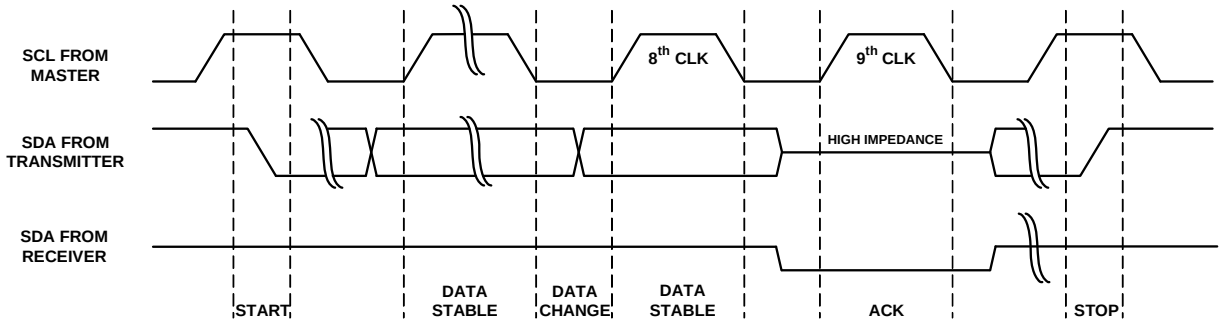


FIGURE 11. START, DATA STABLE, ACKNOWLEDGE AND STOP CONDITION

Read Operation

The ISL29035 has two basic read operations: Byte Read and Burst Read.

BYTE READ

Byte read operations allow the master to access any register location in the ISL29035. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/$\overline{W}$ bit set to “0”, receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/$\overline{W}$ bit set to “1”. This is followed by an acknowledge from the device and then by the 8-bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition (refer to Figure 12).

BURST READ

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition (refer to Figure 13).

For more information about the I^2C standard, please consult the Phillips™ I^2C specification documents.

Power-On Reset

The Power-On Reset (POR) circuitry protects the internal logic against powering up in the incorrect state. The ISL29035 will power-up into Standby mode after V_{DD} exceeds the POR trigger level and will power-down into Reset mode when V_{DD} drops below the POR trigger level. This bidirectional POR feature protects the device against ‘brown-out’ failure following a temporary loss of power.

The POR is an important feature because it prevents the ISL29035 from starting to operate with insufficient voltage, prior to stabilization of the internal bandgap. The ISL29035 prevents communication to its registers and greatly reduces the likelihood of data corruption on power-up.

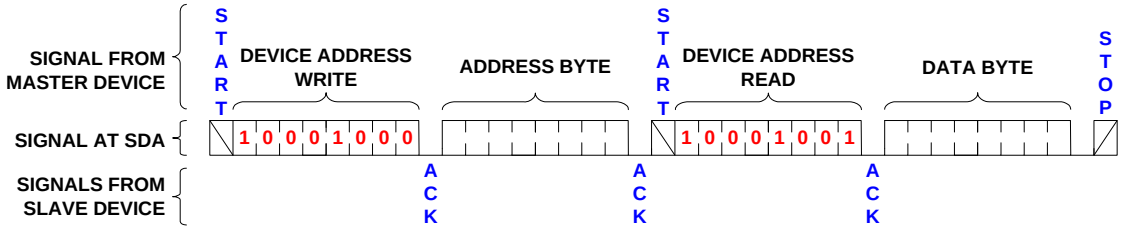


FIGURE 12. BYTE ADDRESS READ SEQUENCE

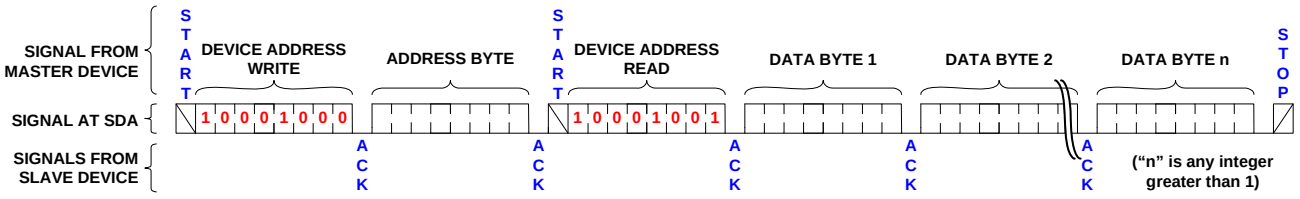


FIGURE 13. BURST READ SEQUENCE

TABLE 1. REGISTER MAP

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
COMMAND-I	0	0x00	OP2	OP1	OP0	RESERVED		$\overline{INT}$	PRST1	PRST0	0x00	RW
COMMAND-II	1	0x01	RESERVED				RES1	RES0	RANGE1	RANGE0	0x00	RW
$DATA_{LSB}$	2	0x02	D7	D6	D5	D4	D3	D2	D1	D0	0x00	RO
$DATA_{MSB}$	3	0x03	D15	D14	D13	D12	D11	D10	D9	D8	0x00	RO
INT_LT_LSB	4	0x04	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00	RW
INT_LT_MSB	5	0x05	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8	0x00	RW
INT_HT_LSB	6	0x06	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF	RW
INT_HT_MSB	7	0x07	TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8	0xFF	RW
ID	15	0x0F	BOUT	RESERVED	1	0	1	RESERVED			1x101xxx	RW

Register Description

Following are detailed descriptions of the control registers related to the operation of the ISL29035 ambient light sensor device. These registers are accessed by the I^2C serial interface. For details on the I^2C interface, refer to “Serial Interface” on page 7.

All the features of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. All RESERVED bits are Intersil used bits ONLY. The value of the reserved bit can change without notice.

Decimal to Hexadecimal Conversion

To convert decimal value to hexadecimal value, divide the decimal number by 16, and write the remainder on the side as the least significant digit. This process is continued by dividing the quotient by 16 and writing the remainder until the quotient is 0. When performing the division, the remainders, which will represent the hexadecimal equivalent of the decimal number, are written beginning with the least significant digit (right) and each new digit is written to the next more significant digit (the left) of the previous digit. Consider the number 175 decimal.

TABLE 2. DECIMAL TO HEXADECIMAL

DIVISION	QUOTIENT	REMINDER	HEX NUMBER
175/16	10 = A	15 = F	0xAF

Command-I Register (Address: 0x00)

TABLE 3. COMMAND-I REGISTER ADDRESS

NAME	ADDR (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
COMMANDI	0x00	OP2	OP1	OP0	RESERVED		$\overline{INT}$	PRST1	PRST0	0x00

The Command-I register consists of control and status bits. In this register, there are two interrupt persist bits, one interrupt status bit, and three operation mode bits. The operation mode bits and the interrupt persist bits are independent of each other. The default register value is 0x00 at power-on.

INTERRUPT PERSIST BITS (B0 - B1)

The interrupt persist bits provide control over when interrupts occur. There are four different selections for this feature. A value of *N* (where *N* is 1, 4, 8, and 16) results in an interrupt only if the value remains outside the threshold window for *N* consecutive integration cycles. For example, if *N* is equal to 16 and the ADC resolution is set to 16-bits, then the integration time is 100ms. An interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing the COMMAND register with the CLEAR bit set. Table 4 lists the possible interrupt persist bits.

TABLE 4. INTERRUPT PERSIST BITS

B1	B0	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

INTERRUPT STATUS BIT (B2)

The interrupt status bit ($\overline{INT}$) is a status bit for light intensity detection. The bit is set to logic HIGH when the light intensity crosses the interrupt thresholds window (register address 0x04 - 0x07), and set to logic LOW when it is within the interrupt thresholds window. Once the interrupt is triggered, the $\overline{INT}$ pin goes low and the interrupt status bit goes HIGH until the status bit is polled through the I^2C read command. Both the $\overline{INT}$ pin and the interrupt status bit are automatically cleared at the end of the 8-bit Device Register byte (0x00) transfer. Table 5 shows the interrupt status states.

TABLE 5. INTERRUPT STATUS BIT ($\overline{INT}$)

BIT 2	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

OPERATION MODE BITS (B5 - B7)

The ISL29035 has different operating modes. These modes are selected by setting B5 - B7 bits on register address 0x00. The device powers up on a disable mode. Table 6 lists the possible operating modes.

TABLE 6. OPERATING MODES BITS

B7	B6	B5	OPERATION
0	0	0	Power-down the device (Default)
0	0	1	The device measures ALS only once every integration cycle. This is the lowest operating mode.
0	1	0	IR once
0	1	1	Reserved (DO NOT USE)
1	0	0	Reserved (DO NOT USE)
1	0	1	Measures ALS continuously
1	1	0	Measures IR continuous
1	1	1	Reserved (DO NOT USE)

Command-II Register (Address: 0x01)

TABLE 7. COMMAND-II REGISTER BITS

NAME	ADDR (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
COMMANDII	0x01	RESERVED				RES1	RES0	RANGE1	RANGE0	0x00

The Command-II register consists of ADC control bits. In this register, there are two range bits and two ADAC resolution bits. The default register value is 0x00 at power-on.

FULL SCALE LUX RANGE (B0 - B1)

The full scale Lux range has four different selectable ranges. The range determines the full scale Lux range (1k, 4k, 16k, and 64k). Each range has a maximum allowable Lux value. Lower range values offer better resolution. Table 8 lists the possible values of Lux.

TABLE 8. RANGE REGISTER BITS

RANGE SELECTION	B1	B0	FULL SCALE LUX RANGE (LUX)
0	0	0	1,000
1	0	1	4,000
2	1	0	16,000
3	1	1	64,000

ADC RESOLUTION (B3 - B2)

B2 and B3 determine the ADC's resolution and the number of clock cycles per conversion. Changing the number of clock cycles does more than just change the resolution of the device; it also changes the integration time, which is the period the device's analog-to-digital (A/D) converter samples the photodiode current signal for a measurement. Table 9 lists the possible ADC resolution.

TABLE 9. ADC RESOLUTION DATA WIDTH

B3	B2	NUMBER OF CLOCK CYCLES	n-BIT ADC
0	0	2^{16} = 65,536	16
0	1	2^{12} = 4,096	12
1	0	2^{8} = 256	8
1	1	2^{4} = 16	4

Integration Time

TABLE 10. INTEGRATION TIME OF n-BIT ADC

n # ADC BITS	INTEGRATION TIME (ms)
4	0.0256
8	0.41
12	6.5
16	105

Data Registers (Addresses: 0x02 and 0x03)

TABLE 11. ADC REGISTER BITS

NAME	ADDR (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
$DATA_{LSB}$	0x02	D7	D6	D5	D4	D3	D2	D1	D0	0x00
$DATA_{MSB}$	0x03	D15	D14	D13	D12	D11	D10	D9	D8	0x00

The ISL29035 has two 8-bit read-only registers to hold the upper and lower byte of the ADC value. The upper byte is accessed at address 0x03 and the lower byte is accessed at address 0x02. For 16-bit resolution, the data is from D0 to D15; for 12-bit resolution, the data is from D0 to D11; for 8-bit resolution, the data is from D0 to D7 and for 4-bit resolution, the data is from D0 to D3. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power-on.

TABLE 12. ADC DATA REGISTERS

ADDRESS (HEX)	CONTENTS
0x02	D0 is LSB for 4-, 8-, 12- or 16-bit resolution; D3 is MSB for 4-bit resolution; D7 is MSB for 8-bit resolution
0x03	D15 is MSB for 16-bit resolution; D11 is MSB for 12-bit resolution

Lower Interrupt Threshold Registers (Address: 0x04 and 0x05)

TABLE 13. INTERRUPT REGISTER BITS

NAME	ADDR (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
INT_LT_LSB	0x04	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00
INT_LT_MSB	0x05	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8	0x00

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the ALS value crosses below or is equal to the lower threshold, an interrupt is asserted

on the interrupt pin and the interrupt status. Registers INT_LT_LSB (0x04) and INT_LT_MSB (0x05) provide the low and high bytes, respectively, of the lower interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 0x00 upon power-up.

Upper Interrupt Threshold Registers (Address: 0x06 and 0x07)

TABLE 14. INTERRUPT REGISTER BITS

NAME	ADDR (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
INT_HT_LSB	0x06	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF
INT_HT_MSB	0x07	TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8	0xFF

The upper interrupt threshold registers are used to set the upper trigger point for interrupt generation. If the ALS value crosses above or is equal to the upper threshold, an interrupt is asserted on the interrupt pin and the interrupt status. Registers INT_HT_LSB (0x06) and INT_HT_MSB (0x07) provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 0xFF on power-up.

ID Register (Address: 0x0F)

TABLE 15. ID REGISTER BITS

NAME	ADDR (Hex)	REGISTER BITS								DFLT
		B7	B6	B5	B4	B3	B2	B1	B0	
ID	0x0F	BOUT	RESERVED	1	0	1	RESERVED			1x101xxx

The ID register has three different type of information.

RESERVED BITS (B0 - B2 AND B6)

All RESERVED bits on the ISL29035 are Intersil used bits only. Bit0 - Bit2 and Bit6 are RESERVED bits where their value might change without any notification to the user. It is advised when using the identification bits to identify the device in a system the software should mask the Bit0 - Bit2 and Bit6 – Bit7 to properly identify the device.

DEVICE ID BITS (B3 – B5)

The ISL29035 provides 3-bits to identify the device in a system. These bits are located on register address 0x0F, Bit3 – Bit5. The identification bit value for the ISL29035 is xx101xxx. The device identification bits are read only bits. It is important to notice that Bit7 is a status bit for brownout condition (BOUT).

BROWNOUT STATUS BIT - BOUT (B7)

Bit7 on register address 0x0F is a status bit for brownout condition (BOUT). The default value of this bit is “BOUT = 1” during the initial power-up, which indicates the device may possibly have gone through a brownout condition. Therefore, the status bit should be reset to “BOUT = 0” by an I^2C write command during the initial configuration of the device.

The default register value is 0xA8 at power-on.

Applications Information

The plot below is a normalized spectral response of various types of light sources for reference.

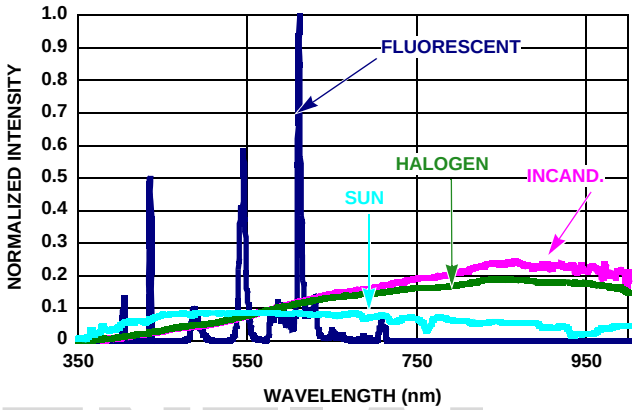


FIGURE 14. NORMALIZED SPECTRAL RESPONSE OF LIGHT SOURCES

Calculating Lux

The ISL29035’s ADC output codes, DATA, are directly proportional to Lux in the ambient light sensing.

$$E_{cal} = \alpha \times DATA \quad \text{(EQ. 1)}$$

Here, E_{cal} is the calculated Lux reading. The constant α is determined by the Full Scale Range and the ADC’s maximum output counts. The constant is independent of the light sources (fluorescent, incandescent and sunlight) because the light sources’ IR component is removed during the light signal process. The constant can also be viewed as the sensitivity (the smallest Lux measurement the device can measure).

$$\alpha = \frac{Range}{Count_{max}} \quad \text{(EQ. 2)}$$

Here, Range is defined in Table 8 on page 11. $Count_{max}$ is the maximum output counts from the ADC.

The transfer function used for n-bits ADC becomes:

$$E_{cal} = \frac{Range}{2^n} \times DATA \quad \text{(EQ. 3)}$$

Here, n = 4, 8, 12 or 16. This is the number of ADC bits programmed in the command register. 2^n represents the maximum number of counts possible from the ADC output. Data is the ADC output stored in the data registers (02 hex and 03 hex).

Enhancing EV Accuracy

The device has on chip passive optical filter designed to block (reject) most of the incident Infra Red. However, EV measurement may be vary under differing IR-content light sources. In order to optimize the measurement variation between differing IR-content light sources, ISL29035 provides IR channel which is programmed at COMMAND-1 (Reg0x0) to measure IR level of differing IR-content light sources.

The ISL29035's ADC output codes, DATA, are directly proportional to the IR intensity received in the IR sensing.

$$DATA_{IR} = \beta \times E_{IR} \quad \text{(EQ. 4)}$$

Then EV accuracy can be found in Equation 5:

$$EV_{Accuracy} = KxDATA_{EV} + \beta \times DATA_{IR} \quad \text{(EQ. 5)}$$

Here, $DATA_{EV}$ is the received ambient light intensity ADC output codes. K is a resolution of visible portion. Its unit is Lux/count. The typical values of K is 0.82. $DATA_{IR}$ is the received IR intensity. The constant β changes with the spectrum of background IR, such as A, F2 and D65 (Notes 8, 9 and 10). The β also changes with the ADC's range and resolution selections. A typical β for range1 and range2 is -11292.86 and range3 and range4 is 2137.14 without IR tinted glass.

Noise Rejection

Electrical AC power worldwide is distributed at either 50Hz or 60Hz. Artificial light sources vary in intensity at the AC power frequencies. The undesired interference frequencies are infused on the electrical signals. This variation is one of the main sources of noise for the light sensors. Integrating type ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. By setting the sensor's integration time to an integer multiple of periodic noise signal, the performance of an ambient light sensor can be improved greatly in the presence of noise. In order to reject the AC noise, the integration time of the sensor must to adjusted to match the AC noise cycle. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms ($k = 1,2...k_i$) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise.

Suggested PCB Footprint

It is important that users check the "Surface Mount Assembly Guidelines for Optical Dual Flat Pack No Lead (ODFN) Package" before starting ODFN product board mounting: TB477

Board Mounting Considerations

For applications requiring the light measurement, the board mounting location should be reviewed. The device uses an Optical Dual Flat Pack No Lead (ODFN) package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location.

Layout Considerations

The ISL29035 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 1µF and 0.1µF, placed close to the device.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, (V_{HIGH} - V_{LOW}), and divide by the temperature extremes of measurement (T_{HIGH} - T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 106 to yield ppm/°C. This is the "Box" method for specifying temperature coefficient.

Digital Inputs and Termination

The ISL29035 digital inputs are guaranteed to CMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are 50Ω lines, then 50Ω termination resistors should be placed as close to the sensor inputs as possible, connected to the digital ground plane (if separate grounds are used).

Typical Circuit

A typical application for the ISL29035 is shown in Figure 15. The ISL29035's I^2C address is internally hard-wired as 1000100. The device can be tied onto a system's I^2C bus, together with other I^2C compliant devices.

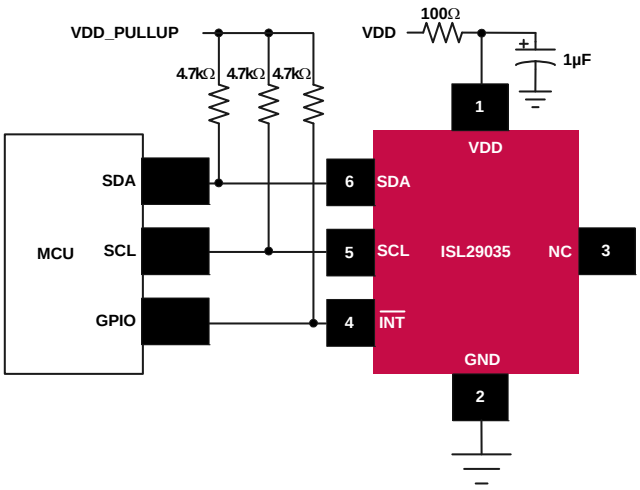


FIGURE 15. ISL29035 TYPICAL CIRCUIT

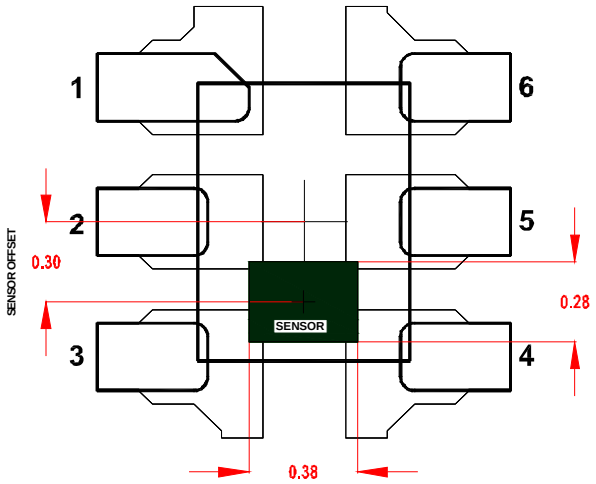


FIGURE 16. 6 LD ODFN SENSOR LOCATION OUTLINE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 18, 2013	FN8371.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

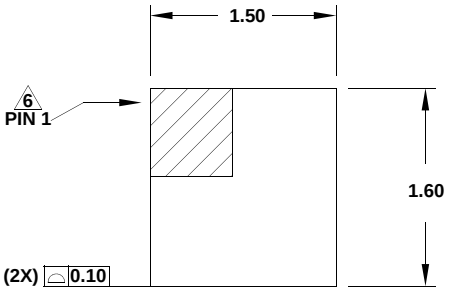
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

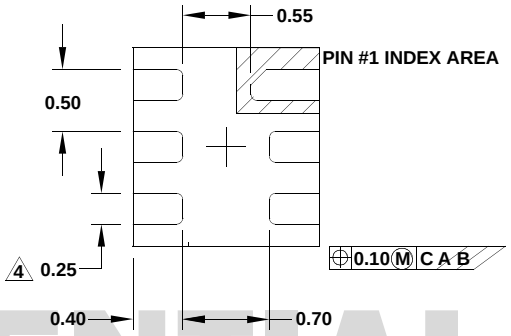
L6.1.5x1.6

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

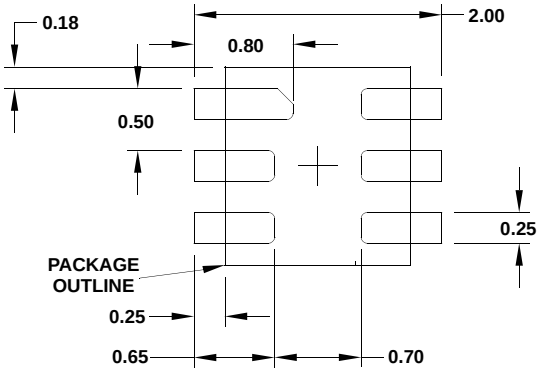
Rev 0, 5/12



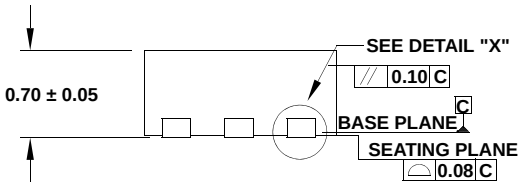
TOP VIEW



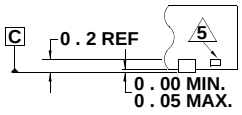
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.