Time of Flight (ToF) Signal Processing IC

ISL29501

The ISL29501 is a Time of Flight (ToF) based signal processing integrated circuit. The sensor enables low cost, low power, long range optical distance sensing when combined with an external emitter and detector.

The ISL29501 has a built-in current DAC circuit that drives an external LED or laser. The modulated light from the emitter is reflected off the target and is received by the photodiode. The photodiode then converts the returned signal into current, which is used by the ISL29501 for signal processing.

An on-chip Digital Signal Processor (DSP) calculates the Time of Flight, which is proportional to the target distance. The ISL29501 is equipped with an I^2C interface for configuration and control.

Use of an external photodiode and emitter allows the user to optimize the system design for performance, power consumption and distance measurement range that suit their industrial design.

The ISL29501 is wavelength agnostic and permits the use of other optical wavelengths if better suited for applications.

Features

- Enables proximity detection and distance measurement
- Modulation frequency of 4.5MHz
- Emitter DAC with programmable current up to 255mA
- Operates in continuous and single shot mode
- On-chip active ambient light rejection
- Auto gain control mechanism
- Interrupt controller
- Supply voltage range of 2.7V to 3.3V
- I^2C interface supporting 1.8V and 3.3V bus
- Low profile 24 Ld 4x5 TQFN package

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Applications

- Mobile consumer applications
- Industrial proximity sensing
- Power management
- Home automation
- Automotive applications

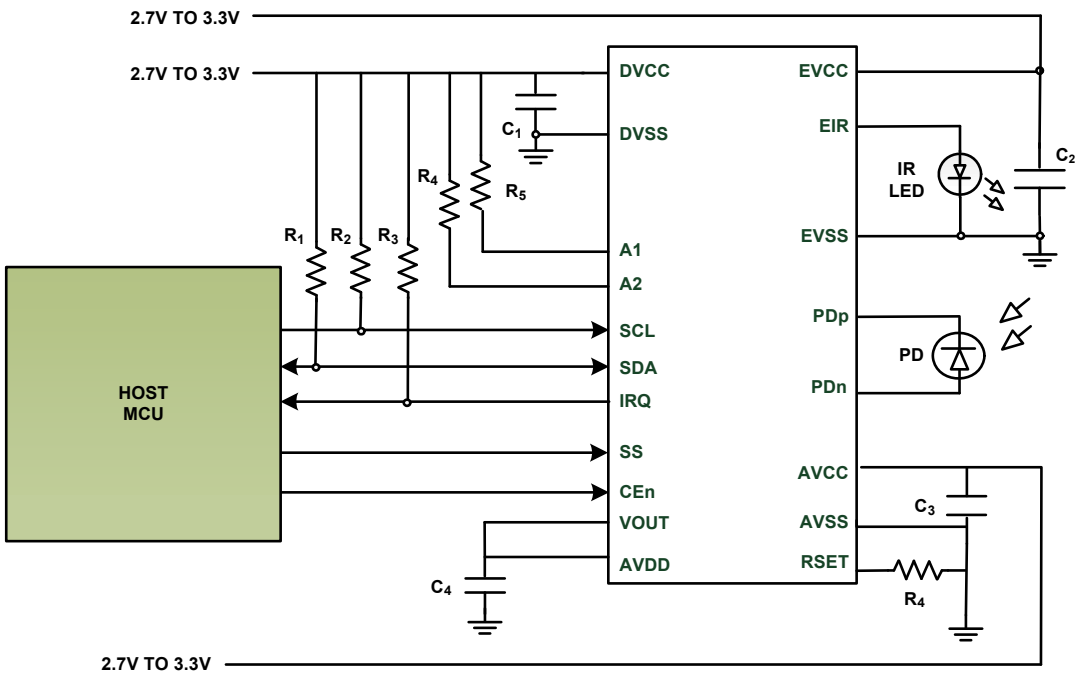

FIGURE 1. APPLICATION DIAGRAM

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram

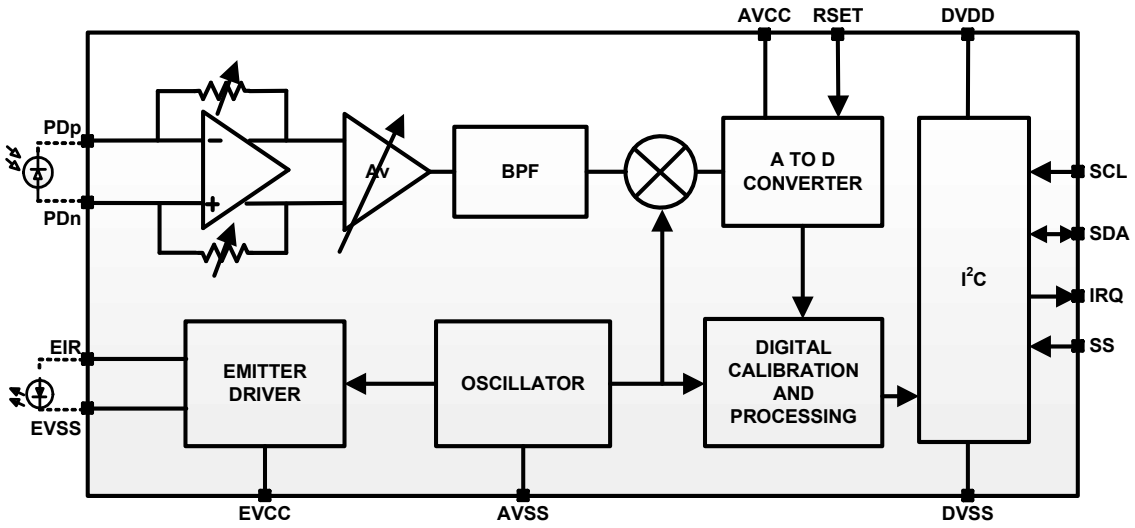

FIGURE 2. BLOCK DIAGRAM

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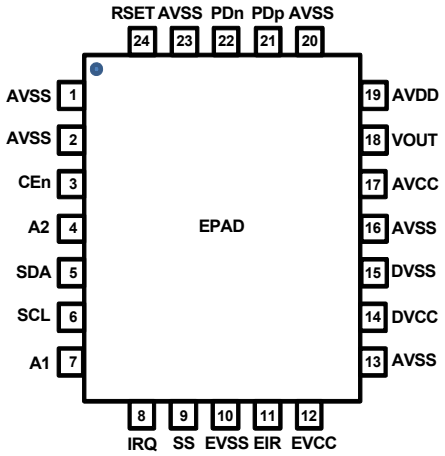
Pin Configuration

ISL29501
(24 LD TQFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1, 2, 13	AVSS	Tie to AVSS.
3	CEn	Chip Enable. Active Low.
4	A2	I^2C address bit, tie to DVCC or DVSS
5	SDA	I^2C data bus
6	SCL	I^2C clock bus
7	A1	I^2C ID address bit, tie to DVCC or DVSS
8	IRQ	Interrupt. Active low open-drain output signal to host. A 2.7kΩ pull-up to supply is required.
9	SS	Sample Start: input signal with hi to low edge active.
10	EVSS	Emitter Driver Ground. Connects to cathode of emitter.
11	EIR	Emitter Driver Output. Connects to anode of emitter.
12	EVCC	Emitter Driver Supply. Decouple with 2.2µF or larger capacitor along with a 0.1µF for high frequency.
14	DVCC	Digital power 2.7V to 3.3V supply.
15	DVSS	Digital power ground
16	AVSS	Analog power ground
17	AVCC	Analog power 2.7 to 3.3V supply.
18	VOUT	AFE LDO Output, tied to AVDD, decouple with 1µF and 0.01µF capacitor pair.
19	AVDD	AFE analog supply
20, 23	AVSS	Analog ground shield
21	PDp	Photodiode cathode input
22	PDn	Photodiode anode input
24	RSET	Sets chip bias current. Tie to 10kΩ resistor 1% to AVSS ground.
	EPAD	Center EPAD: Tied to AVSS

Ordering Information

PART NUMBER (Notes 1, 2, 3,)	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL29501IRZ-T7	29501 IRZ	2.7V to 3.3V	-40 to +85	24 Ld QFN	L24.4x5F
ISL29501-ST-EV1Z	Evaluation Board				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL29501. For more information on MSL please see techbrief TB477.

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Absolute Maximum Ratings

Supply Voltage Range . . . . . -0.2V to 4V
Voltage on All Other Pins . . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E)(Note 6) 2000V
Machine Model (Tested per JESD22-A115-A) 200V
Latch-up (Tested per JESD-78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	35	1.2

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature . . . . . -40°C to +85°C
Supply Voltage . . . . . 2.7V to 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. ESD HBM passed 2kV with exception to pins IRQ and SDA which passed 1kV.

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Electrical Specifications

Unless otherwise indicated, all the following tables are at DVCC, AVCC and EVCC at 3.0V, T_A = +25°C, **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SENSOR PARAMETERS						
f_{mod}	Modulation Frequency	Modulation frequency of emitter	**4.45**	4.5	**4.65**	MHz
DVCC, AVCC, EVCC	Chip Power Supply		**2.7**	3.0	**3.3**	V
tcen_fs	Delay From Chip Enable to First Sample	Note 7		500		µs
tsleep_fs	Delay between Sleep Mode to Start of First Sample	Note 7			**3**	µs
I_{S-HS}	Quiescent Current - Sleep Mode, DVCC+AVCC+EVCC	CEn = 1; I^2C disable; register values are retained; SS = SDA = SCL = V_{CC}			**1.5**	µA
I_{S-SD}	Quiescent Current - Shutdown, DVCC+AVCC+EVCC	CEn = 0; I^2C enable; register values are retained; all other functions are disabled			**1**	µA
IDDact	Chip Current While Measuring, DVCC+AVCC+EVCC	Emitter dutycycle = 50%, 0x90 = 06h, 0x91 = 00h		55		mA
AFE SPECIFICATIONS						
Imax_PD	Max AFE Input Current PDp/PDn	Design recommendation		12.8		µA
VPDp	Voltage at PDp		**1.72**	1.7	**1.73**	V
VPDn	Voltage at PDn		**0.74**	0.75	**0.75**	V
LNA	Low Noise Amplifier	0x97[2], 0 is default, 1 provides 3x gain		3x		N/A
TIA Gain	Differential I to V Conversion Range	0x97[0:1], b0 = 0 and b1 = 0 default		8		kΩ
		0x97[0:1], b0 = 0 and b1 = 1		16		kΩ
		0x97[0:1], b0 = 1 and b1 = 1		32		kΩ
Cmax	Max Photodiode Capacitance Recommended	Design recommendation			**15**	pF

I^2C Electrical Specifications

For SCL, SDA, A1, A2, IRQ Unless otherwise stated, V_{DD} = 3.0V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNITS
V_{I2C}	Supply Voltage Range for I^2C Specification		**1.8**		**3.3**	V
I_{IL}	Input Leakage	V_{IN} = GND to V_{CC}			**1**	µA

I²C Electrical Specifications

For SCL, SDA, A1, A2, IRQ Unless otherwise stated, V_{DD} = 3.0V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNITS
V_{IL}	Input LOW Voltage		**-0.3**		**0.3 x V_{CC}**	V
V_{IH}	Input HIGH Voltage		**0.7 x V_{CC}**		**V_{CC} + 0.3**	V
Vhys	SDA and SCL Input Buffer Hysteresis		**0.05 x V_{CC}**			V
V_{OL}	SDA Output Buffer LOW Voltage	I_{OL} = 3mA	**0**		**0.4**	V
C_{pin}	Pin Capacitance (Note 10)			10		pF
f_{SCL}	SCL Frequency				**400**	kHz
t_{sp}	Pulse Width Suppression Time At SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			**50**	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			**900**	ns
t_{BUF}	Time the Bus Must Be Free Before the Start of A New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	**1300**			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	**1300**			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	**600**			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	**600**			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	**600**			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	**100**			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	**0**			ns
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	**600**			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	**1300**			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	**0**			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	**20 + 0.1 x cb**		**250**	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	**20 + 0.1 x cb**		**250**	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	**10**		**400**	pF
Rpu	SDA and SCL Bus Pull-up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ For Cb = 40pF, max is about 15kΩ ~ 20kΩ	**1**			kΩ
I_{LO}	Output Leakage Current (SDA only)	V_{OUT} = GND to V_{CC}			**1**	µA
V_{IL}	A1, A2, SDA and SCL Input Buffer LOW Voltage		**-0.3**		**V_{CC} x 0.3**	V
V_{IH}	A1, A2, SDA and SCL Input Buffer HIGH Voltage		**V_{CC} x 0.7**		**V_{CC}**	V
V_{OL}	SDA Output Buffer LOW Voltage		**0**		**0.4**	V
C_L	Capacitive Loading of SDA or SCL		**10**		**400**	pF

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NOTES:

7. Product characterization data.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Typical values are for T_A = +25°C and V_{CC} = 3.3V.
10. Cb = total capacitance of one bus line in pF.

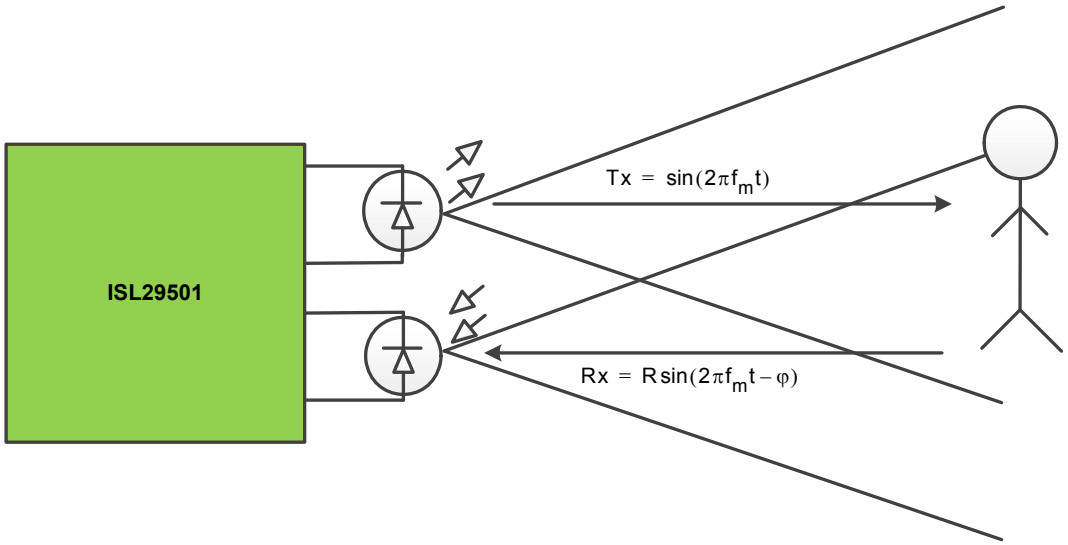

FIGURE 3. TRANSMITTED AND RECEIVED SIGNAL IN A SYSTEM

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Principles of Operation

The ISL29501 operates using the principle of Square Wave Modulated Indirect Time of Flight (SWM-ITOF) method. The sensor operates in frequency domain and takes advantage of the analog mixed signal techniques to obtain distance measurement from phase shift.

The sensor coupled with emitter and detector will function as a distance and ranging sensor.

The emitter driver transmits a modulated square wave (Tx) at a given frequency fm in the FOV using the emitter, the received signal (Rx) is accompanied with phase shift and attenuation dependent on object distance and reflectivity, an illustration is shown in Figure 3.

The phase difference between emitted and received signals of the modulated square wave is determined in frequency domain and converted to distance reading.

The distance is computed using the internal DSP and provided to the host using an I^2C interface. Advanced interrupt control mechanism allows for generating user defined triggers from the sensor.

The phase shift of the return signal is dependent only on the distance of the object from the system and is relatively independent to the object reflectivity.

The distance of the object can be calculated by determining the phase shift of the returns signal using Equation 1.

$$D = \frac{C}{4\pi f_{mod}}\Delta\varphi \quad \text{(EQ. 1)}$$

Where:

D is the distance of the object from the sensor system

f_{mod} is the modulation frequency

$\Delta\varphi$ is the phase difference between emitted and returns signal

C is the speed of light

Key constants can be derived from this expression for f_{mod} = 4.5MHz, these values can be useful in developing a general understanding of the system.

- 5.3m/radian
- 33.3m for cycle (2pi radians)
- 15cm/ns

The range of the system can be optimized by selection of components (emitter, detector) and optics.

The sensor takes advantage of analog quadrature signal processing techniques to obtain the phase difference information, some of the processing steps in the signal chain are listed in the following.

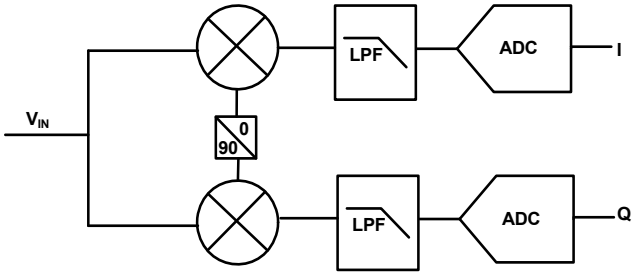

FIGURE 4. I AND Q PROCESSING OF THE SIGNAL

The AFE converts the photocurrent into voltage and the demodulator translates the return signal into I (in phase) and Q (quadrature) components.

I and Q values are filtered and digitized by the ADC, the DSP calculates the distance based on the amplitude, phase and frequency values.

AFE gain in conjunction with max gain from the AGC loop allows for judicious selection of the detector for system design.

ADC relies on the automatic gain control loop to evaluate the optimal gain for the data conversion.

Functional Overview

The ISL29501 is configured using an I^2C interface. An initial power-up sequence ensures stable operation and control.

Power Supply Pins

The ISL29501 operates on a voltage range from 2.7V to 3.3V. It has three power rails, AVCC, DVCC and EVCC. The AVCC and DVCC supply current to the digital and analog part of circuits while the EVCC is dedicated to the emitter driver section.

Intersil recommends decoupling the analog and digital supplies to minimize supply noise and LC filter for systems, which might have high frequency interference.

Capacitors, which have resonance frequencies similar to modulation frequency can be very effective in mitigating supply noise.

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Power-on Reset

When power is first applied to the DVCC pin, the ISL29501 self generates a reset. The reset forces all registers to be loaded with the hardware default values.

Brownout Detection

A brownout detection circuit is designed in the ISL29501. The circuit provides the user a means to ensure the fidelity of the digital logic.

The brownout detection circuit monitors the supply voltage. If the supply drops below the preset threshold for a fixed period, this circuit will set a flag bit 0x69[5] followed by pulling the interrupt signal to notify the host.

Each time ISL29501 is powered on, the BROWN_Out flag bit is set. The host must clear this bit as a part of device initialization procedure before ISL29501 will function normally.

Chip Enable (CEn) Pin

The CEn pin is an active low input pin. When asserted (pull low), the device will bias the internal circuit blocks, band gaps, references and I^2C interface. Configuring 0x01[0] to 0 will enable ISL29501.

When CEn pin is deasserted, the ISL29501 will be disabled with exception of the I^2C interface and registers. Host can access registers via the I^2C interface.

After ISL29501 has been initialized, deasserting CEn (high) will retain the programmed register values.

Sample Start (SS) Pin

Sample Start (SS) pin is an input logic signal, which triggers the free running mode. The purpose is to start the ISL29501 sensing function by the external Host.

If there is an additional request during the process of active data capture the request is ignored.

Command Register

Command register enables configuration of sensor and access to sensor register read and write.

A soft-start can be initiated by writing 0xB0 to 0x49, this register bit emulates the single shot pin.

A soft-reset can be initiated by writing 0xB0 to 0xD7, this action resets all registers to power-on default values with the exception of brownout bit.

A soft-clear can be initiated by writing to 0xB0 to 0xD1, this stops all conversions and resets the accumulators, the sensor will stop if it is in continuous mode.

Interrupt (IRQ) Pin

The ISL29501 can be configured to generate interrupts at the completion of a sensing cycle, providing a queue for the host to get the data for post processing.

The chip can also be configured to generate interrupts when specific conditions are met, see the section "Interrupt Controller" on page 14 for more details. The IRQ pin is an active low output logic pin. It is an open-drain output pin and requires a pull-up resistor to bias it to DVCC.

Sampling modes and various detection methods report its data in the device registers. Each mode and detection method has a corresponding flag bit. The host should service the IRQ request by reading the 0x60 register.

TABLE 1. INTERRUPT CONTROL 0x60

BIT	BIT NAME	DESCRIPTION
0	Data Ready	Goes high after computation is complete
1	Condition_1_Flag	Detection condition 1
2	Condition_2_Flag	Detection condition 2
3	Persistance_Flag	Defined by the persistence counter
4	Change_Flag	
5	Brown_Out_Flag	N/A

On reading of the interrupt control register, the service bit is clear. If the sensor is set to signal sample mode, then the sensing stops and awaits for the next sample start signal. If the ISL29501 is set to continuous mode, then the IC will begin the next sensing sample according to the preconfigured sampling time period.

Sampling Modes

The ISL29501 provides two operating sample modes, single shot mode and continuous mode.

TABLE 2. Reg0x13 SAMPLING MODES

REG	BIT PREFERENCE	MODE OF OPERATION
0x13[0]	0	Continuous sampling
0x13[0]	1	Single shot sampling

Single Shot

In single shot mode, the user will define the sampling period based on the system requirements. The duration of sampling is controlled by MCU with preprogrammed values.

Single shot mode provides the lowest power mode the sensor can operate in as the MCU defines the downtime of the sensor. This minimizes power consumption of the sensor due to reduction in operating duty cycle.

This mode can be configured using I^2C or pin triggered using the SS pin.

The outputs from the sensor are discussed in "Data Outputs" on page 13 and the system designer has the option of choosing either calibrated or uncalibrated data with register control.

Continuous Mode

Continuous mode of operation is used for systems where the sensor is continuously gathering data at a predefined integration and sampling period using the internal timing controller.

The data is available to the host after every sample period and the sensor will keep operating in this mode unless interrupted by MCU.

This mode can be defined by register control using I^2C or pin triggered. The system designer has the option of choosing either calibrated or uncalibrated data with register control.

Each sampling mode can be used with any of the applicable mode enhancement features such as zoning, presence and distance.

Emitter Driver

Integrated in the ISL29501 is an emitter source driver. The driver is designed to drive either the IR LED or laser. The driver circuit is enhanced to provide fast turn-on and turn-off of either LED or lasers. In addition, integrated in the driver circuit are features that can aid and assist the use of these emitters.

EIR Pin

Figure 5 shows a simplified block diagram of the emitter driver. The circuit consists of two primary current DACs, main and threshold DAC.

The emitter can be connected to the ISL29501 via the EIR pin with the anode side while the cathode is tied to ground (EVSS).

Bias current is derived from a combination of a coarse and fine DAC allowing a fine control of bias current.

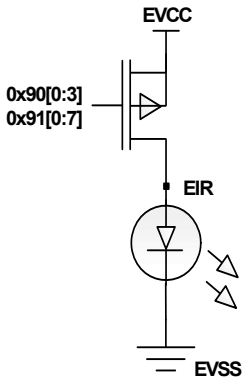

FIGURE 5. EMITTER CONNECTIVITY

Main DAC

The Main DAC is the primary current source to drive an LED or laser. It is designed to output a maximum current of 255mA.

The current setting can be set by programming registers 0x90 and 0x91. Register 0x90 allows coarse control and register 0x91 for fine control of the current.

Depending on the application's desired range and the type of emitter employed, the current level can be set to give the best SNR performance. The system designer will have to determine this value based on component selection.

The IRDR value is determined a combination of the DACs 0x90 and 0x91, this allows for finer control.

IRDR = 0x90[3:0]/15*0x91[7:0]/255*255mA

Threshold DAC

The threshold DAC is designed to support laser emitters by prebiasing before lasing is initiated, this improves the optical output by reducing the time it takes for lasing to occur.

A maximum of 30mA can be driven by the threshold DAC. The current level can be programmed via register 0x93. The detailed description can be found in the "Register Map" on page 19.

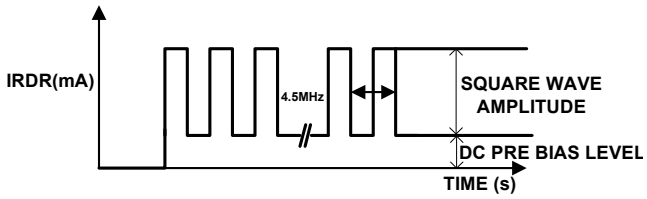

FIGURE 6. TYPICAL EMITTER WAVEFORM AND FEATURES

Note: Due to fast and potentially strong switching currents surging through the emitter circuit, we recommend the emitter cathode be tied to a ground plane that is nearest to the EVSS pin to keep the return noise to a minimum.

We recommend EVSS ground plane to be separated from AVSS and DVSS to minimize coupling.

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Connecting the Photodiode

The photodiode should be connected between the PDn and PDp pins as shown in Figure 7. The photodiode operates in photoconductive mode, the voltages at PDp and PDn nodes are listed in the AFE specifications.

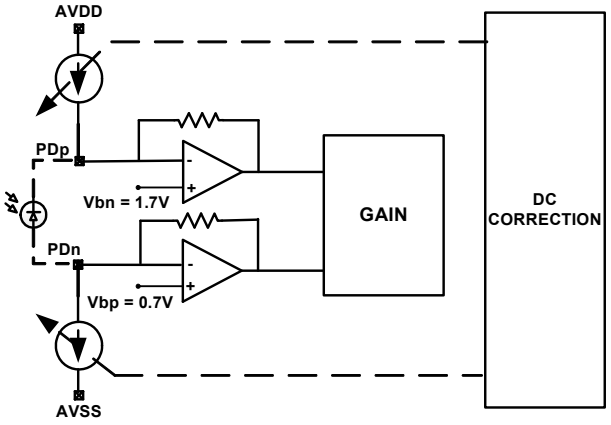

FIGURE 7. CONNECTING PD TO AFE

The photodiode anode is biased at 0.7V and the cathode is biased at 1.7V (1V reverse bias). Biasing the diode in photoconductive mode enables lower effective capacitance/faster operation and efficient collection of photo electrons.

Selecting the Photodiode

This section provides general guidelines for the selection of the photodiode for receiver.

Three key parameters that must be considered:

1. Peak wavelength
2. Capacitance (i.e., area)
3. Rise/fall time

A detector with narrow band sensitivity in the NIR or MWIR would be ideal for proximity sensing as most ambient light will be naturally rejected.

We have to ensure that the emitter peak wavelength is aligned with the detector wavelength to achieve high SNR.

A detector with larger surface area is ideal for collecting the photons, integrated optics such as lensing allows for control of the FOV and collection of optical signal.

Large area diodes are accompanied with larger intrinsic capacitances leading to slow rise and fall times, there is a trade off between detector area and capacitance that need to be considered for system performance.

Ex: AFE specifications such as maximum signal current value and maximum capacitance serve as general guidelines to optimize system performance.

The fully differential front end converts the photocurrent into voltage and allows for common mode noise/crosstalk to be rejected. The programmable gain of the TIA allows for a wider range of operation and improved SNR performance.

The TIA gain can be controlled by 0x97[1:0] in steps of 8kΩ, 16kΩ and 32kΩ. A more detailed description of registers can be found in the "Register Map" on page 19.

An effective capacitance of less than 15pF is recommended for robust performance, for applications where distance measurement is required. Using larger capacitance will cause increase in noise and not functional failure. The decision to use small or large photo diode (i.e., capacitance) has to be made by the system engineer based on the application.

Photodidoes with lenses allows for narrow field of view, which allows sensing longer distances.

The PCB layout should ensure that the trace lengths for anode and cathode are symmetric for PDp and PDn pins in order to avoid injecting non-common mode signals for better performance.

Emitter Selection

The ISL29501 supports the use of light sources such as LEDs, VCSELS and Lasers. The sensor will drive any emitter within the maximum current range supported by the emitter DAC.

We need to allow a 1V head room for the current source for linear operation of the current source.

The sensor working principle is wavelength agnostic and determination of wavelength can be made based on application.

The emitter wavelength should be an NIR or MWIR (i.e., 800nm to 1300nm) in order to minimize the influence of ambient light on the precision.

The selection between LED or laser depends on the target application. Some general system considerations are distance, field of view and precision requirements. While an LED is a reliable light source, it might not be the best suited for long distance due to its dispersion characteristics. However, it is good for short range and large area coverage. For higher precision and longer distances, laser/VCSEL's are ideal. Inverse square law and input referred circuit noise can be used to determine the radiant intensity requirements.

Ambient Light Rejection

Ambient light rejection at the front end allows for distance measurements with minimal interference from ambient light sources.

The feedback loop works by supplying the additional ambient photo current without impacting the signal path. The subsequent stages of the analog signal chain are AC coupled and are not susceptible to DC shifts at AFE.

Ambient performance of a system is dominated by the photodiode behavior (i.e., ambient introduced phase shift).

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In order to ensure minimal dependence of ambient on the system distance measurements, the sensor enables correction algorithms (linear and second order polynomial to correct for any diode related behaviors).

Ambient current value can be found by reading the register 0xe3[7:0] with 3.5µA/LSB.

Power Consumption

In a "Time of Flight" application power consumption has two components, the power consumed within the ISL29501 device and the power consumed by the emitter LED or VSCEL. While the emitter current is load current and not part of the ISL29501 power dissipation, it is included in this discussion to help the user understand the entire "Time of Flight" contribution to the total application power budget.

$$IDD_{ToF} = IDD_{IC} + IDD_{Load} \quad \text{(EQ. 2)}$$

IC POWER CONSUMPTION

The power consumed in the ISL29501 has two components. The first is the standby current, which is present whenever the chip is not integrating (making a measurement). The second is the current consumed during a measurement. Chip current is calculated by multiplying the overall duty cycle by 102mA and adding the standby current (~2mA). The overall duty cycle is defined as (integration time /sampling period/2) in continuous mode or the (integration time /user measurement repetition rate/2) in single sample mode.

$$IDD_{IC} = 102mA \bullet DC_{Overall} + I_{Standby} \quad \text{(EQ. 3)}$$

Typical values for $I_{Standby}$ can be found in the "Power Consumption" parametric table.

TOTAL TIME OF FLIGHT POWER CONSUMPTION

To calculate the total "Time of Flight" module current the load current contribution must be added to the chip current. As with the chip current the measurement duty cycle has a large effect on the load current. The load current is defined as the product of the emitter current and the overall measurement duty cycle.

$$I_{Load} = DC_{Overall} \bullet I_{Emitter} \quad \text{(EQ. 4)}$$

The emitter current is calculated using Equation 5:

$$I_{Emitter} = (reg0x90/15) \bullet (reg0x91/255) \bullet 255mA \quad \text{(EQ. 5)}$$

The duty cycle for this calculation is the same as described in the IC power consumption section. In the application, the best emitter current setting is a balance of the required optical power and the acceptable power consumption. Similarly, the duty cycle is a balance between the precision of a measurement and power consumption. It should be noted that choosing high duty cycles can cause heating of the emitter introducing drift in distance measurements.

For additional details refer to "Emitter Selection" on page 10 and "Integration Time" on page 11 sections.

Shutdown

Shutdown disables all the individual components that actively consume power, with the exception of the I^2C interface. There are multiple options for the system designer based on the time to bring up the system.

The CEn (Chip enable), in conjunction with shutdown, can be used to keep the system passive based on power consumption and speed of response.

Sampling Time

The sampling waveform in Figure 8 dictates the sensor operation. The key elements to understand are integration time and sampling interval.

Integration time dictates the driver waveform active period and sampling frequency provides the data output rate of the sensor. Optimal values for integration time and sampling interval (duty cycle) determine the power consumption and performance of the system (precision). A typical emitter driver waveform is shown in Figure 9 to indicate the controls that are available to the user.

Sampling interval determines the sensor response time or rate of output from the sensor, this is user defined with Equation 6:

$$\text{Sampling frequency} = \frac{1}{450\mu s \bullet (1 + sample\_period[7:0] \bullet 2^{sample\_skip[3:0]})} \quad \text{(EQ. 6)}$$

The value for sampling frequency ranges from 1ms to 1843ms. For a more detailed description of the register please refer to the "Register Map" on page 19.

The ratio of integration time to sampling frequency is the sensor duty cycle. Duty cycle determines the power consumption of the sensor.

When building an optical system, a determination of an effective duty cycle will help optimize power and performance trade-offs in the system.

Integration Time

Integration time sets the emitter DAC active time. The value is user controlled by the register interface.

The total integration time can be determined from Equation 7 from a given sample period.

$$\text{integration time} = [\text{sample period-settling time } (375\mu s) + \text{calibration time}] \quad \text{(EQ. 7)}$$

If the sample integration time is set to be greater than the sample period, then the integration time will default to maximum allowable within the sample period.

Integration time impacts precision and power consumption of the chip and can be used as a measure to optimize the system performance.

$$\text{Default integration time} = 71.1\mu s \bullet 2^{sample\_len[3:0]}$$
$$\text{Maximum integration time} = 71.1\mu s \bullet 2^{11} \text{ (which is 145.6ms)} \quad \text{(EQ. 8)}$$

For more detailed description of register please refer to the "Register Map" on page 19.

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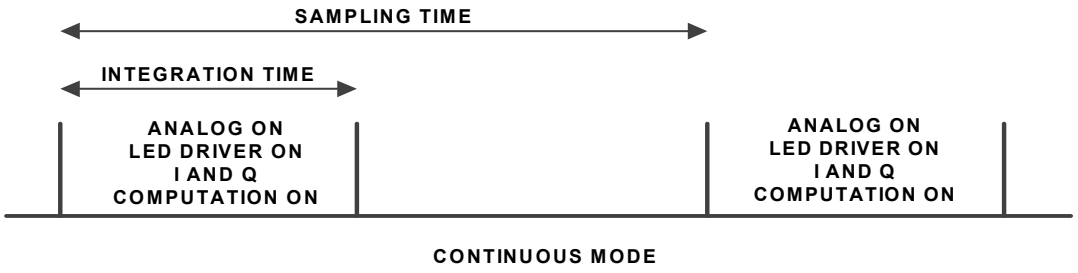

FIGURE 8. WAVEFORM FOR FUNCTIONAL OPERATION

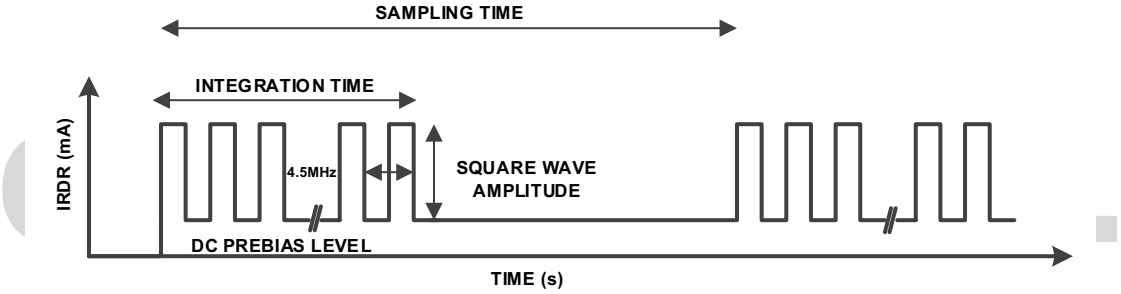

FIGURE 9. EMITTER DRIVER WAVE FORM

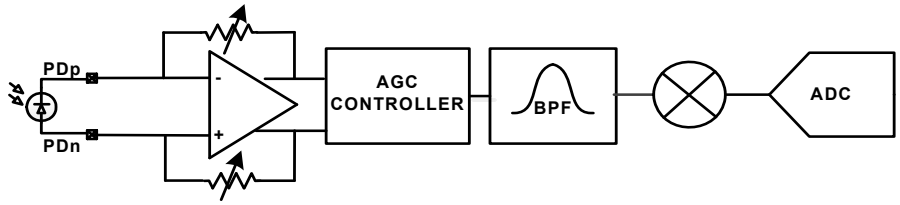

FIGURE 10. AUTOMATIC GAIN CONTROL

Automatic Gain Control

The ISL29501 has an advanced automatic gain control loop which sets the analog signal levels at an optimum level by controlling programmable gain amplifiers. The internal algorithms determine the criteria for optimal gain.

The goal of the AGC controller is to achieve the best SNR response for the given application.

Ambient ADC

Ambient ADC provides the level of ambient signal present in the environment.

The ambient ADC operation doesn't interfere with sensor operation. The ambient information can be read out using the registers 0x7f[7:0]. This register tracks the ambient photocurrent.

The ambient photocurrent values can be used to estimate the best achievable SNR/Precision performance for a given environment.

Collision Detection

This Collision detection allows to minimize interference from other emitters in the vicinity of the system with modulated emitters operating at similar frequencies.

Programming Reg0x13[7] to 1 enables collision detection for the sensor. The length of collision detection time is defined by Reg0x16[3:0].

Please refer to the "Register Map" on page 19 for detailed information regarding register values.

Data Outputs

The sensor outputs a wide variety of information that can be used by the MCU for processing. A list of parameters that can be obtained from the sensor are identified in the following.

The information can be relied upon by the digital logic to generate interrupts for quick decision making or used for other off-chip processing functions.

- Distance information
- Magnitude information
- Raw I and Q values
- Chip junction temperature
- Emitter forward voltage
- Interrupts for proximity and presence detection
- Enable motion computation based on time stamped distance values

The validity of data can be used to screen interrupts based on user requirements enabling robust use cases.

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TABLE 3. DATA OUTPUT REGISTERS AND BIT DEFINITIONS

ADDR	REGISTER NAME	ACCESS	BIT(s)	BIT NAME	FUNCTION
0xd0	Data Invalid [7:0]	RL	0	DC_Saturation Flag	DC Saturation Flag
			1	noise_flag	Noise Flag
			2	squelched_flag	Squelched Flag
			5	peak_detect 1	Peak Detect 1
			6	peak_detect 2	Peak Detect 2
			7	collision_detected	Collision Detected
0xd1	Distance Readout MSB	RL	7:0	distance[15:8]	Distance output
0xd2	Distance Readout LSB	RL	7:0	distance[7:0]	Distance output
0xd3	Precision MSB	RL	7:0	percision[15:8]	For system optimization
0xd4	Precision LSB	RL	7:0	percision[7:0]	For system optimization
0xd5	Magnitude Exponent	RL	3:0	mag_exp[3:0]	Signal Magnitude
0xd6	Magnitude Significand MSB	RL	7:0	mag[15:8]	Signal Magnitude
0xd7	Magnitude Significand LSB	RL	7:0	mag[7:0]	Phase output
0xd8	Phase Readout MSB	RL	7:0	phase[15:8]	Phase output
0xd9	Phase Readout LSB	RL	7:0	phase[7:0]	Phase output
0xda	I Raw Exponent	RL	7:0	i_raw_exp[7:0]	Inphase output
0xdb	I Raw MSB	RL	7:0	i_raw[15:8]	Inphase output
0xdc	I Raw LSB	RL	7:0	i_raw[7:0]	Inphase output
0xdd	Q Raw Exponent	RL	7:0	q_raw_exp[7:0]	Out of phase output
0xde	Q Raw MSB	RL	7:0	q_raw[15:8]	Out of phase output
0xdf	Q Raw LSB	RL	7:0	q_raw[7:0]	Out of phase output
0xe0	Emitter Voltage Before	RL	7:0	ev_before[7:0]	Emitter voltage
0xe1	Emitter Voltage After	RL	7:0	ev_after[7:0]	Emitter voltage

Interrupt Controller

The Interrupt controller is one of the key blocks of the digital core in the ISL29501. The Interrupt controller generates interrupts based on sensor data and user defined thresholds.

The critical function of interrupt controller is detection of user defined events based on distance measurements. The triggering mechanism for detection can be controlled using registers from 0x70 to 0x86 (detection mode control registers).

A detailed description of register can be found in the "Register Map" on page 19.

An interrupt can be generated by any of the sensor outputs by the DSP, a list is provided for reference:

- Interrupt based on every cycle of valid data capture
- Presence/absence detect based on distance zones
- Presence/proximity detection based on magnitude zones
- Enable motion detect and computation off-chip
- Provide inputs to system minimizing noise in detection such as persistence counter/noise thresholds etc.
- SNR based interrupt generation is accomplished using noise buffers.
- Data valid registers

Distance Zones

Distance zones can be classified into three different user defined zones and hysteresis is defined between the zones using the low and high thresholds for a given maximum sensing range of the optical system. Distance zones allow the system designer to make necessary changes to the response of the system with very little or no computation required on the host, making this a very effective tool.

Figure 11 illustrates graphically how the zones are defined and the user defined boundaries that allow for long range presence detection. The register set provides the ability to program based on distance and/or noise.

The register set used to define the zones is from Reg 0x60 to 0x73. The thresholds are modified by the noise buffer based on user definition or default values. The individual bits are register accessible and can be defined by the user. A more detailed description can be found in the "Register Map" on page 19.

- Abs (current distance – reference distance) > threshold
- Threshold = motion_dist_thld[15:0], Reg0x74-75
- Detection flag register = detect_flag[7:0], Reg0x59
- Reference distance = distance_ref[15:0], Reg0x56-57

Magnitude Zones

The sensor has the ability to generate interrupts based on magnitude information.

The return magnitude can be characterized for a given optical system and zones defined based on return amplitude. The user defined magnitude thresholds will be used to generate interrupts.

A magnitude zone allows for segmentation of the signal received into three zones with user defined thresholds for high and low zones.

Thresholds based on change in distance/magnitude:

- Simplified magnitude threshold operation
- Current Magnitude > reference magnitude * (1+Threshold/16)
- Current magnitude < reference magnitude * (1 - Threshold/16)
- Threshold = motion_mag_thld[7:0], Reg0x76
- Reference is updated on read of the detection flag register.
- Detection Flag Register = detect_flag[7:0], Reg0x59
- Reference distance = distance_ref [15:0], Reg0x56-57
- Reference magnitude = magnitude_ref [7:0], Reg0x54-55
- All the flags are independently controlled by registers and can trigger and interrupt.

Persistence Counter

In order to detect presence of an object in a field of view for a certain time or to reconfirm the measurement, persistence can be applied to detection conditions in the sensor. This function minimizes noise in the system level decision making process. An interrupt event flag is set if, and only if, a detection condition persists for N cycles.

N programmable from 1, 2, 4, 8, previous sample's detection flag accessible via register.

Reg0x5b will be updated each cycle, regardless of I^2C and can be accessed by the host.

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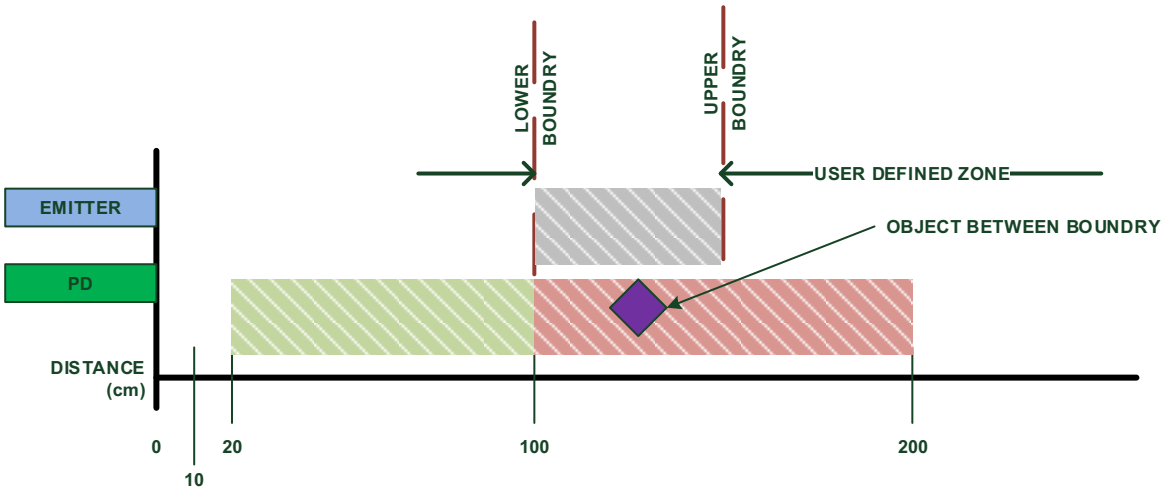

FIGURE 11. GRAPHICAL ILLUSTRATION OF DISTANCE ZONES AND BOUNDARIES

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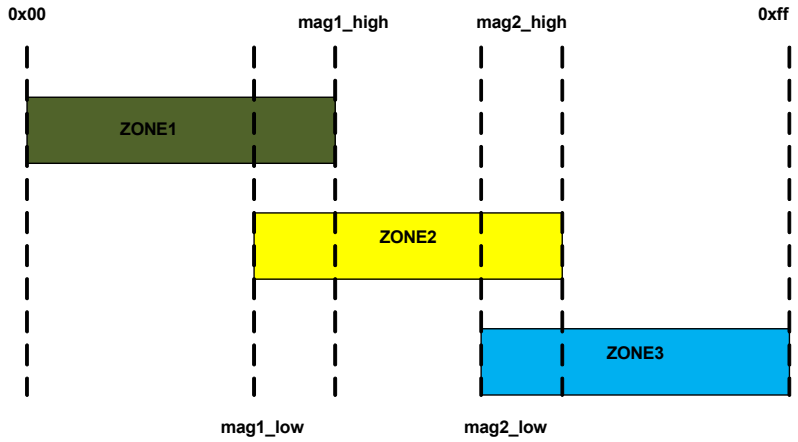

FIGURE 12. ILLUSTRATION OF MAGNITUDE ZONES AND USER DEFINED THRESHOLDS

Change Based Interrupts

Change based interrupts are triggered when an event, as defined by the user, has occurred in the system field of view.

Interrupts in this mode are not generated for data capture (i.e., when changes occur in measurements) for presence detection the detect_flag[7:0] is triggered and can be accessed using I2C interface.

The Datavalid register is another key component which ensures that outputs from sensors are valid.

Presence Detect Mode

Presence detect function is intended to provide the end user with an ability to detect the presence or absence of an object in the desired field of view. This function is coupled with interrupt generation where any significant event in the FOV (presence or absence of an object) triggers a valid output to the MCU.

The sensor should also provide amplitude values corresponding to the distance the phase and amplitude values can be accessed with register control by the system designer for decision making.

The system designer has the ability to define the minimum signal magnitude which can be used to generate an interrupt for a particular system.

Proximity Detect

Proximity detect function can be used by the system designer to determine the closeness of an object to the system.

Distance or minimum signal magnitude can be used to define when a system will generate an interrupt. A detailed description of registers can be found in the "Register Map" on page 19.

Noise Rejection

Electrical AC power worldwide is distributed at either 50Hz or 60Hz and may interfere with sensor operation. The ISL29501 sensor operation takes this into consideration and rejects these noise sources.

I^2C Serial Interface

The ISL29501 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL29501 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Valid Identification (Address)

The ISL29501 responds to the I^2C base address of 0x57.

TABLE 4. IDENTIFICATION BYTE FORMAT

1	0	1	0	1	A2	A1	0
(MSB)							(LSB)

A2 and A1 Pins

A2 and A1 are address select pins and can be used to select one of 4 alternate addresses. A2 and A1 must be set to their corresponding logic levels. The LSB in the Read/$\overline{\text{Write}}$ bit value is "1" for a Read operation, and "0" for a $\overline{\text{Write}}$ operation (see Table 4).

A1 and A2 should be tied to DVCC/DVSS in default mode.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 13 on page 17). On power-up of the ISL29501, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL29501 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 13). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH (see Figure 13). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 14 on page 17).

The ISL29501 responds with an ACK after recognition of a START condition followed by a valid Identification (a.k.a. I^2C Address) Byte. The ISL29501 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

Write Operation

A Write operation requires a START condition, followed by a valid Identification byte, a valid address byte, a data byte, and a STOP condition. After each of the three bytes, the ISL29501 responds with an ACK.

STOP conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the ISL29501 resets itself without performing the write.

Read Operation

A Read operation is shown in Figure 16 on page 18. It consists of a minimum 2 bytes: a START followed by the ID byte from the master with the R/$\overline{\text{W}}$ bit set to 1, then an ACK followed by the data byte or bytes sent by the slave. The master terminates the read operation by not responding with an ACK and then issuing a STOP condition. This operation is useful if the master knows the current address and desires to read one or more data bytes.

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A random address read operation consists of a three byte “dummy write” instruction followed by a current address read operation (see Figure 17). The master initiates the operation issuing the following sequence: a START, the identification byte with the R/$\overline{W}$ bit set to “0”, an address byte, a second START and a second identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL29501 responds with an ACK. The ISL29501 then transmits data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the Read operation from the ISL29501 by issuing a STOP condition following the last bit of the last data byte (see Figure 16).

The data bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the address byte in the read operation instruction and increments by one during transmission of each data byte. Address 04h is the last valid data byte, higher addresses are not available. Data from addresses higher than memory location 04h will be invalid.

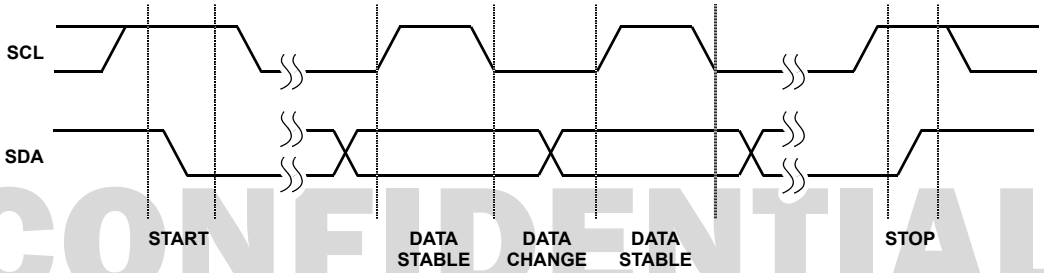

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FIGURE 13. VALID DATA CHANGES, START AND STOP CONDITIONS

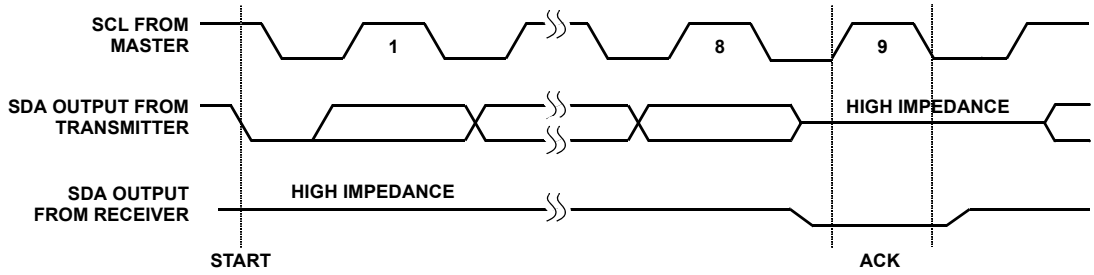

FIGURE 14. ACKNOWLEDGE RESPONSE FROM RECEIVER

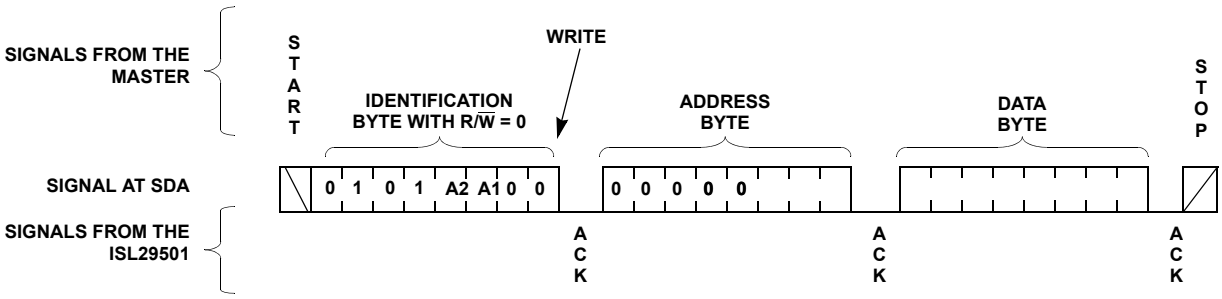

FIGURE 15. BYTE WRITE SEQUENCE

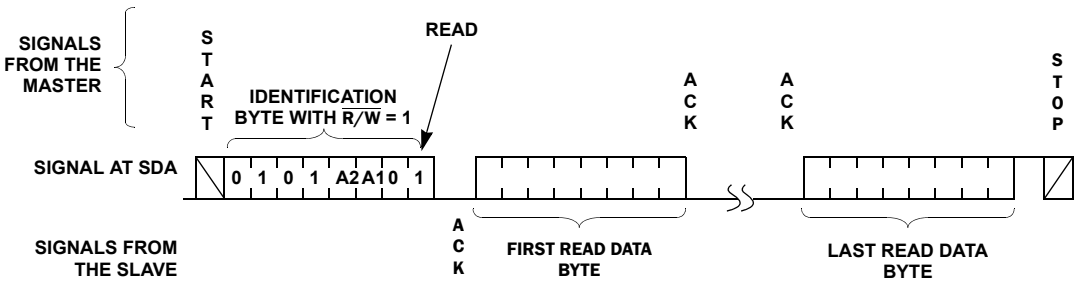

FIGURE 16. ADDRESS READ SEQUENCE

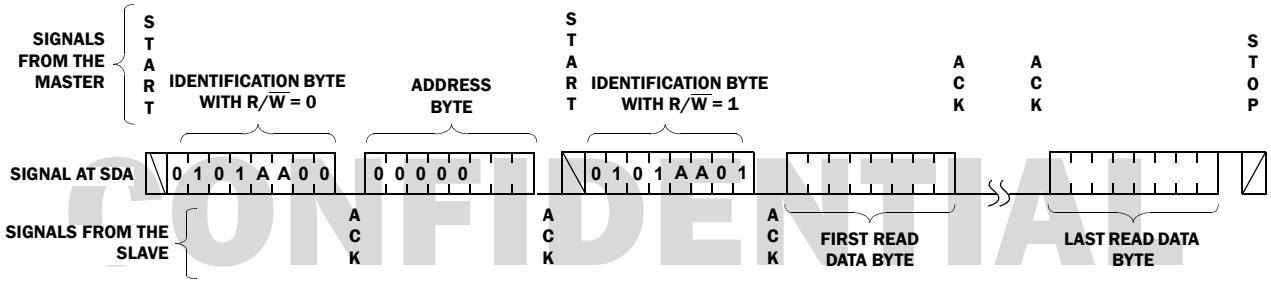

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FIGURE 17. RANDOM ADDRESS READ SEQUENCE

System Level Calibration

The goal of calibration on the ISL29501 is to be able to calibrate the sensor performance for different external components that are paired with the sensor and ensure stable operation across supply range and temperature.

There is no nonvolatile memory on-chip and the user will have to use the I^2C to program the register values during initialization.

Crosstalk Calibration

Electrical and optical crosstalk occurring due to board parasitics or routing can be measured and compensated for using on-chip calibration mechanism. This is a one-time calibration performed at the factory in dark.

The user will be required to read the x-talk values from the sensor and program these values back into the sensor using I^2C interface.

Registers are provided on-chip that can be programmed during initialization. A detailed description of registers is provided in the "Register Map" on page 19, registers 0x24 to 0x2b in the register map provide more detailed information.

Distance Offset Calibration

One time calibration performed at the system integrators factory should account for component nonidealities.

The integrator will place the system at a known distance and measurement captured with the sensor to account for component related offset.

Optical System Design Considerations

A system designed with the ISL29501 requires that emitter and detector are optically isolated for better performance. There needs to be a physical barrier or isolation between the emitter and detector to minimize direct optical signal coupling between emitter and detector.

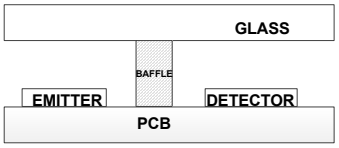

FIGURE 18. SIMPLIFIED OPTICAL SYSTEM

If a glass or other material is placed above the emitter detector, light from the LED can reflect off the glass and enter the sensor. This can limit the range of the proximity measurement and manifests as faint objects in measurements.

Careful attention must be paid to some of the following design parameters:

- Spacing between emitter and detector
- Optical isolation between emitter and detector
- Distance of the PCB from glass or from optical co-package

The ISL29501 architecture rejects most ambient optical interference signals that are lower or higher than the modulation frequency. A review of the ambient sources in the system will help you understand the amount of ambient light and the impacts on the precision measurements.

Register Map

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
PAGE 0: CONTROL, SETTING AND STATUS REGISTERS							
0x00	Device ID	RO	0xA	7:0	chip_id[7:0]	Device ID	Default to '0A'
0x01	Master Control	RW	0x00	0	c_en	Chip enable	Same meaning as CEn pin 0: Enabled 1: Disabled (default)
0x02	Status Registers	RO		0	enout		
				1	ready		
				2	vdd ok		Brown out protection for supply
SECTION 0.1: SAMPLING CONTROL REGISTERS							
0x10		RW	0x02				
			2	3:0	sample_len[3:0] = $71.1\mu s * 2^{\{sample\_len[3:0]\}}$ Maximum = $71.1\mu s * 2^{11} = 145.6ms$	Controls the length of for each sample, which is equal to the time during which the optical pulse is active. Should be ≤ (sample period -375µs + Cal Period), where Calibration period = Sum (0x14[3:0],0x15[3:0]) if calibration within sample period 0 otherwise.	Sample_len is also the integration time and controls the noise bandwidth of the sensor system. This parameter needs to be optimized based on system performance.
			0	7:4	sample_num[3:0]	Number of samples to be collected for multishot	0 Samples = 1 Sample
0x11	Sample Period	RW	0x00	7:0	sample_period[7:0]	Controls the time between the start of each sample	Sample Period = 450µs*(sample_period[7:0]+1)
0x12	Sample Period Range	RW	0x00				
				1:0	sample_skip[1:0]	Sample skipping select	0: Sample period multiplied by 2^0 1: Sample period multiplied by 2^1 2: Sample period multiplied by 2^2 3: Sample period multiplied by 2^3 (default)
0x13	Sample Control	RW	0x7C				
			0	0	adc_mode	Single/multishot vs free running	0: Free running, no external TRIGGER required to continue sampling 1: Single or multi shot, will only sample off external trigger
			0	1	cali_mode	Calibration vs light order for single/multishot mode	0: Calibration happens before light samples for single/multishot mode 1: Calibration happens after light samples for single/multishot mode

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
			3	3:2	cali_freq[1:0]	Sets frequency of calibration samples for free running mode	0: Calibration sample after every 16 light samples 1: Calibration sample after every 32 light samples 2: Calibration sample after every 64 light samples 3: Calibration sample after every 128 light samples
			1	4	light_en	Light sample enable	0: Calibration disenabled 1: Calibration enabled
			0	7	collision_det_en	Enable collision detection	0: Collision detection disenabled 1: Collision detection enabled
0x14	DC Cal Integration Time	RW	0x02				
			2	3:0	dc_cal_len[3:0]	Controls the length of integration time for each DC calibration sample. Should be ≤(Sample Period 375µs Signal Integration Time)	Integration Time = $71.1\mu s * 2^{\{DC\ Cal\ IntegrationTime<3:0>\}}$ Maximum Integration Time = $71.1\mu s * 2^{11}$ = 145.6ms
0x15	ZP Cal Integration Time	RW	0x02				
			2	3:0	zp_cal_len[3:0]	Controls the length of integration time for each background ZP calibration sample. Should be ≤ (Sample Period 375µs Signal Integration Time)	Integration Time = $71.1\mu s * 2^{\{Background\ ZP\ Cal\ IntegrationTime<3:0>\}}$ Maximum Integration Time = $71.1\mu s * 2^{11}$ = 145.6ms
0x16	Collision	RW	0x02				
			2	3:0	collision_len[3:0]	Controls the length of each collision sample. Should be ≤(Sample Period, 375µs signal), also needs to allow for any other enabled calibrations	= $71.1\mu s * 2^{\{Collision\ IntegrationTime<3:0>\}}$ Maximum = $71.1\mu s * 2^{11}$ = 145.6ms
SECTION 0.2: ALGORITHM CONTROL REGISTERS							
0x1a	DSP Enable	RW	0x0F				
			1	0	dsp_ol_en		Skip the DSP associate with open loop state. Bypasses phase_offset/i_xtalk/ q_xtalk directly to light state
			1	1	dsp_ts_en		Skip the DSP associate with Temperature sensor state. Behavior III defined if disabled.
			1	2	dsp_cal_en		Skip the DSP associated with Cal state. Behavior III defined if disabled.
			1	3	dsp_light_en		Skip the DSP associated with light state. Behavior III defined if disabled.

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
SECTION 0.3: SIGNAL INTEGRITY REGISTERS							
0x1b	DC Saturation Threshold	RW	0x7F				
				7:0	threshold_dc[7:0]	Threshold for DC saturation flag	Full scale implies 450µA of DC current due to ambient light at the front end
0x1c	Noise Threshold Offset	RW	0x0C				
			12	5:0	noise_thld_os[5:0]	Noise threshold offset for precision flag	Precision flag: precision> noise threshold offset + (distance>>slope) LSB = 8.13mm = 16 distance code LSBs full scale = 0.52m
0x1d	Noise Threshold Slope	RW	0x02				
			2	3:0	noise_thld_slope[1:0]	Noise threshold slope for precision flag	Precision flag: precision> noise threshold offset + (distance>>slope)
0x1e	Magnitude Squelch Exponent	RW	0x00				
				3:0	maq_squelch_exp[3:0]	Magnitude squelch exponent	
0x1f	Magnitude Squelch	RW	0x00				
				7:0	maq_squelch[7:0]	Magnitude squelch	12-bit floating point number (4 exponent bits in magnitude squelch exponent)
0x20	Circuit Noise	RW	0x1a				
				7:0	ckt_noise[7:0]	Circuit noise	Offset for the noise PSD
0x21	Noise Gain	RW	0x10				
				7:0	noise_gain[7:0]	Noise gain	Gain for the precision estimate
0x22	Fixed Error	RW	0x0a				
				7:0	fixed_error[7:0]	Fixed error	Offset for the precision estimate
SECTION 0.4A: CLOSED LOOP CALIBRATION REGISTERS							
0x24	Crosstalk I Exponent	RW	0x00	7:0	i_xtalk_exp[7:0]	Refer to software user manual for number conversion procedure	Cross talk I channel exponent
0x25	Crosstalk I MSB	RW	0x00	7:0	i_xtalk[15:8]		Crosstalk I channel MSB
0x26	Crosstalk I LSB	RW	0x00	7:0	i_xtalk[7:0]		Crosstalk I channel LSB
0x27	Crosstalk Q Exponent	RW	0x00	7:0	q_xtalk_exp[15:8]	Refer to software user manual for number conversion procedure	Cross talk Q channel exponent
0x28	Crosstalk Q MSB	RW	0x00	7:0	q_xtalk[15:8]		Crosstalk Q channel MSB

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
0x29	Crosstalk Q LSB	RW	0x00	7:0	q_xtalk[7:0]		Crosstalk Q channel LSB
0x2a	Crosstalk Gain MSB	RW	0xFF	7:0	gain_xtalk[15:8]	Refer to software user manual for number conversion procedure	Cross talk gain MSB
0x2b	Crosstalk Gain LSB	RW	0x00	7:0	gain_xtalk[7:0]		Cross talk gain LSB
0x2c	Magnitude Reference Exp	RW	0x00	3:0	mag_ref_exp[3:0]	Refer to software user manual for number conversion procedure	Magnitude reference exponent
0x2d	Magnitude Reference MSB	RW	0x00	7:0	mag_ref[15:8]		Magnitude reference significant
0x2e	Magnitude Reference LSB	RW	0x01	7:0	mag_ref[7:0]		
0x2f	Phase Offset MSB	RW	0x00	7:0	phase_offset[15:8]	Refer to software user manual for number conversion procedure	Fixed distance offset calibration MSB
0x30	Phase Offset LSB	RW	0x00	7:0	phase_offset[7:0]		Fixed distance offset calibration LSB
SECTION 0.4B: AMBIENT LIGHT AND TEMPERATURE CORRECTIONS							
0x31	Temperature reference	RW	0x00	7:0	ol_temp_ref[7:0]	Refer to software user manual for number conversion procedure.	Temperature reference
0x32	Emitter Reference	RW	0x00	7:0	ol_emit_ref[7:0]		Emitter reference
0x33	Phase exponent	RW	0x00	7:0	ol_phase_co_exp[3:0]‘		Phase exponent
0x34	Phase Temp Co1	RW	0x00	7:0	ol_phase_temp_co1[7:0]		Phase offset temp Co 1
0x35	Phase Emitter Co1	RW	0x00	7:0	ol_phase_emit_co1[7:0]		Phase offset emitter Co 1
0x36	Phase Ambient Co1	RW	0x00	7:0	ol_phase_amb_co1[7:0]		Phase offset ambient Co 1
0x39	Phase Temp Co2	RW	0x00	7:0	ol_phase_temp_co2[7:0]		Phase offset temp Co 2
0x3a	Phase Emitter Co2	RW	0x00	7:0	ol_phase_emit_co2[7:0]		Phase offset emitter Co 2
0x3b	Phase Ambient Co2	RW	0x00	7:0	ol_phase_amb_co2[7:0]		Phase offset ambient Co 2
0x53	Emitter select	RW	0x00	7:0	emitter_ol_sel		Emitter select for open loop

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
SECTION 0.4: INTERRUPT REGISTERS							
0x60	Interrupt Control	RW	0x00				
				2:0	interrupt_ctrl[2:0]	Select which interrupt mode to be used.	0: Interrupts disabled 1: Data ready 2: Event detection interrupts 3: Interrupts disabled
				3	interrupt_data_invalid	Select the behavior of invalid samples	0: Use invalid samples 1: Ignore invalid samples
				4	condition_1_en	Enables condition 1	
				5	condition_2_en	Enables condition 2	
				6	change_en	Flag change triggered interrupt	0: Repeated Interrupt generation 1: Only trigger Interrupt if there is change in flags (i.e., 0x52 = 0x5a)
				7	ro_irq	Controls effect of interrupt on RO data structure	0: Read out data structure locks when interrupt is raised. 1: Read out data structure refreshes independently to the interrupt
0x61	Data Invalid Mask	RW	0x00	7:0	data_invalid_mask[7:0]	Enables for data invalid flags	Each bit is ANDed with the Data Invalid register before used to ignore invalid samples for interrupt.
0x62	Detection Control	RW	0x00				
			0	1:0	noise_buffer_ctrl[1:0]	Noise buffer control	Adds a buffer to the distance zones based on distance precision Buffer = PRECISION<<NOISE_BUFFER_CTRL[1:0]
			0	2	noise_buffer_sign	Eliminate false positive or false negatives	Determines the direction to apply the buffer defined above.
			0	3	noise_buffer_enable	Enable/disables noise buffer feature	
			0	5:4	persistence[1:0]	Persistence	0: 1 Sample (i.e., no persistence) 1: 2 Samples 2: 4 Samples 3: 8 Samples
0x63	Detection Condition 1	RW	0x00		condition_1_ctrl		
				0	c1_motion_distance_en	Distance based motion detect enable	abs(distance-distance_ref) > motion_dist_thld ± noise_buffer
				1	c1_motion_magnitude_en	Magnitude based motion detect enable	abs (magnitude-magnitude_ref) > max (magnitude, magnitude_ref)* (precision+motion_mag_thld)
				2	c1_zone1_en	Distance zone 1 interrupt enable	Threshold 0 < distance < threshold 1

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
				3	c1_zone2_en	Distance zone 2 interrupt enable	Threshold 1 < distance < threshold 2
				4	c1_zone3_en	Distance zone 3 interrupt enable	Threshold 2 < distance < threshold 0
				5	c1_mag1_en	Magnitude zone 1 interrupt enable	Magnitude ≤ mag threshold 0
				6	c1_mag2_en	Magnitude zone 2 interrupt enable	Mag threshold 0 < magnitude ≤ Mag threshold 1
				7	c1_mag3_en	Magnitude zone 3 interrupt enable	Mag threshold 1 < magnitude
0x64	Detection Condition 2	RW	0x00		condition_2_ctrl		
				0	c2_motion_distance_en	Distance based motion detect enable	
				1	c2_motion_magnitude_en	Magnitude based motion detect enable	
				2	c2_zone1_en	Distance zone 1 interrupt enable	
				3	c2_zone2_en	Distance zone 2 interrupt enable	
				4	c2_zone3_en	Distance zone 3 interrupt enable	
				5	c2_mag1_en	Magnitude zone 1 interrupt enable	
				6	c2_mag2_en	Magnitude zone 2 interrupt enable	
				7	c2_mag3_en	Magnitude zone 3 interrupt enable	
0x65	Reference Distance for Motion MSB	RO	0x00	7:0	motion_dist_ref[15:8]		Equal to distance from last time detect_flag is cleared. Used for motion detection.
0x66	Reference Distance for Motion LSB	RO	0x00	7:0	motion_dist_ref[7:0]		Equal to distance from last time detect_flag is cleared. Used for motion detection.
0x67	Reference Magnitude Exponent	RO	0x00	7:0	motion_dist_ref[7:0]		Equal to distance from last time detect_flag is cleared. Used for motion detection.

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
0x68	Reference Magnitude Significand	RO	0x00	7:0	motion_mag_ref[7:0]		Equal to magnitude MSB from last time detect_flag is cleared. Used for motion detection.
0x69	Interrupt Flag	RC	0x00				Clear on Read
				0	data_ready	Distance based motion detect event flag	0: No event occurred 1: Event interrupted
				1	condition_1_flag	Indicates that condition 1 is detected	condition_1 = OR (detect_flag[7:0] Bitwise and condition_1_ctrl[7:0])
				2	condition_2_flag	Indicates that condition 2 is detected	condition_2 = OR (detect_flag[7:0] Bitwise and condition_2_ctrl[7:0])
				3	event_flag	Indicates that both condition 1 and Condition 2 are detected, (if enabled).	event_detect = (condition_1 OR NOT condition_1_en) AND (condition_2 OR NOT condition_1_en)
				4	change_flag		0x6a = 0x6b
				5	brownout_flag	Brownout detection	1 = A brownout has occurred; consider restart
0x6a	Detection Flag	RC	0x00		detect_flag[7:0]		Clear on read
				0	motion_distance_flag	Distance based motion detect event flag	0: No Event occurred 1: Event interrupted
				1	motion_magnitude_flag	Magnitude based motion detect event flag	
				2	zone1_flag	Distance zone 1 event flag	
				3	zone2_flag	Distance zone 2 event flag	
				4	zone3_flag	Distance zone 3 event flag	
				5	mag1_flag	Magnitude zone 1 event flag	
				6	mag2_flag	Magnitude zone 2 event flag	
				7	mag3_flag	Magnitude zone 3 event flag	
0x6b	Detection Flag Reference	RO	0x00	7:0	detect_ref[7:0]	Detection flag reference	Equal to detection flag from last time it was cleared. Used for change triggered interrupts.
SECTION 0.6: DETECTION MODE CONTROL REGISTERS							
0x70	Threshold 0 High MSB	RW	0x00	7:0	dist0_high[15:8]	Zone 0 distance high threshold	Default is 0m
0x71	Threshold 0 High LSB	RW	0x00	7:0	dist0_high[7:0]	Zone 0 distance high threshold	
0x72	Threshold 0 Low MSB	RW	0xF0	7:0	dist0_low[15:8]	Zone 0 distance low threshold	Default is -2m
0x73	Threshold 0 Low LSB	RW	0xA0	7:0	dist0_low[7:0]	Zone 0 distance low threshold	
0x74	Threshold 1 High MSB	RW	0x00	7:0	dist1_high[15:8]	Zone 1 distance high threshold	Default is 10cm

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
0x75	Threshold 1 High LSB	RW	0xC5	7:0	dist1_high[7:0]	Zone 1 distance high threshold	
0x76	Threshold 1 Low MSB	RW	0x00	7:0	dist1_low[15:8]	Zone 1 distance low threshold	Default is 5cm
0x77	Threshold 1 Low LSB	RW	0x62	7:0	dist1_low[7:0]	Zone 1 distance low threshold	
0x78	Threshold 2 High MSB	RW	0x00	7:0	dist2_high[15:8]	Zone 2 distance high threshold	
0x79	Threshold 2 High LSB	RW	0x00	7:0	dist2_high[7:0]	Zone2 distance high threshold	
0x7a	Threshold 2 Low MSB	RW	0x00	7:0	dist2_low[15:8]	Zone 2 distance low threshold	
0x7b	Threshold 2 Low LSB	RW	0x00	7:0	dist2_low[7:0]	Zone 2 distance low threshold	
0x7c	Magnitude Threshold 1 High Exponent	RW	0x00	3:0	mag1_high_exp[3:0]	Magnitude threshold 1 high exponent	
0x7d	Magnitude Threshold 1 High	RW	0x00	7:0	mag1_high[7:0]	Magnitude threshold 1 high	
0x7e	Magnitude Threshold 1 Low Exponent	RW	0x00	3:0	mag1_low_exp[3:0]	Magnitude threshold 1 low exponent	
0x7f	Magnitude Threshold 1 Low	RW	0x00	7:0	mag1_low[7:0]	Magnitude threshold 1 low	
0x80	Magnitude Threshold 2 High Exponent	RW	0x00	3:0	mag2_high_exp[3:0]	Magnitude threshold 2 high exponent	
0x81	Magnitude Threshold 2 High	RW	0x00	7:0	mag2_high[7:0]	Magnitude Threshold 2 high	
0x82	Magnitude Threshold 2 Low Exponent	RW	0x00	3:0	mag2_low_exp[3:0]	Magnitude threshold 2 low exponent	
0x83	Magnitude Threshold 2 Low	RW	0x00	7:0	mag2_low[7:0]	Magnitude threshold 2 low	
0x84	Motion Distance Threshold MSB	RW	0x00	7:0	motion_dist_thld[15:8]	Motion distance threshold	
0x85	Motion Distance Threshold LSB	RW	0x00	7:0	motion_dist_thld[7:0]	Motion distance threshold	
0x86	Motion Magnitude Threshold	RW	0x00	7:0	motion_mag_thld[7:0]	Motion magnitude threshold	Threshold in % = motion_mag_thld/256*100%

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Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
SECTION 0.7: ANALOG CONTROL REGISTERS							
0x90	Driver Range	RW	0x00				Double write required to update all bits in this register.
				3:0	driver_s[3:0]	Current DAC scale	Sets the maximum emitter driver 4.5MHz current (i.e., the peak of the square wave)
0x91	Emitter DAC	RW	0x00				Double write required to update all bits in this register.
				7:0	emitter_current[7:0]		Emitter current 4.5MHz peak (i.e., the peak of the square wave) = maximum current (set by 0x80[2:0])*emitter_current[7:0]/255
0x92	Driver Control	RW	0x01				
			0	0	driver_thresh_en		
			0	1	driver_nboost_en		
			0	2	driver_enbal		
0x93	Threshold DAC	RW	0x00	7:0	driver_t[7:0]		Double write required to update all bits in this register.
0x97	Frontend Control	RW	0x00				
			0	1:0	afe_gain[1:0]	Scale TIA gain	0: 4x 1: 2x 2: 1x 3: 1x
			0	2	lna_gain	Scale LNA gain	0: Gain = 1 1: Gain = 3
			0	3	afe_lowcap_mode		Adds 6pF to PDp/PDn terminals. Recommended for applications with ≤4pF PD capacitance.
			0	4	afe_pd_dc		Disables DC reject loop, (limits operation to 25µA DC current)
0xae	Internal RSET	RW	0x00				
				0	rint	Use internal or external R_{SET} resistor	0: External 1: Internal

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PCB Design Practices

- PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip line is used.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize the use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or PCB gaps under these lines). Place vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of 2 power supply decoupling capacitors are recommended (1000pF, 0.01µF) and place as close to the devices as possible. Do not use vias between the capacitor and the device because vias add unwanted inductance. Larger capacitors can be farther away from the device. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

PCB Layout Considerations

The use of multilayer PCB stack up is recommended to separate analog and emitter supplies. Placing a power supply plane located adjacent to the ground plane creates a large capacitance with little or no inductance. This will minimize ground bounce and improve power supply noise. The dielectric thickness separating these layers should be as thin as possible to minimize capacitive coupling.

It is important that power supplies be bypassed over a wide range of frequencies. A combination of large and small width capacitors that self resonate around the modulation frequency will provide ample suppression of fundamental and harmonics that can be coupled to the sensor power supplies (check ESR ratings).

Ensure that photodiode inputs pins (PDp and PDn) have symmetric and short traces and minimize placing aggressors around these routes, The guard shields provided on the IC should help minimize interference.

Ensure that emitter power (EVCC and EVSS) and ground traces are low resistance paths with a short return path to emitter ground.

Minimize trace length and via's to minimize inductance and minimize noise rejection.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to provide heatsinking for the IC. However, because of the connection to the V1- and V2- supply pins through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multilayered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible, an isolated thermal pad on another layer should be used. Pad area requirements should be evaluated on a case-by-case basis.

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General Power PAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

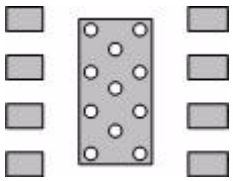

FIGURE 19. PCB VIA PATTERN

We recommend that you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint spaced such that they are center-on-center 3x the radius apart from each other. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

Connect all vias to the potential outlined in the datasheet for the pad, typically the ground plane but not always, so check the pin description. It is important the vias have a low thermal resistance for efficient heat transfer. Do not use "thermal relief" patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
July 1, 2015	FN8681.0	Initial Release

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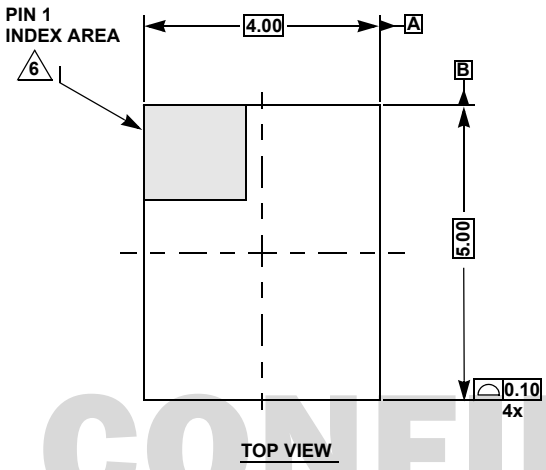
Package Outline Drawing

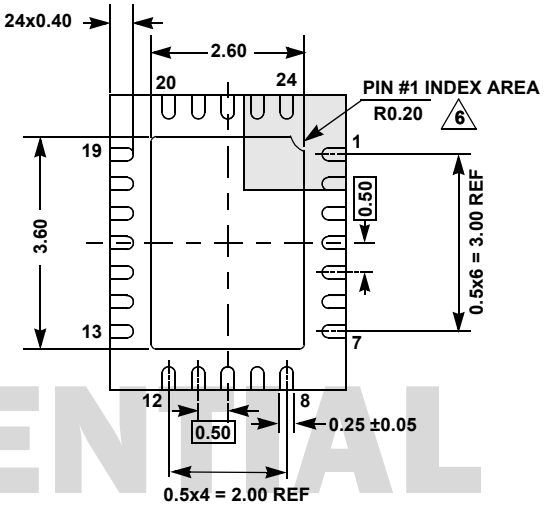
L24.4x5F

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 5/14



TOP VIEW



BOTTOM VIEW

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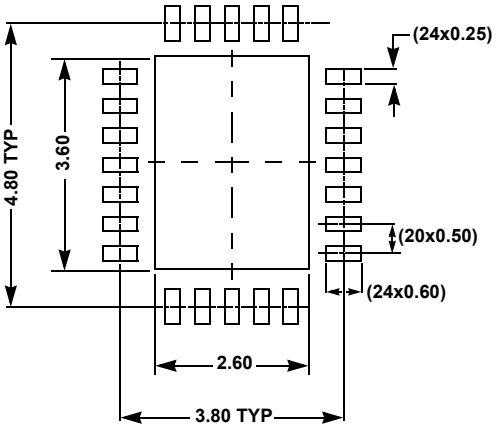
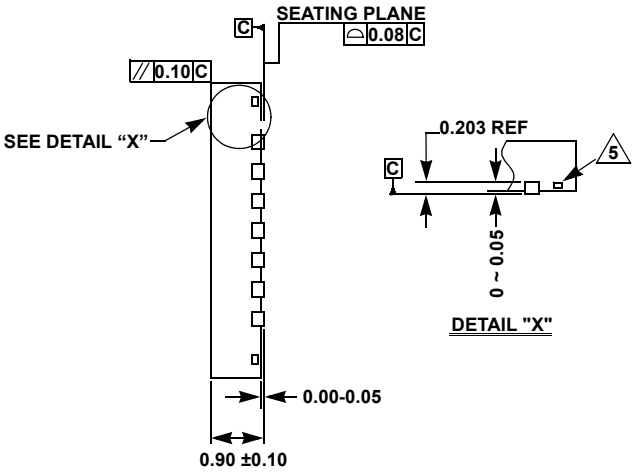


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to ASMEY14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.