intersil | SIMPLY SMARTER™

ISL29501 HDS

Jim Getchell

Intersil

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ISL29501 Hardware Design Specification (HDS)

ISL29501

1 Introduction

The ISL29501 will make us all rich someday.

Contents

2 Register List

Registers are your friends

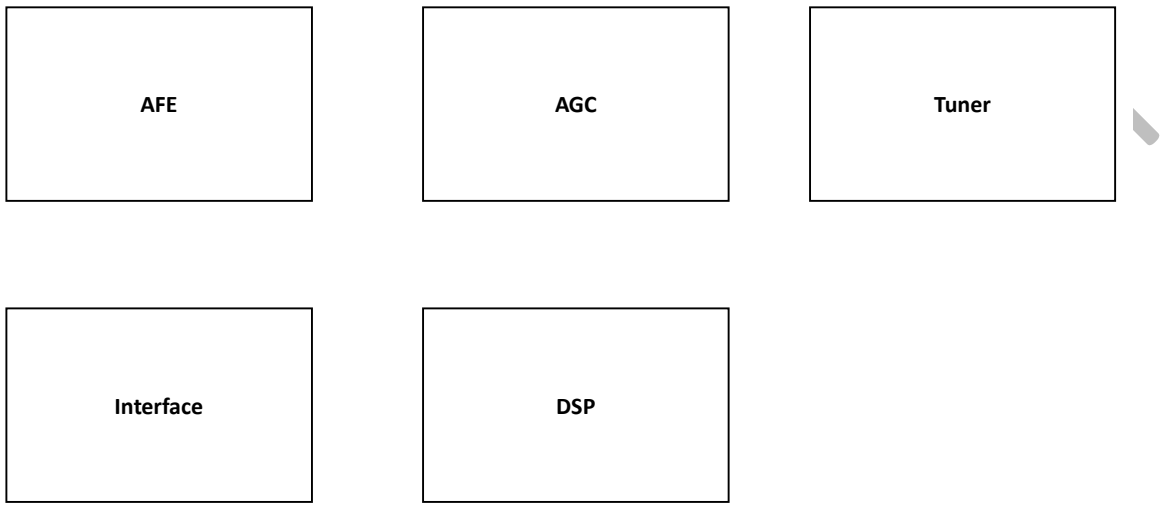
Table 1 ISL29501 Register list

0	DeviceID	**40**	CrosstalkIAmbientCo1	**80**	MagnitudeThreshold2HighExponent	**C0**	FuseOperation
1	MasterControl	**41**	CrosstalkIVGA1Co1	**81**	MagnitudeThreshold2High	**C1**	Fusereg1
2	StatusRegisters	**42**	CrosstalkIVGA2Co1	**82**	MagnitudeThreshold3LowExponent	**C2**	Fuse_reg2
3		**43**	CrosstalkITempCo2	**83**	MagnitudeThreshold3Low	**C3**	Fusereg3
4		**44**	CrosstalkIEmitterCo2	**84**	MotionDistanceThresholdMSB	**C4**	Fusereg4
5		**45**	CrosstalkIAmbientCo2	**85**	MotionDistanceThresholdLSB	**C5**	testreg1
6		**46**	CrosstalkIVGA1Co2	**86**	MotionMagnitudeThreshold	**C6**	testreg2
7		**47**	CrosstalkIVGA2Co2	**87**		**C7**	testreg3
8		**48**	CrosstalkQTempCo1	**88**		**C8**	testreg3
9		**49**	CrosstalkQEmitterCo1	**89**		**C9**	testmux
A		**4A**	CrosstalkQAmbientCo1	**8A**		**CA**	testsample
B		**4B**	CrosstalkQVGA1Co1	**8B**		**CB**	testreadsanple
C		**4C**	CrosstalkQVGA2Co1	**8C**		**CC**	testtrim1
D		**4D**	CrosstalkQTempCo2	**8D**		**CD**	testtrim2
E		**4E**	CrosstalkQEmitterCo2	**8E**		**CE**	testtrim3
F		**4F**	CrosstalkQAmbientCo2	**8F**		**CF**	testtrim4
10	IntegrationTime	**50**	CrosstalkQVGA1Co2	**90**	DriverRange	**D0**	DataInvalid
11	SamplePeriod	**51**	CrosstalkQVGA2Co2	**91**	EmitterCurrentDAC	**D1**	DistanceReadoutMSB
12	SamplePeriodRange	**52**	EmitterSelectforOpenLoop	**92**	DriverControl	**D2**	DistanceReadoutLSB
13	SampleControl	**53**		**93**	ThresholdCurrentDAC	**D3**	PrecisionMSB
14	DCCalIntegrationTime	**54**		**94**	DriverBoost	**D4**	PercisionLSB
15	ZPCalIntegrationTime	**55**		**95**	DriverBoostDuration	**D5**	MagnitudeExponent
16	CollisionIntegrationTime	**56**		**96**	DriverChargeBalancingDAC	**D6**	MagnitudeSignificandMSB
17	AGCControl1	**57**		**97**	FrontendControl	**D7**	MagnitudeSignificandLSB
18	AGCControl2	**58**		**98**	AFEControlRegisters	**D8**	PhaseReadoutMSB
19	AGCControl3	**59**		**99**	AmbientADCTestFeatures	**D9**	PhaseReadoutLSB
1A	DSPEnable	**5A**		**9A**	VGAOffsetCode	**DA**	IRawExponent
1B	DCSaturationThreshold	**5B**		**9B**	VGA1ManualforLight	**DB**	IRawMSB
1C	NoiseThresholdOffset	**5C**		**9C**	VGA2ManualforLight	**DC**	IRawLSB
1D	NoiseThresholdSlope	**5D**		**9D**	VGA1ManualforZP	**DD**	QRawExponent
1E	MagnitudeSquelchExponent	**5E**		**9E**	VGA2ManualforZP	**DE**	QRawMSB
1F	MagnitudeSquelch	**5F**		**9F**	VGA1ControlforCollision	**DF**	QRawLSB
20	CircuitNoise	**60**	InterruptControl	**A0**	VGA2ControlforCollision	**E0**	EmitterVoltageBefore
21	NoiseGain	**61**	DataInvalidMask	**A1**	ADCVrefCode	**E1**	EmitterVoltageAfter
22	FixedError	**62**	DetectionControl	**A2**	PeakDetectorThresholds	**E2**	AFETemperature
23	CollisionPeakSelect	**63**	DetectionCondition1	**A3**	PeakDetectorThresholds	**E3**	AmbientADC
24	CrosstalkIExponent	**64**	DetectionCondition2	**A4**	PeakDetectorThresholds	**E4**	VGA1
25	CrosstalkIMSB	**65**	ReferenceDistanceforMotionMSB	**A5**	EmitterVoltageADCOffset	**E5**	VGA2
26	CrosstalkILSB	**66**	ReferenceDistanceforMotionLSB	**A6**	EmitterVoltageADCMuxSelect	**E6**	GainMSB
27	CrosstalkQExponent	**67**	ReferenceMagnitudeExponent	**A7**	TempSensorRegA	**E7**	GainLSB
28	CrosstalkQMSB	**68**	ReferenceMagnitudeSignificand	**A8**	TempSensorRegB	**E8**	IADCMSB
29	CrosstalkQLSB	**69**	InterruptFlag	**A9**	TempSensorRegC	**E9**	IADCLSB
2A	CrosstalkGainMSB	**6A**	DetectionFlag	**AA**	TempSensorADCMode	**EA**	QADCMSB
2B	CrosstalkGainLSB	**6B**	DetectionFlagReference	**AB**	BPFSelect	**EB**	QADCLSB
2C	MagnitudeReferenceExp	**6C**		**AC**	Oscillator&AAFOffset	**EC**	DCCalibrationIMSB
2D	MagnitudeReferenceMSB	**6D**		**AD**	OscillatorSelect	**ED**	DCCalibrationILSB
2E	MagnitudeReferenceLSB	**6E**		**AE**	InternalRSET	**EE**	DCCalibrationQMSB
2F	PhaseOffsetMSB	**6F**		**AF**	Spares	**EF**	DCCalibrationQLSB
30	PhaseOffsetLSB	**70**	Zone1ThresholdHighMSB	**B0**	Command	**F0**	ZPCalibrationIMSB
31	TemperatureReference	**71**	Zone1ThresholdHighLSB	**B1**	I2CFast	**F1**	ZPCalibrationILSB
32	EmitterReference	**72**	Zone1ThresholdLowMSB	**B2**	RivisionID	**F2**	ZPCalibrationQMSB
33	PhaseExponent	**73**	Zone1ThresholdLowLSB	**B3**	BlockOverride	**F3**	ZPCalibrationQLSB
34	PhaseOffsetTempCo1	**74**	Zone2ThresholdHighMSB	**B4**	BlockOverride	**F4**	ZeroPhaseMSB
35	PhaseOffsetEmitterCo1	**75**	Zone2ThresholdHighLSB	**B5**	StateMachineControl	**F5**	ZeroPhaseLSB
36	PhaseOffsetAmbientCo1	**76**	Zone2ThresholdLowMSB	**B6**	StateMachineOverride	**F6**	ZPMagnitudeExp
37	PhaseOffsetVGA1Co1	**77**	Zone2ThresholdLowLSB	**B7**	StateMachineOverride1	**F7**	ZPMagnitudeMSB
38	PhaseOffsetVGA2Co1	**78**	Znee3ThresholdHighMSB	**B8**	AnalogMonitorControl	**F8**	ZPMagnitudeLSB
39	PhaseOffsetTempCo2	**79**	Zone3ThresholdHighLSB	**B9**	NCOControl1	**F9**	VGA1ZP
3A	PhaseOffsetEmitterCo2	**7A**	Zone3ThresholdLowMSB	**BA**	NCOControl2	**FA**	VGA2ZP
3B	PhaseOffsetAmbientCo2	**7B**	Zone3ThresholdLowLSB	**BB**	NCOControl3	**FB**	TempSensorRawMSB
3C	PhaseOffsetVGA1Co2	**7C**	MagnitudeThreshold1HighExponent	**BC**		**FC**	TempSensorRawLSB
3D	PhaseOffsetVGA2Co2	**7D**	MagnitudeThreshold1High	**BD**		**FD**	AGCState
3E	CrosstalkITempCo1	**7E**	MagnitudeThreshold2LowExponent	**BE**		**FE**	AGCStateZP
3F	CrosstalkIEmitterCo1	**7F**	MagnitudeThreshold2Low	**BF**		**FF**	

3 Functional Blocks

The ISL29501 has 5 major functional blocks shown in Figure 1

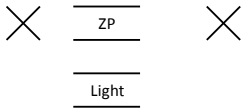
Figure 1 Top Level Block Diagram



3.1 Conversion Controls: ZP, Light & Period

A complete conversion consists of…

Figure 2 Conversion Cycles



sample_len: Controls the length of integration time for each sample, which is equal to the time during which the driver is active.

If sample integration time (or sample integration time plus cal period is cal enabled) is set to be greater than the sample period (including sample skipping), then the sample integration time will default to the maximum allowable value within the sample period. Integration Time =71.1us*2^{sample_len[3:0]} Maximum Integration Time = 71.1us*2^11= 145.6ms

sample_num: Number of Samples to be collected for multishot. 0 Samples = 1 Sample. ***What is multishot?***

Table 2 Conversion Control Registers

Sample Controls									
Addr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10	**IntegrationTime**	sample_num				sample_len			
		sample_num	For Multishot: 1-16						
		sample_len	Max=11; Integration Time= 71.1us * 2^sample_num;						
11	**SamplePeriod**	sample_period: Period = 450us*(sample_period+1)							
12	**SamplePeriodRange**							sample_skip	
13	**SampleControl**	collision_det_en	zp_cal_en	dc_cal_en	light_en	cali_freq		cali_mode	adc_mode
		collision_det_en							
		zp_cal_en							
		dc_cal_en							
		light_en							
		cali_freq							
		cali_mode							
		adc_mode							
14	**DCCalIntegrationTime**					dc_cal_len			
15	**ZPCalIntegrationTime**					zp_cal_len			
16	**CollisionIntegrationTime**					collision_len			

3.2 AFE (Analog Front End)

The AFE is comprised of 2 sub blocks, the TIA & the LNA, shown in Figure 3 including the following controls:

1. User adjustable gain: {1, 2, 4 … 32}
2. Coupling: AC/DC
3. Bandwidth limit
4. Ambient compensation DACs
5. TIA by pass

The details register/field assignments for these controls are shown in Table 3

Figure 3 AFE Block

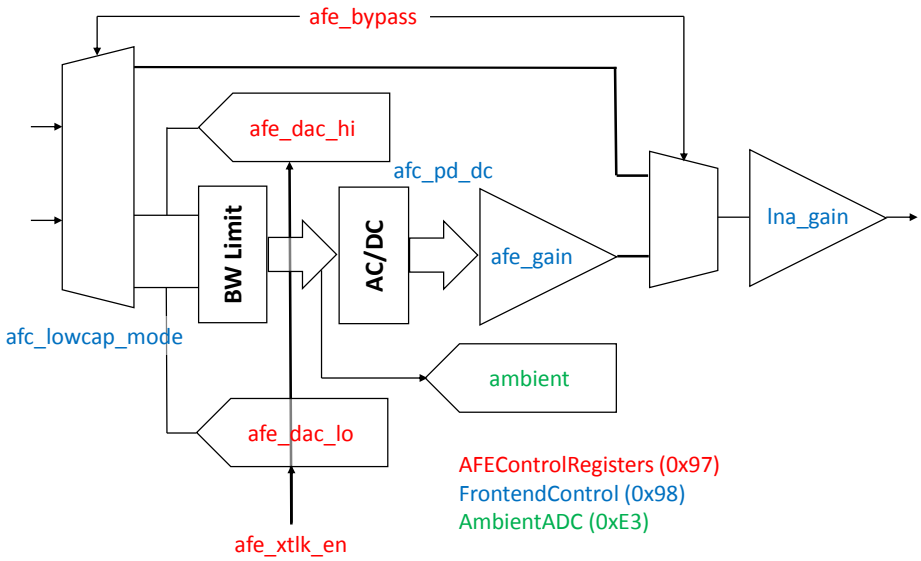


Table 3 AFE Control Registers

AFE									
Addr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
97	**FrontendControl**				afe_pd_dc	afc_lowcap_mode	lna_gain	afe_gain	
		afc_pd_dc	Disable AC coupling (25ua max operation)						
		afc_lowcap_mode	Set to 1 for < 4pF @ pdp&pdn						
		lna_gain	increase by 3x						
		afe_gain	0	0	00: Gain=1				
			0	1	01: Gain=2				
			1	X	1X: Gain=4				
98	**AFEControlRegisters**	afe_bypass	afe_xtlk_en	afe_dac_hi			afe_dac_lo		
		afe_bypass	Disable TIA (use external)						
		afe_xtlk_en	DC/AC coupling						
		afe_dac_hi							
		afe_dac_lo							
E3	**AmbientADC**	ambient[7:0]							

3.3 Partial AGC (VGA) Block

The AGC does really cool things. It makes us happy.

1. vga1 @ FS ~5cm
2. vga2 @ FS ~50cm

Equation 1 VGA – Magnitude Relationship

$$vga1 * vga2 * magnitude \approx K \text{ for } vga2 < 0xFF$$

Figure 4 AGC Functional Block Diagram

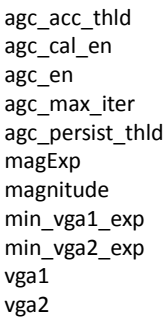


Table 4 AGC Block Control Registers

Addr	Name	7	6	5	4	3	2	1	0
17	**AGCControl1**	agc_max_iter						agc_cal_en	agc_en
		agc_max_iter							
		agc_cal_en							
		agc_en							
18	**AGCControl2**			agc_acc_thld			agc_persist_thld		
		agc_acc_thld							
		agc_persist_thld							
19	**AGCControl3**			min_vga2_exp			min_vga1_exp		
		min_vga2_exp							
		min_vga1_exp							
D5	**MagnitudeExponent**					magExp[3:0]			
D6	**MagnitudeSignificandMSB**	magnitude[15:8]							
D7	**MagnitudeSignificandLSB**	magnitude[7:0]							
E4	**VGA1**	vga1[7:0]							
E5	**VGA2**	vga2[7:0]							

4 System Behaviors

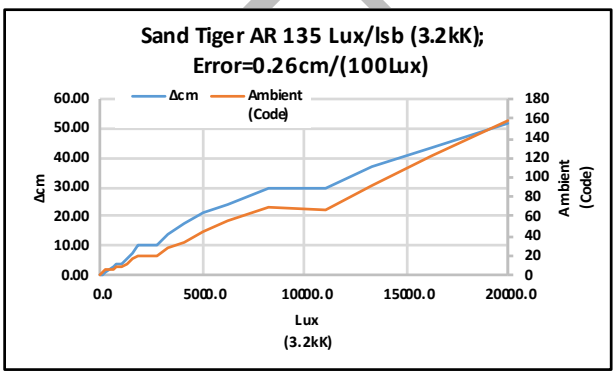
Describe interactions between controls.

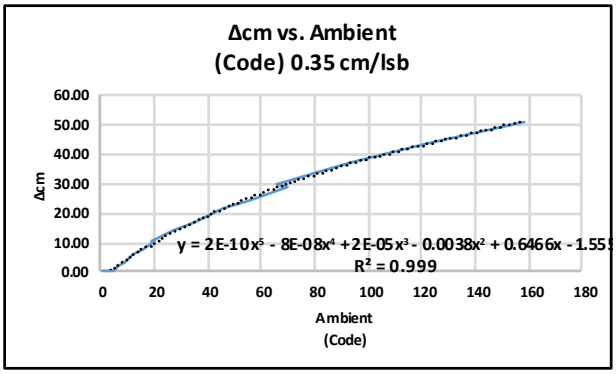
4.1 Ambient Rejection

Not very good, ≈2.5mm / 100 Lux (3.2kK)

Figure 5 Sand Tiger AR Curves

Sand Tiger AR 135 Lux/lsb (3.2kK); Error=0.26cm/(100Lux)							
Mag (dB)	Degrees	Ambient (Code)	Lux (3.2kK)	5.66	Δcm	Δ°	Poly5°
-26.701	69.19	158	3540	20036.4	51.48	5.56	0.00
-26.488	68.32	122	2866	16221.6	43.43	4.69	-0.02
-26.359	67.65	93	2340	13244.4	37.22	4.02	0.05
-26.197	66.84	66	1946	11014.4	29.72	3.21	0.09
-26.197	66.80	70	1455	8235.3	29.35	3.17	-0.09
-26.114	66.27	55	1090	6169.4	24.44	2.64	-0.07
-26.120	65.93	45	885	5009.1	21.30	2.30	0.00
-26.105	65.50	35	716	4052.6	17.31	1.87	0.02
-26.104	65.13	27	584	3305.4	13.89	1.50	0.04
-26.115	64.72	19	485	2745.1	10.09	1.09	0.07
-26.106	64.73	20	362	2048.9	10.19	1.10	0.02
-26.112	64.74	20	329	1862.1	10.28	1.11	0.03
-26.123	64.47	16	270.6	1531.6	7.78	0.84	-0.01
-26.120	64.46	16	266.2	1506.7	7.69	0.83	-0.02
-26.136	64.23	12	217.8	1232.7	5.56	0.60	-0.01
-26.152	64.01	9	181	1024.5	3.52	0.38	-0.05
-26.147	64.02	9	134.4	760.7	3.61	0.39	-0.04
-26.159	63.90	7	100.6	569.4	2.50	0.27	-0.03
-26.219	63.72	5	25.68	145.3	0.83	0.09	-0.08
-26.168	63.69	3	20.74	117.4	0.56	0.06	0.02
-26.265	63.63	1	0	0.0	0.00	0.00	0.10





5 Sequences

Algorithms occur here.

5.1 Load time sequence

Description of register set load required to support minimal operation. Should be adequate for the simplest µC operation.

5.2 Calibration sequence

From Steve Wickland…

5.3 AGC Loop (including AFE)

The current implementation only varies the gain on the VGA with an RF peak detector limiting the range to about 50cm (Sand Tiger: 18% grey, ∞ size). A control loop is required to include the AFE gain adjust detailed in § 3.1.

6 References

Table 5 Reference Data Files (available from Intersil (MLP) Intranet)

§2	"Original" Register List: ISL29501_Register_Map.pdf
	501_TOF Register List
§3	501_TOF Register Fields
	ISL29501_Number Formats
	Signed number representations
§3.3	ISL29501_AGC_Review.pdf
§3.1	AFE+VGA_Block Diagram