ISL29501 HDS

Jim Getchell

Intersil

3/9/2015



ISL29501 Hardware Design Specification (HDS)

ISL29501

# Introduction

The will make us all rich someday.

Contents

[ISL29501 Hardware Design Specification (HDS) 2](#_Toc413669696)

[1 Introduction 2](#_Toc413669697)

[2 Register List 3](#_Toc413669698)

[3 Functional Blocks 4](#_Toc413669699)

[3.1 Conversion Controls: ZP, Light & Period 5](#_Toc413669700)

[3.2 AFE (Analog Front End) 6](#_Toc413669701)

[3.3 Partial AGC (VGA) Block 7](#_Toc413669702)

[4 System Behaviors 8](#_Toc413669703)

[4.1 Ambient Rejection 8](#_Toc413669704)

[5 Sequences 9](#_Toc413669705)

[5.1 Load time sequence 9](#_Toc413669706)

[5.2 Calibration sequence 9](#_Toc413669707)

[5.3 AGC Loop (including AFE) 9](#_Toc413669708)

[6 References 9](#_Toc413669709)

# Register List

Registers are your friends

1. ISL29501 Register list



# Functional Blocks

The ISL29501 has 5 major functional blocks shown in Figure 1

1. Top Level Block Diagram



## Conversion Controls: ZP, Light & Period

A complete conversion consists of …

1. Conversion Cycles



**sample\_len**: Controls the length of integration time for each sample, which is equal to the time during which the driver is active.

If sample integration time (or sample integration time plus cal period is cal enabled) is set to be greater than the sample period (including sample skipping), then the sample integration time will default to the maximum allowable value within the sample period. Integration Time =71.1us\*2^{sample\_len[3:0]} Maximum Integration Time = 71.1us\*2^11= 145.6ms

**sample\_num**: Number of Samples to be collected for multishot. 0 Samples = 1 Sample. ***What is multishot?***

1. Conversion Control Registers

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Sample Controls** | | | | | | | | | |
| **Addr** | **Name** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **10** | **IntegrationTime** | sample\_num | | | | sample\_len | | | |
|  | | sample\_num | For Multishot: 1-16 | | | | | | |
| sample\_len | Max=11; Integration Time= 71.1us \* 2^sample\_num; | | | | | | |
| **11** | **SamplePeriod** | sample\_period: Period = 450us\*(sample\_period+1) | | | | | | | |
| **12** | **SamplePeriodRange** |  | | | | | | sample\_skip | |
| **13** | **SampleControl** | collision\_det\_en | zp\_cal\_en | dc\_cal\_en | light\_en | cali\_freq | | cali\_mode | adc\_mode |
|  | | collision\_det\_en |  | | | | | | |
| zp\_cal\_en |  | | | | | | |
| dc\_cal\_en |  | | | | | | |
| light\_en |  | | | | | | |
| cali\_freq |  | | | | | | |
| cali\_mode |  | | | | | | |
| adc\_mode |  | | | | | | |
| **14** | **DCCalIntegrationTime** |  | | | | dc\_cal\_len | | | |
| **15** | **ZPCalIntegrationTime** |  | | | | zp\_cal\_len | | | |
| **16** | **CollisionIntegrationTime** |  | | | | collision\_len | | | |

## AFE (Analog Front End)

The AFE is comprised of 2 sub blocks, the TIA & the LNA, shown in Figure 3 including the following controls:

1. User adjustable gain: {1, 2, 4 … 32}
2. Coupling: AC/DC
3. Bandwidth limit
4. Ambient compensation DACs
5. TIA by pass

The details register/field assignments for these controls are shown in Table 3

1. AFE Block



1. AFE Control Registers

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **AFE** | | | | | | | | | | | | | | |
| **Addr** | **Name** | **7** | **6** | **5** | | **4** | | **3** | | **2** | | **1** | | **0** |
| **97** | **FrontendControl** |  | | | | afe\_pd\_dc | | afc\_lowcap\_mode | | lna\_gain | | afe\_gain | | |
|  | | afc\_pd\_dc | Disable AC coupling (25ua max operation) | | | | | | | | | | | |
| afc\_lowcap\_mode | Set to 1 for < 4pF @ pdp&pdn | | | | | | | | | | | |
| lna\_gain | increase by 3x | | | | | | | | | | | |
| afe\_gain | 0 | 0 | | 00: Gain=1 | | | | | | | | |
| 0 | 1 | | 01: Gain=2 | | | | | | | | |
| 1 | X | | 1X: Gain=4 | | | | | | | | |
| **98** | **AFEControlRegisters** | afe\_bypass | afe\_xtlk\_en | afe\_dac\_hi | | | | | | afe\_dac\_lo | | | | |
|  | | afe\_bypass | Disable TIA (use external) | | | | | | | | | | | |
| afe\_xtlk\_en | DC/AC coupling | | | | | | | | | | | |
| afe\_dac\_hi |  | | | | | | | | | | | |
| afe\_dac\_lo |  | | | | | | | | | | | |
| **E3** | **AmbientADC** | ambient[7:0] | | | | | | | | | | | | |
|  |  |  |  |  | |  | |  | |  | |  |  |

## Partial AGC (VGA) Block

The AGC does really cool things. It makes us happy.

1. vga1 @ FS ~5cm
2. vga2 @ FS ~50cm
3. VGA – Magnitude Relationship

vga1\*vga2\*magnitude ≈ K for vga2 < 0xFF

1. AGC Functional Block Diagram



1. AGC Block Control Registers



# System Behaviors

Describe interactions between controls.

## Ambient Rejection

Not very good, ≈2.5mm / 100 Lux (3.2kK)

1. Sand Tiger AR Curves



# Sequences

Algorithms occur here.

## Load time sequence

Description of register set load required to support minimal operation. Should be adequate for the simplest µC operation.

## Calibration sequence

From Steve Wickland…

## AGC Loop (including AFE)

The current implementation only varies the gain on the VGA with an RF peak detector limiting the range to about 50cm (Sand Tiger: 18% grey, ∞ size). A control loop is required to include the AFE gain adjust detailed in §3.1.

# References

1. Reference Data Files (available from Intersil (MLP) Intranet)

|  |  |
| --- | --- |
| §2 | [“Original” Register List: ISL29501\_Register\_Map.pdf](http://paris.mlp.intersil.com/cgi-bin/viewvc.cgi/ALS_%28ambient_light_sensors%29/ISL29501/Applications/ISL29501_Register_Map.pdf?view=co) |
| [501 TOF Register List](http://paris.mlp.intersil.com/cgi-bin/viewvc.cgi/ALS_%28ambient_light_sensors%29/ISL29501/Characterization/jgetchel/registerList.html?view=co) |
| §3 | [501 TOF Register Fields](http://paris.mlp.intersil.com/cgi-bin/viewvc.cgi/ALS_%28ambient_light_sensors%29/ISL29501/Characterization/jgetchel/registerFields.html?view=co) |
| [ISL29501 Number Formats](https://ishare2013.intersil.com/PL/Specialty/OpticalSensors/Optical%20Sensors%20Wiki/ISL29501%20Number%20Formats.aspx) |
| [Signed number representations](http://en.wikipedia.org/wiki/Signed_number_representations) |
| §3.3 | [ISL29501\_AGC\_Review.pdf](http://paris.mlp.intersil.com/cgi-bin/viewvc.cgi/ALS_%28ambient_light_sensors%29/ISL29501/Design/ISL29501%20Design%20Review%20Material/ISL29501_AGC_Review.pdf?view=co) |
| §3.1 | [AFE+VGA Block Diagram](http://paris.mlp.intersil.com/cgi-bin/viewvc.cgi/ALS_%28ambient_light_sensors%29/ISL29501/Characterization/jgetchel/AFE%2BVGA.jpg?view=co) |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |