

Lab 4 - Practice for ISA – Jacob Whitlow

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1. Assume that int array A has 10 elements and \$s1 register has the base address of A.
Write MIPS assembly code segment that swaps A[4] and A[9].

```
lw $t0, 16($s1) # copy from A[4]
lw $t1, 36($s1) # copy from A[9]
sw $t0, 36($s1) # store contents from A[4] in A[9]
sw $t1, 16($s1) # store contents from A[9] in A[4]
```

- For #2 and #3, consider the following register values (represented in Hex number):
\$s1 = A1B2C3D4
\$s2 = 5A6B7C8D
2. Show the contents of \$t1 and \$t2 after executing the following two consecutive instructions.
sar \$t1, \$s1, 3
slr \$t2, \$t1, 1

```
$s1 = 10100001101100101100001111010100
$s2 = 0101101001101010111110010001101
```

Shift operations:

```
sar $t1, $s1, 3 -> $t1 = 11110100001101100101100001111010
slr $t2, $t1, 1 -> $t2 = 01111010000110110010110000111101
```

```
$t1 = F436587A
$t2 = 7A1B2C3D
```

3. Assume that the following three consecutive instructions are executed.
sw \$s1, 4(\$zero)
sw \$s2, 8(\$zero)
lw \$s1, 6(\$zero)

Show the content of \$s1 in Hex number:
How many memory accesses are made?

```
sw $s1, 4($zero) -> zero[4] = A1B2C3D4 # aligned so one mem access
sw $s2, 8($zero) -> zero[8] = 5A6B7C8D # aligned so one mem access
lw $s1, 6($zero) -> $s1 = C3D45A6B # misaligned so two mem access
```

Four memory accesses are made

4. Consider the following MIPS assembly code segment for implementing a while loop.
- | | |
|-----------------------------|--|
| Start: add \$t1, \$s2, \$s1 | instruction type: _____ addressing mode: _____ |
| lw \$t0, 4(\$t1) | instruction type: _____ addressing mode: _____ |
| bne \$t0, \$s5, End | instruction type: _____ addressing mode: _____ |
| addi \$s1, \$s1, 2 | instruction type: _____ addressing mode: _____ |
| subi \$s1, \$s1, 1 | instruction type: _____ addressing mode: _____ |
| j Start | instruction type: _____ addressing mode: _____ |
| End: | |
- (a) Specify the instruction type and addressing mode used in each instruction above.
(b) Write MIPS machine code for the 2nd instruction (lw) in Hex number.
Opcode for lw is 35 in decimal; register numbers for \$t0 and \$t1 are 8 and 9 in decimal, respectively.
(c) Write MIPS machine code for the 3rd instruction (bne) in Hex number.
Opcode for bne is 5 in decimal; register number for \$s5 is 21 in decimal.

a)

Instruction	Instruction Type	Addressing Mode
add \$t1, \$s2, \$s1	r type	register
lw \$t0, 4(\$t1)	i type	base
bne \$t0, \$s5, End	i type	pc-relative
addi \$s1, \$s1, 2	i type	immediate
subi \$s1, \$s1, 1	i type	immediate
j Start	j type	pseudo-direct

b)

Opcode (lw)	rs (\$t1)	rt (\$t0)	offset
100011	01001	01000	0000000000000100

Machine code = 8D280004

c)

Opcode (bne)	rs (\$t0)	rt (\$s5)	offset
000101	01000	10101	0000000000000011

Machine code = 15150003

5. Explain clearly the addressing mode used in the jump (e.g., j Loop) instruction.
You should explain clearly the PC updating process.

In pseudo direct addressing mode a specific address in memory is being jumped to that is not dependent on the current address of the jump instruction. The given 26-bit word address is shifted left 2 bits, causing 2 bits 00 to be appended onto the right side of it. This makes the word address become a 28-bit byte address. The remaining 4 bits at the front of the target address are populated by the 4 bits of the address of the instruction which comes immediately after the jump instruction.