EEC 180: Digital Systems II

Winter Quarter 2025
Department of Electrical & Computer Engineering
University of California, Davis

Units: 5 (3 Lecture/2 Laboratory)
Prerequisite: EEC 18 or EEC 180A
Catalog Description: Computer-aided design of digital systems with emphasis on hardware description languages, logic synthesis, and field-programmable gate arrays (FPGA). May cover advanced topics in digital system design such as static timing analysis, pipelining, memory system design, and testing digital circuits.

Educational Objectives:

1) The students will be able to:
   a) Describe combinational and sequential logic in Verilog
   b) Describe a design using behavioral and structural code
   c) Develop testbenches to verify correctness of designs
   d) Design and verify complex designs using Verilog and CAD tools
   e) Design complex systems using FPGAs
2) Students who have completed this course should have achieved:
   a) Student Outcome 1: an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
   b) Student Outcome 2: an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.
   c) Student Outcome 6: an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

General Announcements

1. Please monitor CANVAS regularly for announcements, solutions, homework, lecture notes etc.
2. Microsoft Teams (https://www.microsoft.com/en-us/microsoft-teams/download-app) will be used for communication and interaction in the class.
3. Use t6ixiyo to join Teams.
4. You will be reported to **SJA** if you violate the UC Davis academic code of conduct. Review here https://ossja.ucdavis.edu/code-academic-conduct

Teaching Staff

Name	Email	Lab / Office Hours
Venkatesh Akella	akella@ucdavis.edu	Wednesday 11:00AM – 12:00PM (2117 Kemper)
Najmeh Bavarsad (TA)	nnazari@ucdavis.edu	Wednesday 9AM – 1PM
Daniel Chevy (TA)	dachevy@ucdavis.edu	Wednesday 1PM – 5PM
Alireza Zeraatkar (TA)	abolhasani@ucdavis.edu	Thursday 1PM – 5PM
Rijuta Ravichandran	rravicha@ucdavis.edu	Reader
Kushagra Tiwari (ULA)	ktiwari@ucdavis.edu	Wednesday 9AM – 1PM
Fatima Sheikh (ULA)	fzshaik@ucdavis.edu	Wednesday 1PM – 5PM
Zhenyi Lu (ULA)	ryalu@ucdavis.edu	Thursday 1PM – 5PM

Textbook

Digital Design: A Systems Approach
William James Dally (Author), R. Curtis Harting (Author)
Cambridge University Press; Illustrated edition (September 17, 2012)
Publisher: Cambridge University Press ISBN-13: 978-0521199506

Laboratory Guidelines

You will work in a two-person team. Both the partners should be from the same lab section. Each partner describes the contribution to the lab in the lab report. Your individual grade for a lab will depend on your contribution to the project.

Hardware for the Lab

The Terasic webpage for the DE10-Lite board contains links to information and resources for the board.
http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=218&No=1021&PartNo=4

Laboratory Schedule (Tentative) Always check the lab handout for the actual due date

Lab	Description	When?	Points
1	Lab1 – Modelsim and Quartus Tutorial Objective: Getting Familiar with The Tools and Design Flow	Week of Jan 6	100
2	Lab2 - Adders and Multipliers Objective: Structural Verilog and Hierarchical Description in Verilog and Testbenches	Week of Jan 13	100
3	Lab 3 – Leading Zero Detector Objective: Combinational Logic Design	Week of Jan 20	100
4	Lab 4 - Sequence Detector Objective - Sequential Logic Design	Week of Jan 27	100
5	Lab 5 – Sequential System Design and RAM Objective: Memory. Datapath and State Machine Extraction	Week of Feb 3 Week of Feb 10	200
6	Lab 6 – Matrix Multiplication in Hardware Project Milestone 1 (Design and Simulation) Project Milestone 2 (HW Implementation)	 Week of Feb 17 Week of Feb 24	 100 100
	Project Milestone 3 (Demo and Optimization)	Week of Mar 4	100
	Extra Credit	Week of Mar 10	100

When is the lab due and what is the late penalty?

Labs must be completed (which involves getting a signature from the TA) and the lab report is due at the beginning of the lab period in the week following the due date of the lab.

You can complete the lab one week late with a late penalty of 25%.

A **lab report** consists of the following:

1. Pre-lab signed by the TA.
2. A brief description of your design, highlighting any special problems that you encountered, design decisions that you took, and the assumptions in your design.
3. Answers to the questions in the laboratory description handout, if any.
4. Verification sheet signed by the TA.
5. Statement of contribution of each team member.
6. Anything else your TA wants.

Exams

Midterm	Thursday, Feb 13 @ 10 AM
Final Exam	Thursday March 20 @ 8 AM

Grading

Laboratory	45%
Midterm Exam	20%
Homework	10%
Final	25%

Tentative Lecture Plan

(Chapters Refer to Chapters from the Textbook)

When?	Topic	Reading Assignment
Week 1	Combinational and Sequential Logic Design. Boolean Algebra	Chapter 1, Chapter 2, Chapter 11.1 and Chapter 11.2 (Review Material from EEC18)
Week 2, Week 3, and Week 4	Modeling and Simulation of Combinational and Sequential Logic in Verilog	Moorby-Thomas Book, Chapter 2, Chapter 7, Appendix A, Verilog Coding Guidelines
Week 5 Week 6	CMOS Implementation of Digital Circuits	Chapter 4 and Chapter 5
Week 7	Programmable Logic, FPGA	Chapter 8
Week 8	Sequential Logic and Timing Analysis	Chapter 15, Chapter 16
Week 9 Week 10	Pipelining, Digital System Design and Optimization, Asynchronous Inputs	Chapter 23