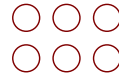
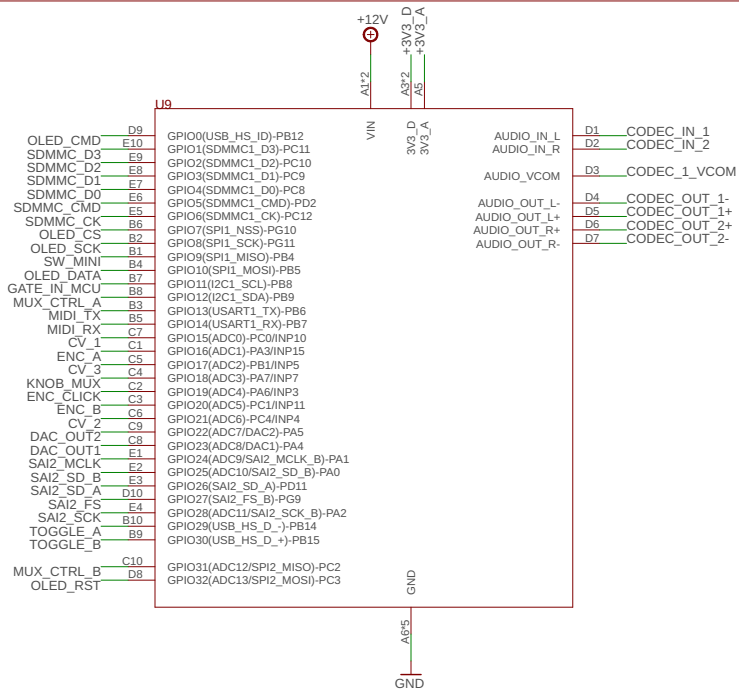
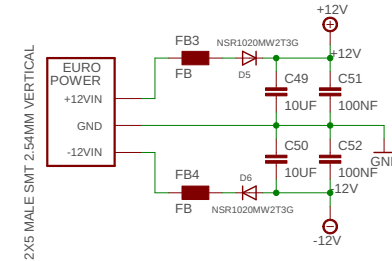


Seed 2 DFM

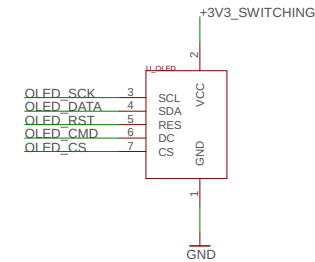


open hardware

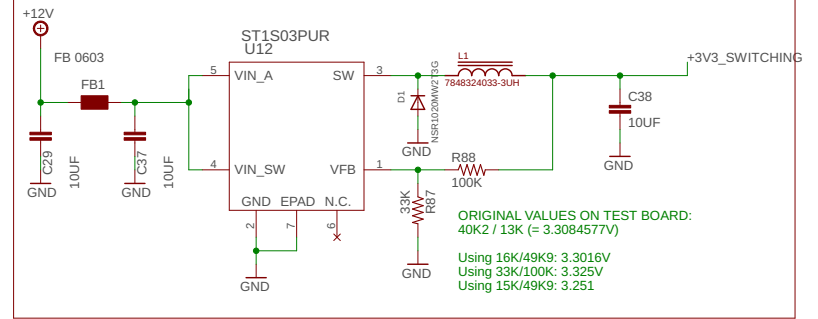
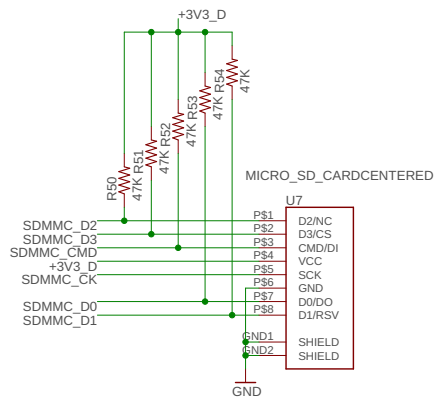
Power Input



OLED



SD Card Slot



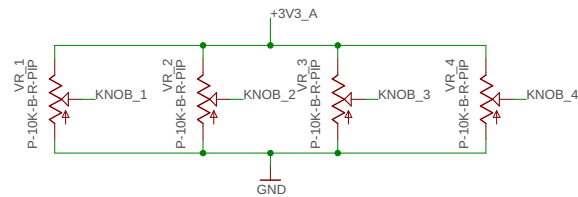
Daisy Seed

ES_Daisy_Seed2_DFM_EVAL_EURO_Rev2

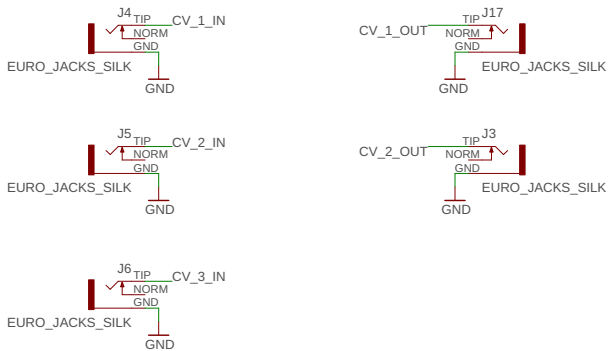
3/28/2023 3:53 PM

Sheet: 1/5

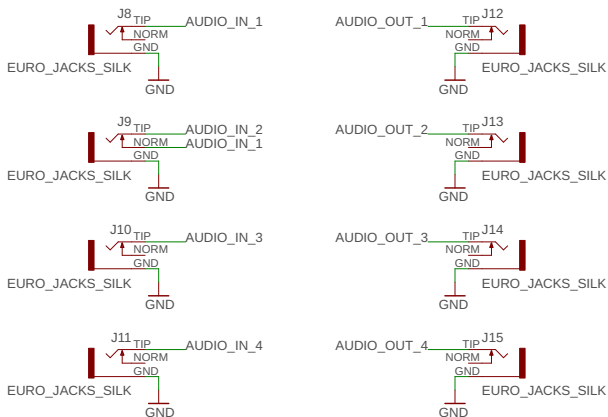
Knobs



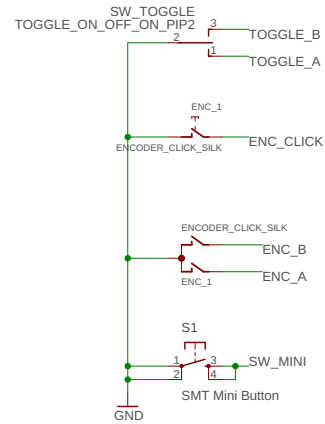
CV I/O



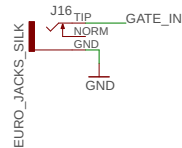
Audio I/O



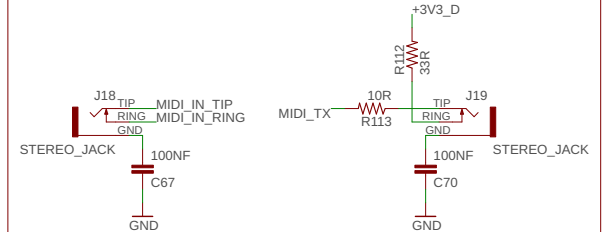
Switches



Gate Input

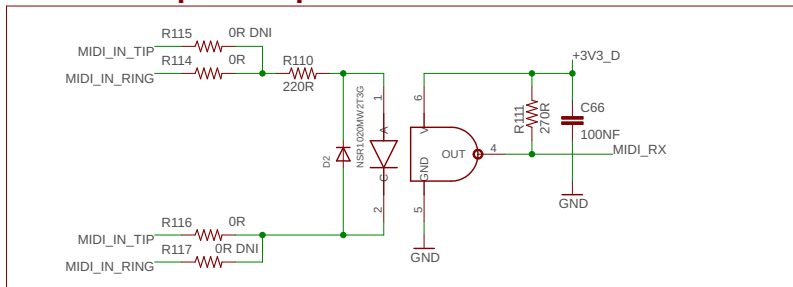


MIDI I/O

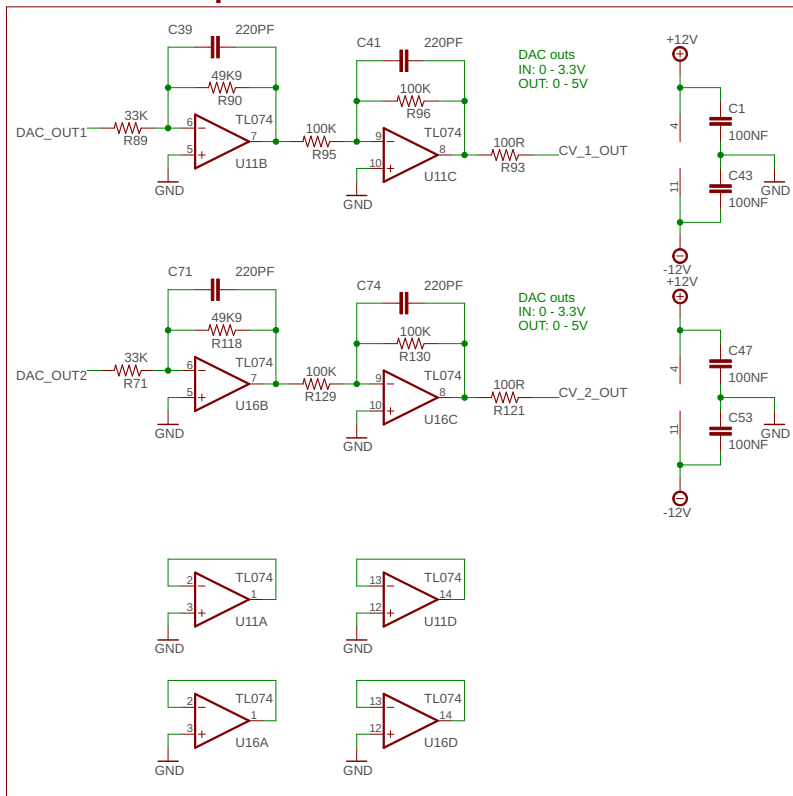


Interface	
ES_Daisy_Seed2_DFM_EVAL_EURO_Rev2	
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Sheet: 2/5	

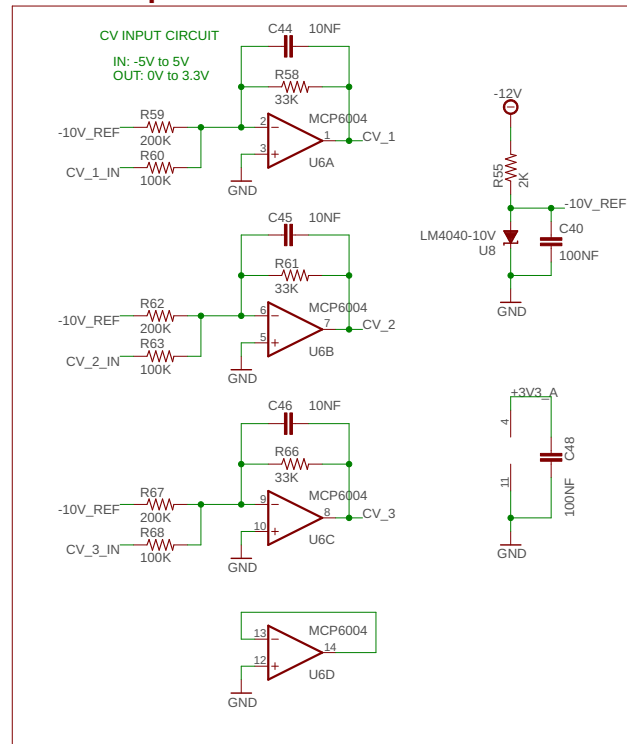
MIDI Input Opto-Isolator



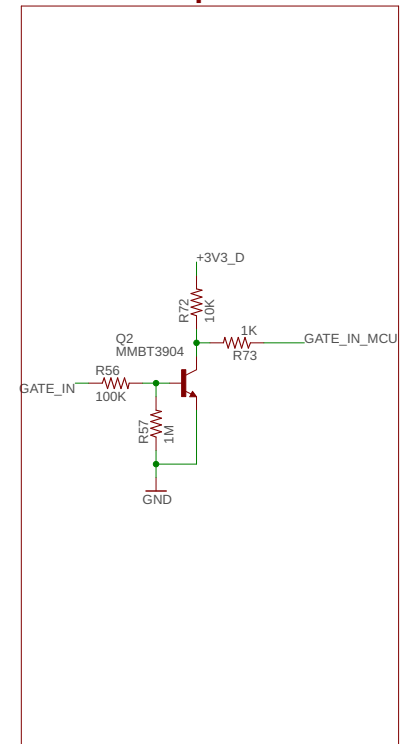
DAC Output



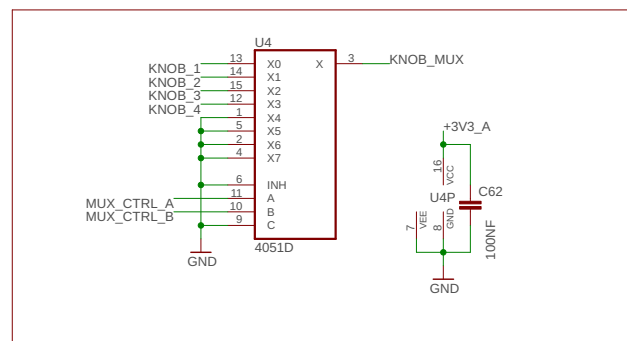
CV Input



Gate Input



Potentiometer MUX



MODE Pin:
VDD - SPI Mode
VDD via 220K pullup - H/W Mode,
single-ended VoutX.
GND via 220K pulldown - H/W Mode,
differential VoutX.
GND - I2C Mode

PCM3060

VDD 3vyp input
DGND 8vyp diff output

VCC
AGND2
AGND1
SGND
ZEROL
ZEROR
VCOM
VINL
VINR
VOUTL+
VOUTL-
VOUTR+
VOUTR-

CODEC_IN_3
CODEC_IN_4
CODEC_OUT_3+
CODEC_OUT_3-
CODEC_OUT_4+
CODEC_OUT_4-

SAI2_SD_B
SAI2_FS
SAI2_SCK
SAI2_MCLK
SAI2_MCLK
SAI2_SCK
SAI2_FS
SAI2_SD_A

DOUT_ADC
LRCK1_ADC
BCK1_ADC
SCK1_ADC
SCK12_DAC
LRCK2_DAC
BCK2_DAC
DIN_DAC

CTRL_1
SCL
SDA

+3V3_D
+5V
GND

The diagram shows a two-stage voltage divider circuit. The first stage consists of a 12V source connected to a series combination of a 100nF capacitor (C58) and a 100nF resistor (FB2). The output of this divider is connected to the input (IN) of a 5V voltage regulator (U14, LD1117-5V). The regulator's output (OUT) is connected to a second stage consisting of a 100nF resistor (FB5) in series with a 10uF capacitor (C57). The output of this second stage is connected to a 10uF capacitor (C60) and is also the final output of the circuit. The ground pin (GND) of the regulator is connected to a common ground.

CODEC Input

