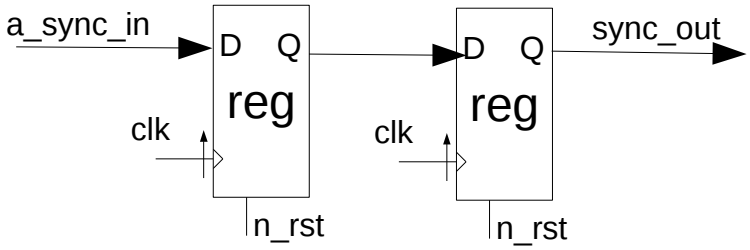
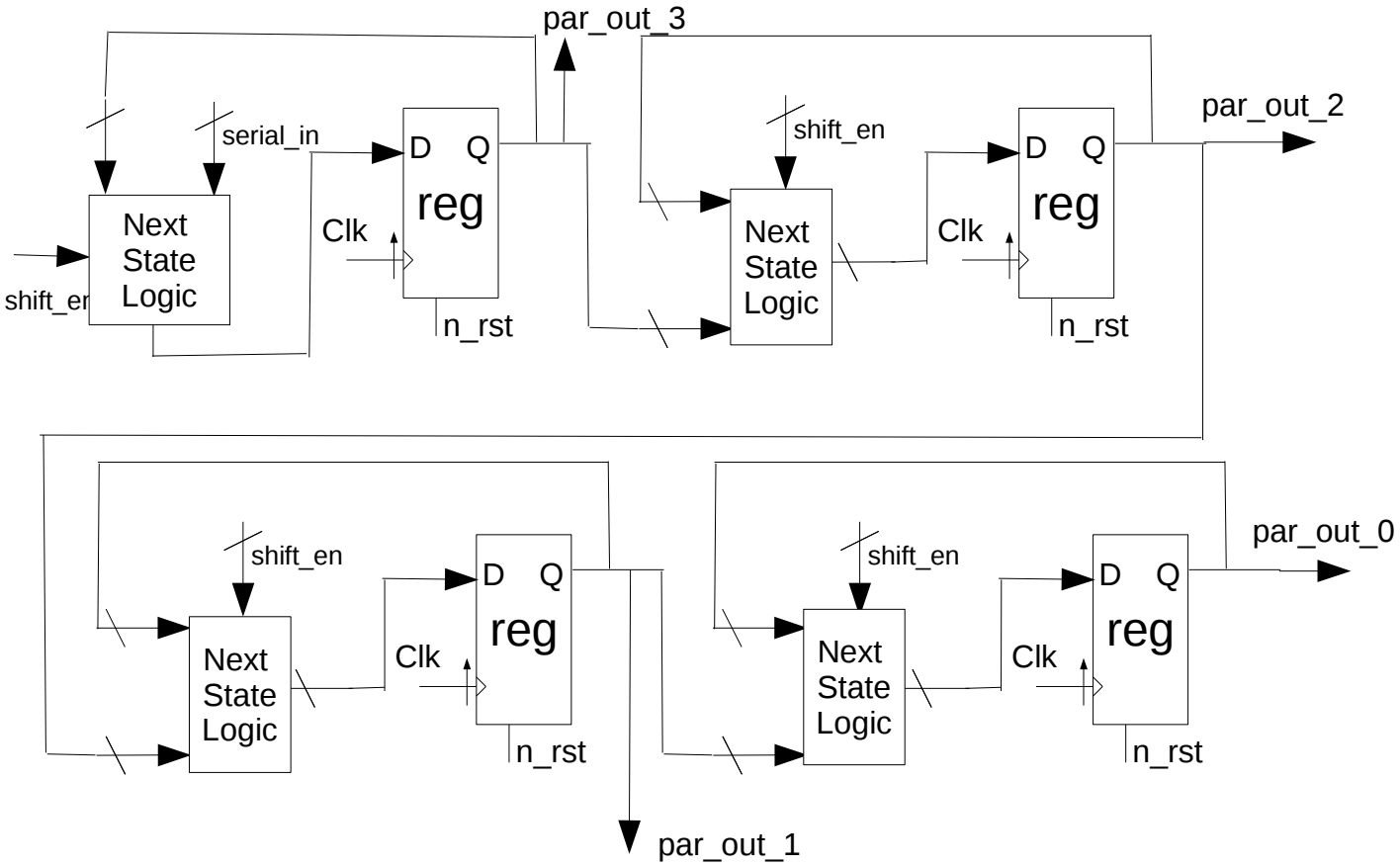
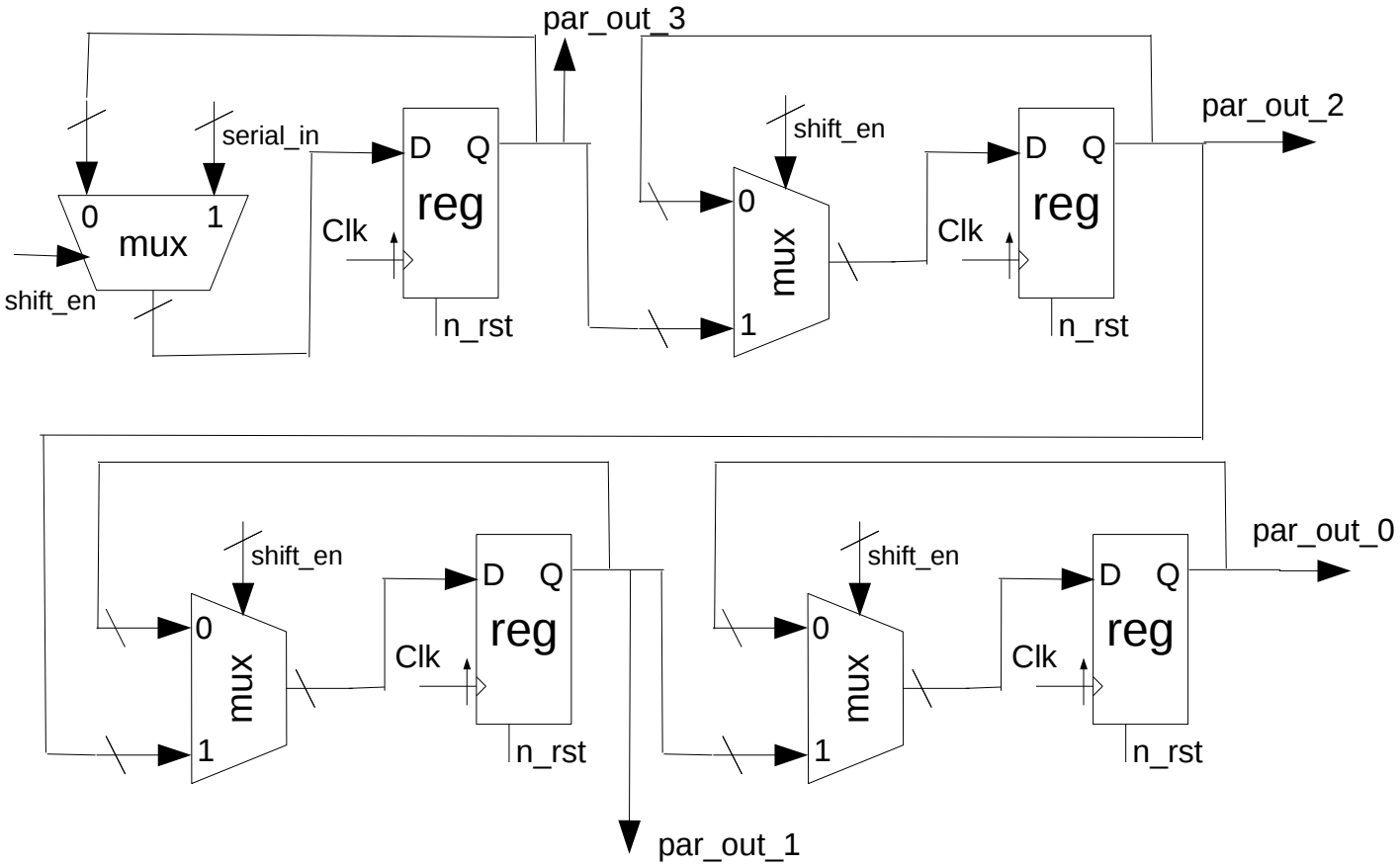
7.3 Schematic diagram of a 2 Flip-Flop synchronizer



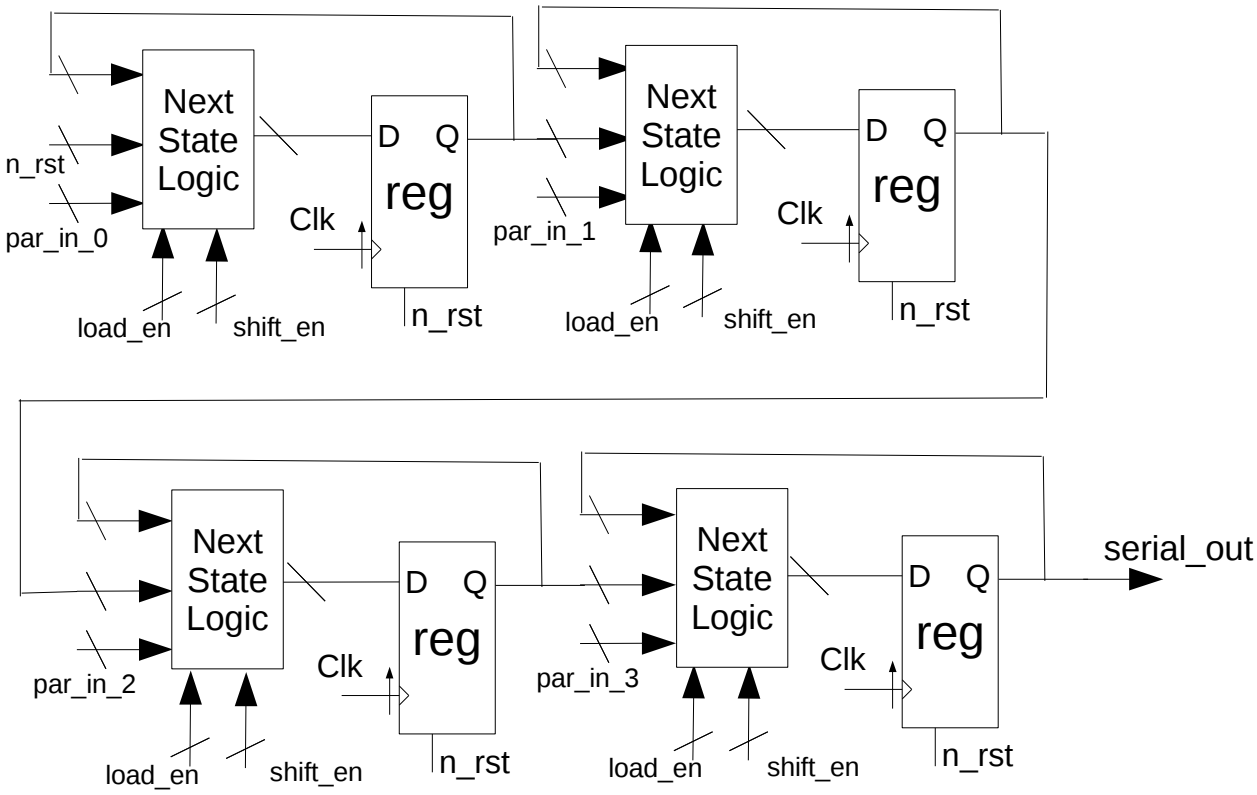
RTL diagram for most significant bit first serial-to-parallel shift register



RTL diagram for most significant bit first serial to parallel shift register



RTL diagram for most significant bit first parallel-to-serial shift register



Schematic diagram for most significant bit first parallel-to-serial shift register