Functional Block Diagram for Timer Block

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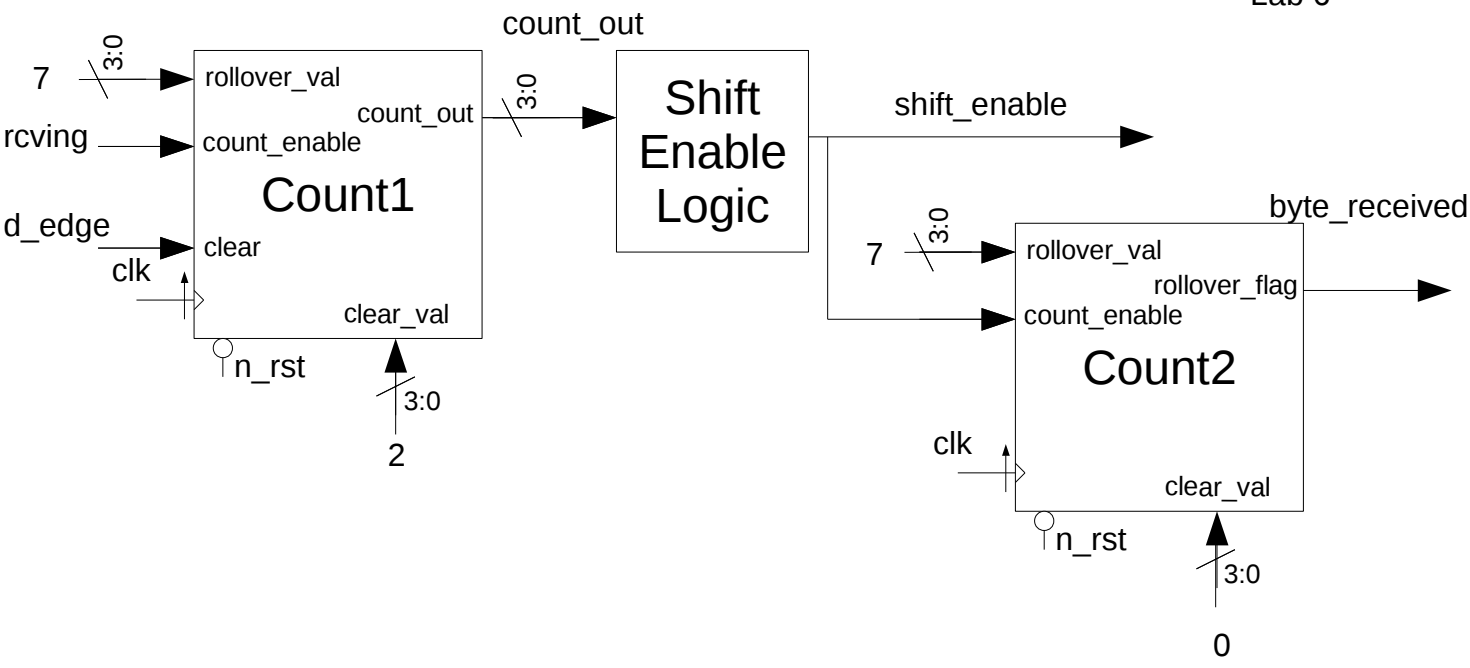
ECE 337
Section 4
Lab 6



Flex Counter:

The flex counter is modified to accept a new input, clear_val. When clear is asserted, count out = clear_val. This enables one counter to handle the cycle where no clear is invoked, and a delay of 8 cycles is needed as well as the situation where d_edge is triggered, resynchronizing the count to the data clock, which requires an initial delay of 6 cycles (see timing diagram).

Shift Enable Logic:

If cnt_out == 4, shift_enable = 1, else shift_enable = 0.