RTL Diagram for Timing Controller

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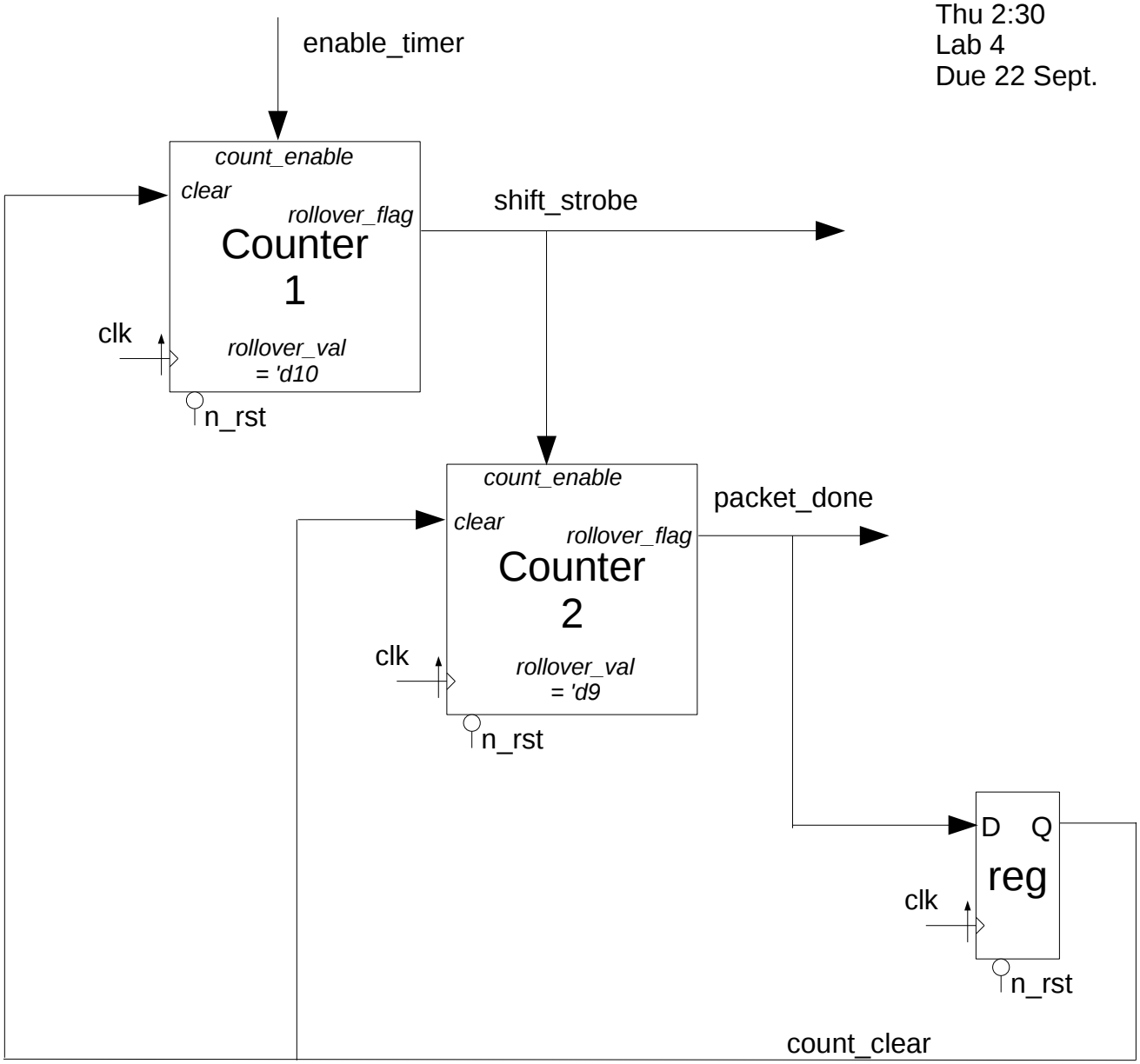
ECE337
Section 4
Thu 2:30
Lab 4
Due 22 Sept.



Counter 1 counts 10 individual 400 MHz clock pulses, then asserts its rollover flag for 1 clock pulse width. The rollover flag is output as the one clock pulse width shift_strobe signal.

Counter 2 is enabled to count by the 1 clock pulse width rollover flag from counter 1, counting up by 1 for each pulse. Once it has counted 9 rollovers from counter 1, it outputs its one clock pulse width rollover flag. This flag is output as the packet_done signal to the RCU, causing it to deassert enable_timer, which stops counter 1 from counting.

The packet_done signal is also clocked into a flip-flop and sent to the clear inputs of the counters. Using a flip-flop introduces a 1 clock pulse width delay that will ensure at the clear signal is received in the same cycle as enable_timer is deasserted. Without the flip-flop, counter 1 would receive the clear signal before it had been disabled and might have stopped at count = 1.