```
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```

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Boruss® CPU Architecture Software Developer's Manual

Volume:

1

NOTE: This document contains Boruss® CPU Architecture Software Developer's Manual.

October 2024

The Boruss CPU Architecture Software Developer's Manual, Volume 1 describes the architecture and programming environment of Boruss® CPU architecture processor.

1.1 BORUSS® CPU PROCESSORS COVERED IN THIS MANUAL
- BorussCPU "Laibach"

1.2 OVERVIEW OF VOLUME 1: BASIC ARCHITECTURE

A description of this manual's content follows:

Chapter 1 – About This Manual. Gives an overview of the BorussCPU.

Chapter 2 - Boruss® Architecture. Introduces the Boruss CPU architecture and gives overview of the features.

Chapter 3 – Basic Execution Environment. Introduces the model of memory organization and describes the register set used by applications.

Chapter 4 – Instruction Set Summary. List all BorussCPU instructions

1.3 NOTATIONAL CONVENTION

This manual uses typical notation described below.

1.3.1 Bit and Byte Order

- **Bit order** (in byte) specifies how bits are arranged within a single byte
    - **MSB** (Most Significant Bit) leftmost bit is the most significant (bit 7)
    - **LSB** (Least Significant Bit first) leftmost bit is the least significant (bit 0)

```
MSB0:  b7 b6 b5 b4 b3 b2 b1 b0   (bits numbered 7 down to 0, left to right)
LSB0:  b0 b1 b2 b3 b4 b5 b6 b7   (bits numbered 0 up to 7, left to right)
       |------------8 bits-----------|
```

- **Byte Order** (Endianness)
    - **Big-endian:** Most significant byte first (higher address = less significant)
    - **Little-endian:** Least significant byte first (lower address = less significant)

```
Memory addresses:    0      1      2      3
Big-endian:         [0x12] [0x34] [0x56] [0x78]
Little-endian:      [0x78] [0x56] [0x34] [0x12]
```

Notices & Disclaimers

Boruss CPU technology require use hardware