Hardware Opportunities in the Machine Learning Lifecycle

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Get the latest slides and links to literature

https://tinyurl.com/isscc-lifecycle

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About Me

- Co-director of the RISE Lab
- Co-founder of Turi Inc.
- Member of the Apache Spark PMC
- Research
  - Artificial Intelligence
  - Data Science
  - Distributed Data Systems
  - Graph Processing Systems
- I don't study processor **architecture**
  - But I probably should …

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Outline

- History and the **Co-evolution** of Hardware and AI
- The **Feedback Cycle** driving the 3rd wave of AI
- Machine Learning is **not a single workload**
  - Stages of the **Machine Learning Lifecycle**
- **Security** is the key to better accuracy

Along the way, I will talk about some of the research in my group addressing interesting aspects of the lifecycle.

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Hardware and the History of AI

- **1950 to 1974:** *Birth of AI*
  - 1951 Marvin Minsky builds first **neural network hardware** (SNARC)
- **1974 to 1980:** *First AI Winter*
  - Limited **processing power** and **data**
- **1980 to 1987:** *Second Wave of AI*
  - XCON (AI for **hardware configuration**) for DEC → boom in AI hardware companies
- **1987 to 1993:** *Second AI Winter*
  - Collapse of the **AI Hardware Market**
- **1993 to 2011:** *AI → Machine Learning*
  - *Confluence of ideas + **Compute** + **Big Data** → AI starts to really work*
- **2011 to 2019:** *Third Wave (Deep Learning)*
  - ***Compute** + **data** + **abstractions** → feedback cycle*

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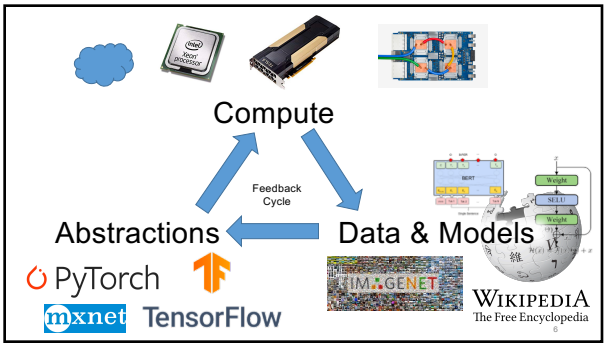

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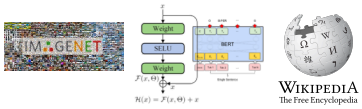
Data & Models



Narrow Waste

Abstractions

PyTorch TensorFlow mxnet

Compute

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Abstractions are Enabling Innovation

- Much of machine learning before 2010:
  - Research focused on machine learning **algorithms**
  - Programs written using **high-level imperative languages**
    - Matlab/R/C++/Java
  - **Big abstractions:** linear algebra, map-reduce, graph systems
- Today:
  - Research focused on **model design**
  - **Models** written in high-level **DSLs**
    - TensorFlow/Pytorch
  - Big abstractions: **tensor operations**, **loss minimization,** linear algebra, …
- Models written in **TensorFlow** can now run on **hardware** that didn't exist when the models were created.

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How do we make **hardware** for Machine learning?

Machine learning is not a single application.

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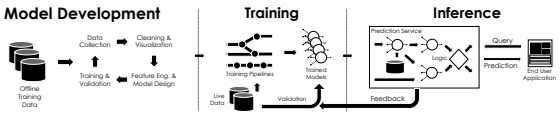
Machine learning is

multiple applications** with **different requirements.



Machine Learning Lifecycle

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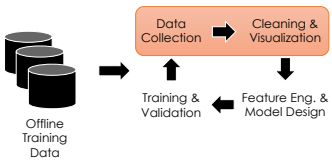
Model Development



Identifying potential sources of data

Joining data from multiple sources

Addressing **missing values** and **outliers**

Plotting trends to identify **anomalies**

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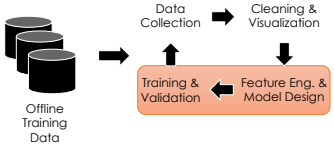
Model Development



Building informative **features functions**

Designing new **model architectures**

Tuning training algos.

Validating prediction accuracy

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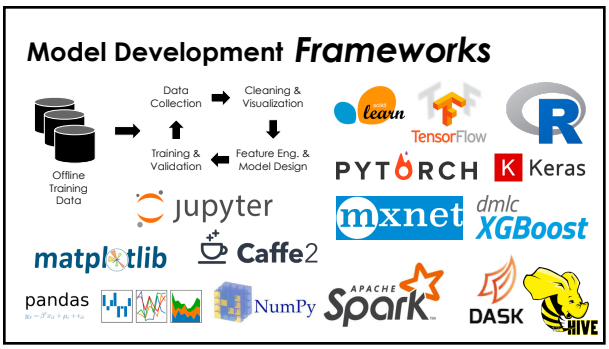

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Model Development → Hardware

- Need to test **multiple designs and hyperparameters** quickly
  - May be better to run many parallel experiments than one experiment faster
- **Debug heavy** → sources of error → data, hyperparams., & model
  - **System should not be a source of error**
  - **Avoid** cutting corners (e.g., quantization, async) for increased performance
    - Unless you can make a case for stable convergence …
- **Data preparation** is often a bottleneck
  - Opportunity for **data tooling** (esp. video)
  - Accelerate data transformation and augmentation
- Emerging Trends
  - **Attention Models** and **Graph Neural Networks**: reduced locality, sparsity
  - **Dynamic Networks**: gating, cascades, mixtures, …
  - Increased emphasis on **DNN features** and **Fine-Tuning**
    - Reuse of common architectures and weights

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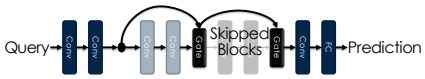
Dynamic Networks for **fast** and **accurate** inference

IDK Cascades: Using the fastest model possible [UAI'18]

SkipNet: dynamic execution within a model [ECCV'18]



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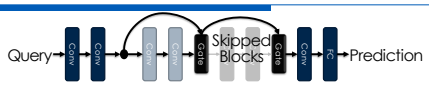
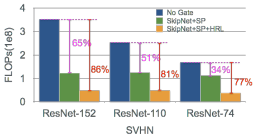
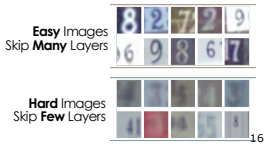
SkipNet: dynamic execution within a model [ECCV'18]



Large Reductions in FLOPS



Skip more layers on clear images



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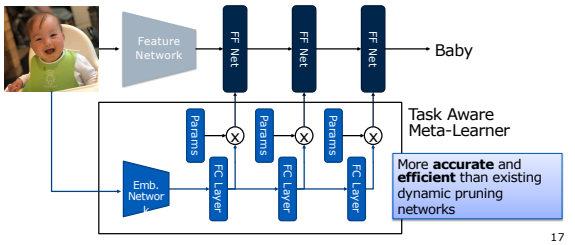
Task Aware Feature Embeddings [CVPR'19]



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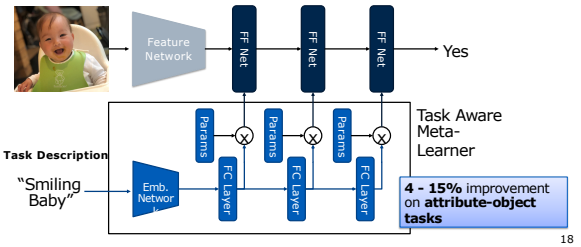
Task Aware Feature Embeddings [CVPR'19]



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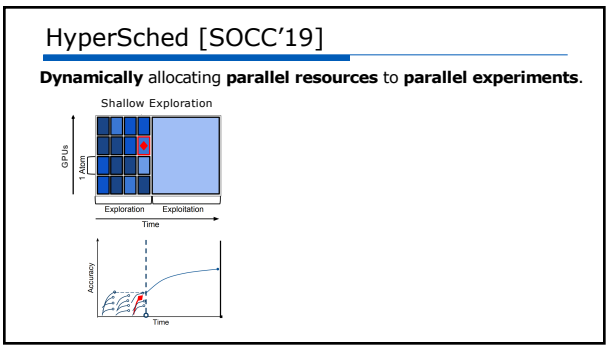

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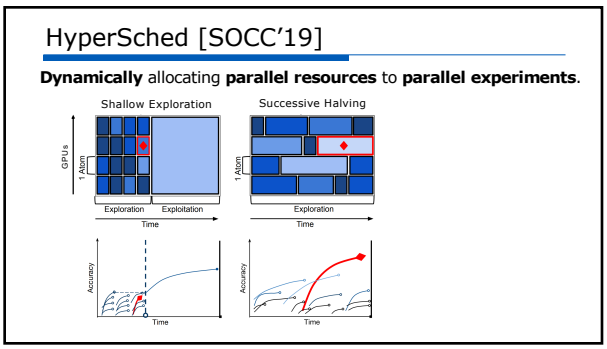

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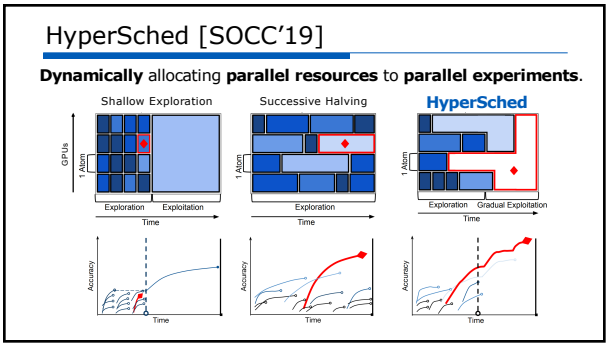

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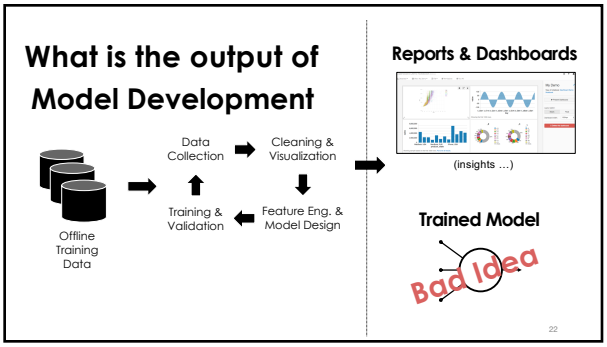

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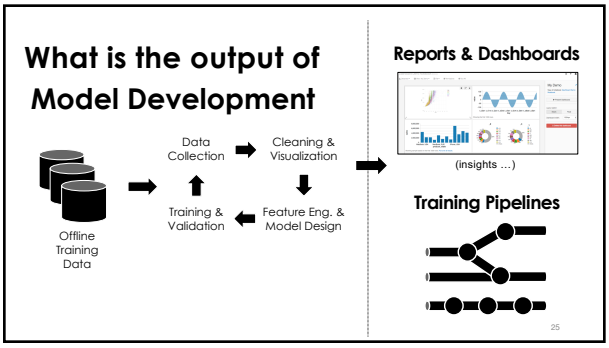

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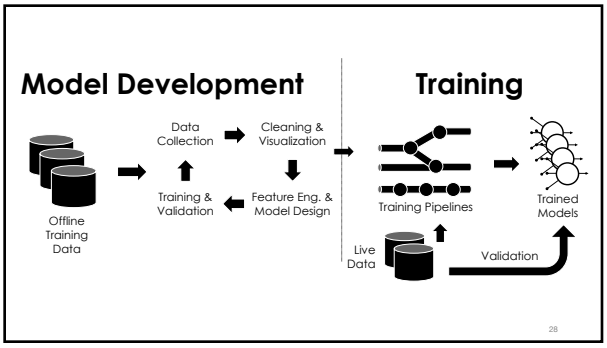

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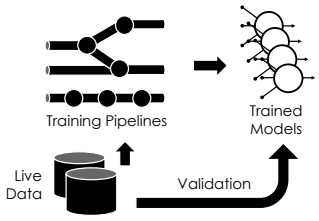
Training



Training models **at scale** on **live data**

Retraining on new data

Automatically **validate** prediction accuracy

Manage model **versioning**

Requires **minimal expertise** in machine learning

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Training *Systems*

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Model Training → Hardware

- Fewer models to train → need **distributed training** of **individual models**
  - Often training with **more data**
- **Larger models** and **mini-batch sizes**
  - Need larger on-device memory
  - Counter trends → reversable networks, **optimal checkpointing**, …
- Models and hyperparameters are vetted → focus on **system optimizations**
  - Can **tolerate** some **system error** (quantization and async.)
  - Need adequate stability to meet deadlines
- **Data preparation** is still potentially an issue (as with model dev.)
- Need to deal with **composition** of multiple models

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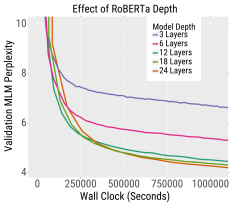
Do Bigger Models Train Faster?

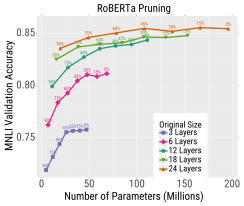
(Preliminary unpublished work.)

- Studying **pre-training** of large **Transformer Models** for NLP task (e.g., BERT)

Deeper Models **Reduce Error Faster**



More Resilient to **Lossy Compression**



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CheckMate [MLSys 2020]

Scaling deep learning training beyond the GPU memory wall.

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Problem:

How do we train models both efficiently and beyond memory limits?

At a per-GPU level, recent state-of-the-art models have hit a memory capacity wall.

Memory is slowing progress in new deep learning models!

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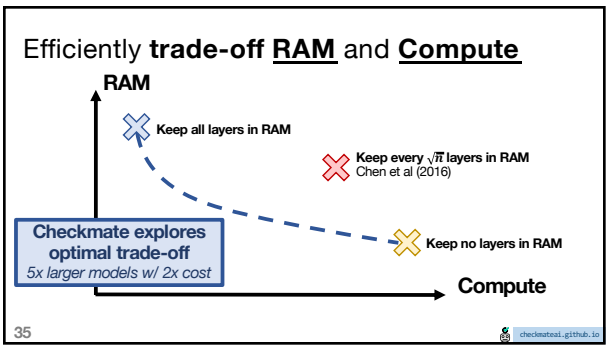

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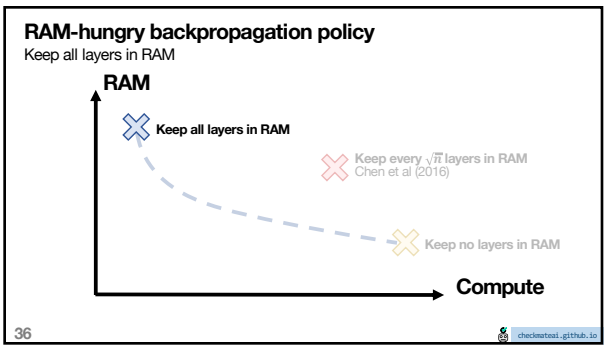

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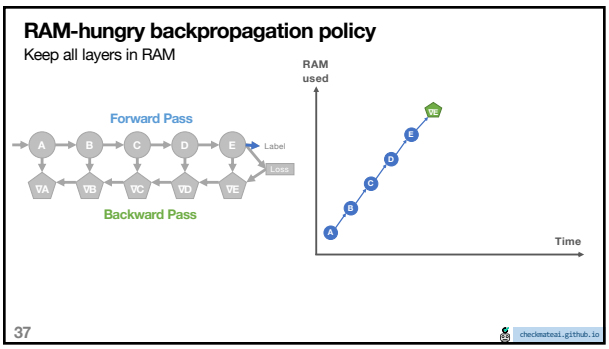

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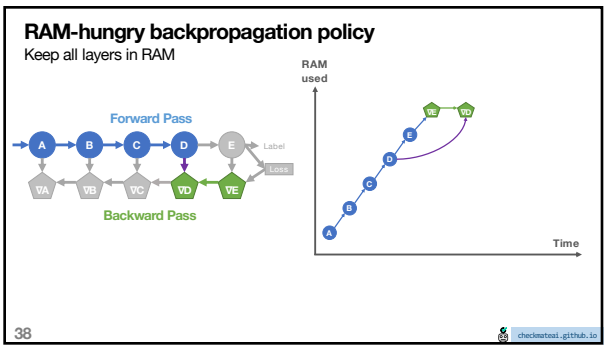

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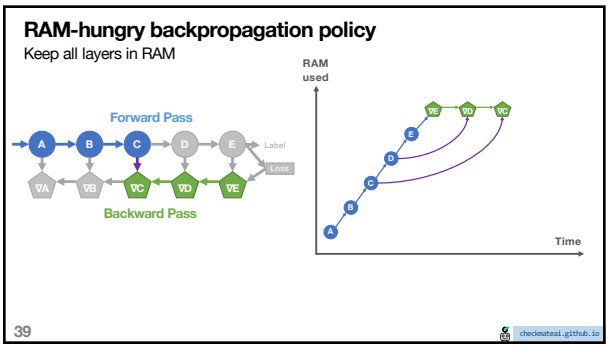

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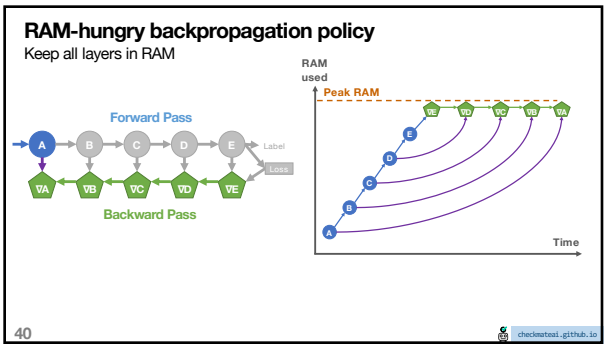

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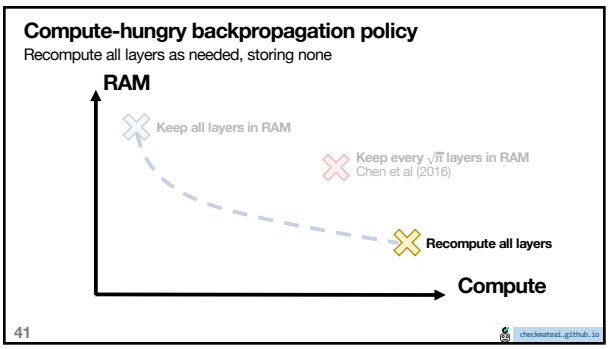

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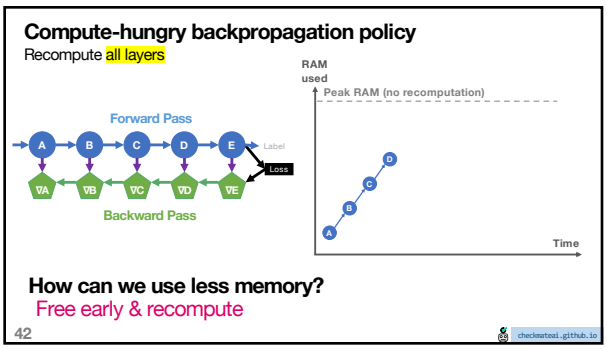

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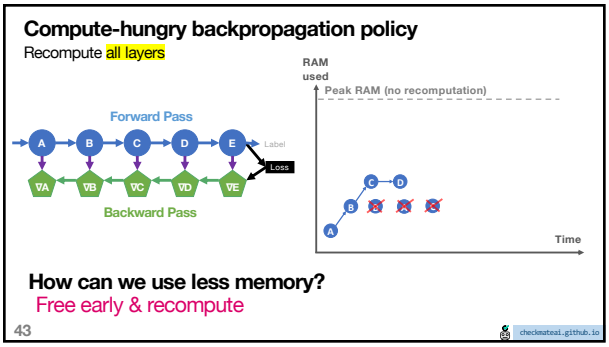

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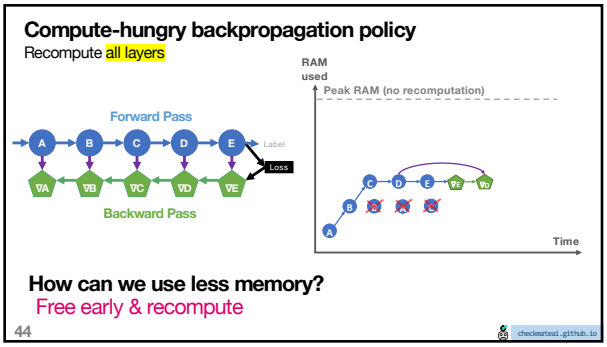

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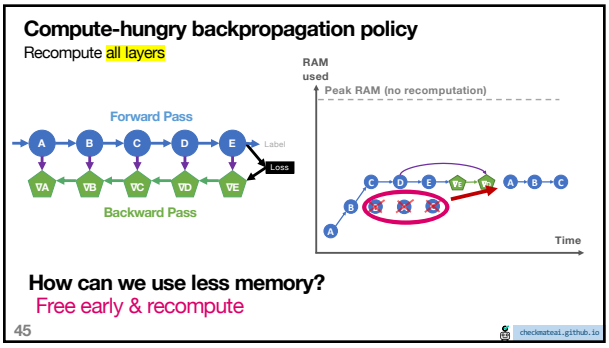

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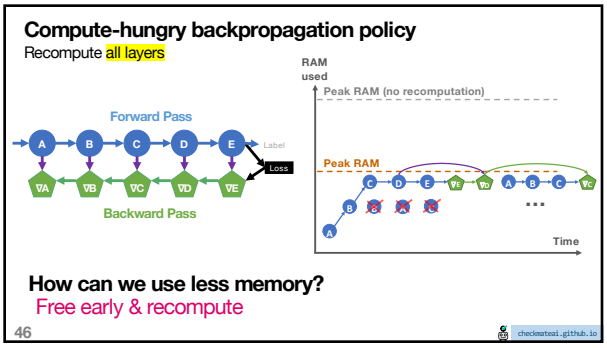

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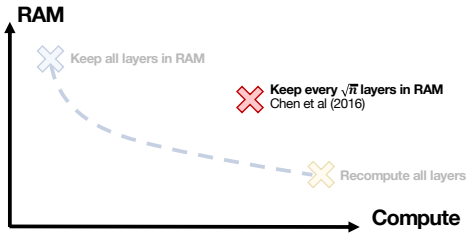
Prior heuristic as an intermediate trade-off point



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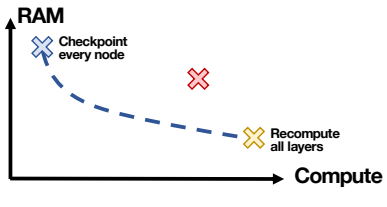
How to trade-off RAM for compute optimally?

Challenges:

1. Variable runtime per layer
2. Variable RAM usage per layer
3. Real DNNs are non-linear



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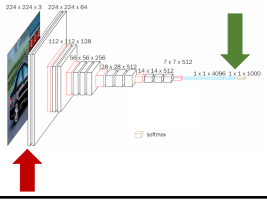
Why do fixed heuristics perform poorly?

1. Latency is not constant between layers

10^6x compute gap between biggest and smallest layer in VGG19



x10^6

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Why do fixed heuristics perform poorly?

2. Tensors are not all the same size

DenseNet-201 has large variability in activation sizes between layers

x10^3

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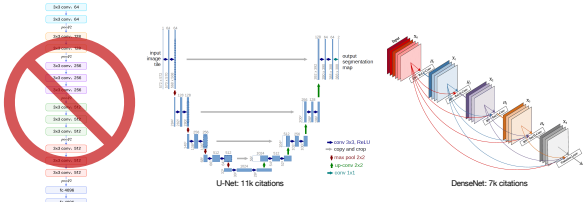
Why do fixed heuristics perform poorly?

3. Real DNN architectures are non-linear



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Checkmate

A system for optimal tensor rematerialization

- Statically optimize graph once (10s to 1hr)
- Train optimized graph for weeks
- Checkmate composed of 3 parts:
  - Profiling: hardware/RAM aware schedules
  - Integer LP: enables finding optimal schedule
  - TF2.0 graph pass: support TPU, GPU, CPU

Profile layers

↓

Solve integer LP

↓

Rewrite TF2.0 graph

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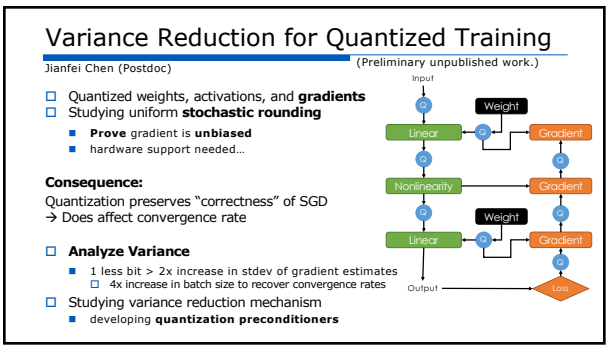

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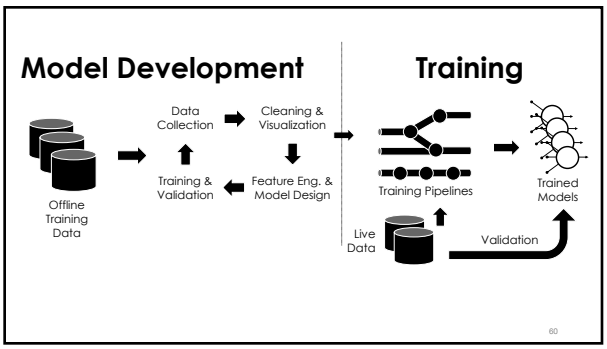

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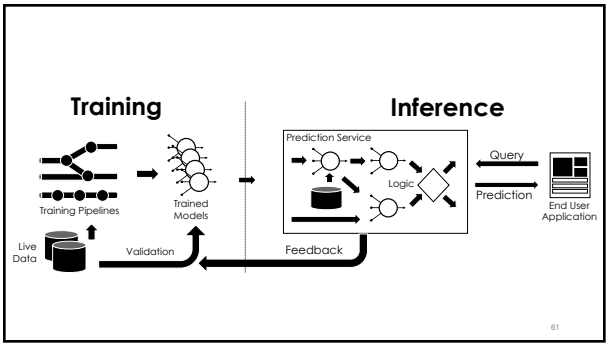

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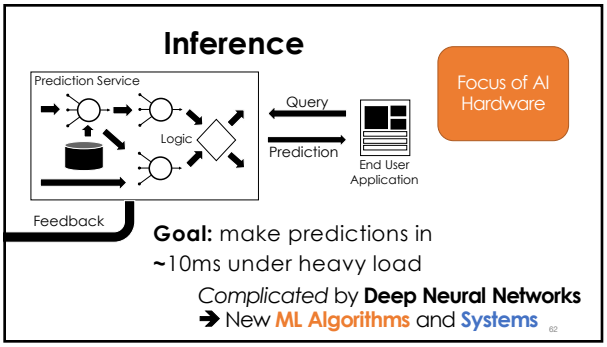

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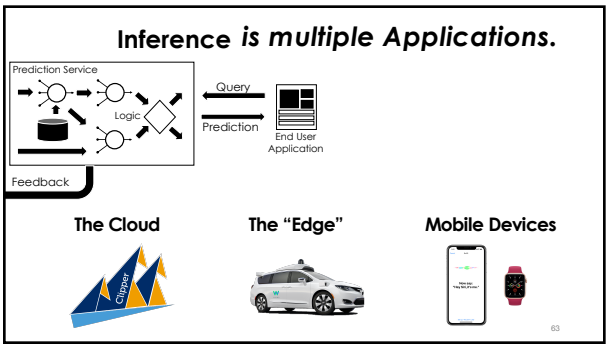

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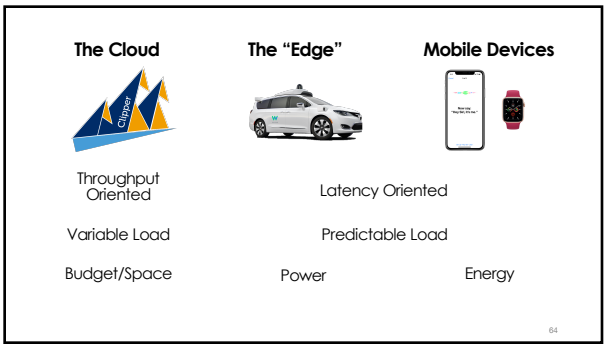

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Basic Linear Models (Often High Dimensional)

- Common for **click prediction** and **text filter models** (spam)
- Query x encoded in sparse Bag-of-Words:
  - x = "The quick brown" = {("brown", 1), ("the", 1), ("quick", 1)}
- Rendering a prediction: $\mathbf{Predict}(x) = \sigma\left(\sum_{(w,c)\in x} \theta_w c\right)$
- θ is a large vector of weights for each possible word
  - or word combination (n-gram models) …
- Focus on fast weight retrieval

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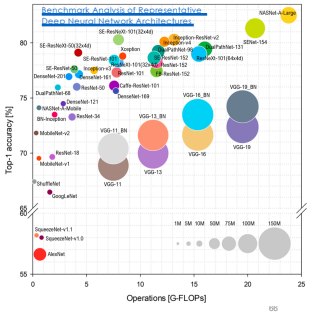
Inference in Deep Learning Models

- **Compute intensive**
- **Less memory intensive** than training



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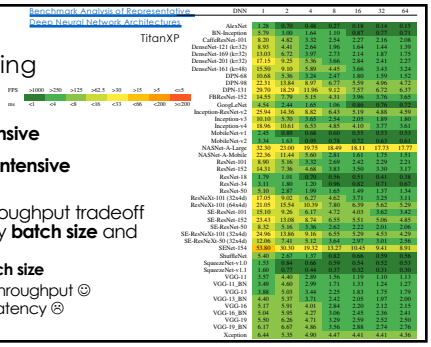
Inference in Deep Learning Models

- **Compute intensive**
- **Less memory intensive** than training
- Latency vs throughput tradeoff determined by **batch size** and **hardware**
  - **Increase batch size**
    - Increase throughput ☺
    - Increase latency ☹



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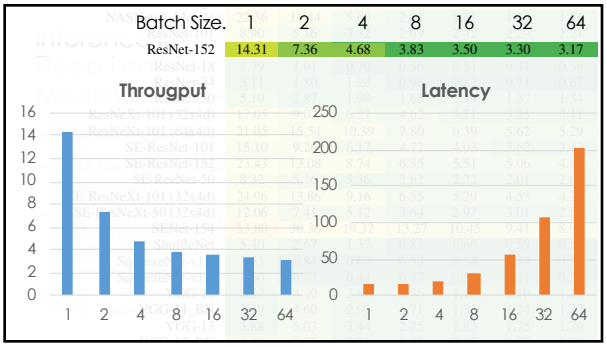

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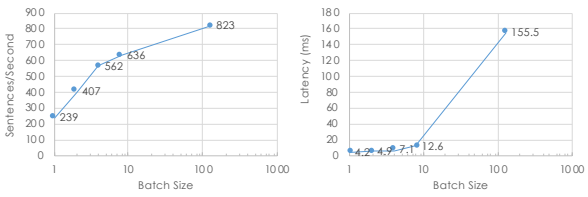
BERT-Large on a V100 (~$10K)



Results included Mixed precision optimizations!

Numbers obtained from: https://developer.nvidia.com/deep-learning-performance-training-inference

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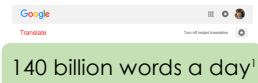
Google Translate

Serving



140 billion words a day[1]

82,000 GPUs running 24/7

Google's Neural Machine Translation System: Bridging the Gap between Human and Machine Translation

"If each of the **world's Android phones** used the new Google voice search for just **three minutes a day**, these engineers realized, the company would **need twice as many data centers.**" – Wired

Designed New Hardware! Tensor Processing Unit (TPU)

[1] https://www.nytimes.com/2016/12/14/magazine/the-great-ai-awakening.html

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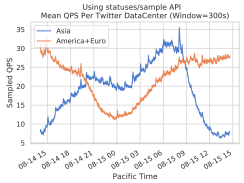
Other Challenges?

- **Bursty load** →
  - overprovision resources →
    - **expensive**
  - TPU reports 28% utilization of vector units in production
  - Solutions
    - statistical multiplexing → hardware not designed for multitenancy
    - could try to predict arrival process → generally difficult to predict
- **Versioning** and **testing models**
- **Prediction pipelines** → more on this soon



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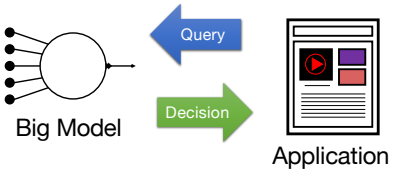
Inference



Two Approaches

- ***Offline:*** Pre-Materialize Predictions
- ***Online:*** Compute Predictions on the fly

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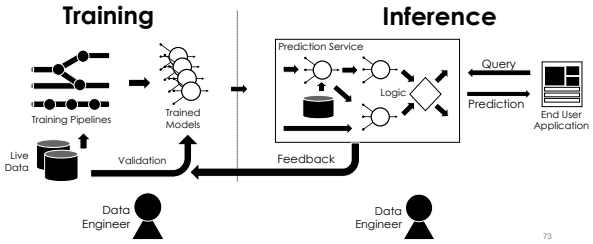
Pre-materialized Predictions



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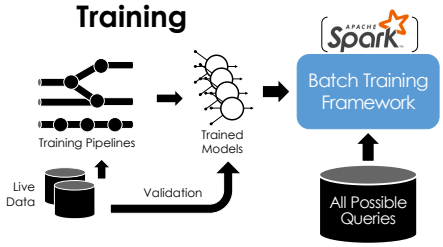
Pre-materialized Predictions



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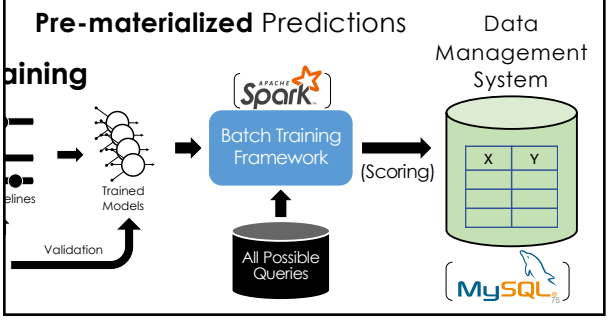
Pre-materialized Predictions



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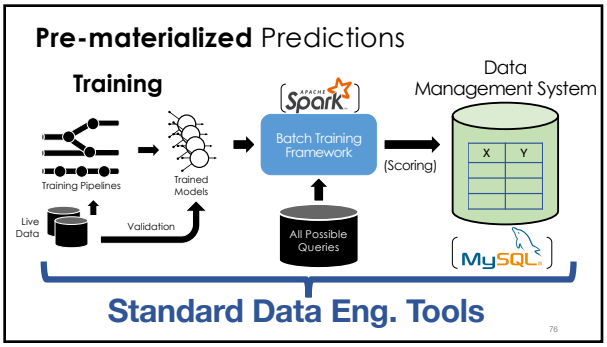
Pre-materialized Predictions



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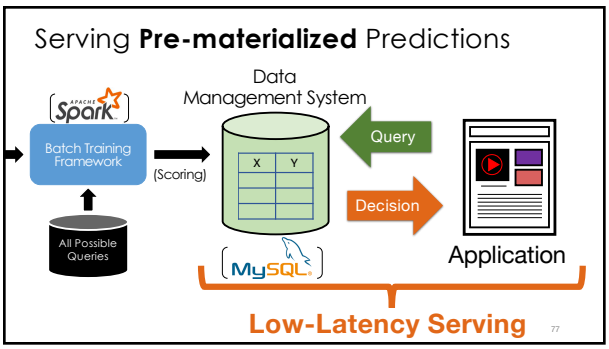

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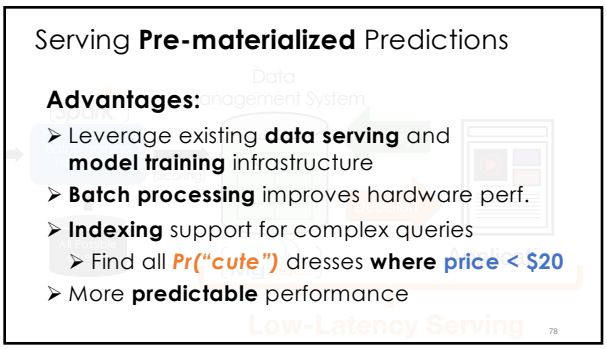

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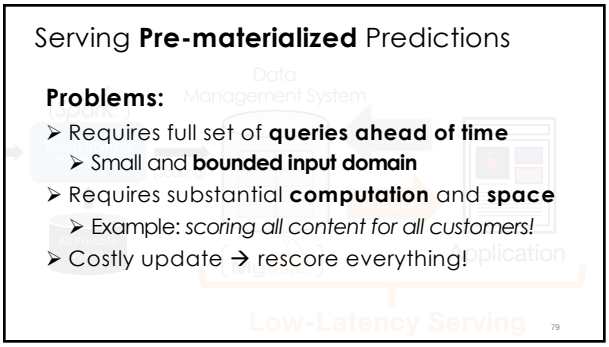

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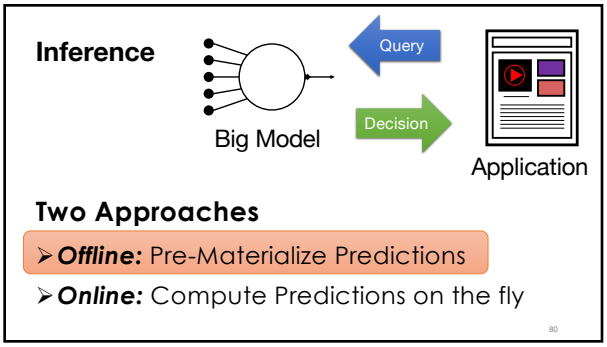

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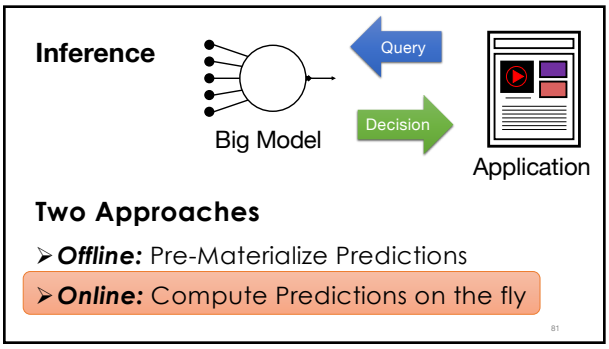

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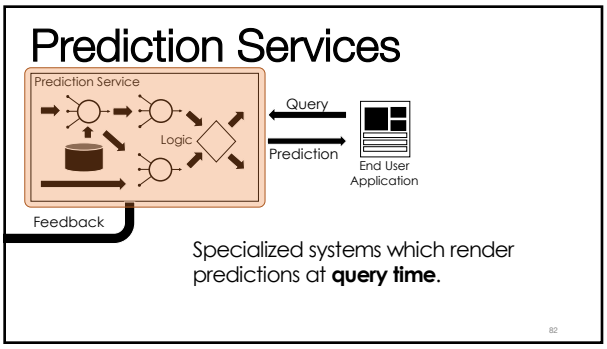

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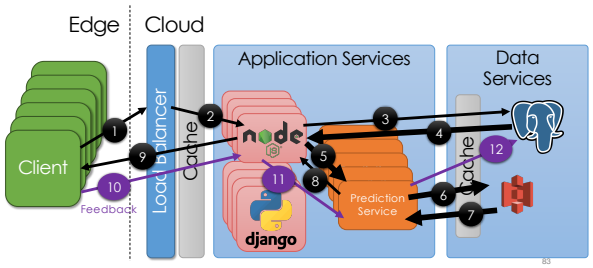
Architecture of a Prediction Service



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Online: Compute Predictions at Query Time

- **Examples**
  - Signals processing: speech recognition & image tagging
  - Ad-targeting based on search terms, available ads, user features
- **Advantages**
  - Compute only necessary queries
  - Enables models to be changed rapidly (e.g., bandit exploration)
  - Queries do not need to be from small ground set
- **Disadvantages**
  - Increases complexity and computation overhead of serving system
  - Requires low and predictable latency from models

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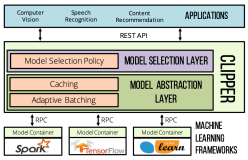
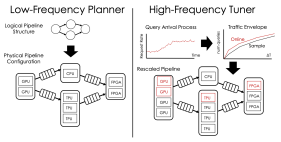
Active Area of Research in my Group

Clipper Prediction Serving System
[NSDI'17]



InferLine Pipeline Provisioning System
[Under review]



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Prediction Serving → Hardware

- Inference requires less memory → **focus on compute**
- Greater emphasis on **latency** instead of throughput
  - Focus on **small batch** inference (batch size = 1)
  - Opportunity to exploit **pipeline parallelism**
  - Need **high availability** → esp. in mission critical settings
- Often runs multiple **concurrent prediction tasks**
  - Cloud → Multitenancy → Performance isolation
  - Edge → supporting multiple data streams
- Tolerate **model compression** and **quantization**
  - As low as 4-bit activations and weights
- **Bursty load**
  - Statistical multiplexing
  - Use inference hardware for background training?

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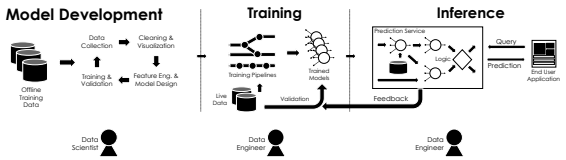
Machine Learning Lifecycle



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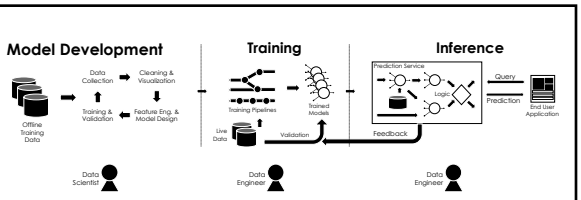

Security?

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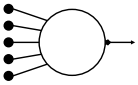
Protect the **data**, the **model**, and the **query**

High-Value **Data** *is* ***Sensitive***

- Medical Info.
- Home video
- Finance

Models capture **value** in data

- Core Asset
- "Contain" the data



Biggest opportunity for hardware in ML.

Queries can be as sensitive as the data



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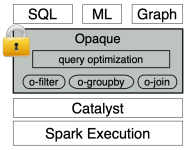
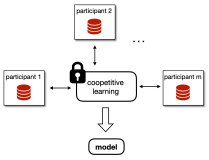
Our recent work in secure ML

Opaque | Oblivious Spark over **SGX**
[NSDI'17]



Helen | **Coopetitive Learning** Using Cryptographic Primitives
[S&P'19]



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Security and Hardware

- Improved Access to Data
  - User willing to share data with models but **not companies (people)**
  - **Differential Privacy** can increase data sharing incentives
- Better **isolation** of co-tenant models on hardware accelerators
- **Coopetitive Learning**: Secure multiparty computation for ML
  - **Example:** *Competing banks collaborate to construct a shared fraud model without sharing data.*
- Models have access **to more sensitive inputs**
  - **Example:** *Alexa could see where you are when asking to turn on a light.*

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Conclusion

- **History:** AI and Computer Systems have Co-evolved
- **Feedback Cycle:** Hardware, Abstractions, and Data
- **ML is many Applications:** *Machine Learning Lifecycle*
  - *Model Development:* Exploration
  - *Training:* Scale and Composition
  - *Inference:* Cloud – Edge Spectrum
- **Security:** Opportunity for hardware innovation in AI

Thank you!

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