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A Review of Electronic-Photonic Heterogeneous Integration at DARPA

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***Abstract*—The Defense Advanced Research Projects Agency (DARPA) has developed programs in integrated photonics for over a decade. From the Electronic-Photonic Integrated Circuits (EPIC) program to the more recent Electronic-Photonic Heterogeneous Integration (E-PHI) program, DARPA programs have established a library of high performance silicon photonic devices and have demonstrated heterogeneous integration processes. These components and integration techniques, combined with automated design software tools, form the basis of the new American Institute for Manufacturing Integrated Photonics (AIM Photonics) which will establish a photonics manufacturing ecosystem in the United States through a combination of public and private funds.**

***Index Terms*— integrated photonics, heterogeneous integration,**

I. Introduction

The fields of optics and photonics have long held promise across a wide application space due to the high frequency of light and low transmission loss through a number of accessible materials. Even at very low fractional bandwidths, these characteristics allow long distance data transmission at rates exceeding 100 Tb/s in a single fiber waveguide [1]. These benefits brought the switch from copper cables to optical fiber in the telecommunications boom in the 1990s. The advantages of fiber are so great that there are over 550,000 miles of optical cable installed in the oceans alone [2] and it is taken for granted that fiber optical transmission is required for the long-haul internet backbone. Today we are seeing the introduction of wired optical communication at shorter distances for high performance computing, intra-datacenter communications and board-to-board communications. Fiber is the preferred solution when the product of the data-rate and propagation length exceed 100 Gbps·m [3]. As data-rates increase, photonic systems will be needed for continually shorter links.

While the telecommunication and datacommunication industries continue to be the dominant market for photonics, there are several less-obvious applications of photonics to be revolutionized through integration. It is well known that optical oscillators have exceptionally high Quality Factor (Q). Optical transitions in atoms such as Strontium and Ytterbium have Qs on the order of 10^{14} and are the basis of modern precision timing

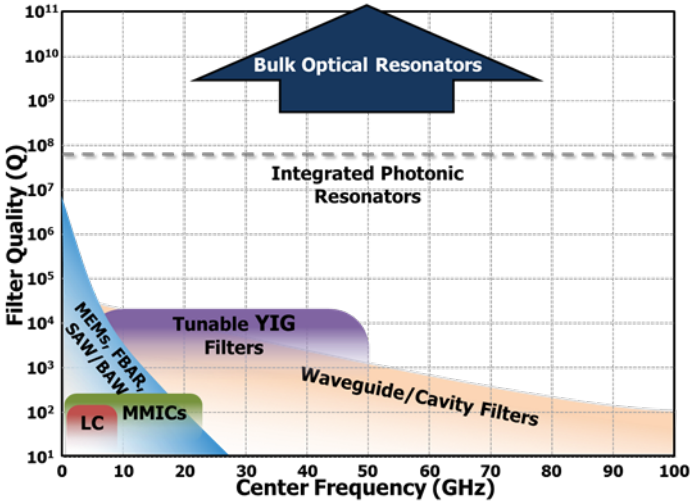

Figure 1: Filter Quality Factor as a function of RF frequency. The acronyms are as follows: LC: inductor-capacitor, MMICs: monolithic millimeter wave integrated circuits, MEMS: microelectromechanical systems, FBAR: film bulk acoustic resonator, SAW: surface acoustic wave, BAW: bulk acoustic wave, YIG: yttrium iron garnet.

standards. Bulk optical resonators, such as CaF_2 whispering gallery mode resonators, have been demonstrated with Qs greater than 10^{11} [4]. Figure 1 illustrates the Quality Factor for oscillators across the radio frequency (RF) spectrum. Note that integrated SiN optical resonators have demonstrated Qs exceeding 80 million [5]. At this point tunable optical filter bandwidths below 10 MHz are possible in a photonic integrated circuit, on par with large and power-hungry RF YIG filters. The compact footprint of optical technologies, coupled with their low-loss and high-Q, make integrated photonics a promising candidate for tunable, precision frequency sources, agile software defined radios and wideband digitizers. The high frequency of light also allows for precision ranging and pointing through LIDAR. All of these applications were achievable to some degree in a laboratory environment or with large, expensive systems. Through integration, however, they become mobile and expendable.

Over the last decade, the Defense Advanced Research Projects Agency (DARPA) has sought to develop the capability to shrink these large, temperature-sensitive systems to robust, chip-scale technologies. Through a series of DARPA programs,

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a comprehensive suite of silicon photonic devices, heterogeneous integration of III-V photonic devices and their associated driver circuits has been developed. The goal of these programs is to assemble a catalog of devices and design tools, allowing industry and academia to construct complex electronic-photonic systems. Ideally, this would follow the path of fabless electronics design as established by the metal oxide semiconductor implementation service (MOSIS) under earlier DARPA efforts [6]. The path to open access for advanced electronic-photonic manufacturing is now under construction with the American Institute for Manufacturing Integrated Photonics (AIM Photonics) which will offer a multi-project wafer service.

II. The Early Years: EPIC, UNIC and POEM

The early 2000s brought widespread availability of Silicon-On-Insulator (SOI) wafers for microprocessors, allowing for low-loss and low-leakage single-mode optical waveguides. Commoditized optical lithography with resolution much smaller than 1550 nm light was also commonplace and silicon modulators had been demonstrated with intrinsic bandwidths of 10 GHz [7]. In 2005, DARPA identified that the technology base was ready for silicon-based photonic systems and launched the Electronic-Photonic Integrated Circuits (EPIC) program.

While basic waveguides [8], [9] and modulators had been demonstrated in silicon, the goal of the EPIC program was to demonstrate high-performance silicon photonic devices manufactured in CMOS-compatible foundries. The motivation for silicon photonics was threefold. First, silicon substrates are two orders of magnitude less expensive than the traditional III-V substrates used for the fabrication of active photonic devices. Second, silicon allows the photonics industry to employ the existing manufacturing infrastructure established by the CMOS electronics industry. Finally, photonic devices in silicon enable co-integration with advanced electronics, providing interconnects with low parasitic capacitance and high-speed operation.

EPIC developed device fabrication techniques, culminating in demonstration systems ranging from analog-to-digital converters to data-communications transceivers. The EPIC team led by BAE Systems and the Massachusetts Institute of Technology (MIT) constructed a wideband RF channelizer. Integration of the channelizer onto an optical chip can offer lower loss and power consumption than a conventional wideband RF receiver, while reducing the size and weight of the filter manifold. Monolithic integration of silicon photonics and CMOS electronics was employed in a 150 nm CMOS process. In addition to fabricating high performance modulators and detectors, the team also fabricated 4th order micro-ring filters in silicon nitride. These filters had a passband of 1 GHz and 25 dB of rejection. The tuning range was measured to be over +/-2.5 GHz [10]. A second team consisting of MIT and MIT Lincoln Laboratory demonstrated a high performance analog-to-digital converter, which delivered a chip with modulators, demultiplexers and photodetectors made in a CMOS-compatible microfabrication process and a 20-channel silicon filter bank [11]. Finally, the Luxtera team demonstrated a 4 x 10 Gb/s transceiver for chip-to-chip communication. Tens of optical components were monolithically integrated with hundreds of thousands of transistors. This chip was fabricated in a 130 nm SOI CMOS process modified to include germanium photodetectors [12]. This chip became the basis for Luxtera's commercial "Blazar" transceiver chip, delivering 4 channels at variable data rates from 1 Gb/s to 10.5 Gb/s.

The EPIC program paved the way for the Ultraperformance Nanophotonic Intrachip Communications (UNIC) program in 2008 which transitioned into the Photonically Optimized Embedded Microprocessors (POEM) program in 2010. These efforts built on the successes of the EPIC program, notably Luxtera's digital link results, and pushed the performance of silicon photonic devices and their associated driver circuits to the high speed and low power consumption necessary for digital communications. The POEM program particularly focused on high performance data-links between microprocessors and also between the microprocessor and off-chip memory to overcome limitations of the memory wall.

POEM has recently demonstrated 2 low-power links using different approaches to electronic-photonic integration. In the first, Oracle demonstrated a 6 channel link using a 3 μm thick SOI layer and driver circuits fabricated in TSMC's 45 nm CMOS line. The electronic driver chip was flip-chip bonded to the photonic chip using micro-bump bonds with capacitance of ~15 fF. The aggregate bit rate of the link was 48 Gb/s and ran at an average of 1.95 pJ/bit [13]. In the second demonstration a team composed of Berkeley, MIT and the University of Colorado demonstrated a link between a dual core microprocessor and memory. The chip consisted of 70 million transistors and 850 photonics components, providing a memory bandwidth of 5 Gb/s at 1.3 pJ/bit [14]. Standard 45 nm CMOS fabrication was used for the photonics in the same process as the electronics in what has been deemed "zero-change CMOS photonics." While this has the advantage of simplified integration, conventional CMOS processing presents several constraints on the photonics devices [15]. For example, silicon photonics process flows tend to include pure germanium growth to fabricate photodetectors. In this result, germanium was not available so fully strained SiGe was used in the photodetector pMOSFETs. This pushed the link from the traditional 1550 nm wavelength to operation at 1180 nm wavelength to accommodate the SiGe bandgap.

In order to increase the routing and processing of data in the optical domain, the creation of optical memory on a silicon photonic platform was considered to be a complementary technology to the transceiver technologies under intense development, both through DARPA-funded and other international work. In a non-DARPA-funded effort, researchers at Ghent University developed the first-ever electrically-pumped, all-optical flip-flop using heterogeneously-integrated InP-based active media on an SOI platform [16]. The device utilized a single microdisk laser coupled to an SOI wire waveguide, with electrical power consumption of a few milliwatts and switching time of 60 ps. The creation of sophisticated integrated photonic devices such as this, as well

as demonstrations from the DARPA EPIC, UNIC, and POEM programs, illustrated the rapidly growing maturity of silicon photonic technology.

Integrated photonics for digital communication will be driven to improve as bit rate demands increase and power envelopes grow more constrained. A number of companies are pursuing silicon photonics for data center applications, as evidenced through the acquisitions of silicon photonics companies by Cisco, Mellanox, and Huawei. These companies also continue to demonstrate prototype devices at popular technical conferences, indicating that products will be deployed soon. However, this technology push is not likely to develop additional photonic devices outside of those required for digital datacommunications. Devices such as high-speed, linear modulators, high-speed photodetectors, high power-handling devices and efficient mode-locked lasers are unlikely to see development in the commercial sector.

III. The E-PHI Program

As evidenced by the results of EPIC, UNIC and POEM, silicon photonics can be a power-efficient solution for several applications. Silicon and silicon nitride technologies can produce low-loss passive structures, high-speed modulators and detectors. It is in light generation, optical power handling and optical non-linearities that silicon has come up short. The Electronic-Photonic Heterogeneous Integration (E-PHI) effort was developed to address the limitations of silicon through the heterogeneous integration of chiplets of other media onto a silicon substrate. In this way, III-V light sources and amplifiers could be co-integrated with silicon photonics, silicon nitride passives, high-performance CMOS, GaAs driver circuits and non-linear media. Such integration would allow for complex and compact optical systems that are implicitly ruggedized for stressing environments. Co-integration would not only make for lower cost and complex optical systems, however. This integration would allow for systems not possible with bulk components. Using integrated measurement and control circuits with femto-Farad capacitance, control loops can be closed on nanosecond timescales. Ultra-low noise optical and RF systems can be constructed, making a system that is much greater than the sum of its parts. Such intimate integration also holds the promise of scalable optical phased array technology for sensing and communications.

DARPA launched the E-PHI program in 2011 as a manufacturing effort to construct a catalog of heterogeneous photonic devices, fabrication technologies, and corresponding integration schemes and design tools. E-PHI targeted component development and system demonstrations of precision frequency sources, sensing and RF applications as opposed to data communications. There are four prime E-PHI performer teams consisting of Aurrion with subcontractors University of California (UC), Santa Barbara and the University of Virginia, MIT with subcontractors UC Berkeley and the College of Nanoscale Science and Engineering in Albany, UC Berkeley with subcontractor University of Illinois, and UC San Diego with subcontractor Lucent Technologies.

A. *Heterogeneous Photonic Integration*

E-PHI has demonstrated a number of components integrated on a silicon platform that are key to new application spaces. The main missing component from silicon photonics is on-chip gain for optical amplification and lasing. UC Santa Barbara and Aurrion have matured an approach to front-end integration of III-V materials on silicon for photonic applications. This begins with a low temperature bond between the silicon photonic wafer and III-V chiplet through an oxygen plasma treatment. This results in a thin oxide layer on both surfaces and enables a high quality bond at temperatures below 200°C. The low temperature avoids difficulties associated with thermal expansion coefficient mismatches and results in a stronger bond than other common bonding approaches such as hydrophilic surface treatments [17]. The bonding is completed prior to lithographic patterning, loosening the tolerances to the chiplet alignment as the III-V waveguide is defined after bonding.

Prior to E-PHI, the POEM program had efforts to develop an efficient on-chip laser leveraging Aurrion's work on low temperature bonding of III-V chiplets to silicon [18],[19] and Oracle had developed back-end integration of reflective semiconductor optical amplifiers with silicon waveguides [20]. Under the E-PHI program, Aurrion and UCSB have improved their low temperature bonding yield and throughput to make a manufacturable process and can now reliably and repeatably bond small III-V chiplets to silicon wafers, with a program goal of bonding 1 mm x 1 mm chiplets. Hybrid III-V lasers have been demonstrated with long-life operation and avoid hermetic packaging due to the absence of external III-V optical facets [19]. Incorporating electronics chips in this process allows for a side-by-side approach to integration with electronics, as

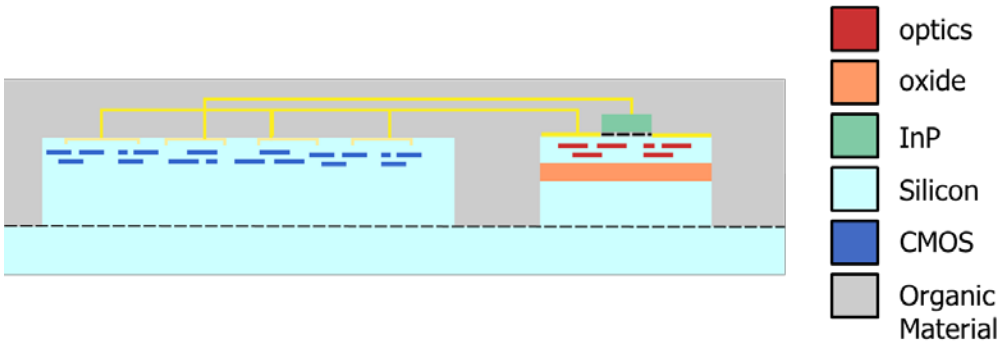

Figure 2: Illustration of co-integration of electronic and photonic integrated circuits together on a single substrate.

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illustrated in Figure 2. In this case, the two separate chiplets are mounted on a silicon interposer and planarized with an organic material. After planarization, standard lithographic processing is used to interconnect the chips with metal traces.

The ability to co-integrate III-V active media with low-loss silicon photonics has enabled a variety of optical components. In many cases, these devices can exceed the native capability of a single material. One exemplar is in hybrid Si/III-V semiconductor lasers. Using heterogeneous integration techniques, semiconductor lasers have been demonstrated with linewidths less than 1 kHz (see Figure 3) [21]. This was accomplished by employing different, optimal materials for the laser gain medium and high-Q resonator. In this scheme, a III-V active region was bonded to a high-Q silicon optical cavity with the lasing mode designed to have low overlap with the gain region. This served to significantly increase the total Quality factor with minimal impact on the modal gain [22]. Thus by integrating the InP gain medium with the high-quality silicon photonics structure, a world-record semiconductor laser linewidth was demonstrated, an improvement of three orders of magnitude over conventional distributed feedback lasers.

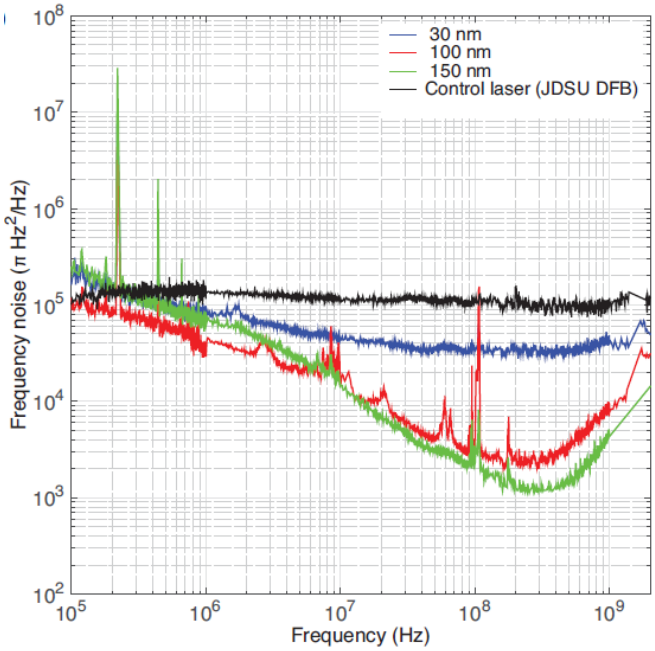

Figure 3: Frequency noise spectra of hybrid Si/III-V semiconductor lasers with three different geometries and control laser (JDSU DFB). The lines correspond to different spacer thicknesses between the III-V gain material and the silicon waveguide, directly controlling the amount of overlap of the optical mode with the gain medium. Adapted from [21].

In addition to ultra-low linewidth fixed lasers, the heterogeneous III-V on silicon platform has been used to fabricate low-noise tunable lasers. UCSB recently demonstrated a narrow linewidth laser tunable over 54 nm in the O-band [23]. The team employed low loss silicon waveguides (0.67 dB/cm) to form a 4 cm long external cavity and achieved broad tuning with thermal tuners in the two Vernier rings and a linear phase section. This geometry is illustrated in Figure 4. Narrow linewidth across the tuning range was achieved with an external cavity consisting of a 3 cm

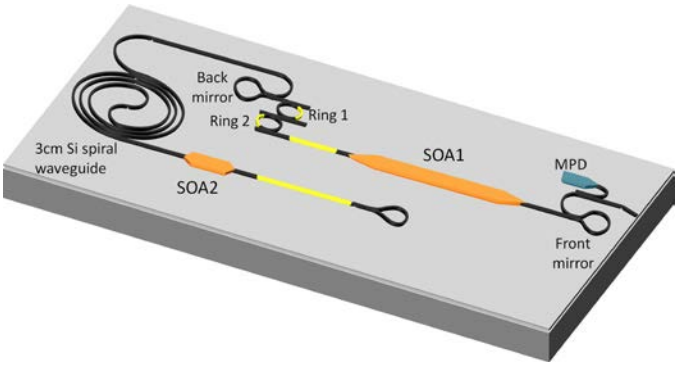

Figure 4: Schematic of the widely tunable external cavity laser. Yellow regions show thermal tuning sections and orange indicates semiconductor optical amplifiers. Adapted from [23].

integrated delay, a semiconductor amplifier, a thermal phase tuner and a loop mirror. In aggregate, this created a 4 cm long external cavity to achieve coherent feedback in a long external cavity. The length of the integrated external cavity, equivalent to 15 cm in free-space, was critical to stable operation and only achievable through the heterogeneous integration with low-loss silicon waveguides. A linewidth of less than 100 kHz was achieved across the entire tuning range. Taking this technology further, two tunable lasers were co-integrated and packaged with an optical coupler, amplifier and photodiode, shown in Figure 5 [24]. This created an agile, packaged frequency source tested up to 20 GHz, as limited by the photodetector. Such a compact and tunable RF source has applications in metrology and RF phased array technologies and work is continuing to further reduce the linewidth to the theoretical values of sub-kHz linewidths. Additional light sources, such as room-temperature quantum dots and narrow-linewidth mode locked lasers, have also been developed and detailed information can be found in reference [25].

Heterogeneous integration has also enabled world-record high-power, high-frequency photodiodes. In many cases, the power-handling, bandwidth and efficiency of the photo-detector can be the limiting parameters for RF applications, as illustrated in the previous example. High-speed, high-power photo-detection tends to be constrained by a compromise between device area and speed. Achieving high saturation currents, and therefore high-power output, pushes the device toward a large absorbing area. This large area, however, can limit high-speed response due to the larger capacitance. Heterogeneous integration allows for an optimization of these parameters. By designing the coupling between the silicon

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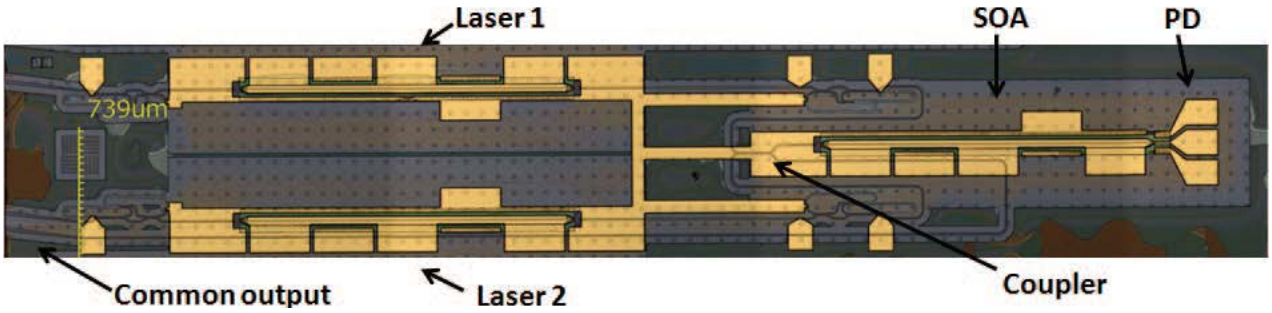

Figure 5: Optical micrograph of UCSB photonic microwave generator comprised of two tunable lasers, a coupler, booster semiconductor optical amplifier (SOA) and photodetector (PD). Adapted from [24].

waveguide and InP structure along the length of the device, the absorption profile can be flattened to prevent saturation and maximize bandwidth. This optimization cannot be achieved in conventional bulk photo-diodes. The previous record output power for waveguide-integrated photodiodes was 6.7 dBm at 10 GHz and 3.9 dBm at 30 GHz [26]. The University of Virginia and Aurrion team integrated the InP Modified Uni-travelling Carrier photodiode onto a tailored silicon waveguide to construct the highest power-bandwidth product photodiode integrated with a single-mode waveguide. The E-PHI device delivered output power of 16.6 dBm at 10 GHz and 13.5 dBm at 30 GHz [27].

Heterogeneous integration also offers the ability to employ low-loss passive structures in the same optical system as silicon photonics. High-Q resonators for narrow optical filtering are critical components for RF photonic applications but past work on integrated optical filters have been limited to bandwidths on the order of 1 GHz. This bandwidth is typically not sufficient for agile radios or jammer removal. In recent work, the loss for integrated waveguides has been reduced from ~1 dB/m to ~0.05 dB/m [28, 29] through use of materials (SiN) and modal engineering. These approaches, however, can be unsuitable for complex RF photonic circuits because of their intricate microfabrication that is incompatible with a complete process flow or very loosely confined optical modes that were not compatible with dense integrated photonic circuits. Under E-PHI, these approaches were developed to make the waveguides integrated with other photonic devices and compatible with more “traditional” photonics processing. A recent result from UC Santa Barbara has demonstrated a microdisk resonator with a Q of 81 million in silicon nitride. The resonator was coupled to a silicon nitride waveguide using a “weakly tapered gap” to mitigate loss in the coupling region [5].

Heterogeneous integration under the E-PHI program has not been limited to the Aurrion platform. UC San Diego also developed wafer bonding of InP gain media to silicon and silicon nitride photonics. This was used to develop both lasers and amplification stages for the singular purpose of integrated, cavity-less comb generation. Prior work in optical fiber has shown that wideband combs exceeding 100 nm can be generated with high optical-signal-to-noise ratio with only two continuous wave lasers as a seed. This is achieved without a cavity through multiple stages of high-nonlinearity waveguides for four-wave mixing interspersed with dispersive waveguides to form high-peak power in the time domain [30]. Under the E-PHI program, this shock-wave mixer topology was adapted from the conventional bulk fiber components to a fully integrated comb source. Through waveguide engineering, stages of high dispersion for chirp and near-zero dispersion for four-wave-mixing have been developed in silicon waveguides. InP amplification stages have been integrated to overcome the two-photon absorption in silicon. Several four-stage mixers have been tested, demonstrating more than 65 tones over 60 nm with an optical signal to noise ratio of 48 dB. The integrated mixer is depicted in Figure 6.

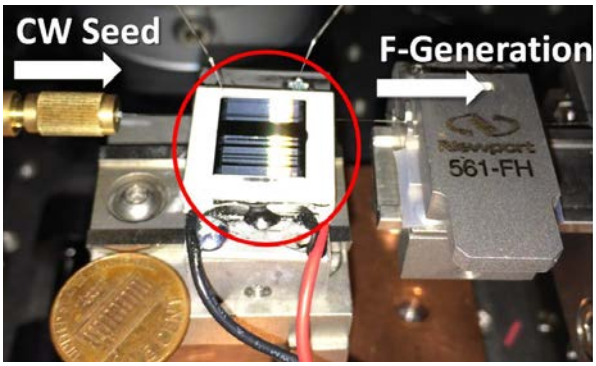

Figure 6: Image of UCSD integrated mixer for cavity-less comb generation.

B. Electronic-Photonic Integration

The utility of photonic devices is greatly enhanced when co-integrated with control and feedback electronics. Previous approaches to electronic-photonic integration involved either flip-chip bonding, in which the size of the micro-bump pads will set a floor for the parasitic capacitance, or complete monolithic integration which limits both the performance of the photonic devices and the materials used in the process. E-PHI has matured integration schemes by fabricating the electronics and the photonics on separate wafers and in different fabrication lines for bonding in a later process step. This allows the optimization of the materials, cost and fabrication tools for the photonics and electronics. The latest CMOS electronics can be integrated as they become available.

The UC Berkeley team developed a through silicon via (TSV) approach for compact packaging. TSVs are typically used in chip stacking of electronic die and are rapidly maturing.

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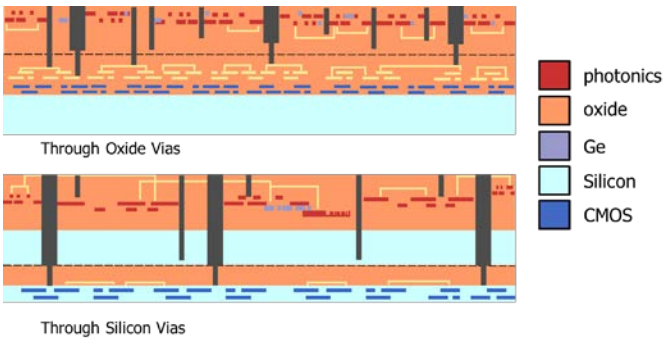

Figure 7: Illustrations of a Through Oxide Via (TOV) geometry (above) and Through Silicon Via (TSV) geometry (below)

Using through-silicon-vias in integrated electronic-photonic systems allows the team to build on advances made by the larger semiconductor industry. An illustration of the Berkeley approach can be seen in Figure 7 with the electronics chip on the bottom and the photonics chip on the top.

The MIT team has pursued a through oxide via (TOV) approach. This is a wafer-scale process where the electronics wafer and the photonics wafer are bonded prior to chip dicing. While a newer and less developed technology than TSVs, TOVs are capable of lower parasitic capacitance than TSVs because the via must only traverse the thin oxide layers rather than the thick silicon substrate. This is illustrated in Figure 7. The team recently demonstrated a parasitic capacitance of the via at 1.45 fF, more than an order of magnitude less than the 30 fF representative of TSVs. Driving down capacitance is critical to low-power and high-speed applications such as on-chip interconnects. A demonstration of the TOV technology enabled on-chip photonic transmit and receive modules which were used in a 5 Gb/s link consuming 250 fJ/bit, including the on-chip optical power [31]. The yield of the TOV process is nearly 100% [32].

The MIT team, with subcontractor CNSE, developed an entire library of silicon photonic components. These include silicon and silicon nitride waveguides, germanium detectors with 1 A/W responsivity, optically pumped lasers and amplifiers, Mach-Zehnder modulators and tunable filters. These components have been captured in parameterized cells (p-cells) at various layers of abstraction and included in their photonics-CMOS process design kit (PDK). This PDK includes Verilog models of the photonic devices with complete timing information of both the electronics and the photonics. The PDKs have integrated design rules that can, for example, exclude metal in close proximity to waveguides and ensure that TOVs or TSVs are not etched through devices on the photonic layer.

C. *Integrated Demonstrators Using the E-PHI Platform*

The maturing design and manufacturing capabilities developed under E-PHI have enabled the performers to develop demonstration systems that far exceed the capabilities of bulk components. In most cases, these demonstrators were chosen to be an electronic-photonic microsystem that employs both the advanced components and the complexity afforded by the design tools.

Optical phased arrays are a prime example of advanced capability not available to bulk optics. It is well known that arrays have transformed radio frequency apertures, allowing for rapid, non-mechanical beam steering and agile multi-beam generation. To be useful, however, the spacing of the emitters and receivers must approach the free-space wavelength, ideally at one-half wavelength for a wide field of regard. At optical wavelengths, it is simply not possible to fit the array components such as phase shifters, apertures and control electronics into the micron-scale pitch without integration. Under E-PHI, the MIT team has used their photonics process and design tools to attack this problem in several steps. Early efforts delivered a static optical phased array with 64 x 64 emitters that combined to form the MIT logo in the far field. With over 4000 photonic components, this was the most complex integrated photonic circuit made on a single chip [33]. This work proved the stability of the coherent, planar aperture to both manufacturing variances and the perturbations of an indoor environment. The emitter spacing, however, was

Figure 8: Depiction of 2-D 64-element x 64-element on-chip optical phased array on silicon (left) and far-field image radiation pattern from the 2-D optical phased array, producing the MIT logo (right) [33].

approximately 6 wavelengths in both directions, creating grating lobes as seen in Figure 8.

Moving away from the full 2-dimensional phased array allows for much tighter emitter spacing. This can be achieved by employing arrays of long, linear waveguide gratings. This design achieved a world record 51° spacing between grating lobes in the far field and the beam could be continuously swept in one dimension at 100 kHz by thermal modulation of the phase between the array elements [34]. The geometry, shown in Figure 9, consists of 16 waveguide emitters with progressively stronger gratings to create a uniform, 32 μm x 32

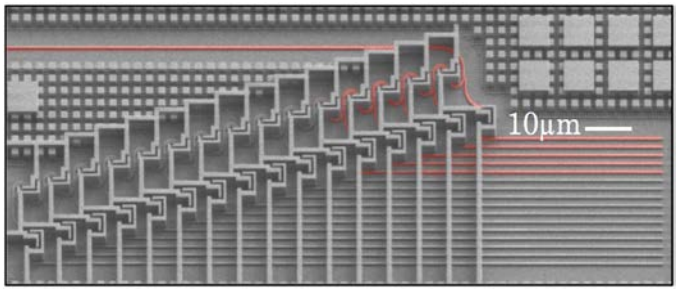

Figure 9: SEM image of on-chip optical phased array on silicon with fast, wide-angle beam steering [34]

μm patch emitter. These are individually fed by a cascade of thermal phase shifters, non-mechanically scanning the output beam in the vertical direction. While not demonstrated in this architecture, horizontal scanning can also be achieved by tuning the frequency of the off-chip laser source [35]. This work has proven the viability of a scalable optical transmit/receive array for LIDAR and communications, compressing the optical system into a planar, integrated device. In the remaining months of the program, the MIT team is working to deliver a fully integrated, chip-scale LIDAR system with 10 mm^2 transmit and receive apertures for ranging to 10 m.

UC Berkeley also fabricated a demonstration system for LIDAR, however they developed sub-systems for the electronic-photonic back-end rather than non-mechanical beam-steering. A 180 nm CMOS chip was integrated with a 250 nm silicon photonics chip using the TSV process to construct a frequency modulated continuous wave (FMCW) LIDAR system. The photonic chip contained a Mach-Zehnder interferometer and a photodetector and the electronic chip contained the ramp linearization circuitry. Using their TSV integration, the team made a compact electro-optical phase locked loop to ensure a constant slope to the optical wavelength. This feedback circuit enables 8 μm of root-mean-squared error at a target distance of 50 mm [36].

The Aurrion team projects several final demonstration systems, including a temperature insensitive laser, using passive techniques to maintain a constant wavelength, and a distributed drive integrated modulator. The latter leverages a packaging approach developed for a high throughput digital optical switch demonstration which used integrated III-V semiconductor optical amplifiers with Mach-Zehnder switch elements. The switch controller was fabricated in 130 nm CMOS and integrated on a silicon interposer with the photonics chip [37]. Under the E-PHI program, the integration approach was expanded to incorporate high performance electronics chips made from materials such as GaAs and InP. If successful, this would allow a break from the conventional design of high-speed modulators. Simulations of the distributed drive modulator project operation at 40 GHz bandwidth and a $V\pi$ of approximately 1 V. This design is only possible through heterogeneous integration and mitigates the high RF gain requirements of a conventional modulator. The distributed drive modulator design is currently in fabrication and is expected to be demonstrated by the conclusion of the program in 2016.

The final demonstration of the E-PHI program is a compact, ultralow noise, tunable RF oscillator under development at UC San Diego. It is well known that an arbitrary RF frequency can be generated by beating two optical frequencies on a photodetector, provided the detector has sufficient bandwidth. A system employing this technique was described in section IIIA of this manuscript. The compromise in RF generation using this technique is in the phase noise of the final signal. Tunable lasers typically have inferior stability and linewidth compared to fixed lasers. This system will employ a fixed laser, a tunable laser and the chip-scale shockwave optical mixer to provide stabilizing feedback to the tunable laser source. This is accomplished by seeding the mixer with the fixed laser and tunable laser. Through four wave mixing, additional tones are generated with phase noise increasing with the order of the tones. One of the higher order tones is sent through a low-Q etalon which converts its frequency fluctuations to amplitude fluctuations. These amplitude fluctuations are then sent to a photodetector and used to seed a Pound-Drever-Hall loop to stabilize the tunable laser's linewidth by rapidly changing its current about its bias point. This architecture has been demonstrated with fiber-optic components. Through E-PHI, all of the necessary components now exist to make such a system on chip, including the narrow linewidth fixed laser, the tunable laser, the low-noise comb generation and the low-Q etalon. The demonstration will be completed by the end of 2016.

IV. AIM Photonics

As part of an effort to reinvest in American manufacturing, the United States government created a series of Institutes for Manufacturing Innovation (IMIs) beginning with investment in additive manufacturing (America Makes) in 2012. Photonics was a potential IMI under consideration in the summer of 2014 when a request for information (RFI) was issued by the government. The photonics community responded to this RFI in large numbers and integrated photonics was ultimately selected to be the sixth IMI.

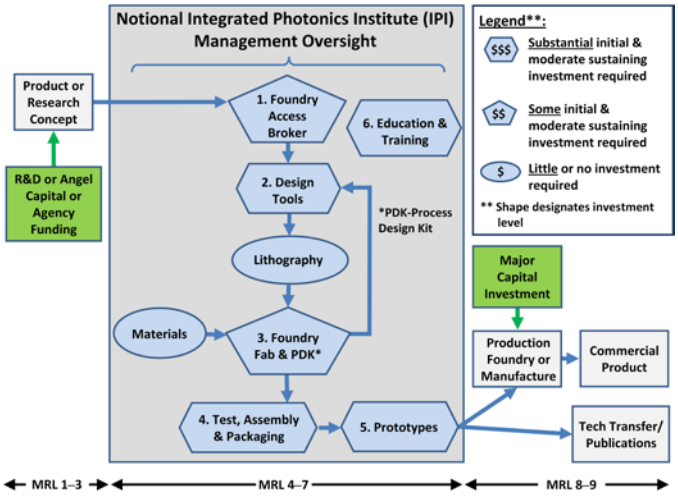

Figure 10: Notional layout of the desired ecosystem to create a functional institute in integrated photonics. Adapted from [38].

The government-envisioned structure for the resulting integrated photonics institute for manufacturing innovation (IP-IMI) is depicted in Figure 10 and calls for development in several aspects of manufacturing as well as the interactions between those areas. While DARPA investment has developed integrated components and systems in this field, advancing the technology readiness level and making the formation of such an Institute possible, past efforts have not developed end-to-end manufacturing. To date, the barrier to entry in integrated photonics remains high (requires either development of an advanced microelectronic fabrication facility, or a private partnership with an existing microelectronic facility), and advances made by one team tend to stay isolated as their competitive advantage.

There have been a number of initiatives across the international integrated photonics community to establish an

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integrated photonics foundry (see [39] for a more complete review). In recent years, silicon photonic foundry offerings have emerged using fabrication facilities such as Singapore Institute of Microelectronics (IME), Imec, and the Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA)-Leti. These foundries offer multi-project wafer services to enable small-volume silicon photonic production. They offer a variety of component technologies, including Si passives, Ge photodetectors, Si Mach-Zehnder and ring modulators, couplers, and packaging. They also provide process design kit support for several mainstream microelectronics CAD tools. The IP-IMI will share many features with these silicon photonic foundry capabilities.

In response to the government's IP-IMI solicitation, the Research Foundation for the State University in New York (RF SUNY), submitted a proposal entitled "AIM Photonics" that was selected to implement the IP-IMI vision. This selection was publically announced on July 27, 2015, and rebranded the IP-IMI as AIM Photonics. The foundational photonics manufacturing at SUNY Albany was developed from scratch under the DARPA E-PHI program. Now the US Government's $110M contribution makes AIM the largest Institute to date; a distinction it will likely maintain well into the future. These funds will be enhanced with cost matching secured by AIM to result in totals of $612M over the five-year life of the cooperative agreement.

At its core AIM is creating a multi-project wafer and assembly (MPWA) service to provide open access not only to integrated photonic circuits but also packaging options. AIM embraced E-PHI's heterogeneous integration vision to include the necessary electronic integration to realize complex photonics systems. The envisioned MPWA service, depicted in Figure 11, will collect and aggregate user designs to employ shared mask sets. Just as in semiconductor MPW runs, this approach will reduce the price to realize a design by spreading the costs of mask sets and fabrication fees over many users. To address the needs in this area MOSIS was recently selected to serve as AIM's Aggregator – a role they pioneered years ago in semiconductor manufacturing. AIM is also seeking to offer access to a number of foundries with technologies ranging from pure silicon photonics to indium phosphide as well as access to heterogeneous platforms. Assembly and testing will be offered by AIM to lower the barrier to entry for packaged components.

To provide the service necessary for advanced photonics, general investment in the underlying manufacturing technologies is required. AIM is addressing this through four technology working groups. These areas of development include MPWA, electronic-photonic design automation (EPDA), inline control and test (ICT), and test assembly and packaging (TAP). The EPDA will seek to provide end users with robust design tools that accurately predict system-level performance and enable first-pass design success while ICT will ensure high-yield fabrication to guarantee working chips are returned to users. TAP will support the assembly portion of MPWA and also provide final testing services focused on improving the end-to-end manufacturability.

To effectively focus these manufacturing investments toward recognized market-relevant needs, AIM also created four application-specific key technology manufacturing areas. These areas were created as business units and include very

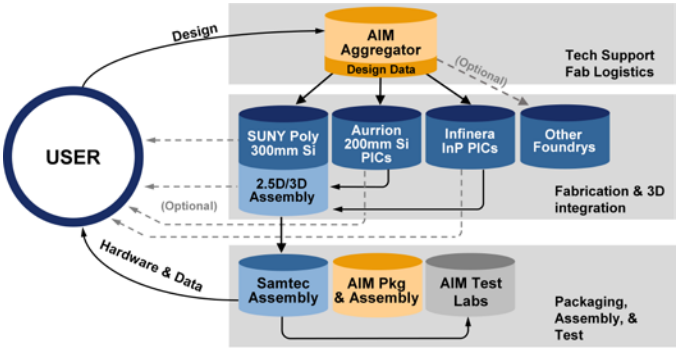

Figure 11: AIM's MPWA service which will provide open access to integrated photonic circuits [40]. The providers identified in this figure are subject to change and may grow in time.

high-speed digital data and communications to investigate well-known and emerging applications in data centers and computing; Analog and RF Applications, which will address as microwave photonics; integrated photonics sensors, focused on biological, chemical, and physical sensors; and PIC array technologies for applications that require the creation of 1xN and NxM array architectures.

AIM will offer the user community MPW access through existing commercial design tools. The intent is to maintain up-to-date offerings by providing new PDK releases every six months while MPW runs will occur at least once per year but more frequently as demand dictates.

V. Conclusion

Heterogeneous integration of silicon photonics with advanced CMOS, RF electronics and III-V optical sources and detectors has enabled complex devices whose functionality can exceed the native material. In several cases, the performance exceeds that of bulk components and integration has enabled complex electronic-photonic systems. With the establishment of AIM Photonics, these design, fabrication and packaging tools will become available to the greater public. This will enable a new group of designers to use photonics in niche markets and disruptive applications.

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