# Low-thermal-budget monolithic integration of optical isolators for silicon photonics

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## Abstract

Integrated optical isolators are crucial components of photonic integrated circuits (PICs) and have garnered significant attention. Monolithic integration using magneto-optical materials is ideal for optical isolator fabrication due to its compact footprint, broadband, polarization-diverse operation, and scalability. However, current monolithic optical isolators face a major challenge: a high thermal budget required for the deposition and crystallization of magneto-optical materials, hindering their integration into foundry-processed PICs. This study introduces a novel approach for monolithic integration of on-chip optical isolators with a low thermal budget, compatible with standard CMOS back-end-of-line (BEOL) processes. The proposed optical isolators employ Bismuth Yttrium Iron garnet with a lower crystallization temperature and integrated micro-doped silicon heaters for local heat treatment, presenting a new method for incorporating non-reciprocity into various integrated photonic devices.

**Keywords:** Integrated photonic circuit, monolithic optical isolator, CMOS BEOL

## 1. INTRODUCTION

Silicon photonics is an emerging platform with huge potentials, and advancing rapidly in performance and capability. It combines the advantages of optical communications (high speed, wide bandwidth, and low power) with the controllability of CMOS-based electronics [1]. Optical elements in silicon photonics such as optical waveguides, optical switches, optical modulators, lasers, and photodetectors, typically operate at the 1550 nm communication wavelength and are built on or integrated into silicon-on-insulator (SOI) substrates. Nevertheless, a critical component remains missing for fully realizing photonic integrated circuits (PICs): optical isolators. To control the flow of light in PICs, optical isolators need non-reciprocity effect, which is usually achieved through magneto-optical (MO) effects. Significant efforts have been made to develop optical isolators [2, 3], which can be classified based on how magneto-optical materials are integrated into the platform: heterogeneous integration [2] and monolithic integration [3]. Common used magneto-optical materials such as cerium-substituted yttrium iron garnet (Ce:YIG) are challenging to grow on silicon substrates due to a substantial lattice constant mismatch. In heterogeneous integration, the iron garnet (IG) is grown separately and bonded onto the SOI while monolithic integration involves directly depositing IG onto the SOI substrate. On one hand, the heterogeneous integration can provide high-quality single-crystalline IG films and typically delivers better isolator performance than monolithic integration. On the other hand, the monolithic integration offers superior scalability and compatibility with various processes and devices [3]. Nevertheless, a significant drawback of current monolithic integration methods is their high thermal budget, which prevents compatibility with CMOS backend processes. For instance, growing Ce:YIG on SOI typically involves the following steps: depositing a YIG seed layer at 450°C, annealing the YIG film at 900°C for crystallization, depositing the Ce:YIG layer at 650°C, and annealing to crystallize the MO film at 850°C. All of these steps ar exceed the maximum allowable temperature of CMOS back-end-of-line processes which is about 200°C - 250°C.

In this study, we propose, for the first time, optical isolators fabricated using a fully CMOS back-end-of-line compatible monolithic integration process. We utilized bismuth-substituted yttrium iron garnet (Bi:YIG) as the magneto-optical material, along with integrated doped silicon micro-heaters, which are used to crystallize the garnet on-chip. Bi:YIG has been demonstrated as a promising alternative to Ce:YIG due to its lower crystallization temperature [4]. Additionally, Bi:YIG does not exhibit an absorption peak near 1.3 eV with an extending tail into the near-infrared range, unlike Ce:YIG, which causes considerable loss at wavelengths below 1550 nm. Furthermore, Bi:YIG has low damping and fast magnetization dynamics, making it a promising material for spintronic applications.. The doped Si heaters were fabricated along with the photonic devices, which are racetrack resonators, on an SOI substrate (Figure 1). The silicon was n-type doped by spin on dopant method and the waveguides were patterned by electron-beam lithography and etched using a $Cl_2$-based dry etching process. The garnet was subsequently deposited on the chip with a patterned photoresist mask at room

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temperature, followed by a lift-off process. Finally, the garnet was crystallized on-chip using the doped silicon heaters. The doped silicon heaters can operate under both DC and AC applied voltages, reaching a maximum temperature of 900-1000°C.

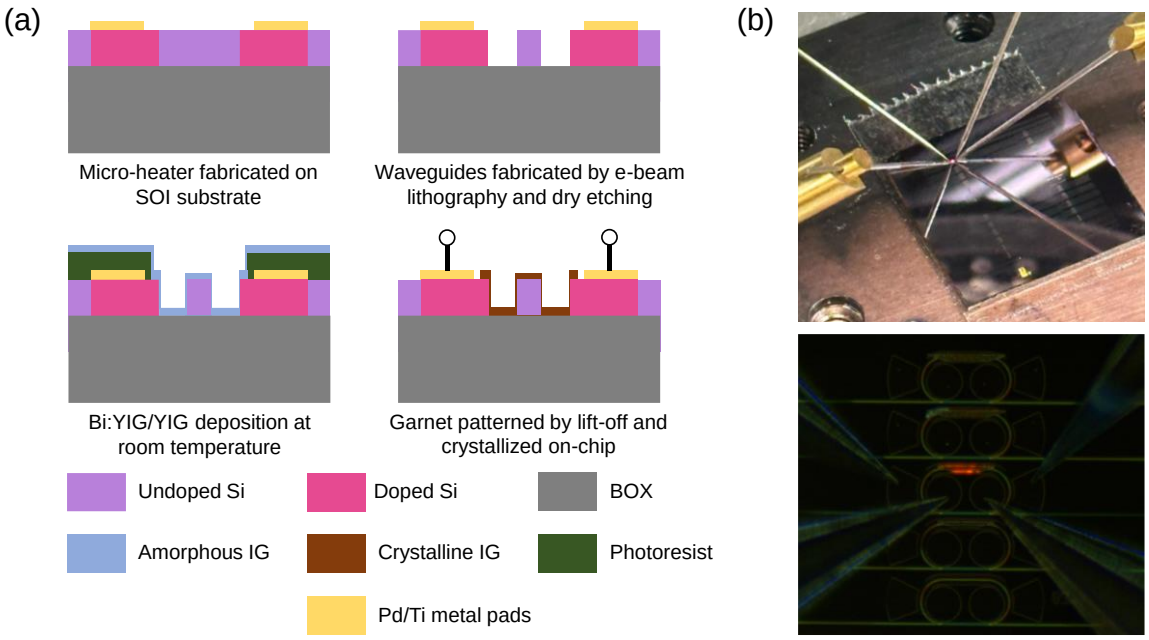


Figure 1. Schematic of the low-thermal-budget monolithic integration of optical isolators on Silicon substrate: (a) Fabrication flow, and (b) on-chip crystallization process.

## 2. RESULT AND DISCUSSION

### Bi:YIG/YIG film characterization

The IG film is directly deposited onto a silicon (Si) substrate using a two-step deposition process. First, a 60 nm layer of YIG is deposited onto the Si substrate at room temperature. Subsequently, a 120nm layer of Bi:YIG ($Bi_{1.5}Y_{1.5}Fe_5O_{12}$) is deposited on top of the YIG seed layer, also at room temperature. The entire film is then crystallized in a rapid thermal annealing chamber at 700°C. The characterization result is summarized in Figure 2. The result verify the feasibility to achieve polycrystalline Bi:YIG/YIG film with room-temperature deposition and post deposition crystallization.

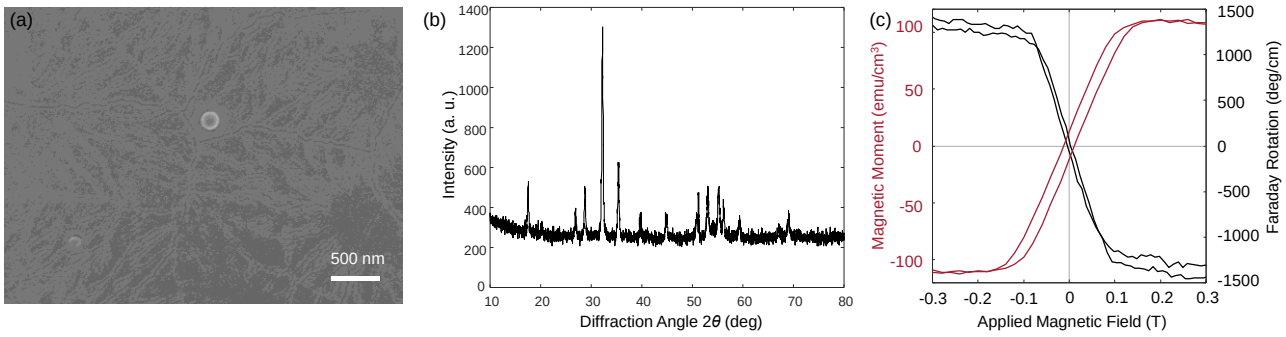


Figure 2. SEM image (a), XRD pattern (b), and Faraday Rotation (c) of the crystallized Bi:YIG/YIG film

### Bi:YIG/YIG on-chip characterization and optical isolation performance

Since the transverse magnetic (TM) mode is required for optical isolators with magneto-optical (MO) material cladding, a strip waveguide configuration is necessary. This configuration, however, prevents the implementation of micro-heaters

directly underneath the garnet, as is commonly done with other photonic devices featuring integrated micro-heaters [5]. To address this, we employed a side-heater design, where the conducting wires run alongside the waveguides, as shown in Figures 1 and 3. The heavily doped silicon appears pink rather than the typical brownish color of undoped silicon. To fully crystallize the garnet cladding on top of the waveguide, the doped silicon wires (serving as heating regions) were heated to 900–1000°C during the crystallization process. Garnet annealing was achieved by applying an AC voltage of 50 V for 180 seconds. Visible damage was observed on the garnet located in these areas (Figure 3b) and on some of the heaters as well. However, since the heaters are designed as one-time-use devices, this damage does not affect the waveguides or the garnet on top of them. The crystallinity of the garnet was verified using Raman spectroscopy. We observed an isolation effect between the forward and backward propagating light, as shown in Figure 3d. The average peak shift from four separate measurements (flipping the transmission direction four times) was 6.2 ± 1.2 pm. This corresponds to a device insertion loss of -25 ± 3 dB and an isolation ratio of 11 ± 2 dB. The estimated Faraday rotation of the garnet was 220 deg/cm.

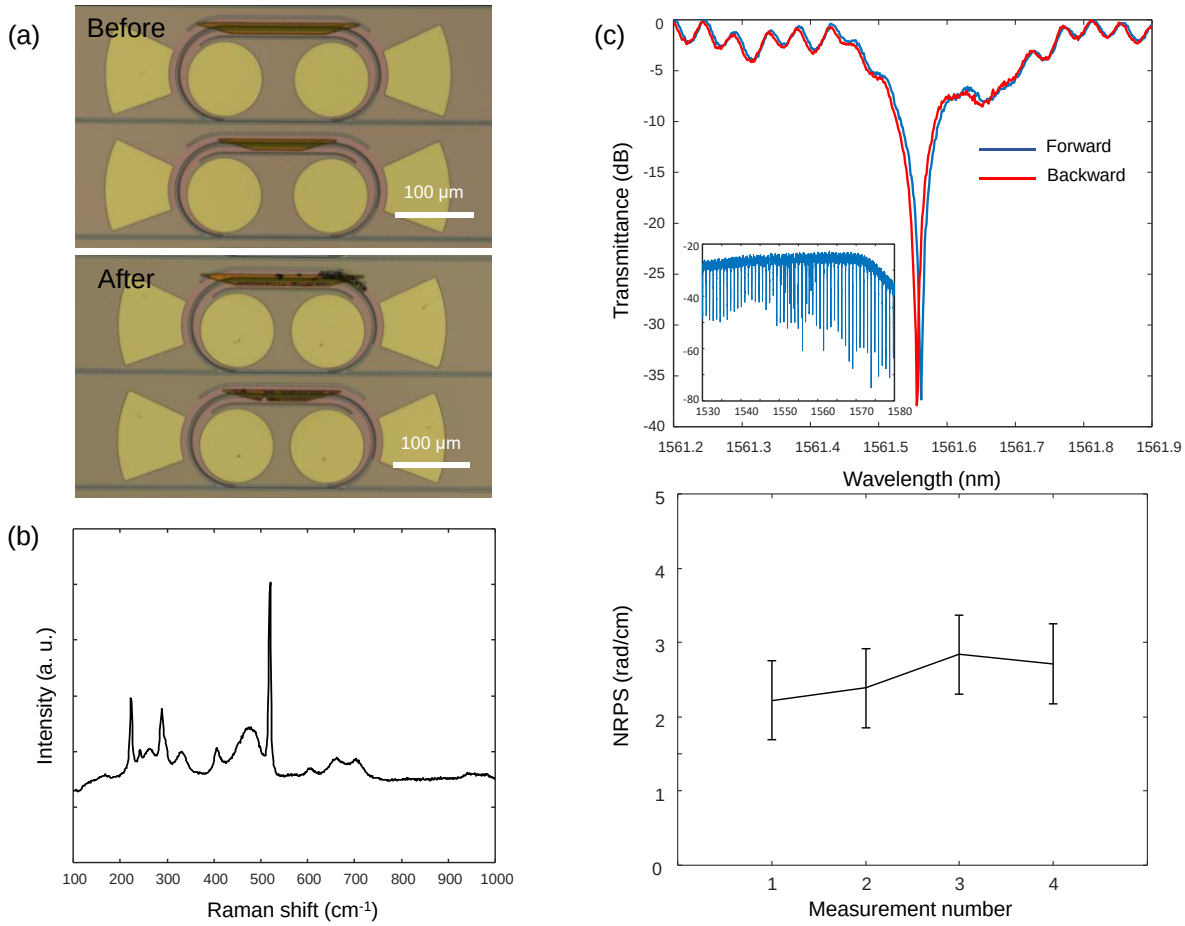


Figure 3. (a) Microscopic pictures of the devices before and after the on-chip IG crystallization. (b) Raman spectrum of the garnet crystallized on-chip, (c) Transmission spectra of TM mode of forward and backward directions with averaged NRPS of four separated measurements.

## 3. DISCUSSION AND CONCLUSION

For the first time, we successfully achieved a CMOS back-end-of-line compatible monolithic integration of optical isolator on SOI substrate with the magneto-optical material crystallized on-chip. However, the results are far from optimal due to limited information about on-chip crystallization conditions and the total optical loss from the on-chip crystallized Bi:YIG/YIG. The temperature across the actively heated area was not uniform, leading to varying levels crystallinity of

the garnet and the potential formation of secondary phase compounds. The YIG seed layer, being closer to the micro-heaters, was crystallized more completely compared to the Bi:YIG layer on top. Since Bi:YIG and YIG exhibit opposite signs of Faraday rotation, the opposing contributions of the YIG layer led to a reduced effective Faraday rotation constant in the film. Further engineering and optimization on heater design [6], annealing conditions, and racetrack resonator design are expected to significantly enhance the overall performance of the optical isolator. In conclusion, we presented the first demonstration of the monolithic integration of magneto-optical (MO) oxides on a CMOS foundry chip with a thermal budget compatible with back-end-of-line (BEOL) integration. Our results confirm the feasibility of CMOS-BEOL-compatible optical isolators, thereby elevating the potential of photonic integrated circuits (PICs) for a wide range of applications.

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