The Smallest Engine Transforming Humanity: The Past, Present, and Future

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Abstract – Semiconductors, amongst one of the most important innovations of the 20th century, have played a pivotal role in the creation of a digitalized, modern industrial society. The global pandemic caused by COVID-19 has further accelerated the already ongoing transition towards a digital economy, and created many new opportunities for the semiconductor industry. It is true that certain concerns about the industry's ability to sustain its growth trajectory do exist, with some believing that Moore's law is no longer valid. As such, it is of paramount importance and also timely that our community comes together to courageously stand up to the challenges at hand, and takes action in a coordinated and concerted manner to advance further for many generations to come.

I. The Future of Tomorrow: Powered by Semiconductors

Amongst all of the 20th century's scientific achievements, no single invention has had a greater impact on our lives than the advent of transistors, or semiconductors. Since the 1960s, when we entered the era of computing, we have witnessed a number of notable transformational shifts, such as the transition to PCs, and then mobile technologies. Humanity is now about to experience the digital transformation, a transition that is further accelerated by the recent pandemic. Following the emergence of COVID-19 in 2020, countries around the world have implemented lockdowns that restricted the movement of people. This has resulted in the "contact-free" economy, also coined "untact economy" increasingly going mainstream. While COVID-19 continues to affect the world, it has also accelerated changes that are now creating previously unexplored opportunities, some of which are explained below.

First, IT technology has become an indispensable and essential part of everyday life. During the last two years, we have witnessed the development of many platforms enabling remote work, learning, and e-commerce, all of which rely on semiconductor technology. We only need to look at the recent pandemic for examples of the enormous impact these technologies can have on society. For example, even during the most restrictive periods of lockdowns, many of us were able to go on with life; all thanks to semiconductor powered products. This may not have been possible 50 years ago.

Second, non-face-to-face experiences are increasingly accelerating the semiconductor-based digital transformation and leading to greater acceptance of IT-driven services within society. Due to COVID-19, consumers have become increasingly accepting of non-face-to-face transactions, while businesses have been able to ascertain the effectiveness of remote work and e-commerce. According to recent studies, digitization has accelerated by three years in the consumer sector, and seven years in the business sector [1]. Additionally, the demand for non-face-to-face engagements continues to remain high, even as COVID-19 related restrictions are slowly being lifted. It is expected that these changes will continue to stay and increase in the future.

For us in the semiconductor industry, the economy's new digitization represents a significant growth opportunity. The transition is driving demand for new devices and its supporting infrastructure. Information gathered across many edge devices, platforms and sensor networks needs to be both stored locally and in the cloud, and also requires a significant increase in high-performance computing power for data analyses and data processing in real-time.

II. Continued Technology Innovation

Despite all the promising trends, the semiconductor industry is at the same time facing challenges. For example, some are questioning the industry's ability to continue its growth trajectory, given that technological advancements are becoming increasingly difficult, incremental, and expensive. Over the past 50 years, improvements to scaling technology have dramatically improved the performance of semiconductors, while simultaneously reducing their cost [2,3]. The number of transistors per wafer increased by almost 10 million times, while the speed of the processors increased by 100,000 times, and the cost per transistor decreased by more than 45% annually (Fig. 1) [4]. However, the environment is now changing due to greater technological difficulties and the increasing investments required for sustained technological progress.

While the industry is facing some challenges at present, this should not be a reason for concern. Technology limits are meant to be broken, and hurdles have always been overcome by our relentless drive for innovation, and an ecosystem-wide, shared effort. Continued collaboration, within the ecosystem and beyond, will ensure that we continue on this journey for decades to come, and help break now, the sub-nanometer wall, an achievement that will be comparable in significance to our entrance into the nanometer era in the early 2000s.

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While it is easy to get caught up in technical details, it is important to note the core functions of semiconductors. As part of our daily lives, we are consistently sensing, processing, and storing information. Modern semiconductor technologies are increasingly mimicking these activities, with CIS (CMOS Image Sensors) responsible for sensing, logic responsible for processing, and storage responsible for remembering. As such, I will next discuss the past, present, and future of continued silicon technology innovation from this perspective.

1. Data Sensing

In recent years, intelligent information-aware devices such as smartphones, sensors, actuators, tablets, and RFID (radio-frequency identification) devices have led the exponential growth of data creation, replication, and consumption. For image sensors in particular, the number of applications continues to expand, moving from visible into invisible spectra such as UV (ultraviolet) for medical diagnosis, NIR (near infra-red) for depth measurement, SWIR (short wave infra-red), and LWIR (long wave infra-red) for "seeing the invisible" imaging.

The primary drivers for CIS technology are resolution and image quality. Over the past 20 years, we have been able to continuously shrink pixel area by using several innovations to structure that resulted in the pixel area shrinking to 1/100th of its initial area (Fig. 2). For 1.4μm pixel, BSI (backside illumination) was adopted to improve SNR (signal to noise ratio) by maximizing sensitivity. For 1.0μm pixel, Samsung Electronics invented a three-dimensionally isolated pixel structure named ISOCELL™ [3,5,6]. ISOCELL™ was introduced to improve the SNR, which it accomplishes by suppressing the optical crosstalk with F-DTI (full-depth, front-side deep trench isolation) and greatly improving FWC (full well capacity) with vertical transfer gate. In addition, innovative multi-pixel structures such as Tetra-cell and Nona-cell help maintain a high SNR, despite reduced number of photons at low light conditions.

Beyond 0.7μm pixel, inter-pixel crosstalk above Si contributes significantly to SNR degradation, which can be suppressed via the use of a grid wall of low refractive index materials, with air grid being the preferred solution. As we continue scaling down to 0.5μm pixel and beyond, one can expect to run into physical challenges related to quantum efficiency and noise. In order to get more light into a small pixel, a novel technology such as MPCR (meta-photonics color routing) with a quantum efficiency of more than 100% is required (Fig. 3) [7]. The readout noise of a pixel transistor presents another challenge and can be reduced by increasing the width of a transistor. We note that device technologies such as FinFET widely used in logic may be implemented to help further reduce this noise.

A suite of novel image sensors are emerging, and are creating new opportunities for the CIS market. For example, these include a) 2PD (two photodiodes) in a pixel for all pixel PDAF (phase-detection auto focus), b) global shutter with no jello effect, and c) high dynamic range sensor. For years, it was impossible to reduce the 2PD pixel pitch below 1.2μm, which was due to AF performance limits stemming from inter-photodiode crosstalk. The use of ISOCELL™ enabled the reduction of 2PD pixel pitch below 1.0μm. In addition, global shutter with an in-pixel DRAM cell capacitor can help achieve very low parasitic light leakage and low noise performance [8]. The dynamic range of mobile and automotive image sensors can be greatly enhanced by employing a large in-pixel capacitor as a reservoir to store overflowing signal electrons.

2. Data Processing

2.1. SoC (System-on-Chip)

Mobile SoCs have, over the course of three decades, evolved significantly. This evolution was not only driven by the ever-increasing wireless communication speed, but also by the exponential growth of digital data demand stemming from new services and applications, such as voice calls, text messages, mobile internet, mobile games, video streaming, video conferencing, AR (augmented reality), VR (virtual reality), and NN (neural network).

In 2019, 5G was first introduced to the world, and now offers a maximum data transfer speed of up to 10 Gbit/sec. This represents a dramatic increase when compared to the 14.4~60 kbit/sec transfer speed offered by 2G in the early 1990s. In order to address the ever-growing performance demands, mobile SoCs have started to incorporate not only modems and general-purpose CPUs, but also application-specific hardware engines such as GPUs and image signal processors. Enabled by advanced logic process technologies, single CPU performance has improved by about 30% annually - 20% from improvements to system architecture, and 10% from an increased clock frequency. The current clock speed of 3GHz is comparable to that of PCs and servers, thus marking a 50x performance increase when compared to mobile SoCs 10 years ago.

The primary drivers for mobile SoCs are performance, power consumption, and form factor. In addition to process technology innovation, three-cluster CPU configuration adopting big.LITTLE heterogeneous multi-core architecture can greatly increase performance without sacrificing power efficiency. Off-loading the workload of a CPU to application-specific processors such as GPUs and NPUs (neural processing units) can enhance the system's power efficiency. It is worth noting that large cache memory capacity, and a memory sub-system with short latency and high bandwidth are critical to improving the performance and power efficiency of parallel processing systems.

Mobile's small form factor, combined with the ever-growing need for circuit functionality, continues to drive the need for innovations for process integration, chip design, and packaging. 3D integration can be used to re-construct the functional SoCs by integration of multiple small chiplets laterally or vertically, and thus increase the potential for improved yield and lower overall cost. This approach is expected to become increasingly important for HPC (high

performance computing) applications.

2.2. Logic

The primary drivers for logic technology are performance, power consumption, chip density, and cost. Around the turn of the millennium, CMOS scaling reached an inflection point, with the rate of power-performance improvements against geometric scaling starting to slow down, and physical limits starting to emerge. Industry and academia then turned their attention to novel materials to continue with CMOS logic scaling (Fig. 4). Samsung Electronics has pioneered the introduction of High-k dielectrics, metal gates [9] and strain engineering with silicon-based heterostructures [10], all of which are examples of novel materials that enabled increased performance and scaling of CMOS technologies in the 45~20nm nodes.

In addition to materials, innovations for MOSFET structures represent another area for breakthroughs in logic technology. FinFET (Fin field-effect transistor) devices, which represent today's state of the art CMOS technology, feature superior electrostatic control of the channel potential, and enable scaling of Vth (threshold voltage) and Vdd (operating voltage) for low power and high-energy efficiency. This is accomplished by utilizing novel process capabilities to pattern fins with small pitch and narrow rectangular shaped vertical profile, and subsequent transistor components in nanometer scale. In 2012, Samsung's foundry business was first to use FinFET in 14nm products [11,12], after which it continued to innovate FinFET design and process technologies for the next generations, down to the 4nm node.

Furthermore, in the 3nm node generation, Samsung Electronics is introducing the world's first GAA (gate-all-around) transistor, also known as MBCFET™ (multi-bridge channel FET) [13,14]. MBCFET™ provides maximum electrostatic control of the channel potential, increasing transistor performance per layout area, and the ability to increase performance by stacking additional channel layers vertically [14,15]. Compared to FinFET, MBCFET™ has intrinsic advantages in a) current drivability, b) reduced mismatch, c) device layout flexibilities, and d) lower Vmin. For generations to come, MBCFET™ is expected to enable continued scaling of power-performance, and improvements to logic technology progress. Moreover, MBCFET™ structures are also expected to help enable future device technologies like 3D-stacked FETs (Fig. 5).

Area and density scaling are, in addition to device performance, also key to increasing computing power and functionality while simultaneously reducing cost, all of which are critical elements of CMOS technology. The advancements in lithography have driven CMOS scaling for years. As an example of these efforts, we at Samsung Electronics have adopted EUV (extreme ultra violet) lithography for the most critical patterning in high volume manufacturing of 7nm and subsequent nodes [16].

Separately, from a design standpoint, DTCO (design-technology co-optimization) techniques have become an important mainstream methodology that can further enhance performance and area scaling without lithographic pitch scaling. Some notable examples of DTCO methodology in recent years include SDB (single diffusion break), cross-couple special constructs, and gate contacts over active [17]. We expect DTCO to continue to contribute to technology scaling, especially as we migrate towards transistor structures that are vertically integrated, and use innovative wire routing processes that mitigate interconnect bottlenecks and RC delays.

The industry is, in order to progress beyond 2nm, already working on ways to overcome many physical and technology limits, with particular attention being given to structures, materials, and co-optimizations, all of which will help fuel advancements in next generation logic technology.

3. Data Storage

3.1. DRAM

Bit density, power consumption, and bandwidth are the drivers of DRAM technology. The advances to DRAM performance over the past 30 years have been significant, with the design rule reducing by almost 100%, DRAM bit density increasing from 64 Mb to 24 Gb, and the supply voltage decreasing from 5V to 1.1V, all of which was accomplished through innovations in structure, materials, and circuits. As an example of these advances, we at Samsung Electronics have recently developed a 14nm DRAM technology with the smallest bit cell area reported to date.

Further breakthroughs for DRAM require Cs (cell storage capacitance) maximization and Cbl (bit-line capacitance) minimization in 1T1C DRAM cell architecture. Even with innovative high aspect ratio cell capacitor structures and high permittivity dielectric materials providing higher Cs, novel approaches such as GIDL (gate-induced drain leakage) suppression and innovative S/A (sense amplifier) circuitry can prove to be beneficial when a reliable data retention time is desired. For example, GIDL can be greatly suppressed by lowering the electric field with dual gate work-function engineering, and by reducing the interface traps with high quality gate oxide. In addition, data-sensing window can be further improved by cancelling out the transistor mismatches in response to the ever-decreasing amount of charge stored in the storage capacitor.

To continue DRAM scaling beyond 10nm, advancements in cell transistor structure, capacitor and process integration are essential. For example, VCT (vertical channel transistor) can provide a very compact unit cell area ($4F^2$). However, side effects such as a high sub-Vt leakage current can result from floating body effects, and should be minimized. A vertically stacked capacitor can also help address the challenges of high aspect-ratio processes without sacrificing cell storage capacitance. To further overcome this, one can aim to develop an innovative multi-layer cell structure that stacks bit cells on top of each other

in a fashion that resembles V-NAND (vertical NAND) cell structures (Fig. 6). In addition to these innovations in structures, one may be able to make further improvements to sensing margin via a novel S/A, which enhances its ability to eliminate pattern noises and to implement two-step offset calibration.

Emerging applications like ML (machine learning) and AI (artificial intelligence) require significantly higher bit density and I/O data bandwidth (Fig. 7). To address this, we at Samsung Electronics have recently introduced several new DRAM architectures, which include a) HBM-PIM (high bandwidth memory based on processing-in-memory), b) AX-DIMM (accelerated DIMM), and c) CXL (compute express link) based DRAM. HBM-PIM can increase system performance gains up to 2.5x, while simultaneously reducing power consumption by 70%. AX-DIMM can increase the energy efficiency of AI accelerator systems by minimizing data traffic between CPU and DRAM. Last, CXL-DRAM can substantially reduce system latency and accelerate processing HPC workloads of data centers by providing memory capacity in the Tera-bits (Tb) range.

3.2. NAND

The primary drivers for NAND technology are density and cost per bit. Since the early 2010s, V-NAND has replaced 2D planar NAND in order to meet the increasing need for higher bit density growth, while reducing its cost. A significant reduction to the number of stored charge limits the ability to further shrink 2D lateral dimension below 15nm.

Innovations for V-NAND cell structure have galvanized vertical stacking of memory cells without needing to shrink the memory bit cell size, thus enabling a density growth rate of +30% in every generation to date, resulting in bit density increasing to approximately 10 Gb/mm^2, and the number of layers stacked increasing to 170 (Fig. 8). At Samsung Electronics, we expect that cost effective manufacturing of V-NAND with over 1,000 stack layers can be achieved via innovations in next generation processes and novel materials.

For next generation V-NAND, the HARC (high aspect ratio contact) etching process and the cell current in V-NAND architecture are critical. Even with new equipment, processes and materials for the HARC etching process, we are still facing great challenges with regards to the shrinkage of vertical pitch for each stack, thus leading to an increased stack height, which needs to be addressed via certain novel structures like multi-stacking. In addition, high trap density and low electron mobility in poly-Si channel string reduces its cell current, resulting in a narrow signal sensing margin. To reduce grain boundaries, innovative processes like recrystallization technology can be used. Additionally, to maximize channel mobility, novel channel materials such as IGZO (In-Ga-Zn-O) need to be explored.

In parallel to the aforementioned innovations, advancements in multibit solution technology such as 4-bit, 5-bit multi-level cells (MLC) and beyond can further increase memory density per unit area (Fig. 9). While 3-bit MLC SSDs have gained significant traction in the storage market, they have not been able to replace lower cost HDDs due to their lower reliability and higher price. In the near future, one can expect that a 4-bit or higher-bit MLC SSDs may have the potential to replace HDDs in the storage market. For successful commercialization and fast market adoption, innovations in control circuitry, which will minimize Vt spread, and novel materials for charge trap layers, are also key.

In order for SSDs to gain even wider adoption in various end-markets and applications, we must simultaneously focus our attention on innovations to I/O bandwidth technology. To meet I/O bandwidth requirements, which are expected to double every three years, greater efforts to address thermal budget reduction and thermal budget decoupling are needed. A wafer-bonding process, as an example, that decouples process thermal budget for memory cells and peripheral transistors is one way to accomplish this.

4. Packaging

The key driver for packaging technology is the density of vertical and horizontal interconnects. After TSV (through silicon via) enabled 3D stacking of DRAM chips in 2010 [18], a virtually unlimited number of vertical interconnects can be constructed due to reduction in bump pitch. Utilizing Si interposer as an intermediate package substrate can provide a ten times larger number of horizontal interconnects structure when compared to a conventional, organic substrate [19]. However, bump connections between vertically stacked chips may restrict the bump pitch to about 20μm, which may be overcome by next generation bumpless direct bonding technology.

As shown in Fig. 10, advanced packaging architectures are expected to lead to the exponential growth of I/O interconnects. For example, a novel chiplet architecture partitions a big die into smaller pieces with fine-pitched short interconnects. This new chiplet architecture is ideal for early adopters of the latest process nodes with a large die size, because splitting a big die into smaller dies may drastically increase manufacturing yield, and results in a larger die count per wafer when compared to monolithic. A cost/benefit analysis of chiplet architecture, which was performed with 3nm node as the process of choice, is illustrated in Fig. 11, and suggests that chiplets become the most cost effective alternative once the die size exceeds 150mm^2.

For chiplet technology, wafer thickness and bump pitch are key. While the current bump technology can achieve bump pitch of about 20μm, a novel bumpless direct bonding technology can achieve bump pitch of 10μm or less. At present, the most advanced HBM (high bandwidth memory) packages have a wafer thickness of less than 40μm, and stack more than 16 dies into a single package. In the near future, zero stress wafer processes, such as laser debonding and plasma dicing will enable the development of wafers thinner than 20μm.

System integration technology is critical for chiplet

architecture, given that it requires the integration of multiple dies. Aside from manufacturing challenges, new design challenges are also emerging. The first challenge relates to thermal engineering. Chiplets are typically packed tightly into a small space, and share a common heat sink. A comprehensive analysis of the heat spreading and dissipation path is required. From a system-cooling standpoint, high-power devices with 500W or more use liquid cooling. Latest research explores thermal solutions for devices with power consumption of several kWs. Applying the liquid channel to the inside of the package allows for power usage of up to 2kW. The feasibility of completely immersing a package is being explored for applications that require more than 2kW. AC noise presents another challenge to the chiplet architecture. Managing the AC noise of multiple dies without a discrete decoupling capacitor also requires a fresh new approach. Silicon device capacitors such as trench capacitor or stacked capacitor are recently being adopted in 2.5D Si-interposer devices. When no Si-interposer is used, a stacked capacitor die or wafer can be directly attached to logic wafers using bumpless direct bonding process. These novel approaches enable a solution for integrating much larger number of devices into the same physical space.

While packaging technology, with fine-pitch bonding and power and thermal integration solutions, will continue to integrate more devices and thus assist the progression of Moore's Law, we expect that it will also enable the fusion of different process technologies such as logic, DRAM, NAND, and MRAM.

III. Three Pillars of Continued Semiconductor Innovation

In the previous chapter, I shared my views on recent technological advancements, and how they are likely going to shape the semiconductor industry's future. In this chapter, I will discuss the three pillars of continued semiconductor innovation, which require collaboration amongst stakeholders such as academia, industry, and governments.

1. Promote the continued development of semiconductor talent

The previously mentioned innovations require an ecosystem-wide emphasis on the development of top-tier talent, which is vital to the competitiveness of the industry.

As such, it is becoming increasingly important for companies and academia to collaborate, and promote academic research and the development of an ecosystem that fosters a new generation of scientists and engineers. With semiconductors further expanding into other industries such as biotech or next generation automotive, we can expect this to also help the competitiveness of many other industries.

Therefore, we should direct our efforts towards ensuring that we not only attract the best and the brightest, but also provide them with access to an exceptional, semiconductor-focused education. Thankfully, our industry has recently witnessed a considerable increase in governmental support, a development that may serve as an excellent starting point for increased industry-academia collaboration.

Additionally, we should consider the creation of a global joint R&D network for AI, Big Data, AR and VR technologies in order to democratize and increase the quality of education, which we expect will increasingly become mainstream in the future.

2. Increase government policies that foster global collaboration

Throughout the years, the semiconductor industry has witnessed an increasing amount of specialization and division of labor, leading to separate regions focusing on different supply chain activities. For example, production equipment and software such as EDA are a US specialization, while Europe specializes in Discrete, Analog and Optoelectronics (DAO), Japan in materials, and East Asia in manufacturing and back-end processing. We are however, since the escalating trade disputes in 2018, followed by a COVID-19 and recent natural disasters globally induced semiconductor shortage, increasingly witnessing attempts of major players to create a self-sufficient supply chain.

These developments are understandable given recent events. Having that said, it is important that we approach this matter very carefully, given that it can have unintended consequences, such as inadvertently driving up the price of chips, and further exacerbating supply chain imbalance with oversupply.

As shown in Fig. 12, the global semiconductor production is expected to increase by 56% from 8.4 million WPM (12" equivalent) in 2020 to 13.2 million WPM in 2030 [20]. The amount of capital needed to support this is significant, and expected to further increase if the world's major economies choose to de-couple. It is projected that the cost of major countries creating their own, insulated supply chain will approximate $1 Trillion USD, while raising the price of chips by 35% to 65%, and lead to higher prices for consumer products [21].

As such, it is important that we avoid the allocation of excessive capital to areas that are not innovative. While it is true that the pandemic highlighted certain risks stemming from a global supply chain as currently present, we should not overlook the benefits of it. Therefore, it would be best for the industry to come together, and find ways to improve the resilience of the existing supply chains, while ensuring that the underlying market dynamics are not distorted.

3. Develop eco-friendly products and manufacturing capabilities

Climate change is an inevitable and urgent global challenge that requires a decisive, industry-wide effort. Fig.

13 shows that, in 2020, over 70% of the world's greenhouse gas emissions are generated by the energy sector, pointing out that power consumption is the leading cause for global warming [22]. Additionally, it is predicted that the power consumption of the ICT (information and communication technology) industry, which includes data centers and networks, will increase dramatically [23]. As it stands, it is estimated that the ICT industry accounts for approximately 9% of the global power consumption, a figure that they predict will increase to 20% by 2030 [24]. As such, the ICT industry should direct its efforts towards reducing its current and future carbon footprint. Here, RE100, a global initiative to engage, support and showcase global companies committed to using 100% renewable power is notable, as it helps companies gain a better understanding of the advantages to being 100% renewable, and encourages peer-to-peer learning as they work towards achieving their climate reduction goals.

It is well known that the manufacturing of semiconductors is energy intensive. Given semiconductor's current and projected prevalence, it is important that we continue reducing the carbon footprint of its manufacturing processes and the devices themselves.

IV. Semiconductors Will Lead The Future

In short, the commercialization of high-end and high-speed electronic devices has led to significant performance improvements, while simultaneously achieving scaling for size reductions. Modern society as we know it would not exist without electronic devices, and semiconductors will continue to play a critical role in a future that we expect to be further transformed by technologies such as AI, autonomous driving, and edge computing.

The importance of semiconductors in today's day and age cannot be overstated. Semiconductors have greatly contributed to the well-being of society, and we expect future innovations to have an even greater impact. Although the industry is facing some challenges at present, we at Samsung Electronics are confident that these can be overcome by the industry's relentless drive for innovation, and mark the beginning of a tremendous, transformational journey. As an industry, we will continue to pursue our ultimate goal, which is to develop solutions that help the world's citizen live better lives, and address society's most pressing problems.

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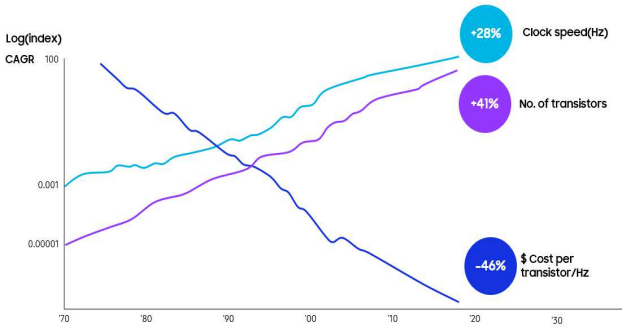

Fig. 1. Trends for number of transistors per microprocessor, performance, and cost [4].

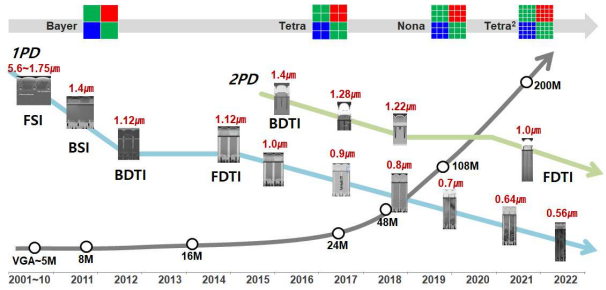

Fig. 2. CIS pixel technology evolution.

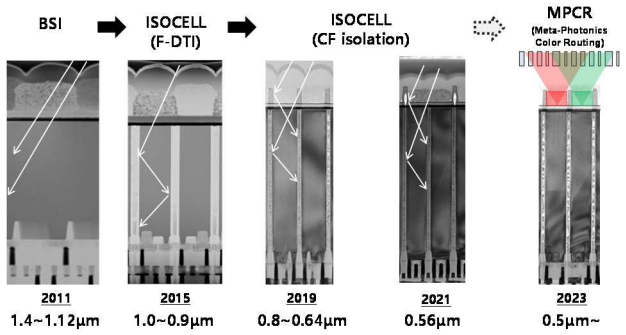

Fig. 3. CIS pixel optical structure innovations.

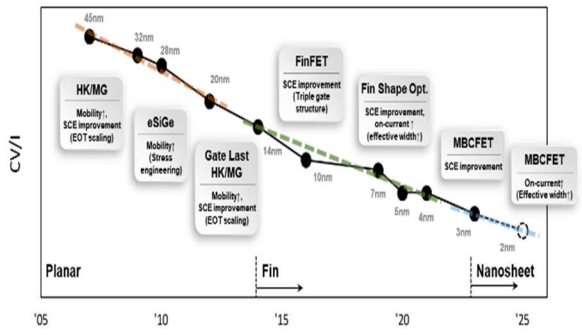

Fig. 4. Trend for Logic standard cell performance.

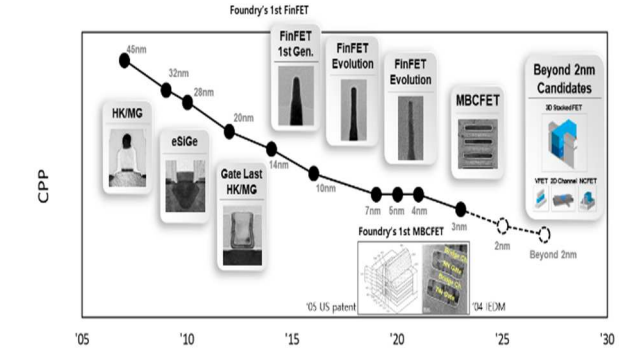

Fig. 5. Logic technology evolution.

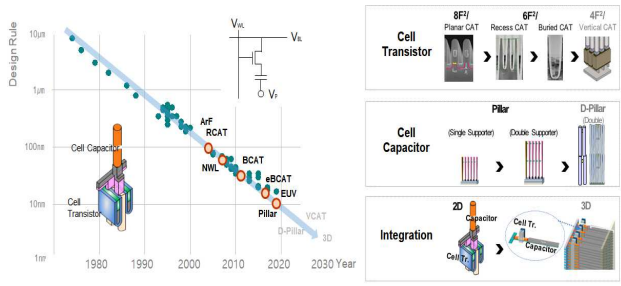

Fig. 6. DRAM technology evolution and structure innovations.

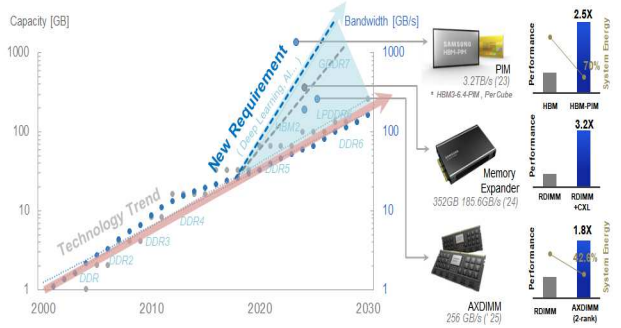

Fig. 7. Trends for DRAM memory capacity, I/O bandwidth and architectural solution.

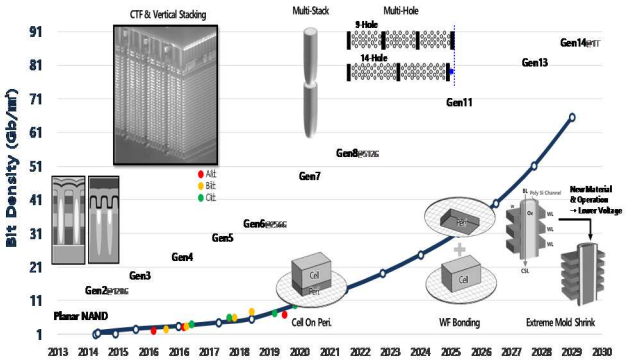

Fig. 8. Trends for NAND memory bit density and technology evolution.

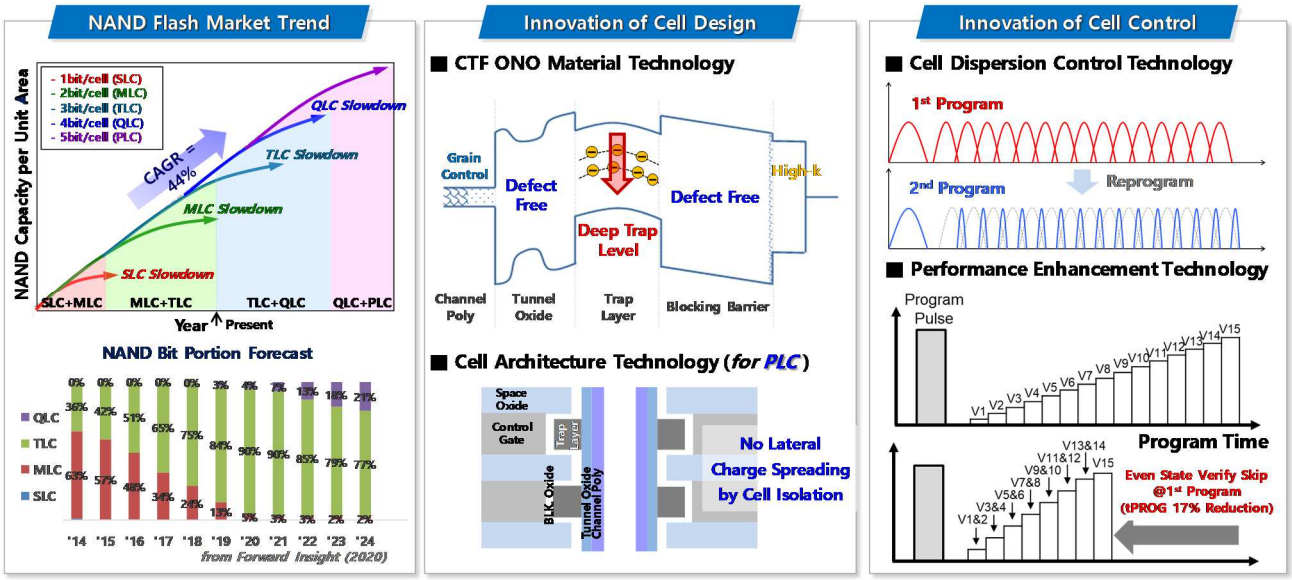

Fig. 9. Trends for NAND memory density per unit area and MLC (multi-level cell) technology innovations.

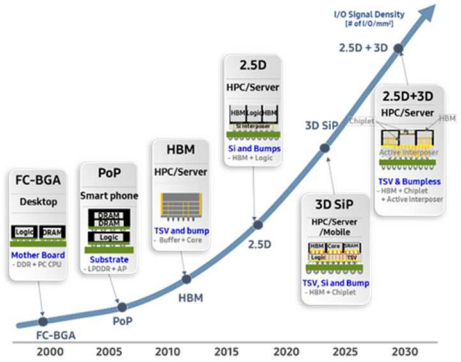

Fig. 10. Trends for I/O signal density and package technology evolution.

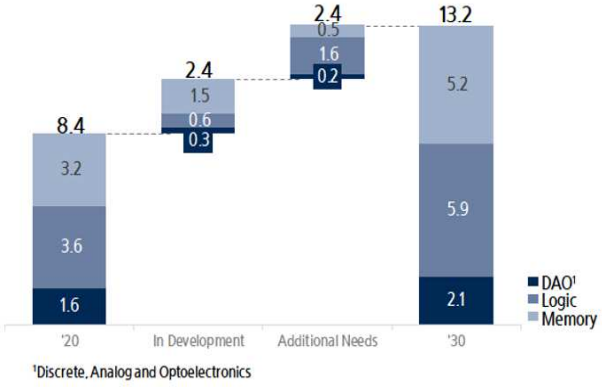

Fig. 12. Breakdown of projected incremental 2020 ~ 2030 global capacity by development status (M wpm, 12" equivalent) [20].

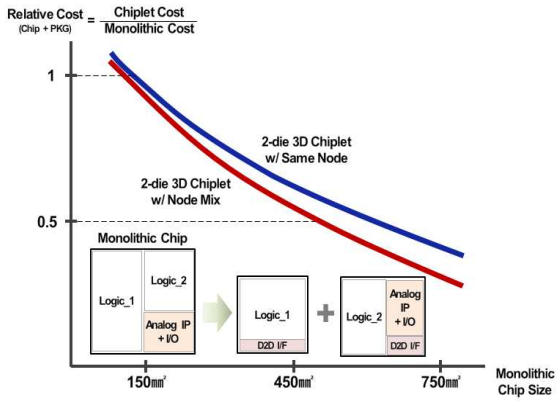

Fig. 11. Relative cost of chiplet architecture against monolithic chip with various chip sizes and technology nodes.

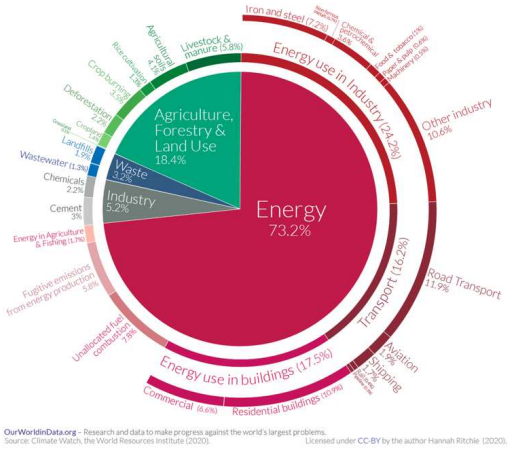

Fig. 13. Global greenhouse gas emissions by sector [22].