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High-density wiring solution for 500-qubit scale superconducting quantum processors

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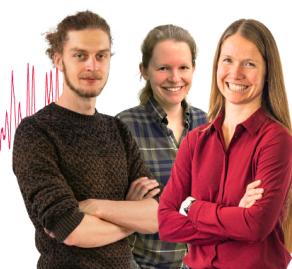
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ABSTRACT

Scaling superconducting quantum processors to hundreds of qubits is essential for demonstrating quantum advantage and implementing quantum error correction codes with larger distances. A key challenge is integrating control and readout wiring without compromising cryogenic or electronic performance. To address this, we performed a systematic analysis of the thermal budget within a dilution refrigerator and developed high-density 0.5 mm SCuNi–CuNi coaxial cable sets optimized for heat load management. This enables the integration of 696 control lines and 40 readout amplification chains into a dilution refrigerator with a cooling power of 1 mW at 100 mK, maintaining a stable base temperature of \sim 8 mK for over a year. We validated the platform's performance with two large-scale quantum processors: a 540-qubit processor with an average T_1 of 35 μ s and a 156-qubit processor with 182 tunable couplers, achieving average fidelities of 99.9% for single-qubit gates and 99.0% for two-qubit gates. This study demonstrates a viable high-density wiring solution for controlling and measuring processors at the 500-qubit scale and provides critical engineering insights for larger-scale quantum computing systems.

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I. INTRODUCTION

Quantum computing holds significant promise in certain computational problems that are intractable for classical computers.^{1,2} Among the leading platforms,^{3–6} superconducting quantum circuits⁷ have made substantial progress, with processor scale now reaching over 100 qubits.⁸ This advancement has enabled several key milestones, including demonstrations of quantum computational advantage,^{5,9} implementation of quantum error correction below the surface code threshold with distance $d = 7$,¹⁰ and complex quantum simulations utilizing up to 127 qubits in conjunction with error mitigation techniques.¹¹ However, achieving quantum advantage for practical applications and constructing fault-tolerant logical qubits necessitates a further substantial increase in processor scale.

Scaling superconducting quantum processors presents significant challenges for both chip fabrication and packaging technologies,¹² as well as the supporting cryogenic infrastructure.¹³ Specifically, scaling up processor control and measurement requires integrating proportionally more control and readout lines within a single dilution refrigerator (DR). Standard wiring solutions, such as SMA connectors with typically 13–16 mm spacing, limit wiring density, restricting the number of lines in a DR. In addition, the increased number of readout lines necessitates more cryogenic low-noise amplifiers (LNAs), with each amplifier contributing a heat load of \sim 15 mW, leading to elevated heat loads at the 4 K stage. This increased heat load presents several engineering challenges. First, excessive heat deposition on the quantum processors increases the effective thermal noise of the qubits, resulting in significant decoherence. Second, the heat load at various stages, particularly the

4 K stage and still stage, compromises the stability of the dilution circulation.

Researchers have begun to address these engineering challenges. Krinner *et al.*⁸ provided valuable engineering guidelines for cryogenic wiring in 2019, while alternative approaches such as photonic interconnects and multiplexing techniques are under active investigation.^{14–16} We also noticed that high-density wiring (HDW) solutions are commercially available from companies such as Delft Circuits and Bluefors. In addition, Ref. 17 provides systematic experimental results aimed at evaluating the equivalence of flexible strip line and coaxial cables for superconducting qubit control and readout. However, there remains a deficit in practical engineering efforts that evaluate the ultimate wiring capacity of contemporary DRs. Furthermore, comprehensive heat budget analysis and optimization specifically targeting wiring densities approaching the 1000-line scale are lacking.

In this study, we report the successful integration and sustained operation of 696 control lines and 40 readout amplification chains within a commercial DR over a period exceeding one year. The system maintained a stable base temperature of 8.1 mK, with a fluctuation of ~ 0.4 mK. During the integration process, we observed that using standard 0.86 mm SCuNi–CuNi (silver-plated CuNi inner conductor–CuNi outer conductor) coaxial cables beyond 400 lines introduced a significant passive heat load to the still stage. This excessive heat load caused an increased gas flow rate, thus compromising the turbo pumps' performance and disrupting stable dilution circulation. These observations led to a comprehensive thermal budget analysis across all stages, with particular focus on the 4 K, still, and mixing chamber (MC) stages. To address the heat load issues, we developed customized 0.5 mm SCuNi–CuNi high-density coaxial cable sets. We also replaced 50% of the conventional InP-based High Electron Mobility Transistor (HEMT) with SiGe Heterojunction Bipolar Transistor (HBT) amplifiers, reducing power dissipation by over 10 mW per amplifier. The details of the bandwidth, gain, noise temperature, and working conditions for these two types of LNAs can be found in the [supplementary material](#), Sec. S-II.

To rigorously evaluate the performance of this integrated cryogenic system, we installed and characterized two distinct quantum processors. The first processor, consisting of 540 fixed-frequency qubits, exhibited an average longitudinal relaxation time (T_1) of 35 μ s. The second processor, which consists of 156 fixed-frequency qubits and 182 tunable couplers, showed improved coherence properties with an average T_1 and the transverse relaxation time (T_2^{Echo}) of 77 and 58 μ s, respectively. We performed comprehensive calibration of both single- and two-qubit gates on all functional qubits. Using standard randomized benchmarking (RB), we achieved an average single-qubit gate fidelity of 99.9%. For the two-qubit controlled-Z (CZ) gates, interleaved RB demonstrated an average fidelity of 99.0%. The 156-qubit processor has been successfully deployed as a quantum computing cloud platform (Baihua, <https://quafu-sqc.baqis.ac.cn>), providing reliable public access for over a year with stable performance.

These results demonstrate that our developed high-density wiring (HDW) scheme effectively meets the control and measurement requirements for superconducting quantum processors at the 500-qubit scale. This study establishes a robust experimental foundation and provides valuable engineering guidelines for scaling quantum computing systems.

II. HEAT LOAD ANALYSIS

The primary objective of this study is to develop a control and measurement system for a 540-qubit quantum processor. This processor consists of 540 fixed-frequency transmons arranged in a 36×15 lattice. Each row of 15 qubits shares a common transmission line for readout, with their resonators coupled to the transmission line to enable simultaneous readout operations. This architecture requires 540 control lines, 36 read-in lines, and 36 read-out amplification chains within a single DR. To improve readout efficiency, we incorporate a Josephson parametric amplifier (JPA) as the pre-amplifier in each readout chain, which necessitates additional pump lines. In addition to the near quantum-limited amplifier, there are two cascade amplifiers. Typically, the second stage LNA is installed at the 4 K stage, and the third stage amplifier is installed at room-temperature. However, we found that the varying ambient temperature causes drifting of the gain and signal phase of room-temperature amplifiers (measured gain and phase drifting data are illustrated in the [supplementary material](#), Sec. S-V), leading to a frequent readout calibration. Therefore, the third stage amplifiers are installed at the 50 K stage in the DR.

We employ a commercial DR (model XLD1000sl, Bluefors) as our cryogenic infrastructure, providing six ISO100 and four KF40 flanges for wiring. To fulfill the signal routing requirement of at least 648 lines, we need to install four sets of HDW cables, each containing 168 lines, and two sets of SMA cables, each containing 32 lines. The KF40 flanges are dedicated to twisted-pair DC wire connections. Final experimental detailed configuration specifications are provided in Sec. III A.

Prior to the installation of cables and amplifiers, we conducted a comprehensive thermal analysis to assess the feasibility of the HDW scheme, considering two distinct contributions as follows:

- *Passive heat load.* This results from thermal conduction through the cables between different temperature stages. Our analysis focuses specifically on the additional heat load introduced by the cable assemblies.
- *Active heat load.* This originates from the power dissipation of microwave and DC signals in the control lines.

A. Passive heat load

The SCuNi–CuNi coaxial cable is the standard choice for inter-stage wiring in cryogenic systems. This cable features a silver-plated CuNi alloy inner conductor, a CuNi outer shell, and a polytetrafluoroethylene (PTFE) dielectric layer between them. We begin our analysis with the commonly used cable diameter of 0.86 mm. Thermal power transferring through the cable is described by the following formula:¹⁸

$$P_i = \int_{T_{i-1}}^{T_i} \frac{\rho_o(T)A_o + \rho_d(T)A_d + \rho_c(T)A_c}{L_i} dT, \quad (1)$$

where ρ_o , ρ_d , and ρ_c are the thermal conductivities of the outer conductor, the dielectric PTFE, and the inner conductor, respectively. A_o , A_d , and A_c are their corresponding cross section areas. L_i is the length of the cable between the $(i-1)$ th stage and the i th stage. The thermal conductivity of the CuNi alloy is referred to in Ref. 19, while the thermal conductivity of PTFE is provided by the cable manufacturer Hermercs Co., Ltd. According to Eq. (1), the

TABLE I. Passive heat load budget for different types of 1000 cables.

Stage	Space (m)	Cooling power	0.86 mm cable		0.5 mm cable	
			L (m)	Power	L (m)	Power
50 K	0.193	110 W	0.243	~11.07 W	0.507	~2.15 W
4 K	0.271	4 W	0.321	~0.38 W	0.585	~0.084 W
Still	0.233	~50 mW	0.283	~2.55 mW	0.547	~0.53 mW
CP	0.154	...	0.204	~0.53 mW	0.311	~0.14 mW
MC	0.154	~30 μ W	0.204	~21.81 μ W	0.311	~5.60 μ W

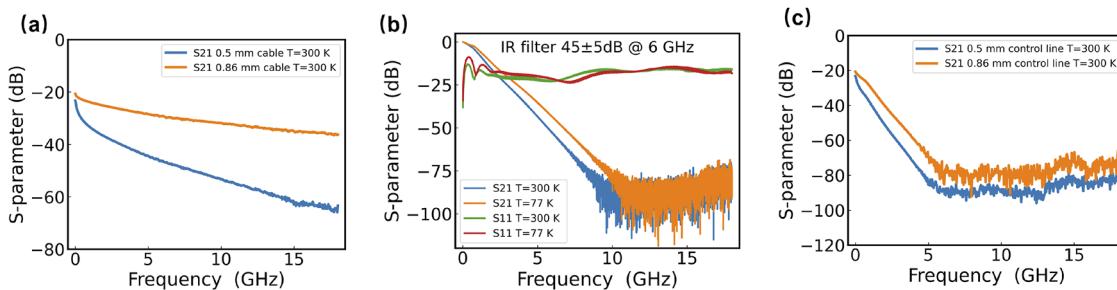


FIG. 1. Measured S-parameters of the HDW lines. (a) Transmission characteristics of 0.86 mm SCuNi–CuNi cables (orange) and 0.5 mm SCuNi–CuNi cables (blue). (b) Transmission and reflection characteristics of a HIR filter under room temperature (blue for $|S_{21}|$ and green for $|S_{11}|$) and under LN_2 temperature (orange for $|S_{21}|$ and red for $|S_{11}|$). (c) Transmission characteristics of fully installed control lines (orange for 0.86 mm SCuNi–CuNi cables and blue for 0.5 mm SCuNi–CuNi cables).

thermal transfer power between different cold stages is calculated and summarized in Table I.

The calculated passive heat load per cable between the 4 K and still stages is about $2.55 \mu\text{W}$. For our configuration, the total passive heat load for the still stage is estimated to be about 1.8 mW . The heat load per cable between the cold plate (CP) and the MC stage is calculated to be about 21.8 nW . As a result, the total passive heat load for the MC stage is $\sim 15 \mu\text{W}$, and its temperature can be raised to $\sim 13\text{--}15 \text{ mK}$ according to the cooling power measurement results.

We considered the following approaches to mitigate the cable-induced passive heat load into the MC stage:

- Increase the length of the cable between the CP stage and the MC stage.
- Reduce the diameter of the cable.
- Change the material of the conductor with lower thermal conductivity.

A straightforward way is to change the CuNi material into a superconducting material (e.g., NbTi alloy), which has very poor thermal conductivity after the superconducting transition. However, such a solution will greatly increase the cost, especially for our scale of integration. A much more economical solution relies on the other two approaches. From Eq. (1), the most efficient way is to reduce the cable diameter since the power is proportional to its square. To further reduce the heat load, we could increase the cable length at the same time. Therefore, we developed a 0.5 mm SCuNi–CuNi cable and increased the cable length to an appropriate value. The total passive heat load induced by the cables to the MC stage can be reduced to about $5.6 \mu\text{W}$. Compared to the original 0.86 mm cable, the total attenuation (after removing the 10 dB attenuator on the still stage)

of the 0.5 mm cable is increased by about 10 dB, which is acceptable for qubit driving. Typical S-parameters of these cables are shown in Fig. 1(a), while the simulated S-parameters can be found in the supplementary material Sec. S-I.

B. Active heat load

The active heat load is generated by dissipation in the control lines during the application of driving or biasing signals. Proper attenuation of the microwave and DC signals is required to suppress the noise from higher temperature stages. In principle, the attenuation value is determined by the ratio between the black-body radiation spectra of the two relevant temperatures,²⁰

$$A_{i,\text{ref}} = -10 \log \left(\frac{e^{\hbar\omega/k_B T_i} - 1}{e^{\hbar\omega/k_B T_{i-1}} - 1} \right). \quad (2)$$

The vast majority of the energy is dissipated primarily within the attenuators, which are installed at appropriate cold stages. Furthermore, since these attenuators also serve as thermal anchors for the inner conductors of the coaxial cables,²⁰ 0 dB attenuators are also added on the cold stage, even where no attenuation is required.

In addition to the attenuators, suitable filters must also be installed on the signal lines to suppress unwanted frequency bands. These filters should be inserted as close as possible to the quantum processor. In a traditional scheme from Ref. 21, 8 GHz low-pass filters are inserted for the XY-control and read-in/out lines individually, and 500 MHz low-pass filters are installed for the Z-control lines. Furthermore, infrared (IR) filters^{22–24} are necessary for suppressing spurious infrared photon scattering in the cables so as to improve the coherence properties of the qubits.

To simplify the filtering configuration and meet all the filtering requirements listed earlier simultaneously, we developed a heavy IR (HIR) filter with a CR-124 absorber. Its transmission characteristic is shown in Fig. 1(b). The HIR filter exhibits negligible attenuation at DC, while providing 20–50 dB of attenuation within the typical qubit and readout frequency band. For higher frequencies up to the infrared band, the filter absorbs severely, reducing the signal to an undetectable level. Therefore, only one HIR filter is necessary and is installed on each control line or read-in line, providing a typical attenuation value of 45 dB at 6 GHz. The transmission characteristic of a control line with a HIR filter is shown in Fig. 1(c).

Our attenuation configuration is shown in Fig. 2(a). To achieve a π -pulse length ranging from 10 to 30 ns, the driving strength is estimated to be $\Omega_0 = \pi^2/(2t_p) \approx 2\pi \times 26.2 - 2\pi \times 78.5$ MHz, where t_p is the π -pulse length, and the pulse has a cosine envelope. The corresponding driving power is then estimated to be $P_{\text{avg}} = P_{\text{peak}}/2 = \hbar\omega_0 T_1^{\text{lim}} \Omega_0^2/8 \approx -67.4 \sim -76.9$ dBm. Here, we assume a driving induced T_1 limit of $T_1^{\text{lim}} = 2$ ms and a qubit frequency of 4.5 GHz. The total attenuation value of the control lines at 4.5 GHz, according to the measured $|S_{21}|$ result shown in Fig. 1(c), is about -60 dBm. As a result, the input driving power is about -17 to -7 dBm. We can further assume a typical duty cycle of 30% (estimated by a RB sequence) for the driving signal during the execution of quantum algorithms. The duty cycle is the ratio of the driving or biasing time to the whole quantum circuit execution time.

The active heat load on each qubit driving line is then estimated to be about 6–60 μ W.

DC-pulse or biasing is required to bias the idle frequency of the qubit or the JPA, adjust the tunable coupler to turn off the residual ZZ-interaction, and realize the two-qubit CZ gate, etc. In our design, the mutual-inductance between the Z-control line and the SQUID loop is about $0.5 \Phi_0/\text{mA}$. The qubits' idle frequencies are usually near their sweet points. The couplers' ZZ turn-off points are usually 1.5 GHz away from their sweet points, corresponding to a flux bias of about $0.2 \Phi_0$ and a current bias of 0.4 mA. To implement a two-qubit CZ gate, a fast Z pulse is applied to the coupler's Z-control line. This pulse requires a current bias of about 0.4 A. Assuming a typical pulse duration of 50–100 ns and a duty cycle of 50%, the active heat load on each Z-control line is then estimated to be about 400 μ W.

Another dissipation source comes from the JPA pump line, consisting of a DC bias current and the pumping microwave near its critical point. A typical bias current is 2–5 mA, and a typical pumping power is 0–10 dBm. As a result, the active heat load on each JPA pump line is about 1.2–11.2 mW.

The LNAs installed at the 4 K stage also introduce considerable heat during functioning. For the InP HEMT, the typical power consumption is about 16 mW. If all the readout lines are configured to install the InP HEMTs, the total heat load caused by them at the 4 K stage is over 600 mW. To alleviate this heat load, we replaced 20 of them with SiGe HBT amplifiers, which introduce only about 2 mW

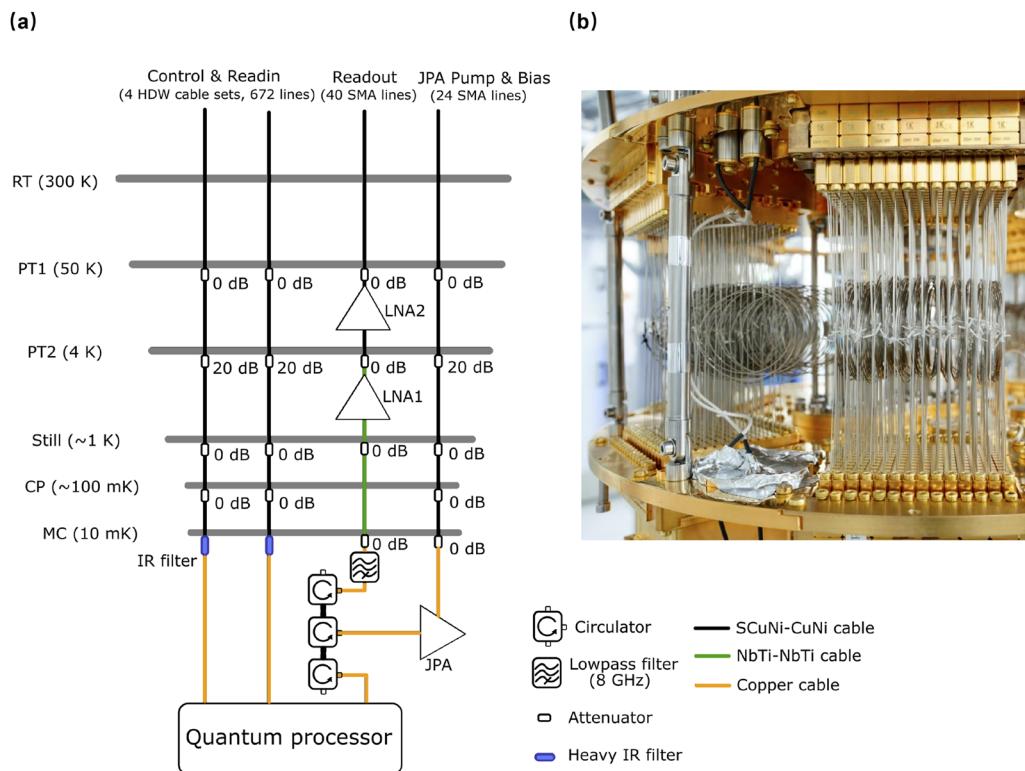


FIG. 2. Schematic (a) and photograph (b) of the HDW configuration. The four sets of HDWs (672 lines) are used for routing the XY/Z control and read-in signals. 40 SMA lines are configured as readout chains, and the other 24 SMA lines are configured as the JPA pump lines.

TABLE II. Calculated active heat load by control lines.

Stage	XY-pulse ^a Power	Z-pulse or bias ^b Power	JPA pump ^c Power	Amplifier ^d Power
50 K	~6 W
4 K	3–30 mW	~200 mW	48–448 mW	~360 mW
Still	0.48–4.48 mW	...
MC	3–30 μ W

^a Assuming 500 qubits are driven simultaneously.

^b Assuming 500 couplers are biased simultaneously.

^c Assuming 40 JPAs are pumped simultaneously.

^d With 40 amplifiers on.

while working. Furthermore, we installed the third stage amplifiers at the 50 K stage. It contributes a heat load of about 150 mW each.

Based on the above-mentioned analysis, the total active heat load on the control lines and their distribution are calculated and shown in **Table II**. Here, we estimate the total active heat load assuming 500 qubits, 500 couplers, and 40 JPAs are driven or biased simultaneously so as to properly evaluate the heat load when a larger quantum processor is in operation.

III. CONFIGURATION AND TESTING

In this section, we describe the configuration of the HDW system, as well as the results and discussion of heat load testing at low temperatures.

A. Wiring configuration

To achieve the control and measurement of larger-scale quantum processors, we installed 672 control or read-in lines, 40 read-out lines, and 24 JPA pump lines within the 1 mW refrigerator. Four sets of HDWs using super-small miniature push-in (SSMP) connectors were installed on the ISO100 flanges (each set comprising 168 cables). In addition, two sets of cables using SMA connectors were installed on the other two ISO100 flanges (each set comprising 32 cables), with 40 cables employed as readout amplification chains and the other 24 as JPA pumping lines. **Figure 2(a)** illustrates the whole wiring configuration, while **Fig. 2(b)** shows a photograph of the installed cables.

The 50 K stage amplifiers are also illustrated in **Fig. 2(b)**. These amplifiers we developed are low-noise and low-power-consumption devices that can work under the liquid-nitrogen (LN_2) temperature.

Temperature fluctuations at the 50 K stage are typically maintained below 0.1 K for a DR, significantly lower than those of the ambient temperature. As a result, the gain and other properties of the amplification chain are greatly stabilized in such a full cryogenic configuration.

The 0.86 mm SCuNi–CuNi coaxial cables above the 4 K stage and the 0.86 mm NbTi–NbTi cables below the 4 K stage are employed as the read-out lines, as illustrated in **Fig. 2(a)**. A three-junction isolator is inserted into each readout line at the MC stage to prevent thermal noise from upper stages while routing the readout signal to the amplification chain with minimal insertion loss (≤ 0.2 dB per junction).

For the control lines, we first installed four sets of 0.86 mm SCuNi–CuNi HDW cable sets. However, after several runs of cooling down tests, we found that the temperature of the 4 K stage rose by about 1 K and that the temperature of the still stage rose by about 0.5 K. The temperature increase of the still stage considerably raises the flow rate of the circulating helium gas, resulting in the load of the turbo pumps increasing to over 200 W, near their limit.

We evaluated the actual passive heat load caused by all the wiring by applying a current to the still heater (a resistor of $R = 120 \Omega$) of an almost empty refrigerator with the same cooling capacity. When the still heater power reaches 22 mW, the still stage temperature and the flow rate come close to those of the wired system. The measured passive heat load is about an order of magnitude higher than the calculated value, indicating that a considerable excess heat load is introduced by the cables. One of the possible reasons is the actual temperature gradient between the 4 K stage and the still stage is much higher than that shown on the thermometers because of the limited efficiency of the thermal anchor of the cables, especially their inner conductor. Another reason is the practical heat conductivity of CuNi alloy is much higher. Based on the open heat quality data from Keycom Corp., we estimate the heat load from the 4 K stage to the still stage to be about $33 \mu\text{W}$ for each line. For all 696 cables, the total heat load is added to about 22.9 mW. Considering the former reason together, the actual passive load may be even higher.

Crosstalk is a very important issue for the control and measurement of superconducting qubits. To assess the cable induced crosstalk, we measured inter-line crosstalk using a vector network analyzer and obtained results of < -80 dB in the range of 0.01–14 GHz. As a result, we can safely neglect the crosstalk introduced by the cables. The results and scheme for the cable crosstalk measurement are provided in the [supplementary material](#), Sec. S-III.

TABLE III. Heat load test for four different configurations.

Stage	Bare	Configuration 1		Configuration 2		Configuration 3		Configuration 4 ^a	
		0.86 mm × 672	0.86 mm × 504 + 0.5 mm × 168	0.86 mm × 336 + 0.5 mm × 336	0.5 mm × 672				
50 K	35.8 K	40.0 K	39.5 K	39.4 K	40.8 K				
4 K	2.92 K	3.42 K	3.35 K	3.26 K	3.46 K				
still	1.02 K ^b	1.01 K	0.93 K	0.88 K	0.91 K				
MC	8 mK	15.7 mK	12.6 mK	11.6 mK	8.1 mK				

^aWith 40 amplifiers on.

^bWith still heater on.

B. Heat load tests

To mitigate the passive heat load, we changed all the HDW cable sets to thinner ones with a 0.5 mm outer diameter. The cross section area of this cable is reduced by about 66.7% compared to that of the 0.86 mm cable. Furthermore, we also increased the cable length by double winding in the middle of the cable ("O²"-folding), with a winding diameter of about 5 cm. As a result, the heat power from the 4 K stage to the still stage is reduced by about 80% compared to the 0.86 mm cable case. The passive heat load for other cold stages also decreases significantly, as shown in Table I.

To fully evaluate the passive heat load of the HDW cable sets, we conducted four rounds of cooling down experiments with different wiring configurations. First, we cooled the system with four sets of 0.86 mm "W"-folding HDW cables and two sets of SMA cables. After the system went into a stable circulating state, we recorded the temperature of all the stages. Then we changed one set of the HDW cables into a 0.5 mm one. We found that the temperature of all the stages decreased. As a result, we changed all the HDW cable sets into the thinner ones.

The cooling down test results are shown in Table III. After all the HDW cable sets were changed to 0.5 mm ones, the temperatures of the 4 K stage, the still stage, and the MC stage were controlled in an acceptable range.

IV. APPLICATION RESULTS

To demonstrate the practicality and performance of the HDW system, we first characterized the coherence properties of a 540-qubit quantum processor and then characterized a 156-qubit processor and fully calibrated the single- and two-qubit gates of all the functional qubits in it. Calibration procedures are similar to those in Refs. 5, 25, and 26, with more details discussed in the supplementary material, Sec. S-VI.

A. Characterization of a 540-qubit processor

According to the 540-qubit processor configuration described in Sec. II, it requires at least 540 control lines, 36 read-in lines,

and 36 read-out lines to control and measure all these qubits individually. We connected all the signal lines required and then characterized the qubits to evaluate the actual performance of the HDW scheme. First, we measured the spectra and the time-Rabi oscillations of all the qubits to determine their $\pi/2$ -pulses. After that, we characterized their coherence properties, including T_1 , T_2^{Ramsey} , and T_2^{Echo} . Cumulative histograms of these coherence properties of all the qubits are shown in Fig. 3(a). An average T_1 of 35 μs was obtained, which indicates that the noise level is well controlled. Further discussion of the decoherence properties appears in the supplementary material, Sec. S-VII. The characterization process lasted approximately one month, with stable DR circulation and a base temperature maintained below 10 mK.

B. Calibration of a 156-qubit processor

Another 156-qubit quantum processor was then installed, characterized, and fully calibrated. This processor includes 156 fixed-frequency transmons and 182 tunable transmons working as couplers. The qubits are arranged in a 12×13 array; each row of them shares a readout transmission line. On average, each qubit connects to 2.38 couplers. Figure 3(b) shows the decoherence of the qubits, with average $T_1 \approx 77 \mu\text{s}$, $T_2^{\text{Ramsey}} \approx 30 \mu\text{s}$, and $T_2^{\text{Echo}} \approx 58 \mu\text{s}$. Figure 3(c) shows the error rates of single-qubit gates, state readouts, and two-qubit CZ gates after fine calibration, reaching the average fidelities of 99.9%, 94.0% (for $|1\rangle$), and 99.0%, respectively. Although each qubit shares its control line with one of the nearby couplers in this processor, which is a relatively compact and effective design, the total 182 channels of DC pulses introduce a considerably increased active heat load when compared to the 540-qubit processor, as analyzed in Sec. II B. Furthermore, this processor based on the HDW scheme has been serving as a quantum computing cloud platform for over a year, during which the DR stably circulated, and the base temperature remained under 10 mK. The recently calibrated gate error rates and long-term base temperature records are shown in the supplementary material, Sec. S-IV.

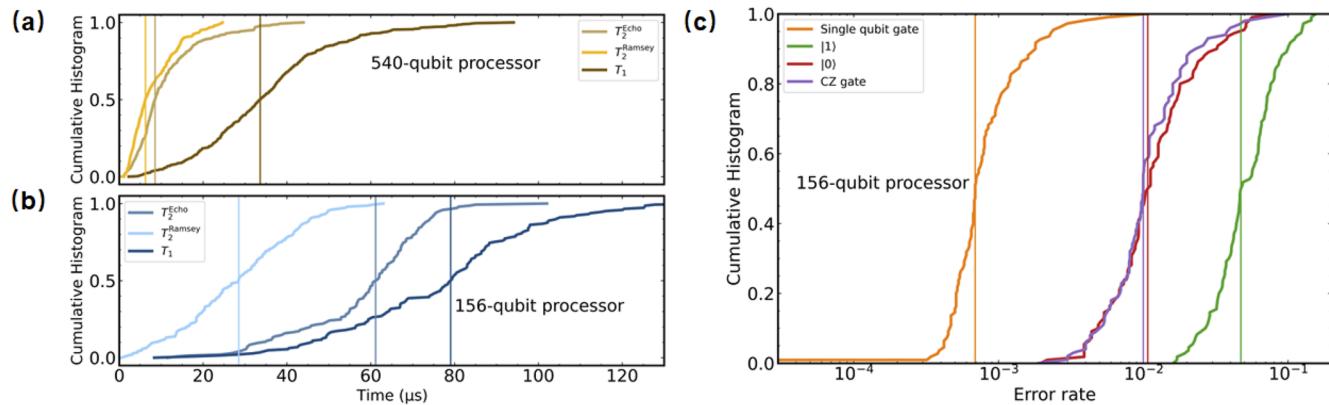


FIG. 3. Statistics of the characterization and calibration results. (a) A cumulative histogram of T_1 (brown), T_2^{Ramsey} (tan), and T_2^{Echo} (orange) of all qubits for the 540-qubit processor. (b) A cumulative histogram of T_1 (dark blue), T_2^{Ramsey} (blue), and T_2^{Echo} (light blue) of all the functional qubits in the 156-qubit processor. (c) A cumulative histogram of the calibrated error rates of the single-qubit gates (orange), two-qubit CZ gates (purple), and readout of $|0\rangle$ (red) and $|1\rangle$ (green) for the 156-qubit processor.

V. SUMMARY AND OUTLOOK

In conclusion, we successfully built a cryogenic system (~ 8.1 mK) capable of controlling and measuring more than 500 qubits using the 0.5 mm SCuNi–CuNi HDW scheme. This system includes 736 lines, 40 cryogenic LNAs, and other microwave components. In this HDW system, we characterized and calibrated two quantum processors. For the 540-qubit processor, a full characterization was conducted, and an average T_1 of $35\ \mu\text{s}$ was obtained. For the 156-qubit processor, we characterized and calibrated it, with average fidelities of single-qubit and two-qubit CZ gates optimized to 99.9% and 99.0%, respectively. The latter has been serving as a quantum computing cloud platform for over a year, working stably with the base temperature maintained under 10 mK. Through the application of these two processors, we show that our HDW scheme satisfies the control and measurement requirements for 500-qubit-scale quantum processors. In addition, our systematic heat load analysis and tests provide valuable guidance for building practical cryogenic infrastructure for large-scale quantum computing systems.

The development of cryogenic infrastructure for large-scale quantum computing systems remains a complex and long-term undertaking, requiring incremental technological advancements across multiple components. Our engineering practices suggest several viable directions for improvement. First, the commonly used 0.86 mm SCuNi–CuNi cable introduces a heavy heat load when the number of cables increases over 400. Thinner cables of diameter 0.5 mm can well suppress the heat load when the number of cables is large. Second, LNAs installed on the 4 K stage need to be changed to ones with much lower power consumption and comparable performance. Fine-tuned GeSi HBT amplifiers can be a good choice. Meanwhile, advancements in cryogenic components also contribute to more compact large-scale systems. Examples include the miniaturization of circulators^{27,28} and the performance enhancement of traveling-wave parametric amplifiers.^{29–31}

To construct larger-scale systems capable of accommodating quantum processors on the order of 1000 qubits, the development of cost-effective HDW solutions with low thermal conductivity, such as superconducting flexible strip lines, represents a promising direction. Furthermore, multiplexing technologies for the qubit control offer the potential to substantially reduce the demand for cryogenic wiring. Addressing these engineering challenges requires the concurrent optimization of the DR, wiring infrastructure, miniaturization of bulky microwave devices, quantum processor design, and packaging.

SUPPLEMENTARY MATERIAL

We provide the [supplementary material](#) to support the findings reported in this study, including additional details on the technical HDW development (Sec. S-I), amplifier specifications (Sec. S-II), crosstalk measurements (Sec. S-III), system stability (Sec. S-IV), gain variations of the RT amplifiers (Sec. S-V), calibration procedures (Sec. S-VI), and discussions on the coherence time (Sec. S-VII).

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

J. J. Tian: Conceptualization (equal); Data curation (equal); Investigation (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Y. Song:** Data curation (equal); Investigation (equal); Validation (equal); Visualization (equal). **P. Liu:** Data curation (equal); Investigation (equal); Writing – review & editing (equal). **W. G. Zhang:** Funding acquisition (equal); Project administration (equal); Resources (equal); Writing – review & editing (equal). **H. F. Yu:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Project administration (equal); Resources (equal); Writing – review & editing (equal). **Y. R. Jin:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Software (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data analysed during the current study are available from the corresponding authors on reasonable request.

REFERENCES

- ¹J. Biamonte, P. Wittek, N. Pancotti *et al.*, *Nature* **549**, 195 (2017).
- ²D. J. Egger, C. Gambella, J. Marecek *et al.*, *IEEE Trans. Quantum Eng.* **1**, 3101724 (2020).
- ³C. D. Bruzewicz, J. Chiaverini, R. McConnell, and J. M. Sage, *Appl. Phys. Rev.* **6**, 021314 (2019).
- ⁴Y. Zhang, N. Cai, V. Chan *et al.*, *Biosensors* **13**, 311 (2023).
- ⁵F. Arute, K. Arya, R. Babbush *et al.*, *Nature* **574**, 505 (2019).
- ⁶D. A. Awschalom, L. C. Bassett, A. S. Dzurak *et al.*, *Science* **339**, 1174 (2013).
- ⁷M. H. Devoret and R. J. Schoelkopf, *Science* **339**, 1169 (2013).
- ⁸S. Krinner, S. Storz, P. Kurpiers *et al.*, *EPJ Quantum Technol.* **6**, 2 (2019).
- ⁹D. Gao, D. Fan, C. Zha *et al.*, *Phys. Rev. Lett.* **134**, 090601 (2025).
- ¹⁰R. Acharya, D. A. Abanin, L. Aghababaie-Beni *et al.*, *Nature* **638**, 920 (2025).
- ¹¹Y. Kim, A. Eddins, S. Anand *et al.*, *Nature* **618**, 500 (2023).
- ¹²R. N. Das, V. Bolkhovsky, A. Wynn *et al.*, in 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), 2020.
- ¹³A. Mota-Babiloni, M. Mastani Joybari, J. Navarro-Esbrí *et al.*, *Int. J. Refrig.* **111**, 147 (2020).
- ¹⁴F. Lecocq, F. Quinlan, K. Cicak *et al.*, *Nature* **591**, 575 (2021).
- ¹⁵X. Han, W. Fu, C.-L. Zou *et al.*, *Optica* **8**, 1050 (2021).
- ¹⁶G. Arnold, T. Werner, R. Sahu *et al.*, *Nat. Phys.* **21**, 393 (2025).
- ¹⁷V. Y. Monarkha, S. Simbierowicz, M. Borrelli *et al.*, *Appl. Phys. Lett.* **124**, 224001 (2024).
- ¹⁸P. Duthil and *et al.*, “Material properties at low temperature,” [arXiv:1501.07100](https://arxiv.org/abs/1501.07100) (2014).
- ¹⁹N. Raicu, T. Hogan, X. Wu *et al.* [arXiv:2502.01945](https://arxiv.org/abs/2502.01945) [quant-ph] (2025).
- ²⁰J. D. Teufel, “Superconducting tunnel junctions as direct detectors for submillimeter astronomy,” Ph.D. thesis, Yale University, Connecticut, 2008.
- ²¹J. M. Martinis, *Quantum Inf. Process.* **8**, 81 (2009).

- ²²G. Spahn, N. Kurinsky, S. Lewis *et al.*, *J. Low Temp. Phys.* **209**, 1032 (2022).
- ²³A. I. Ivanov, V. I. Polozov, V. V. Echeistov *et al.*, *Appl. Phys. Lett.* **123**, 204001 (2023).
- ²⁴A. D. Córcoles, J. M. Chow, J. M. Gambetta *et al.*, *Appl. Phys. Lett.* **99**, 181906 (2011).
- ²⁵P. Krantz, M. Kjaergaard, F. Yan *et al.*, *Appl. Phys. Rev.* **6**, 021318 (2019).
- ²⁶Z. Chen, “Metrology of quantum control and measurement in superconducting qubits,” Ph.D. thesis, University of California, Santa Barbara, 2018.
- ²⁷M. Colangelo, D. Zhu, D. F. Santavicca *et al.*, *Phys. Rev. Appl.* **15**, 024064 (2021).
- ²⁸A. Ruffino, Y. Peng, F. Sebastian *et al.*, *IEEE J. Solid-State Circuits* **55**, 1224 (2020).
- ²⁹H. Renberg Nilsson, D. Shiri, R. Rehammar *et al.*, *Phys. Rev. Appl.* **21**, 064062 (2024).
- ³⁰Y. Zhang, H. Xu, Y. Song *et al.*, *Chip* **2**, 100067 (2023).
- ³¹C. S. Kow and M. T. Bell, “Traveling-wave parametric amplifier with passive reverse isolation,” [arXiv:2505.04059](https://arxiv.org/abs/2505.04059) [quant-ph] (2025).