Atom Chip technology for use under UHV conditions

Alexander Kassner[1], Mathias Rechel[1], Hendrik Heine[2], Waldemar Herr[2], Marc Christ[3], Markus Krutzik[3],Ernst M. Rasel[2] and Marc C. Wurz[1], Leibniz University Hannover - [1]Institute of Micro Production Technology (IMPT), An der Universität 2 30823 Garbsen, [2]Institute of Quantum Optics (IQO), Welfengarten 1 30167 Hannover, [3]Joint Lab Integrated Quantum Sensors, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Gustav-Kirchhoff-Straße 4 12489 Berlin, Germany, Kassner@impt-uni-hannover.de

1 Introduction

In matter wave interferometry, the wave properties of atoms are used for the precise measurement of inertial forces by investigating the frictionless free fall of atoms in a vacuum. Analogous to the Mach-Zehnder interferometer with its mirrors and beam splitters, the matter wave interferometer uses light pulses to manipulate the atoms [1]. In this case, Bose-Einstein condensates (BEC) serve as a source for matter wave interferometry to further improve drift and accuracy performance compared to atom interferometers. To generate a BEC, an ensemble of atoms (here: Rb) is trapped in a magneto-optical trap (MOT) and cooled by laser cooling. It is utilised that the momentum of an atom changes through the absorption and (spontaneous) emission of a photon, because temperature is defined by distribution function of all kinetic energies of all atoms involved. If this function is very broad, the ensemble is hot, if this distribution function is narrow, the ensemble is cold. The atom cloud is compressed by the reduction of the magnetic field gradient, then the MOT is switched off and an optical molasses is applied for a few milliseconds to further reduce the temperature. This is followed by a 100 µs laser pulse for optical state preparation. The planar tracks of the atom chip are energized and the atoms are trapped in the pure magnetic field by the Zeeman effect. The temperature of the atom cloud is cooled down to the critical temperature for Bose-Einstein condensation by radiofrequency evaporative cooling [2]. The sensitivity of the measurement increases squarely with the free fall time of the BEC [3]. A longer free fall of atoms in the interferometer increases the sensitivity [4, 5], therefore experiments were performed in microgravity environment [6, 7]. The miniaturization and further development of atom chips as a source of Bose-Einstein condensates (BECs) in transportable quantum gravimeters for the use in the field or on board sounding rockets, as demonstrated in [8], represents a manufacturing challenge with regard to the integration of the chips and their reliability. Since the operation takes place under ultra-high vacuum conditions, the use of non-adhesive connection techniques is given the highest priority. In addition, optical access to the chip surface is required for laser interferometry and laser cooling in order to realize a magneto-optical trap. In order to reduce the number of laser beams required, optical gratings are used on the chip surface to enable single beam operation. These require planar surfaces. In the following, the manufacture of the atom chip on a micro technological basis and the

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joining of the chip to a carrier system using transient liquid phase bonding are described. Furthermore, first approaches for backside contacting of the chip by vertical interconnect access are investigated.

2 Micro technological production of the atom chip

In order to obtain a planar surface required for interferometry, the atom chip structures are embedded in the silicon substrate as shown in figure 1. Etching of

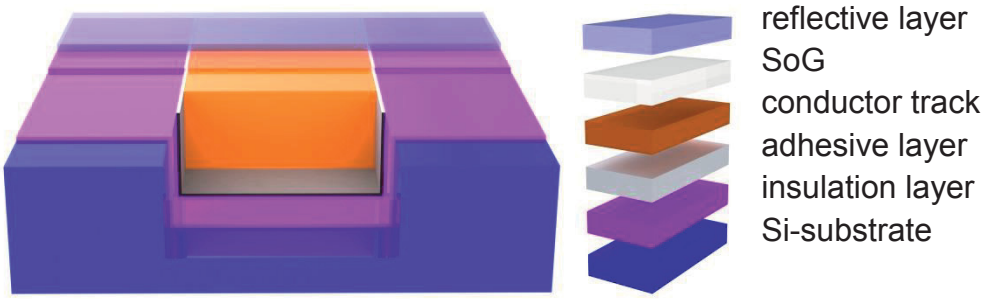

Fig. 1: Layer structure of the atom chip.

cavities is performed by deep reactive ion etching after masking the substrate with photoresist. An additional hard-bake ensures the necessary stability of the photoresist during the etching process. The depth of the cavities is determined by the required current carrying capacity. In the present case, designs with 10 µm and 20 µm were used. After the photoresist has been removed, a SiO_2 layer is deposited over the entire surface using PECVD to insulate the conductive tracks. If required, this can be extended with further Si_3N_4 layers to form a sandwich composite. Alternatively, an Al_2O_3 layer can be applied by Atomic Layer Deposition. In preparation for electroplating, an adhesive layer like Cr, Ti or Ta is sputtered followed by Cu seed layer. After re-masking with photoresist, the copper is electroplated until the cavity is filled. The sputtered seed layer for Cu electroplating also covers the side walls of the cavities. This circumstance is necessary in order to electrically contact the seed layer at the bottom of the cavities, but also leads to the electroplated copper also growing on the sidewalls both laterally and in height. In addition, the electrical field in the area of the edges is increased, which leads to increased growth at the edges. In order to flatten the surface during the electroplating process, the surface is planarized using chemical mechanical polishing (CMP). To level local unevenness, a 500nm thick spin-on glass (SoG) layer is applied by spin-coating and heating. A reflective layer for interferometry was applied by Laseroptik GmbH. Figure 2 shows the first Atom Chip prototype. The first iteration of the system was mechanically contacted with clamping contacts on the sides of the chip, which were fastened by screws, which at the same time represent the electrical contact to the underside. The characterisation of the structural adhesion under temperature load was carried out according to MIL-STD-883K 1010.9 D temperature cycling test with ten temperature

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cycles from -65°C to 200°C, whereby we extended the upper limit to 220°C and subsequent visual inspection. The cold/hot change was made in less than ten seconds.

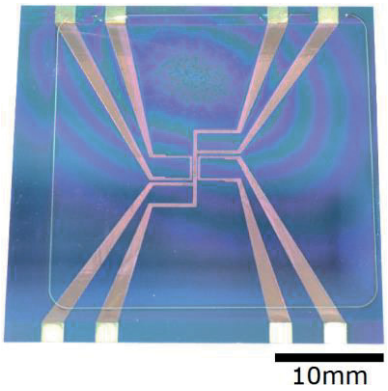

Fig. 2: First atom chip prototype.

3 Non-adhesive bonding techniques for vacuum applications

Transient liquid phase diffusion bonding (TLPDB) is used to achieve a stable surface connection between the Atom Chip and the ceramic carrier. Since the joining process takes place after the processing of the atom chip, a melting temperature of the eutectic that is as low as possible is essential in order to avoid delamination of the layers with their different thermal expansion coefficients due to the thermal load. The use of non-magnetic materials is also important in order to avoid an influence of the magnetic fields generated by the conductor tracks of the chip. Au-In-Au is used as the material system for the bonding process, with the Au layers on the underside of the atom chip and the top of the ceramic carrier acting as parent metals and the In as interlayer. The layer structure of the joint is shown in figure 3. Cr layers are also used as adhesive layers. The chip and carrier are then brought into contact with each other.

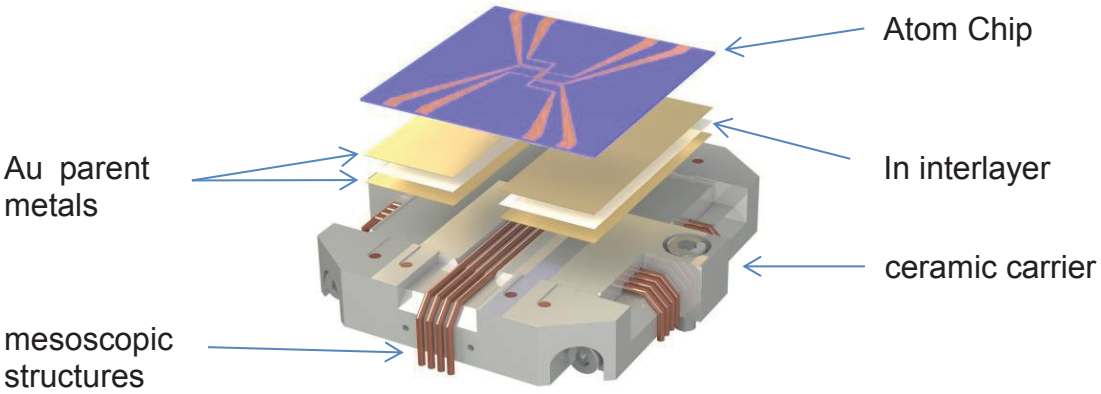

Fig. 3: Layer structure of the joint.

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The influence of temperature and pressure leads to melting and homogenization of the In interlayer. By reaction with the parent metals, intermetallic compounds with a higher melting point in the range above 500°C are formed. This ensures that the connection will not separate when the vacuum chamber is heated out later. The ceramic carrier contains recesses for Kapton® wires, which run below the Atom Chip and represent the mesoscopic structures of the chip. This type of cable is marketed by the manufacturer as vacuum compatible due to extremely low outgassing rates. Figures 4a to 4d show the individual steps of the joining process. First, the atom chips are joined to a carrier subsystem, which is then connected to the complete carrier system in a following step. In order to ensure reproducible handling with sufficient accuracy during TLPDB, a clamping and adjustment device was designed and manufactured. This adjustment device is shown in Figure 4a with the carrier subsystem. It has mesoscopic structures manufactured by precision mechanics to fix the inserted wires. A seed layer was first sputtered onto the surface of the carrier subsystem and the underside of the atom chip and then electroplated with gold. The indium was cut and applied in the form of a 50 µm thick indium foil. The atom chips were in turn placed on the carrier subsystem and fixed in the alignment device by means of clamping jaws, see Figure 4b. The process of TLPDB is shown in Figure 4c. The parameters pressure, temperature and time are relevant. A base plate equipped with heating cartridges introduces the temperature from below into the system to be joined. The temperature was increased with a ramp function from 2°C/min to 220°C, held for 90 minutes and then slowly cooled down again to room temperature. For uniform pressure application of 0.0524 MPa the stamp is guided in a holder. Possible tilting of the atom chip is compensated by a Teflon intermediate holder with a conically milled recess in the surface. Figure 4d shows the carrier subsystem with the joined atom chip and four mesoscopic wires. The atom chip with the carrier subsystem can in turn be joined to the overall system using the same joining process. For reasons of time, the two ceramics were bonded with a ceramic adhesive for this first experiment, future systems will completely avoid the use of adhesive. Figure 5 shows the first complete system.

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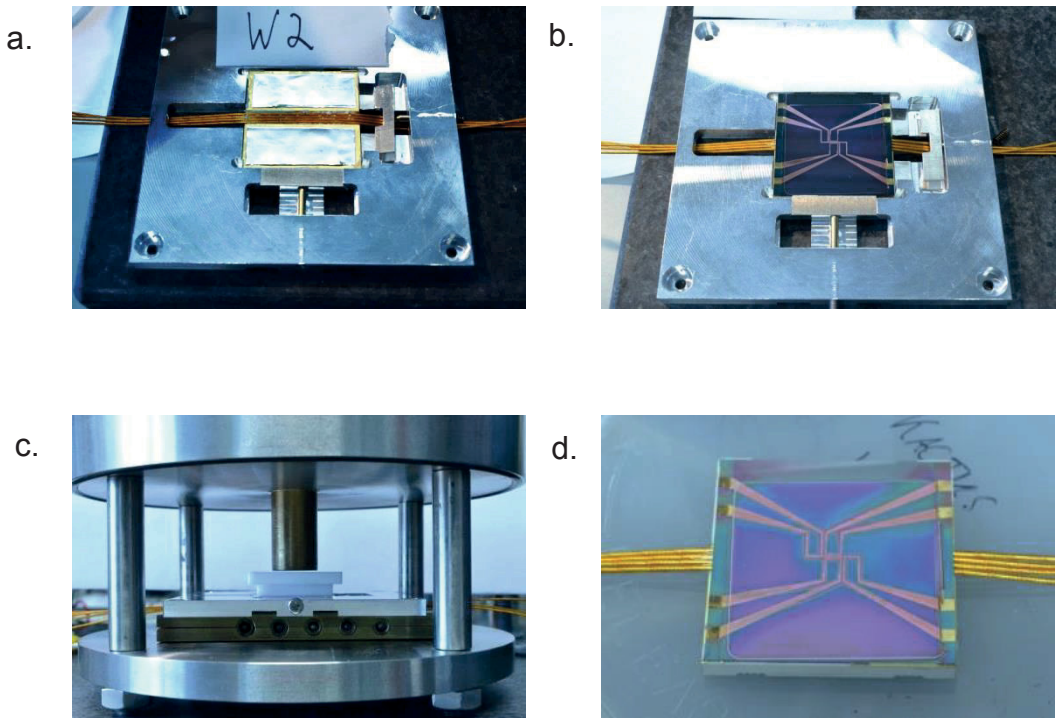

Fig. 4: The single process steps during TLPDB of the prototype atom chip.

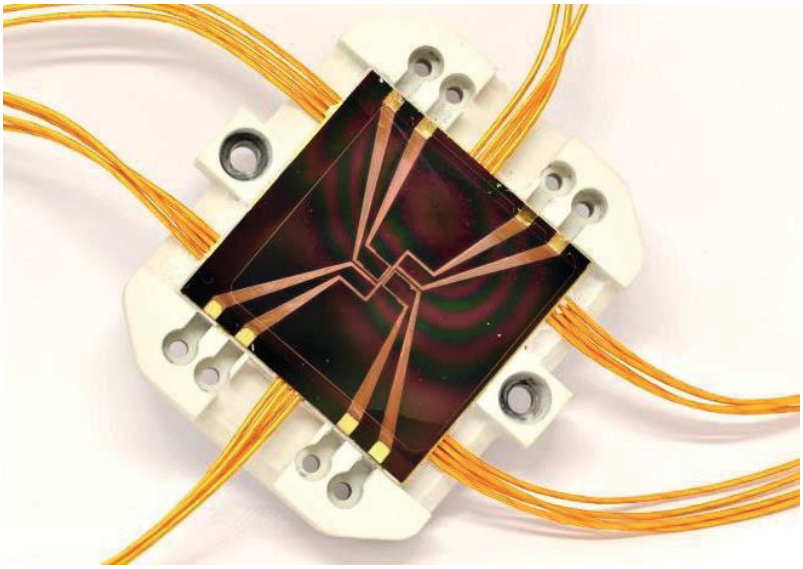

Fig. 5: First complete system.

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4 Conclusion

We have been able to produce an atom chip with non-adhesive joining techniques that does not require the extensive use of adhesives. By reducing the outgassing rate, it is possible to further reduce the pump performance and thus the payload. The temperature load during the joining process lies within the range characterized by us, a temperature-related delamination of the different layers by different thermal expansion coefficients did not occur in the case of 10 µm thick conductor tracks. In the case of the 20 µm thick conductor tracks, delamination symptoms occurred sporadically. Subsequent tests of the maximum current carrying capacity showed that even with 10 µm thick tracks there are sufficient reserves so that the future atom chips are based on this track thickness. After the successful first experiments, in the future the two components of the ceramic holder will also be joined using TLPDB. Our project partners from the Joint Lab Integrated Quantum Sensors developed and are setting up a versatile UHV qualifications setup exceeding the common ASTM E595 norm by multiple orders of magnitude. With this setup, integration technologies, materials, optical components and the complete atom chip assembly can be qualified regarding outgassing rate and gas species.

5 Outlook

Currently, vertical interconnect access is being developed in order to avoid surface contacting and to keep the beam path free in every spatial direction. For this purpose, through-holes are etched in the area of the contact pads using deep reactive ion etching, the side walls are isolated and filled by an electroplating process. To further miniaturize the measurement system and the associated payload, novel optical concepts based on diffractive gratings are used to realize a single-beam system. This reduces the number of lasers and thus the electrical power and mass of the electronics. These gratings are currently sourced from external suppliers and then bonded to the atom chips using adhesive joining techniques. In addition to the high outgassing rate, which is a matter of principle, adjustment and planarity must also be taken into account in this process. Our goal is to integrate the gratings into the atom chip as part of the manufacturing process in order to avoid the use of adhesives. These gratings have geometric dimensions in the sub-micrometre range and are produced micro technically at the IMPT. In addition to structuring the silicon substrate, additional functional layers of various materials can also be applied and structured.

6 Acknowledgement

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