Advanced E-Beam Systems for Manufacturing

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ABSTRACT

E-beam lithography systems are being employed as pattern generators in the semiconductor manufacturing process. The TV-like raster exposure of a scanning electron beam under computer control provides the resolution, flexibility, and accuracy needed for the generation of high density integrated circuit patterns. E-beam mask making has become the technology of choice, while e-beam direct writing on the wafer has remained largely a niche application. Here the throughput handicap of serial exposure presented an economic hurdle, which limited applications to exploratory research and prototyping rather than manufacturing - with few exceptions: IBM, for example, has applied its internally developed high-throughput EL-series systems worldwide in large scale manufacturing of ASIC-type bipolar logic products. The recent progress in state-of-the-art of manufacturing-oriented e-beam systems for mask making and direct writing, together with results achieved with these advanced systems, is the subject of this paper.

1. INTRODUCTION

Electron beam exposure systems have been used at the leading edge of micro- and nano-fabrication for many years[1,2]. The superior lithographic resolution capability of e-beam systems has effectively been employed in exploratory research and development work. The first large scale manufacturing application, however, did not make use of high resolution; instead it exploited the ability of electron probe systems to directly generate pattern under computer control. E-beam pattern generation for mask manufacturing has become the dominant technology throughout the semiconductor industry[3]. The recent trend towards phase shifting and 1x masks for DUV and X-ray lithography has re-emphasized resolution and presents other formidable challenges for advanced e-beam mask manufacturing systems[4].

The most desirable e-beam lithography process, is to write directly on the semiconductor wafer eliminating the expensive and time-consuming mask step entirely. The unique flexibility for maskless pattern generation has, however, an associated disadvantage: The image elements or pixels must be exposed serially. This imposes a severe limitation on exposure speed or the rate at which pattern information is transferred onto the semiconductor wafer. From a mask where the pattern information is stored, optical projection systems transfer up to 10^9 pixels onto the wafer in parallel. In contrast, the conventional e-beam system writes the pattern with a finely focused Gaussian round beam exposing one pixel at a time. This throughput handicap limited Gaussian round beam systems to research applications[2].

The development of the shaped beam approach enhanced the exposure efficiency significantly and made the use of e-beam direct write systems in semiconductor manufacturing lines economically acceptable[5]. For this direct-write strategy to succeed, the e-beam systems had to keep pace with the increasingly stringent requirements of semiconductor manufacturing. The most stringent one of the requirements has been and still is throughput. In spite of significant exposure speed enhancements (measured in pixels per second), the throughput of direct-write tools (measured in wafers per hour) has steadily declined[6]. The reasons are the continually increasing density and complexity of inte-

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grated circuits and the expanding wafer size which led to explosive growth in the number of pixels to be exposed per wafer.

In an attempt to reverse the trend of throughput erosion through further increase of parallelism in pixel exposure beyond the variable shaped beam concept, character projection[7] and more recently cell projection[8] techniques have been introduced. These projection schemes provide a trade-off between pattern generation flexibility with pattern writing speed, and are most efficient in the exposure of repetitive patterns like memory arrays.

2. MASK MANUFACTURING

2.1 E-Beam Pattern Generation

With the advent of VLSI in the late 1970's, e-beam systems began to replace the slow opto-mechanical pattern generators and photo-repeaters in the mask shops of the semiconductor industry. A 64K DRAM pattern with over 10^5 components could run for 24 hours on an artwork generator while an e-beam system completed the job in less than an hour. The trend of DRAM's toward ever higher levels of integration has continued since with a 4x density improvement every three years, driving the lithography requirements for minimum features and mask overlay (Fig. 1). A corresponding increase in the number of pixels per chip and the numerical control (NC) data volume required for pattern generation is shown in Fig. 2.

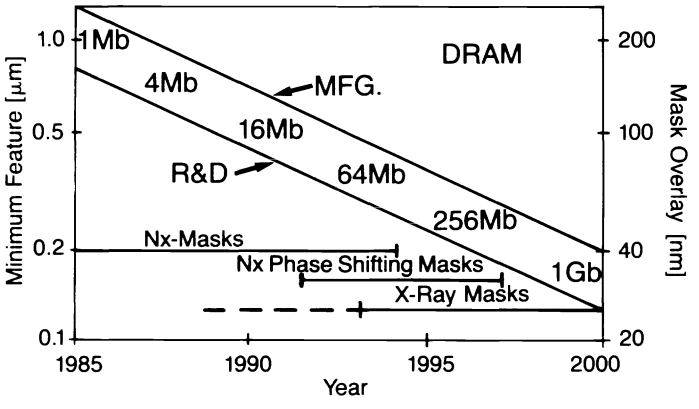

Figure 1. DRAM technology trend as lithography driver for minimum feature size and mask overlay.

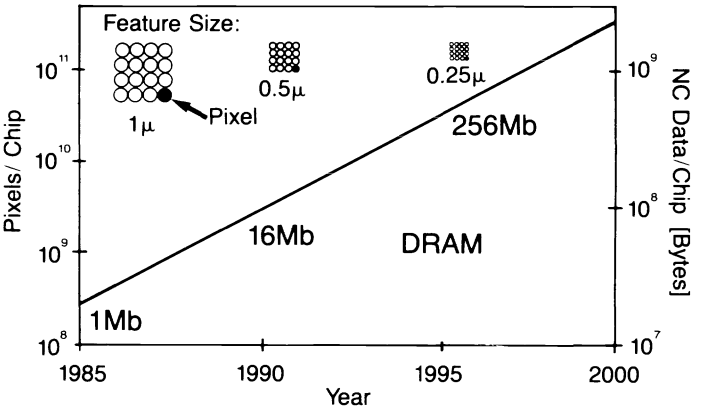

Figure 2. DRAM density in pixels per chip and the corresponding numercial control data volume required for pattern generation.

2.2 Gaussian Beam Raster Scan

MEBES[9] machines, manufactured by ETEC, Inc., became the most successful e-beam mask makers; approximately 130 systems have been installed to date worldwide. The writing-on-the-fly strategy of MEBES combines a small telecentric raster scan deflection of Gaussian beam in one axis and the table continuously moving back and forth in the orthogonal axis, with a laser interferometer feeding the table position back to the electron beam. The small raster deflection, typically 1/4 - 1mm, permits the use of a short-focal length lens for high beam stability and high resolution; it also favors high speed deflection. The telecentric arrangement maintains normal beam landing, thus, avoiding beam

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placement errors resulting from plate height variations in non-telecentric systems. Beam drift is checked and corrected using a reference mark on the table. Interactions of beam and table movement are avoided by placing the stage drive mechanism in a separate chamber outside the vacuum.

To accommodate the semiconductor technology trend towards higher levels of integration and the steadily rising demands for writing speed, placement accuracy, line-width reduction and design grid resolution four generations of tools with successively higher performance levels have been introduced over the years. The most visible improvement in writing speed advanced from 20 MHz (MEBES I) to 40MHz (MEBES II) and 80 MHz (MEBES III) to 160 MHz (MEBES IV)[10]. The latest tool generation employs a new high speed blanker and a high brightness thermal field emission gun[11] in support of higher pixel rate; further throughput advantages are achieved through multi-phase printing using larger beam diameters. More subtle improvements have been made to stage, autoload system, temperature control, work table, deflection electronics and software.

An important goal of the tool enhancement strategy has been the protection of customers investments in the approximately 80 installed MEBES III machines; all new MEBES IV features are retrofittable on those machines.

2.3 Shaped Beam Vector Scan

The major trend in lithography has been toward 4x and 5x reduction steppers and away from the earlier 1x technology. This approach brought temporary relief for mask making by reducing demands on pixel resolution, pixel writing speed, and pattern placement accuracy. The return to 1x masks for synchrotron based x-ray lithography and other 1:1 exposure techniques as well as phase shifting mask for 64M and 256M DRAM's represent formidable challenges. At IBM, the internally developed variable shaped beam system EL-3 has been employed in advanced mask making.

The variable shaped beam approach has proved effective in dealing with throughput demands for both direct write and mask making. Unlike the Gaussian beam, it produces a rectangular beam spot of varying size which decouples resolution (edge acuity of intensity profile) from the size (width of intensity profile). Consequently, up to several hundred pixels can be written in parallel without compromising resolution providing up to 1 GHz of effective pixel writing rate. In addition, design grid variations can be accommodated by moving the edge of the beam intensity profile at any required increment without affecting throughput. The design grid resolution of EL-3 is 12.5nm; the edge acuity is 70nm. This allows for precise image size control at sub-half micron critical dimensions. We recently reported on a new e-beam mask maker, designated EL-3+, which is installed and operating in the IBM Advanced Mask Facility in Burlington, Vermont[12]. This tool represents state-of-the-art in mask manufacturing.

The primary mission of EL-3+ is the production of 1x x-ray masks and it routinely operates at 0.35um ground rules achieving 70nm (mean + 3 sigma) placement accuracy to grid. Exposures are made with a shaped beam spot of maximal 2x2um^2 size at 50keV beam energy, stitching together 2.1x2.1mm^2 fields on ring bonded Si-membrane masks. Beam addressing within a field is accomplished through a combination of magnetic and electric deflections employing a variable axis immersion lens. The magnetic channel is stepping the beam from subfield to subfield in a repetitive serpentine mode, while the electric deflection provides high speed random vector addressing of the spot within the 37.5um subfield. The system automatically corrects deflection distortions of both channels to a residual error of 6.25nm using a calibration reference grid and automatically cancels repeatable stage errors which are determined via a precalibrated reference mask plate[4]. During exposure, the pattern data is stored on-line in a high speed 1 G-byte buffer which is loaded directly from an IBM 4381 host computer.

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Further performance enhancements are currently being implemented on a prototype of the next generation tool EL-4, aiming for 0.25um lithography with 50nm ('93) and 35nm ('95) overlay targets. Key system features are:

- Variable Axis Immersion Lens
- Precision Planar Stage
- New Data Path Electronics
- High Volume Data management

Fig. 3 shows overlay targets for the various tools as a function of time with the solid curves indicating results achieved. A prerequisite for the above described mask strategy is a corresponding improvement of metrology tools to provide the necessary measurement accuracy and repeatability.

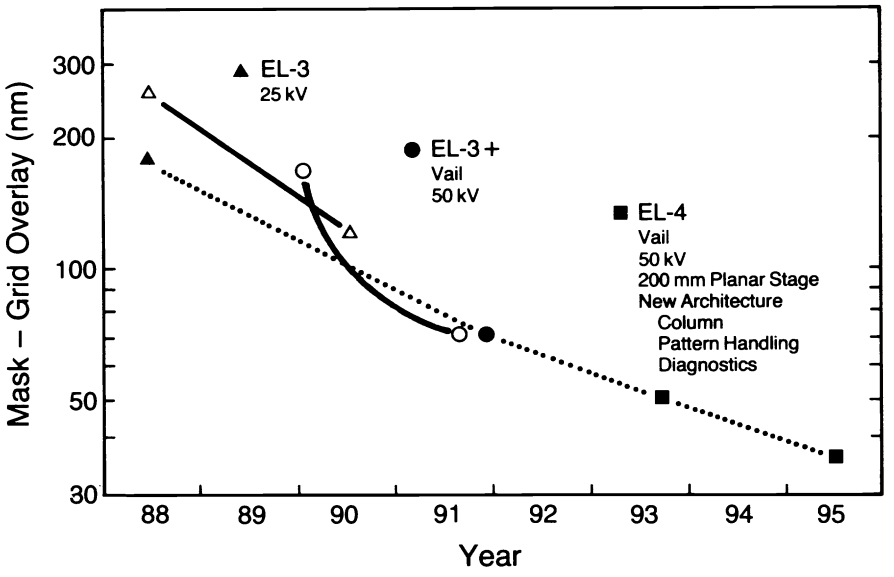

Figure 3. Overlay goals (dotted line) and actual results (solid lines) as a function of time for various EL systems.

3. DEVICE MANUFACTURING

3.1 The IBM Experience

IBM has pioneered the use of electron beam lithography in semiconductor device manufacturing[13]. The corner stone of this direct-write strategy was the development of the shaped beam technique[14]. The first generation of shaped beam EL-1 systems was introduced into IBM's Quick-Turn-Around-Time (QTAT) production facility at East Fishkill in 1976[15]. The highly automated EL-1 tools were specifically designed for the manufacturing lines and had a throughput of 22 57mm-wafers per hour. The application of the EL tools, which provided the incentive for their development, was the production of Application Specific Integrated Circuits (ASIC) - type devices. Currently, third generation EL-3 tools are being used in IBM's semiconductor manufacturing lines worldwide in an optical/e-beam mix-and-match approach. They expose the application specific metallization layers of bipolar logic chips with up to 16 different chip

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designs per wafer. IBM's direct-write manufacturing capability provided a unique flexibility for its computer architects and circuit designers. The "open part number set" strategy allowed to define as many different chip designs as needed for optimum use of silicon and packaging space and material. Large numbers of engineering changes could be turned around quickly providing rapid learning during product development cycles. Several thousand part numbers could be maintained including those required for only very low volume, which were manufactured cost-effectively through the mix of different chip designs on a single wafer. Fig. 4 shows the installation of three EL-3 systems in one of IBM's highly automated bipolar circuit manufacturing lines at the East Fishkill facility.

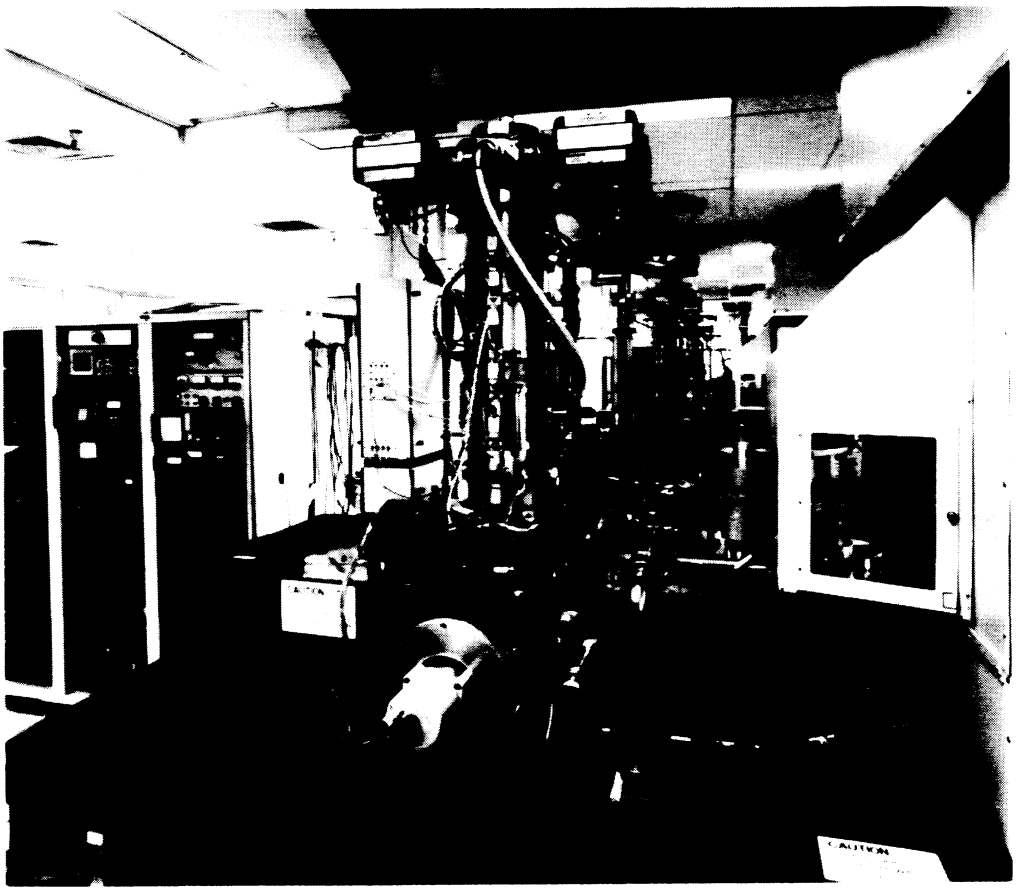

Figure 4. Installation of three EL-3 systems in one of IBM's automated bipolar manufacturing lines at East Fishkill, New York.

The e-beam strategy for the production of bipolar logic chips has been based on the concept of large field deflection and step-and-repeat stage moves. Large field deflection enables detection of registration marks in the four corners of the chip and subsequent exposure of the entire chip without field stitching requiring intermediate stage moves. This concept provides the most reliable overlay, but becomes increasingly difficult to implement. Fig. 5 illustrates the performance improvements achieved with EL-3 tools during the past decade to meet the increasing requirements of ASIC manufacturing. During the early 1980's, 2.5um design rules were used with 5x5 mm^2 chips; by 1990 the requirements had reached 0.7um minimum features and 10x10mm^2 chips. Fig. 6 shows the evolution in wafer size from 82mm in 1980 to 200mm in 1990 and the reduction of overlay errors during the same period.

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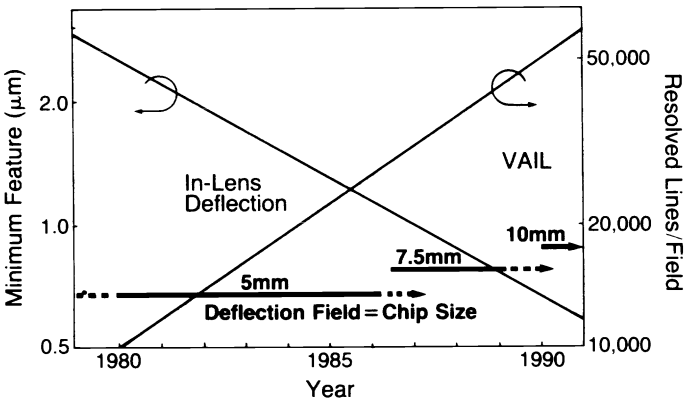

Figure 5. EL-3 performance evolution; minimum features, field size and resolved lines per field.

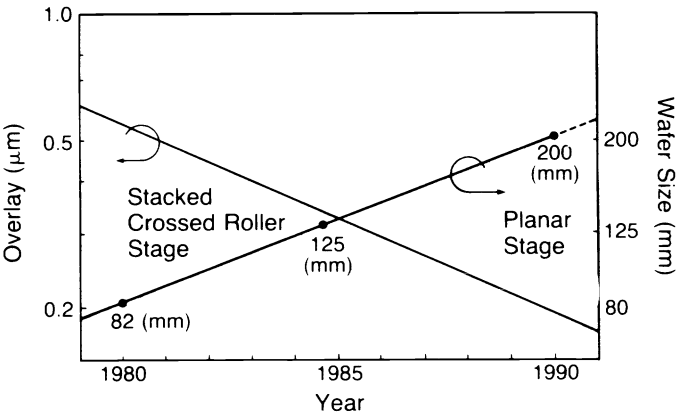

Figure 6. EL-3 wafer handling capability and overlay accuracy evolution.

3.2 EL-3 Tool Status

To maintain the writing strategy of chip size deflection, it was necessary to advance the state-of-the-art in imaging and deflection techniques. Beam deflection is usually limited by aberrations which increase with the distance of the deflected beam from the electron optical axis of the imaging system. Our solution to this problem is the Variable Axis Immersion Lens (VAIL)[16,17]. The optical axis is shifted in synchronism with the pre-deflected beam, which eliminate off-axis aberrations, since the beam effectively remains "on-axis" throughout the scan field. VAIL also provides telecentricity maintaining normal beam landing at all points of the scan field[18]. As in mask making, high speed writing is accomplished through dual channel major magnetic and minor electric deflection, both in telecentric imaging mode. Deflection distortions of both channels are measured and corrected through an automated calibration scheme[19]. There are approximately 20,000 subfields in a 10.35 x 10.35 mm^2 field and 80,000 points are being measured to calibrate the major and minor deflections. This fully automated calibration technique is a key element of the manufacturing oriented EL-tool writing strategy. It permits measurement and correction of systematic, tool specific errors and assures tool inter-changeability - an important requirement in semiconductor manufacturing lines. It also proved to be a powerful diagnostic tool enhancing the productivity under manufacturing conditions.

The beam energy of the latest EL-3 tools (EL-3+) has been increased from 25 to 50 KeV to significantly improve resolution through reduced Coulomb interaction between beam electrons. A 2x improvement is achieved at the higher beam current density used to compensate for the loss in resist sensitivity. The VAIL configuration further improves resolution through the short focal length which results from immersion of the wafer into the lens field. Through this technique, it was possible to improve field size and resolution simultaneously as illustrated in Fig. 5.

A novel servo guided planar stage[20] has been developed to operate inside the narrow pole piece gap of the lens. All moving parts of the stage are a) non-magnetic to avoid interference with the lens and yoke fields, b) largely non-conductive (no bulk conductors) to suppress eddy currents otherwise generated by the dynamically changing deflection fields and by the stage movement within the static lens field. The stage is designed to handle 200mm wafers which are held by an electrostatic chuck mounted to the stage plate. The stage can be operated at 1g acceleration and a velocity of up to 250mm/sec; a 10.35mm move is completed in approximately 120 msec.

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3.3 Recent Results

IBM's most advanced direct-write shaped-electron beam lithography system EL-3+ has been installed in the Advanced Semiconductor Technology Center (ASTC) at the East Fishkill facility. The system is being used in a mix and match mode with optical steppers exposing 10.35 x 10.35mm^2 bipolar logic chips at 0.7 um lithography ground rules and 200nm overlay. The exposures are done on 200mm wafers with a variable shaped spot of maximal 4x4um^2 and 4uA beam current at 50 keV beam energy; the pattern features are delineated with an edge accuity of 1/4 of the critical dimension; the full spot edge resolution is 0.2um corresponding to 50000 resolved lines per field. Fig. 7 shows resist images of 0.5um lines and spaces in the center and the four corners of the 10.35x10.35mm^2 deflection field. The micrographs show that the image quality achieved at the center of the field is maintained throughout, and no deterioration or distortion of the images due to deflection aberrations can be detected. Equally important is the beam placement accuracy over the field of deflection. The auto-calibration scheme, which measures and corrects deflection errors via precision calibration grids, results in typical mean plus 3 sigma values of 75nm. Fig. 8 illustrates the overlay performance of the tool in a mix and match mode with an optical stepper. The vector plot reflects 242 measures made at 9 chips per wafer. The mean plus 3 Sigma errors is 179um in X and 190um in Y direction, well within the 200nm specification.

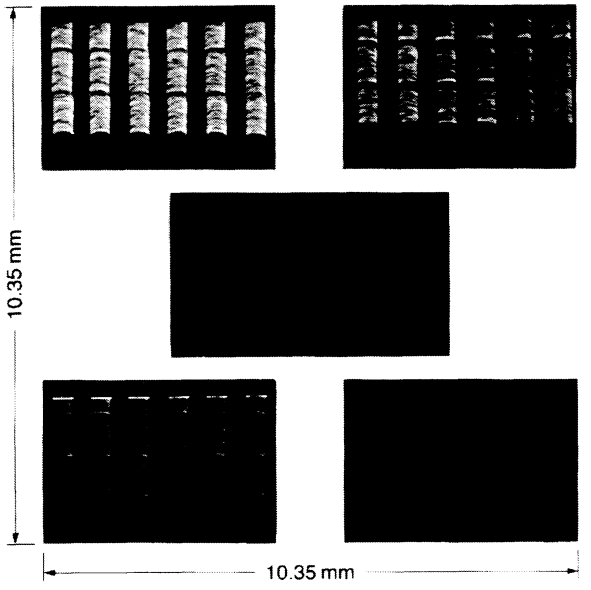

Figure 7. Test Pattern, resist images of 0.5 um lines and spaces in the center and the 4 corners of a 10.35x10.35mm^2 deflection field.

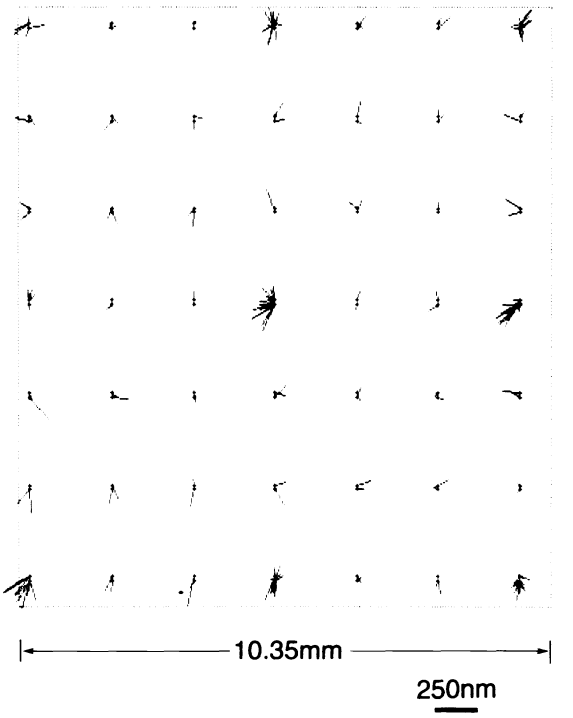

Figure 8. Overlay results; vector plot of EL-3+ overlay errors to an optical stepper level exposed on 200mm wafers; mean plus 3 sigma x = 179um, y = 190nm. 242 data points per wafer.

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4. TECHNOLOGY TRENDS

Fig. 1 and 2 provide a projection of the lithography trends in semiconductor technology. The rapid increase in pixel density represents a formidable challenge for e-beam pattern generators. For both mask making and direct write to remain viable significant improvements in exposure efficiency are needed in the future.

4.1 Scanning/Projection Techniques

The introduction of the variable shaped spot technique, as mentioned earlier, provided 1-2 orders of magnitude improvement in writing speed over single pixel machines through parallel exposure of pixels. A shaped spot can project square or rectangular pattern elements containing up to several hundred pixels.

A further enhancement in writing speed is possible through the projection of repetitive pattern "characters"[21] or "cells"[8] which can contain thousands of pixels. Fig. 9 shows schematics of both the variable shaped spot and the character projection technique developed at IBM[7]. A character projection prototype system had been built in support of a bubble memory project during the late 1970's demonstrating basic feasibility of the technique with exposures of working bubble memory race tracks on garnet wafers[22]. The highly repetitive nature of memory arrays is conducive to the technique and compatible with the rather limited selection of different characters in the shape aperture. Fig. 10 illustrates the formation of bubble memory patterns by selection and composition of shapes stored in the character aperture[19,22].

More recently, Hitachi[8,23] has reported on a cell projection technique intended for use of 64Mb DRAM exposure. Fujistsu[24] has published on a similar block projection technique.

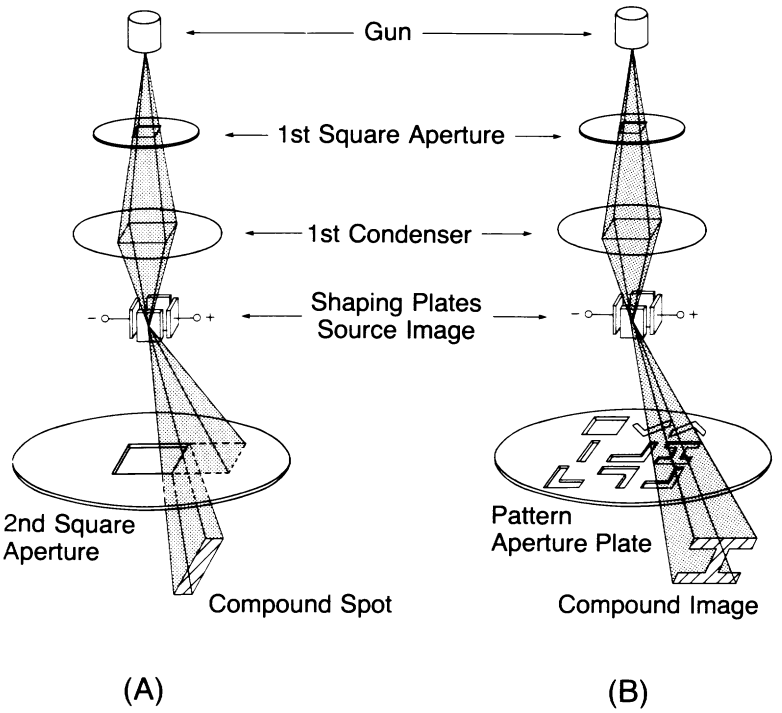

Figure 9. Beam shaping techniques; (A) variable shaped spot, (B) character projection.

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These scanning/projection techniques promise significant increase in parallelism of pixel exposure without sacrificing the pattern generation capability, which has been the most important virtue of e-beam lithography in semiconductor manufacturing.

4.2 Projection Techniques

Highest exposure efficiency has always been the potential of mask-based projection electron-beam lithography. This electron optical analogue of the optical stepper has been pursued since the early beginnings of e-beam lithography[25-28]. Unlike scanning systems, projection e-beam lithography systems have not achieved manufacturing maturity and have not yet been applied in semiconductor production. One key limitation has been the fabrication and use of absorbing stencil masks. All projection e-beam systems, with exception of the photo-cathode systems[29-31], use stencil masks in transmission mode; 1x masks for shadow projection[32] and Nx masks for reduction projection[27,28]. In both cases, the mask technology has to deal with the absorbed beam energy and with the "doughnut" problem of ring shape patterns.

New interest in e-beam projection lithography has been stimulated by recent publications from AT&T Bell Laboratories[33-35]. The reports describe a "scattering with angular limitation in projection electron-beam lithography" (SCALPEL) technique. The technique uses a membrane supported transparent mask and exploits the scattering contrast rather than absorption contrast. This technique offers a solution to the doughnut problem as well as to the absorption of beam energy in the mask. Rather than flooding the mask, illumination can be carried out with a narrow beam which is scanned and dynamically corrected for off-axis aberrations. There is also the potential of combining character or cell projection with SCALPEL. Successful implementation of these electron-beam projection techniques could provide the tools of choice for manufacturing devices with sub - 0.25um design rules[33].

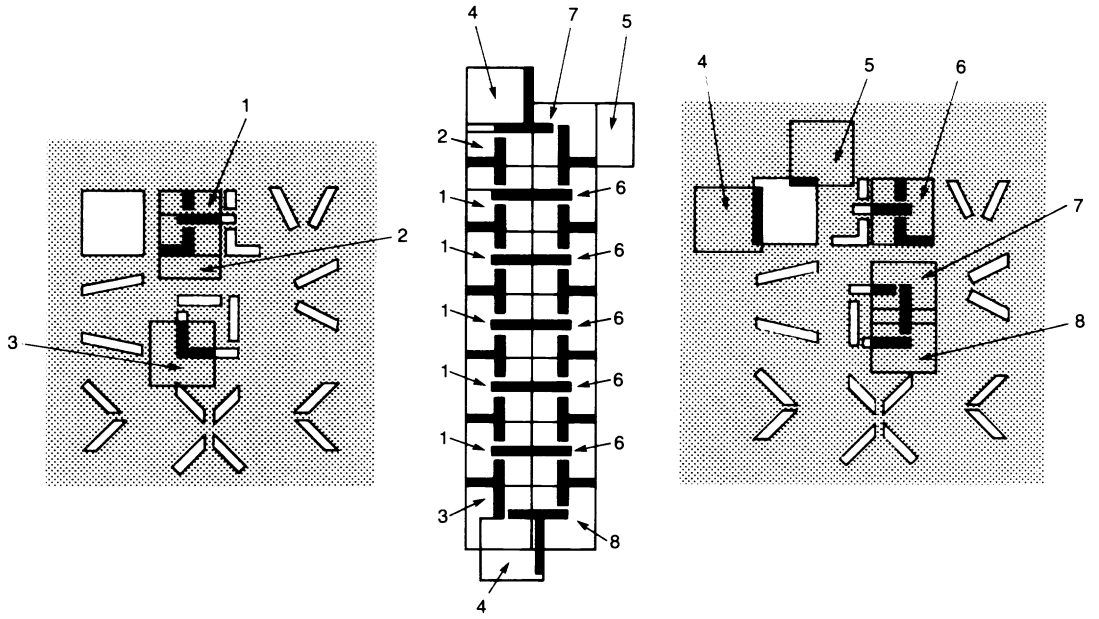

Figure 10. Pattern composition of bubble memory race track using 8 characters selected from a shape aperture.

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5. CONCLUSION

Electron beam systems have become indispensable in the semiconductor manufacturing process. Any mask-based lithography technology depends on the excellence and the continuing advancements of electron beam pattern generators. In selected cases, E-beam direct write systems have been employed to great advantage in prototyping and ASIC manufacturing. Probe forming electron beam systems have demonstrated superior lithographic capability in a broad spectrum of research based nano-fabrication applications. The most severe limitation of the technology is its slow exposure speed resulting from the serial exposure of pixels. Combinations of projection and scanning techniques have alleviated the throughput handicap through some parallelism in the pixel exposure. Further enhancements of this approach are conceivable and are being pursued.

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