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Junction fabrication by shadow evaporation without a suspended bridge

Florent Lecocq, Ioan M Pop, Zhihui Peng, Iulian Matei, Thierry Crozes, Thierry Fournier, Cécile Naud, Wiebke Guichard and Olivier Buisson[1]

Institut Néel, CNRS and Université Joseph Fourier, F-38042 Grenoble, France

E-mail: olivier.buisson@grenoble.cnrs.fr

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Abstract

We present a novel shadow evaporation technique for the realization of junctions and capacitors. The design by e-beam lithography of strongly asymmetric undercuts on a bilayer resist enables *in situ* fabrication of junctions and capacitors without the use of the well-known suspended bridge (Dolan 1977 *Appl. Phys. Lett.* **31** 337–9). The absence of bridges increases the mechanical robustness of the resist mask as well as the accessible range of the junction size, from 10^{-2} μm^2 to more than 10^4 μm^2. We have fabricated Al/AlO$_x$/Al Josephson junctions, phase qubit and capacitors using a 100 kV e-beam writer. Although this high voltage enables a precise control of the undercut, implementation using a conventional 20 kV e-beam is also discussed. The phase qubit coherence times, extracted from spectroscopy resonance width, Rabi and Ramsey oscillation decays and energy relaxation measurements, are longer than the ones obtained in our previous samples realized by standard techniques. These results demonstrate the high quality of the junction obtained by this bridge-free technique.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

On-chip metallic junctions are the building blocks for a wide variety of nanoelectronic devices such as single-electron transistors [2], spin-based electronic devices [3, 4] and superconducting circuits such as SQUIDs [5], voltage standard circuits [6], RSFQ logic circuits [7], nanofridges [8] and superconducting qubits [9]. The shadow evaporation technique (ShET) [1] with a suspended bridge of resist appears as a very useful technique to realize these circuits. For ShET the two metal evaporations, as well as the oxidation to obtain the tunnel barrier, are made without breaking the vacuum, therefore enabling high quality junctions. ShET is simple (one lithography step) and flexible (independent of the metal choice) and enables submicron-size tunnel junctions. These performances make this technique often preferable compared to the multi-layer technique (MLT) [10, 11]. However, ShET presents important limitations due to the suspended bridge. One of the ShET disadvantages is the fragility of the bridge. It makes any etching by plasma difficult in order to clean the substrate surface before evaporation. In addition, the bridge prevents an efficient cleaning of the junction surface before evaporation since it is located just above the junction. As a consequence the resist residues can contaminate the tunnel barrier and alter its oxide quality [12]. Moreover, the mechanical strains on the suspended bridge make impossible the fabrication of large tunnel junctions (typically larger than 10 μm^2) and large capacitors.

In this paper we report on a Josephson junction phase qubit made by a novel technique using shadow evaporation but without using suspended bridges. This technique, called hereafter the bridge-free technique (BFT), is based on the control of strongly asymmetric undercuts in a bilayer resist. By adjusting the undercut position and its depth, we select for each angle of evaporation whether the metal will be deposited onto the substrate or on the resist wall which will be removed after lift-off. In this way we can control which wire will be connected to the junction. Using the BFT, we have fabricated a Camelback phase qubit based on a zero current bias SQUID. Josephson junction current–voltage (IV) and qubit coherence properties have been characterized and

[1] Author to whom any correspondence should be addressed.

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compared to our previous Camelback phase qubits made by the multi-layer technique (MLT) [13] and ShET techniques [14].

2. Junction fabrication

The BFT was developed using a 200 nm thick PMMA imaging layer on top of a 700 nm thick copolymer PMMA/MAA support layer spun on an Si/SiO_2 wafer. To reach a strongly asymmetric undercut, an e-beam writer operating at 100 kV draws two successive types of patterns, using a double-exposure technique [15]. The first one, using a high dose exposure (1500 $\mu C\,cm^{-2}$), defines the opened wires in the imaging layer. The second pattern using a low dose (400 $\mu C\,cm^{-2}$) defines the undercut in the support layer (figure 1(a)). These two different patterns are possible because the PMMA sensitivity is around three times lower than the PMMA/MAA one. After development (MIBK(1): IPA(3) during 30 s and rinsing with pure IPA) we obtain the asymmetric undercut (figure 1(b)). Typically we achieve on one side a designed undercut with a depth up to more than 1 μm, while on the other side we observe an undesired residual undercut smaller than 50 nm. A light oxygen plasma RIE cleans the resist residues on the wafer. The next step consists of the two angle evaporations θ of, respectively, $-45°$ and $+45°$, separated by an *in situ* oxidation (figure 1(b)). The first evaporation produces a wire on the substrate whereas the second one is deposited on the resist wall. After resist lift-off only one wire remains on the substrate. In the case of an undercut designed on the other side, the situation is symmetrically reversed, so the second evaporation is deposited on the substrate and the first one on the resist and is removed after lift-off. Therefore the BFT enables us to design undercut patterns such that we select for each evaporation which connecting wire remains or not on the substrate.

Figure 2(a) illustrates the typical resist mask design to realize a junction using the BFT. The central opened area defines the junction. The two opened lines, on both sides of the central area, define the two wires connecting the junction to the external circuit. A 1 μm deep undercut is present on the right of the upper connecting wire and on the left of the lower connecting wire. The cross section of the upper and lower wires are illustrated in figures 2(c) and (e), respectively. To realize a junction we perform two evaporations with opposite angles as mentioned previously. The first evaporation, coming from the left, only deposits on the substrate the bottom electrode of the junction (figure 2(d)) and the upper wire (figure 2(c)). The evaporation of the lower wire is deposited on the resist wall. Similarly, the second evaporation, coming from the right, deposits on the substrate the top electrode of the junction (figure 2(d)), the lower wire on the substrate (figure 2(e)) and the upper wire on the resist wall. Figure 2(b) shows the junction after lift-off. The two evaporations are shifted by about 1.6 μm because of the different evaporation angles.

3. Feasibility of the BFT

In order to successfully obtain a junction by this technique, the connecting wires must have a finite width W which satisfy

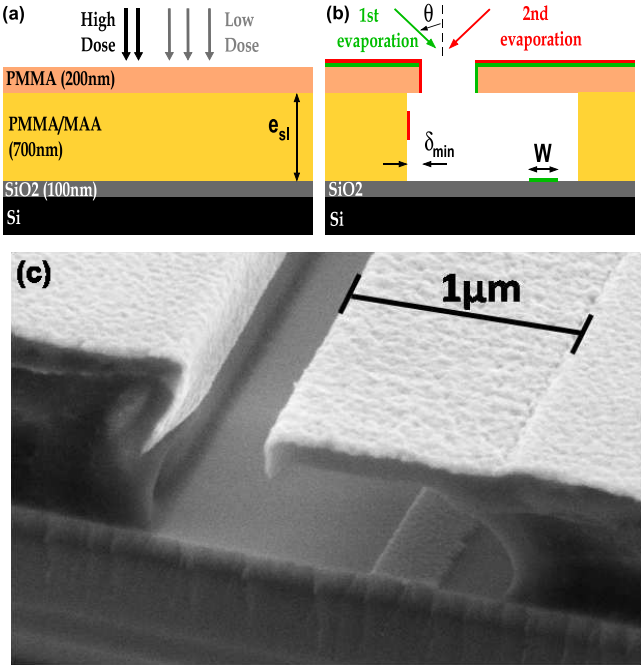

Figure 1. Schematic cross-sectional diagram of the BFT. (a) During the e-beam exposure. (b) During the evaporation, after the resist development. (c) A cross-section SEM image before lift-off obtained by cleaving the Si wafer. The first evaporated wire is below the undercut. The second evaporated wire is on the resist wall. The thicknesses of the two evaporated layers are, respectively, 15 and 30 nm.

the condition $W < tg(\theta) * e_{sl} - \delta_{min}$. e_{sl} is the support layer thickness and δ_{min} the residual undercut depth (see figure 1(b)). If the width is too large, both angle evaporations will be deposited onto the substrate and will short-circuit the junction. W is maximized for a strongly asymmetric undercut with δ_{min} as small as possible. It requires precise and local control of the undercut.

In order to quantify the undercut control in our process, we measured the undercut depth obtained after development as a function of the designed depth for two e-beam voltages of 20 and 100 kV (see figure 3). The data were obtained by measuring the undercut depth before lift-off on each side of a 250 nm large wire. For target undercut depths of more than 300 nm, the measured depths are equal to the designed depths, for both 20 and 100 kV. For a target undercut of zero, a residual undercut, δ_{min}, is observed. It is mainly produced by forward scattering of the electrons in the resist and therefore is strongly dependent on the e-beam voltage [16]. As shown in the insets in figure 3, δ_{min} drops from 250 to 40 nm when the voltage increases from 20 to 100 kV. This effect shows the advantage of having a high voltage for the control of strongly asymmetric undercuts. Therefore we developed the BFT using a 100 kV e-beam to minimize δ_{min} and maximize W. We obtain maximum connection wire widths of $W_{max}^{100\ kV} = 650$ nm and $W_{max}^{20\ kV} = 450$ nm at 100 kV and 20 kV, respectively. We would also like to mention that there are other ways of decreasing δ_{min} other than by increasing the e-beam voltage. The use of another developer instead of MIBK (for example, water and IPA [17, 18]) can increase the contrast of the

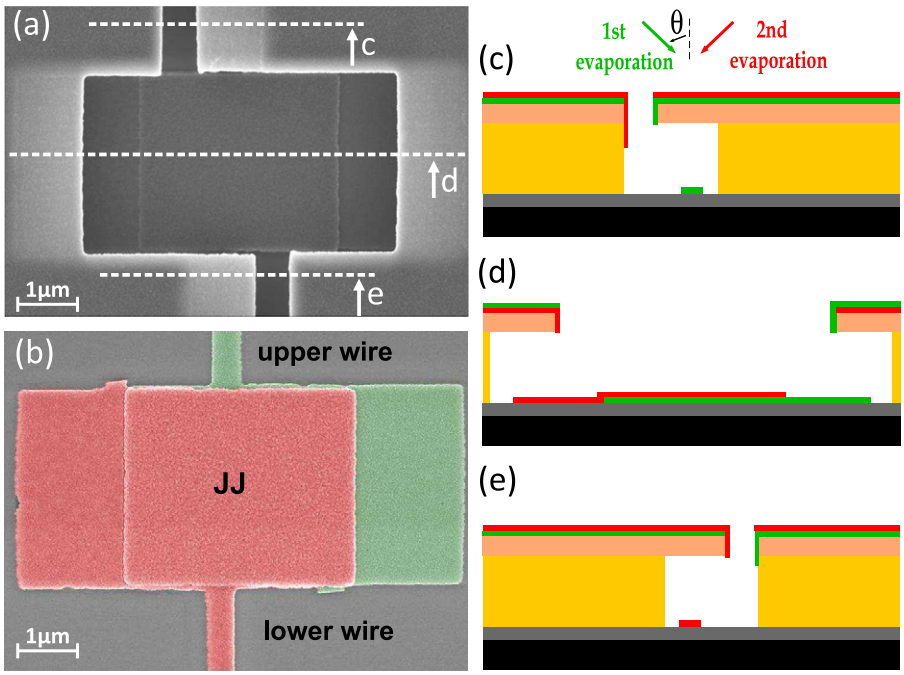

Figure 2. (a) SEM pictures of a junction (central part) and its two connecting wires before lift-off. The bright areas indicate the undercuts, the dark area the developed resist. The three white dashed lines refer to the schematic cross-sectional diagrams (c)–(e). (b) False-color SEM pictures after lift-off. The upper and lower wires, which correspond respectively to the first and the second evaporation (with respective thicknesses of 15 and 30 nm), connect the bottom and top electrode of the Al junction to the circuit.

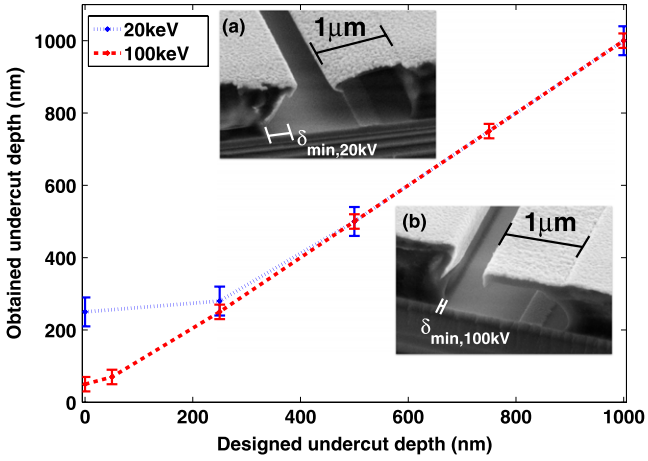

Figure 3. Obtained undercut depth after development versus designed undercut depth for electron beam energies of 20 and 100 keV. Insets (a) and (b) present SEM images of an asymmetric undercut, with the minimum achievable undercut depth $\delta_{\min}$ on the one side and a 1 μm deep undercut on the other side, for electron energies of 20 keV and 100 keV, respectively.

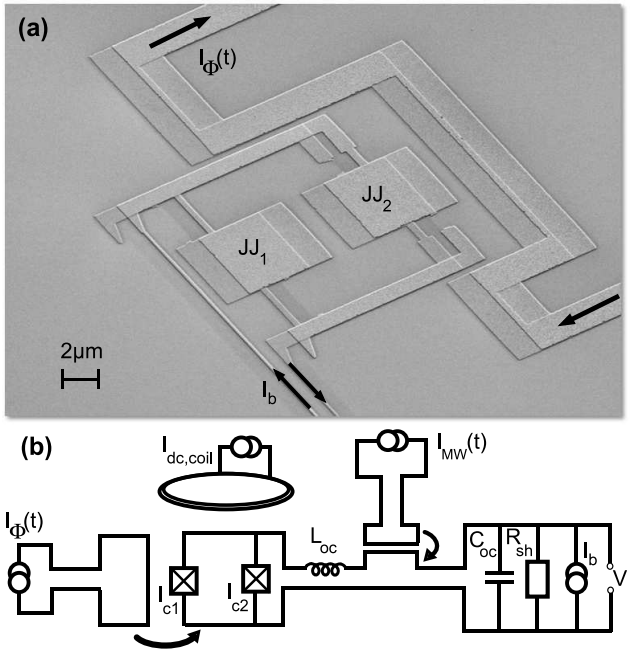

Figure 4. SEM image of a Camelback phase qubit based on a dc SQUID after lift-off. (b) The dc SQUID phase qubit is controlled by a dc bias current I_b and flux Φ_b, manipulated by an MW current and measured by a nanosecond flux pulse. The qubit is decoupled from the environment by a large kinetic inductance $L_e = 10$ nF and capacitance $C_e = 200$ pF and is shunted by a resistance $R_{sh} = 20$ kΩ.

PMMA/MAA and therefore decrease $\delta_{\min}$. The use of different resists for the support layer (like PMGI [15]) allows the use of separate developers for the support layer and the imaging layer, increasing the control of the undercut.

4. Camelback phase qubit realization

A Camelback phase qubit has been fabricated using the BFT. Figure 4(a) shows an SEM image of the device after lift-off. The SQUID loop with the two 10 μm^2-JJ (central part) is connected by two 100 nm thin and 200 μm long current bias lines (visible on the left bottom side). The larger wire on the right side is the antenna for the high frequency bias flux.

Figure 4(b) shows the electrical circuit for the measurement of the Camelback phase qubit.

The Al/AlO_x/Al qubit tunnel junctions and the device were formed by evaporating from a $-45°$ angle 15 nm of Al in a high vacuum chamber, oxidizing for 10 min in 30 mbar of oxygen, depositing at a 45° angle 30 nm of Al, and then lifting off the pattern. The IV characteristics at low temperature ($T = 40$ mK) of the dc SQUID gives the normal resistance of the two parallel tunnel junctions, $R_n = 246\ \Omega$. The total critical current, $I_{c,1} + I_{c,2} = 1.426\ \mu$A, measured at zero magnetic flux, is consistent with the Ambegaokar–Baratoff formula, $\frac{\pi\Delta}{2eR_n} = 1.405\ \mu$A, where $\Delta = 215\ \mu$eV is the Al superconducting gap extracted from IV characteristics. The subgap resistance is larger than the 20 kΩ of the shunt resistance and the retrapping current is less than 1 nA. Moreover the measurement of the I_c versus flux shows a very small critical current asymmetry between the two JJ of the SQUID, $I_{c,1} - I_{c,2} = 3$ nA. The small values of the retrapping current and critical current asymmetry as well as the large subgap resistance is a first proof of the high quality of the JJ made by the BFT.

We present results on the quantum dynamics at zero current bias when the potential is quartic and the qubit is insensitive to current noise [13]. Spectroscopy measurements were performed by applying a current bias microwave pulse of duration 800 ns. An adjusted nanosecond flux pulse is applied just after the microwave pulse and produces an escape whose probability P_{esc} is proportional to the occupancy of the excited qubit state [19]. Spectroscopy with a resonant peak corresponding to the transition between level $|0\rangle$ and level $|1\rangle$ of the qubit is shown in figure 5 inset (a). The phase qubit presents resonance peaks at ν_{01} with a width of $\Delta\nu_{0,1} = 4$ MHz. In figure 5, escape probability is plotted versus bias flux Φ_b and microwave frequency. The experimental energy spectrum $\nu_{01}(\Phi_b)$ is precisely described by the Camelback potential theory [13]. Relaxation time of about 200 ns has been measured on the qubit. Rabi oscillations were observed with a 170 ns exponential decay time (figure 5 inset (b)). From Ramsey oscillations we deduce a coherence time of about 160 ns which is consistent with the time extracted from the resonance peak width.

The spectroscopy also probes the microscopic two-level systems (TLS) which are coupled to the qubit [13, 20–22]. A density of about 25 visible TLS per GHz is measured with a typical coupling strength ranging between 10 and 40 MHz. These values are similar to the ones obtained on phase qubits with comparable JJ sizes realized by MLT and ShET techniques [20–22]. The BFT does not reduce the TLS density. However, as has been demonstrated [23], this limitation can be avoided by reducing the JJ size.

The coherence time of our device is about five times longer than the one measured in our previous samples, with identical design and electronic set-up but made by SMT [13] or ShET [14]. It is only twice as short than the state of the art in phase qubits [24]. This difference can be explained by the use of much smaller junctions compared to our circuit, enabling a drastic reduction of the TLS number. The coherence time in our device is significantly larger than the ones obtain

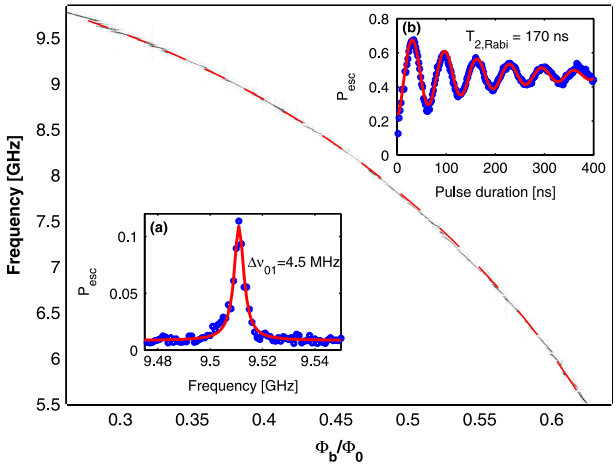

Figure 5. Camelback phase qubit dynamics. (a) Spectroscopy: P_{esc} versus reduced flux and microwave frequency for a current bias $I_b = 2$ nA. P_{esc} is enhanced when the frequency matches ν_{01}. Dark and bright grayscale correspond to high and small P_{esc}. Dashed line is ν_{01} versus reduced flux derived from the theory presented in [13]. Insets (a): qubit spectroscopy at $\Phi/\Phi_0 = 0.308$ and $I_b = 2$ nA. In this particular frequency window TLS are not visible. The fit is made by a Lorentzian curve. Inset (b): Rabi oscillation at the same working point.

recently on phase qubits based on similar junction sizes (several μm^2) [22, 25, 26]. These qubit coherence property measurements validate our novel technique for the fabrication of tunnel junctions.

5. Conclusion

The BFT has specific advantages compared to the standard techniques. It preserves the advantages of the ShET compared to the MLT with a single lithography step and submicron junction area. It enables realization of very large junctions as it eliminates the mechanical constraints imposed by the suspended bridges. It also exhibits higher robustness and reproducibility. The stronger mechanical strength as well as the absence of a bridge located just above the junction area enables direct and efficient cleaning of the junction area by reactive ion etching or ion milling. All these improvements lead to a better junction quality. In comparison with the recent technique based on deep resist trenches [27, 28], BFT also presents significant advantages. Indeed, since the deep trenches technique needs two perpendicular evaporations, it requires a more complex circuit pattern compared to circuits made by ShET and BFT. More sophisticated circuits can be reached with BFT by using, for example, three different evaporation angles and two different oxidations. We would also like to point out that tunnel junctions using the BFT and suspended bridge technique can be realized at the same time.

In conclusion, we present an original lithography process for *in situ* junction fabrication that does not use suspended bridges. This technique is based on the complete control of the bilayer resist undercut. The BFT reduces the usual mechanical limitations inherent to other suspended shadow-mask techniques and enables an improvement of the junction

quality. This novel method is able to realize junctions and on-chip capacitors with an extended size range, from 10^{-2} μm^2 to more than 10^4 μm^2. The IV characteristics as well as coherence properties of the Camelback phase qubit demonstrate the high quality of the junction. These results definitely validate the BFT as a promising method to realize junctions and capacitors for a wide range of devices.

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