High-Resolution Patterning for Panel Level Packaging

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ABSTRACT

More-than-Moore approaches to improve system performance have been a hot topic for a more than a decade as a way to maximize the efficiency and increase the bandwidth of high performance computing systems.

Fan-Out packaging that realizes submicron Redistribution Lines (RDL) and large die sizes is one technology that can help enable complex heterogeneous integration for applications including Artificial Intelligence (AI) and autonomous driving.

For systems requiring large package sizes, Panel Level Packaging (PLP) can offer efficiency and cost advantages over Wafer Level Packaging (WLP). PLP however poses unique technical challenges including the requirement to realize uniform submicron patterning across the entire rectangular panel. To meet this challenge, Canon developed the first patterning exposure tool (stepper) capable of submicron resolution on 500 mm panels.

The panel exposure tool is equipped with wide-field projection optics that offer a large 52 mm x 68 mm image field and a 0.24 NA that is optimum for submicron resolution. The stepper also features an updated panel handling system for processing up to 515 x 515 mm panels.

In this paper, we will report on our study of fine patterning on rectangular panels using the submicron resolution panel stepper and will introduce technology innovations supporting advanced heterogeneous integration. Our study researched photoresist material performance and slit-coating uniformity challenges we identified through collaboration with resist vendors and slit-coating equipment manufacturers.

We will report on the results of our collaborative study and will discuss current and future PLP advantages, challenges and solutions

Keywords: More-than-Moore, Heterogeneous Integration, Panel Level Packaging, Panel exposure tool, Sub-micron patterning

1. INTRODUCTION

As circuit scaling complexity and cost increase, More-than-Moore strategies to help realize higher system chip and system performance for leading-edge semiconductor applications. One More-than-Moore approach is die-to-die interconnection of SoC and DRAM using heterogeneous integration technology.

1.1 Demands for large packaging

Figure 1 illustrates the evolution of Field-Programmable Gate Arrays (FPGA). FPGA system configurations were originally single SoC, but larger chips have been required to improve performance but yield loss increased as chip sizes expanded. FPGA transitioned to a split-die strategy after 2010, with large FPGA die being split into smaller functional segments that can be manufactured with a higher yield. FPGA systems consisting of integrated Known-Good-Die (KGD) were then assembled using silicon interposers. Because demand for high-performance computing is growing, FPGA interconnected with High Bandwidth Memories can communicate with DRAM at a high-bandwidth using this heterogeneous integration technology.

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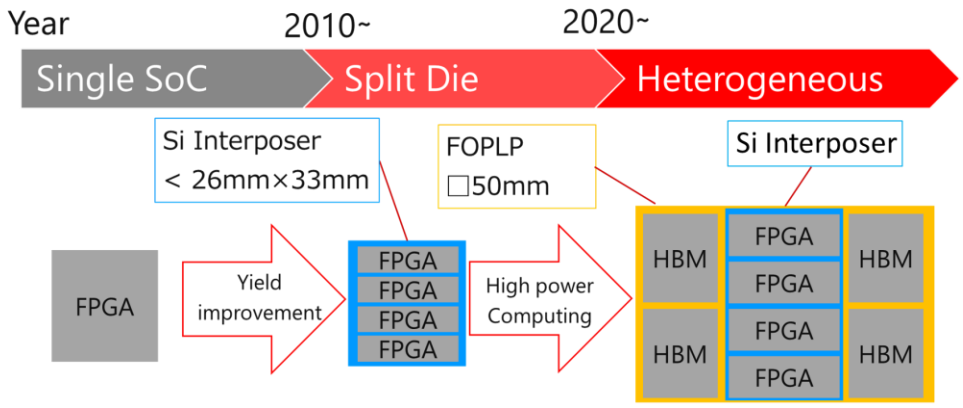


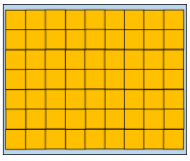
Figure 1. FPGA Evolution

1.2 Advantages of Panel Level Packaging

Two candidates for realizing die-to-die heterogeneous interconnection are Fan-Out Wafer Level Packaging (FOWLP) and Fan-Out Panel Level Packaging (FOPLP). FOWLP has been applied to commercial production of mobile processors and Canon's FPA-5520iV i-line stepper is widely used in this market [1][2][3].

Panel Level Packaging (PLP) can help reduce costs by increasing the number of packages contained on each substrate and can also provide increased substrate utilization for large packages. FOPLP can provide cost advantages, especially in large die-size chip manufacturing and table 1 shows a substrate utilization comparison between FOWLP and FOPLP for 55 mm square package manufacturing. The data compares 300 mm wafer and 510 x 515 mm panel processes and the analysis illustrates that for a 300 mm wafer, approximately 36% of the wafer substrate will unavailable for processing. In contrast, FOPLP process adopters can expect to achieve as high as 90% panel substrate utilization for 55 mm packages.

Table 1. Substrate Utilization for FOWLP & FOPLP

Category	**Packaging method**	
	FOWLP	**FOPLP**
Substrate size	300 mm Circle	510 mm x 515 mm
# shots / substrate	15 shots	63 shots
Effective shot area	64 %	90 %
Layout		

1.3 Panel Level Packaging Challenges

Advanced Graphics Processing Units (GPU) and FPGA require wideband interconnection with memory for autonomous driving and high-performance computing. Next-generation devices require submicron Redistribution Layers (RDL) and large die sizes to enable high-performance GPU and FPGA designs and FOPLP will become a more important technology in the near future.

Conventional panel lithography systems used in packaging substrate manufacturing were originally designed for circuit board fabrication and are typically designed to support RDL design rules with Line & Space Critical Dimensions (CD) of

greater than 5 µm. These systems cannot provide the precision and resolution required for advanced packaging for high-performance GPU and FPGA targeting AI processor applications requiring less than 2 µm resolution.

To fill the resolution gap for panel-based processes, Canon launched the FPA-8000iW panel-based stepper in July 2020.

Lithography system performance for panel level packaging is also related to the associated panel-level process performance. A robust slit coating process with good coating uniformity must be developed and we have collaborated with photoresist and slit coater vendors to study slit coating performance for fine-resolution panel processes.

In this paper, we will provide and update of performance evaluation data of the panel stepper and including panel substrate exposure results.

2. PANEL STEPPER INTRODUCTION

2.1 Panel Stepper Design Concept

The FPA-8000iW is Canon's first panel stepper targeting panel-based advanced packaging applications including FOPLP. [6] Shown in Figure 2, the panel stepper adopts proven units from the FPA-5520iV wafer steppers including projection optics, auto focus and auto alignment system. The panel stepper platform features a unique main-body, stage and substrate handling systems to enable large panel processing.

The panel stepper provides the same imaging performance as FOWLP, but on panel substrates. The panel stepper utilizes a UL82 projection lens that is common to the wafer stepper whose basic performance we reported in 2018[4] and 2019[5]. The panel stepper also adopts an in-situ Optical Tilt & Focus (OPTF) measurement system developed for wafer steppers that measures the focus and tilt position on each field or die. The substrate focus and tilt position is corrected on a die-by-die basis prior to exposure to maximize Depth-of-Focus (DoF) and help realize submicron patterning without productivity loss.

Figure 2. FPA-8000iW Panel Stepper

2.2 Specifications

Table 2 shows the specifications of the panel stepper. It uses a SEMI standard 6 inch reticle as a mask and customers can continue to make high quality masks at conventional mask houses. The system footprint is (W) 3000 mm, (D) 4800 mm and (H) 2700 mm.

The panel stepper optical system offers a variable Numerical Aperture (NA) with a maximum value of 0.24 that is designed for 0.8 µm line and space patterning. The maximum exposure field size is 55 x 55 mm although the stepper is equipped with a masking blade unit that allows the exposed portion of the photomask to be defined by recipe parameters.

The Single Machine Overlay accuracy of the panel stepper is less than 200 nm. Overlay accuracy is important to fine advanced packaging because poor overlay accuracy induces RDL placement error, requiring looser RDL pitch that lower system density.

The Maximum substrate size is 510 mm x 515 mm which is de-facto standard in package substrate process. The throughput is more than 40 panels per hour at 200 mJ/cm^2 exposure dose and 60 shots per panel.

Table 2. Panel Stepper Specifications

Category	**FPA-8000iW**	
	Item	***Specification***
Imaging	Mask	SEMI 6 inch reticle
	Reduction Ratio	2 : 1
	Maximum NA	0.24
	Resolution	0.8 µm
	Distortion	150 nm
	Field Size	55 mm square
Substrate	Maximum Size	510 mm x 515 mm
	Thickness	0.4 - 1.4 mm
Overlay	Single Machine Overlay	200 nm
Productivity	Throughput	40 panels / hour
Footprint	Width	3,000 mm
	Depth	4,800 mm
	Height	2,700 mm

3. PANEL STEPPER PERFORMANCE EVALUATION

A panel stepper debugging tool was developed and assembled to evaluate the panel stepper performance. We will report in-house evaluation data including exposure results from a Copper Clad Laminate (CCL) panel shown in figure 3. The entire panel area was exposed with 55 mm square exposure fields.

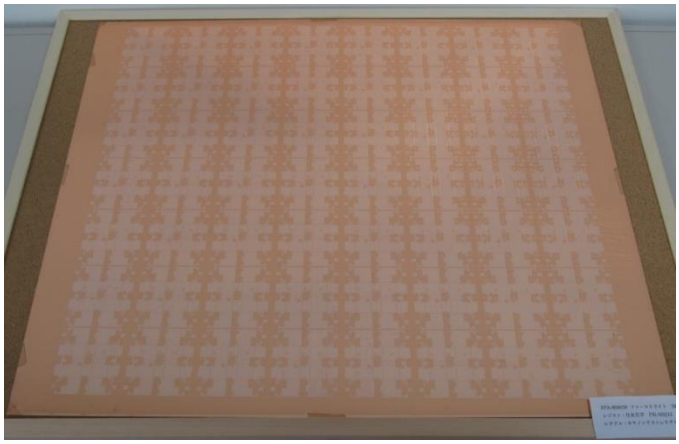


Figure 3. CCL Panel Exposed by a Panel Stepper

3.1 Panel Stepper Resolution (Critical Dimension)

Submicron resolution on a panel is very important to realize advanced packaging for high performance computing chips and we studied submicron patterning using the panel stepper.

Figure 4 offers an imaging comparison of wafer and panel-based steppers. Scanning Electron Microscope (SEM) images for 0.6, 0.7 and 0.8 µm Line & Space features are displayed. Panel evaluation was performed on a glass panel using 1.5 µm thick AZ 7904 photoresist from Merck Performance Materials Ltd. Silicon wafer evaluation used 1 µm thick PFi38 resist from Sumitomo Chemical.

The data shows that both the wafer and panel steppers were able to resolve 0.8 and 0.7 µm line and space patterns. The panel stepper could not resolve 0.6 µm patterns, matching the optical performance of the wafer stepper.

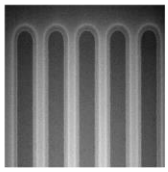
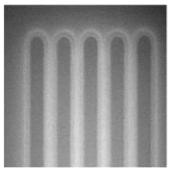
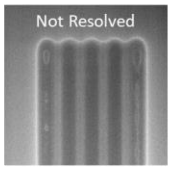
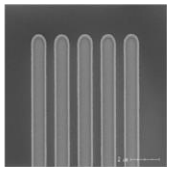
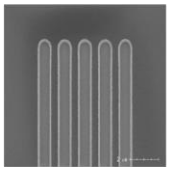
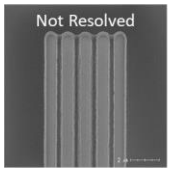
	0.8 µm	0.7 µm	0.6 µm
Panel stepper (FPA-8000iW, NA 0.24) Substrate: Glass panel PR: AZ 7904 1.5 µm thick Pattern: Trench (Space) SEM: A-SEM (Charm Engineering)			
Wafer stepper (FPA-5520iV, NA 0.24) Substrate: Si wafer PR: PFi38 1.0 µm thick Pattern: Trench (Space) SEM: S-9360 (Hitachi High-Tech)			

Figure 4. Panel & Wafer Stepper CD SEM images

Figure 5 shows Depth of Focus (DoF) results based on an evaluation of an exposed glass panel using 1.5 µm thick AZ 7904 photoresist from Merck Performance Materials Ltd.. 1.0 µm Line and Space patterns located at the image center were exposed using different focus positions.

DoF for 1.0 µm L/S patterns with a +-10% Critical Dimension (CD) error was 8.6 µm. This DoF is large enough for flat glass panel production for RDL-first and glass interposer processes but flatness must be carefully controlled throughout the substrate processing.

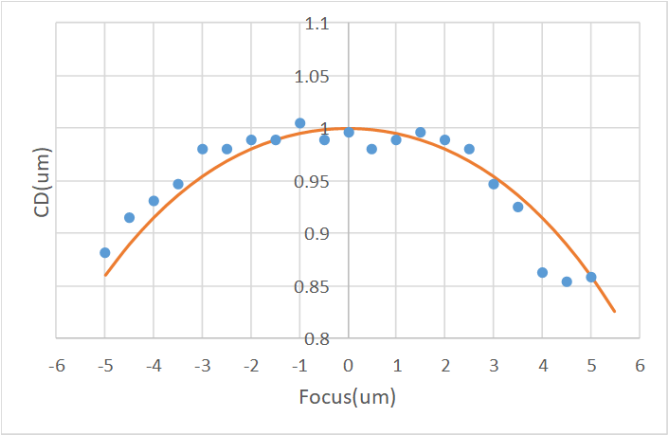


Figure 5. DoF Result for 1.0 µm L/S Patterns on Glass Panel

Figure 6 shows Depth of Focus evaluation results on a 300 mm silicon wafer substrate. The target pattern is 0.8 µm Line and Space patterns measured at 9 points across exposure field. Evaluation data was collected using 1 µm thick PFi38 resist from Sumitomo Chemical. DoF for the 0.8 µm L/S patterns with a +-10% CD error was 9.6 µm.

The DoF of the silicon wafer is larger than the 1.0 µm CD DoF measured on a glass panel and reported in Figure 5. The difference is thought to be due to photoresist compatibility and performance. Panel processes commonly use slit-coaters to deposit photoresist onto substrates the selection of photoresists compatible with slit-coating equipment and processes is limited. Slit-coating process enhancement and DoF expansion may be possible with slit-coating materials and process innovation

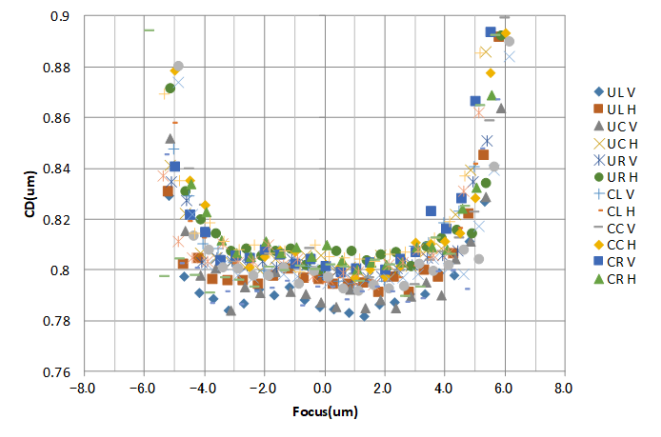


Figure 6. DoF Result for 0.8 µm L/S Patterns on Silicon Wafer

3.2 Resist Cross-Section Analysis

Thick resists are used in packaging processes and it is important to control photoresist cross sectional profiles to improve plating and etch profiles. To understand this relationship we studied thick resist patterning with resist manufacturers using silicon wafers to make cross sectional samples.

Figure 7 is the cross sectional SEM images of 0.8 µm Line & Space patterns in 5 µm thick photo resist, which is THB-801P provided JSR Corporation. Good profile is achieved for 0.8 µm resolution in 5 µm thick photo resist.

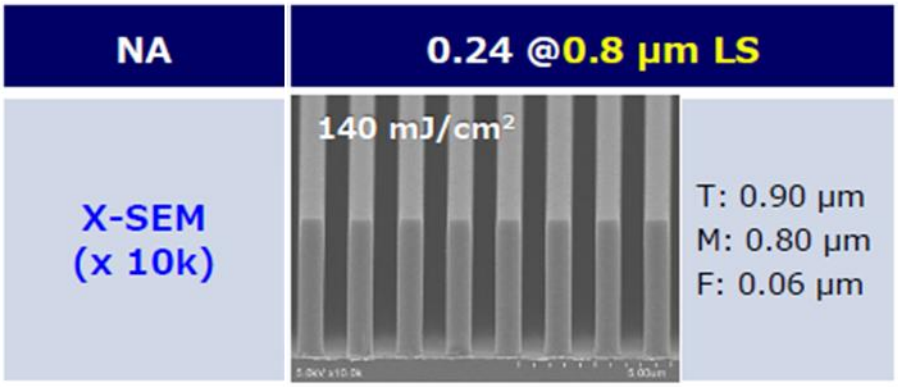


Figure 7. Cross sectional SEM image for 0.8 µm L/S Patterns on Silicon Wafer

Figure 8 shows the cross sectional SEM images of 1.0 to 0.775 µm Line & Space patterns in 4 µm thick XI series photoresists provided by Sumitomo Chemical Co. Ltd. Two materials were evaluated to compare the resolution limits between the two materials. The evaluation showed that both materials A and B have good profiles for 0.8 µm line and space patterns, but material B has better profile for 0.775 µm line and space patterning. From this study, submicron patterning capability of NA 0.24 projection optics has been confirmed and resist optimization is effective for improving cross-sectional profiles.

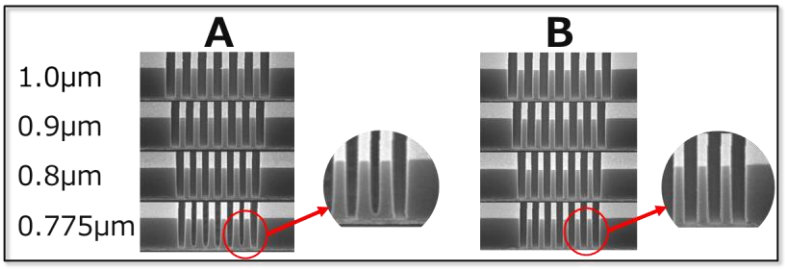


Figure 8. Cross sectional SEM image for submicron L/S Patterns on Silicon Wafer

3.3 Panel Stepper Overlay Performance

Fine-RDL manufacturing requires accurate overlay compensation to align trace and via patterns connecting multiple RDL layers. Improved overlay accuracy can improve process yield and can relax RDL design rules that currently require large RDL pitches and large capture pads to compensate for overlay errors.

Panel steppers target less than 200 nm in single machine overlay and Figure 9 and Table 3 show single machine overlay evaluation data for three panels, 45 shots in each panel with 9 measurement points in each shot. The maximum 3-sigma for panels W1, W2 and W3 was X = 82.4 nm and Y = 76.5 nm. This overlay performance is thought to be sufficient to support fine RDL manufacturing for FOPLP.

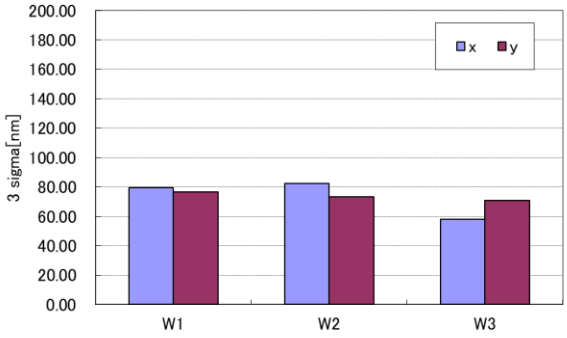


Figure 9. Single Machine Overlay Result

Table 3. Single Machine Overlay Evaluation Results

Panel No	X	Y
W1	79.3 nm	76.5 nm
W2	82.4 nm	73.4 nm
W3	57.9 nm	70.9 nm

3.4 Productivity

One important advantage of FOPLP is cost-effectiveness due to the much larger of chips in one substrate. Stepper productivity is very important to maximize this advantage and to help increase productivity and reduce overall panel

process costs, the panel stepper provides a large 55 x 55 mm field size. The large field size can reduce field count and allow for larger or multiple chips to be exposed in a single shot.

We studied panel stepper throughput under the process conditions described in Table 4 and the throughput evaluation results are showed in Table 5. The panel stepper achieved 63.3 panels per hour with 45 shots per panel and 53.9 panels per hour with 60 shots per panel. By using a larger field size that exposed the entire panel in fewer shots, the panel stepper throughput increased, demonstrating that field size optimization can help improve productivity and Cost of Ownership.

Table 4. Throughput Evaluation Conditions

Item	Condition
NA	0.24
# of shots	45 shots / 60 shots
Dose	2,000 J/m^2 (200 mJ/cm^2)
Focus mode	Die by die tilt and focus

Table 5. Throughput Evaluation Result

# of shots	Panels Per Hour
45 shots	63.3 PPH
60 shots	53.9 PPH

4. PANEL PROCESS OPTIMIZATION

Process development is very important for fine panel level packaging to succeed. Photoresist coating uniformity in panel process is worse than in wafer processes because panel processes use slit coaters and wafer processes use spin coaters.

Figure 10 provides an illustration comparing slit-coating and spin-coating methods for coating substrates. In spin coating, photoresist is dispensed onto the center of a substrate that is being rotated at a specified rotational speed. Centrifugal force created by the rotation causes the photoresist to spread and cover the entire wafer. Coating thickness and uniformity is critical and dependent on a variety of factors including materials size & shape, photoresist material viscosity, temperature, volume and spin speed.

Although spin-coaters are widely used in silicon wafer process, they are rarely used in panel processes due in part to the difficulty achieving uniform coating thickness at the panel corners. Spin-coaters for panel substrates also require a larger footprint to spin the larger panel substrates.

On the other hand, slit coating dispenses photoresist from a nozzle as the nozzle or panel are scanned along the orthogonal direction of the nozzle length. The photoresist is spread by surface tension and slit coating has an advantage in photoresist efficiency because all photoresist remains on the substrate. The disadvantage of slit coating is its difficulty achieving good coating uniformity.

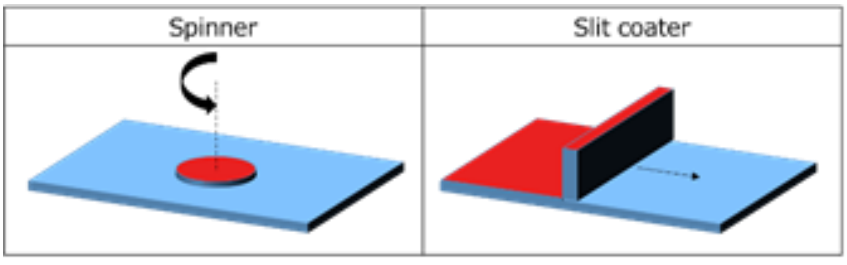


Figure 10. Comparison of Coating Methods

Poor coating uniformity induces poor CD uniformity due to photosensitivity fluctuation due to resist thickness variation. Coating uniformity improvement is a key challenge for FOPLP. To improve CD uniformity improvement in a slit coater process we worked with Merck Performance Materials Ltd. and Toray Engineering Co., Ltd.

4.1 Coating Uniformity

Prior to exposure testing, we performed a simulation to study coating error target values for 1.0, 2.0 and 5.0 µm patterns. Figure 11 shows the photoresist thickness variation target required to maintain CD Uniformity within ±5% of the target CD.

The simulation showed that coating uniformity must be less than 1.6% to maintain pattern fidelity for 1.0 µm Line and Space patterns. 3% photoresist thickness uniformity must be maintained to control 2.0 µm processes and uniformity must be within 10% for 5.0 µm processes.

As a reference, Figure 11 also plots the previously demonstrated 0.23% spin-coating uniformity on silicon wafers which easily satisfies the photoresist coating uniformity requirements for 1.0 µm Line and Space patterning.

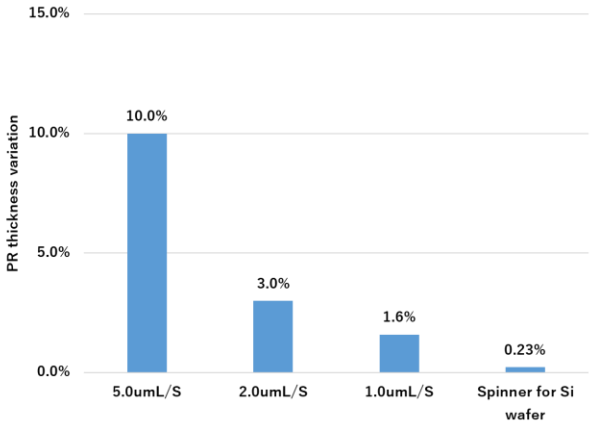


Figure 11. Coating Uniformity Target vs CD

Before starting optimization, we studied coating uniformity performance of our current slit coating process using AZ 7904 resist from Merck Performance Materials Ltd. Figure 12 illustrates the slit-coating uniformity across the panel. The data showed that the non-optimized slit coating thickness uniformity was ±5.7% which was not sufficient for 1.0 µm resolution processes that require 1.6% uniformity [6].

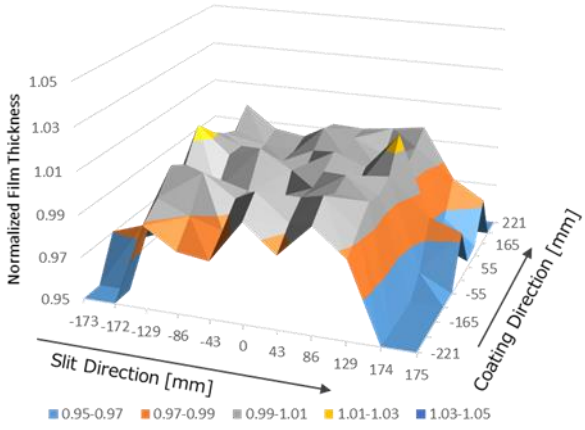


Figure 12. Slit Coating Uniformity BEFORE Optimization

Next we modified the photoresist ingredients and Figure 13 shows slit coating uniformity after optimization. Coating uniformity after modification narrowly missed the uniformity target at ±1.7%. While the slit-coating uniformity achieved is slightly larger than our simulated target, it is substantially improved over the original material and may be a viable option for submicron processes.

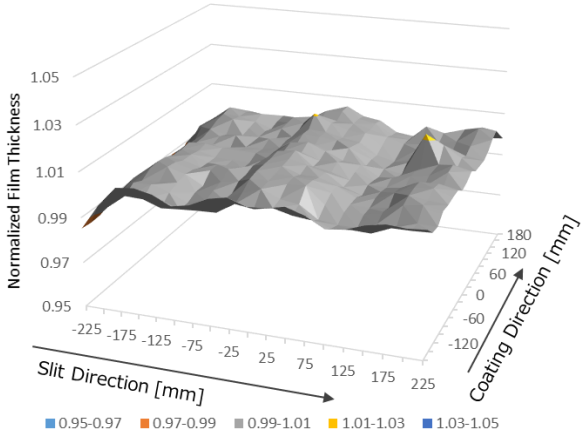


Figure 13. Slit Coating Uniformity AFTER Optimization

4.2 CD Uniformity

To confirm that exposure results matched to the simulation results, we performed a CD Uniformity (CDU) study using the optimized photo resist and panel stepper. Evaluation conditions and detailed in Figure 14 and Table 6. CD variation was +-19.4 nm and is less than +-2% Critical Dimension Uniformity (CDU) for 1.0 µm Line and Space patterns.

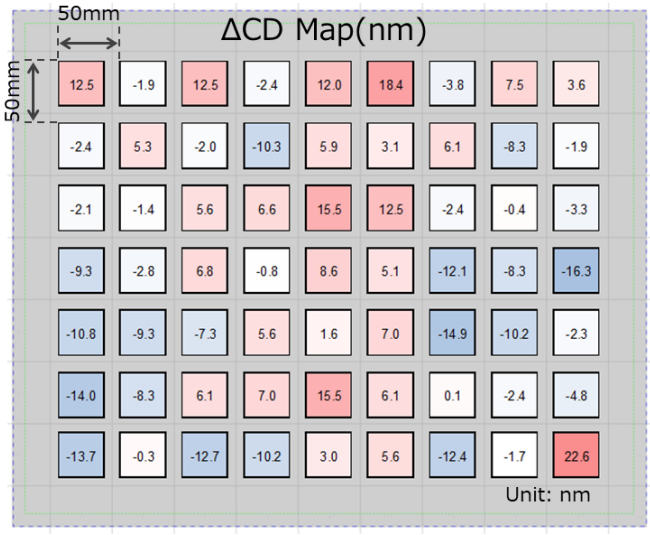


Figure 14. 1.0 µm L/S CD Uniformity Using Optimized Slit Coating Process

CDU data in Table 6 shows that the maximum measured value for any field was 1.0226 µm which is only 22.6 nm or 2.3% greater than the 1.0 µm target. The lowest CDU value was 0.9837 µm, only 1.6% below the 1.0 µm target. Total CDU Range for all 63 fields was only 38.9 nm or ±1.9% of target [6].

Table 6. Critical Dimension Uniformity Evaluation Result

	SEM Result for 1.0 µm (1,000 nm) L/S
Maximum	1,022.6 nm (+2.3 %)
Minimum	983.7 nm (-1.6 %)
Range	38.9 nm (+-1.9 %)

Our result is that current slit coating processes and materials evaluated may not be capable of supporting sub-micron patterning, but we are encouraged by the results and will continue studying panel processes to enable sub-micron FOPLP including optimization of lithography equipment and materials for panel-based processes.

5. CONCLUSION AND FUTURE WORK

Key lithography challenges that must be overcome to realize fine resolution FOPLP in high volume manufacturing include the need for a fine resolution panel stepper and slit coating uniformity improvement.

Solutions offered in this paper include the introduction of a panel based stepper developed to help enable fine resolution RDL fabrication and Panel Level Packaging, and update on work towards slit-coating process and material optimization. Evaluation data presented met all initial design specifications for our results met initial milestones that we hope will help drive panel-based process adoption.

Evaluation of the fine resolution panel stepper demonstrated that the stepper can achieve resolution as low as 0.7 µm on glass panel substrates. Overlay testing also showed that the panel stepper achieved less than 100 nm Single Machine Overlay accuracy.

The fine resolution, overlay and production performance make the panel stepper a viable solution for fine RDL patterning in high-volume FOPLP processes.

Our study also demonstrated that panel photoresist slit-coating uniformity could be controlled within ±1.7% which is a promising result that is close to the simulated uniformity target for 1.0 µm processes. Results showed that slit-coating process uniformity can be improved through photoresist material ingredient and process modification.

Together, the panel stepper and optimized slit coating materials can help enable large size FOPLP packages supporting high-performance and high-bandwidth FPGA and GPU applications.

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