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WHITE PAPER

Monolithic microsystems

Elevate your application to new heights with extra functionalities on top of standard CMOS

Contents

What to expect from this white paper?

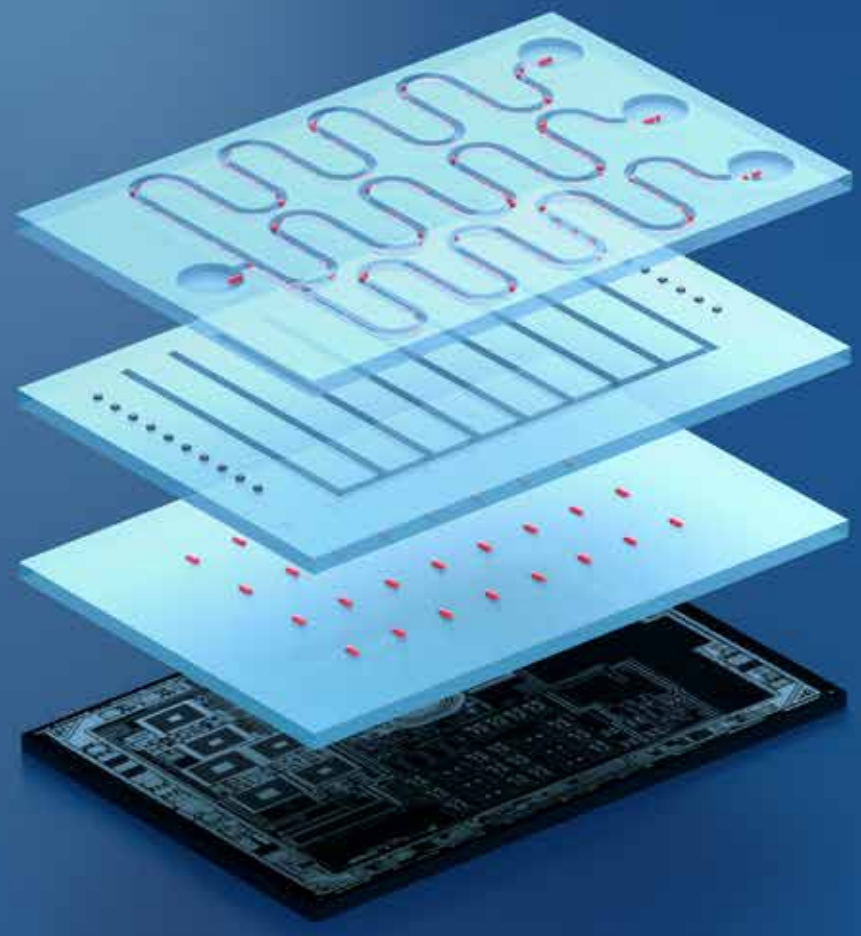
In this white paper, we will discuss how you can make a **more integrated solution of your application**. It deals with an innovative chip-based approach, offering integration of driving and reading electronics with **massive sensing parallelism**. This approach is known as **post-processing or MEMS processing** and adds – in an extremely compact way – sensing technology blocks such as **optical components, integrated photonics, fluidics, electrodes and emerging materials** that are not present in typical CMOS fabs.

Imec experts unveil what kind of functions can be added on top of foundry-fabricated CMOS wafers and how this can contribute to more efficient systems in terms of **speed, performance, cost, user-friendliness** and with the potential of extreme parallelization and miniaturization.

Throughout this paper we will illustrate:

- the technology options with **several project examples (having varying technology readiness levels, TRLs)**
- showcase the capabilities of imec's **200mm and 300mm cleanroom** with its unique and **extremely advanced patterning** options, and its flexibility – also in terms of material use
- the **broad expertise of the team** that allows for cross-disciplinary idea exchange

We wish you lots of valuable insights with this reading.



Introduction

Why turn to monolithic microsystems?

Monolithic microsystems refer to integrated systems that are fabricated on a single semiconductor substrate. Think of a **standard CMOS wafer with electronic functionalities, topped with MEMS, optical, or fluidic components, all on the same chip**. The term 'monolithic' emphasizes the seamless integration of diverse functionalities into a single structure. This approach – as opposed to hybrid approaches where the different components are assembled separately on e.g. a PCB or interposer – is beneficial in terms of cost, size, reliability, speed and performance.

The standard CMOS wafer – 200mm or 300mm in size – is fabricated in a foundry, under tightly controlled conditions. The **'post-processing' of the extra functional layers** – called this way because it happens after the standard CMOS processing is done – is performed at a different facility. This facility must deal with the challenge of **not harming the underlying electronics** (temperature, mechanical stress) and must be extremely **flexible** in terms of making a unique stack or module for the specific application and in terms of using non-standard materials (e.g. platinum).

Monolithic microsystems are relevant for a multitude of application domains: consumer electronics (AR/VR), healthcare (lab-on-chip), automotive (integrated LiDAR), industrial automation (spectral sensors), etc.

Post-processing of CMOS is the close integration of driving and reading electronics with massive sensing parallelism. CMOS is the technology block used for reading and driving, whereas the sensing technology blocks are optical, integrated photonics, fluidics, MEMS or emerging materials that are typically not present in CMOS fabs.

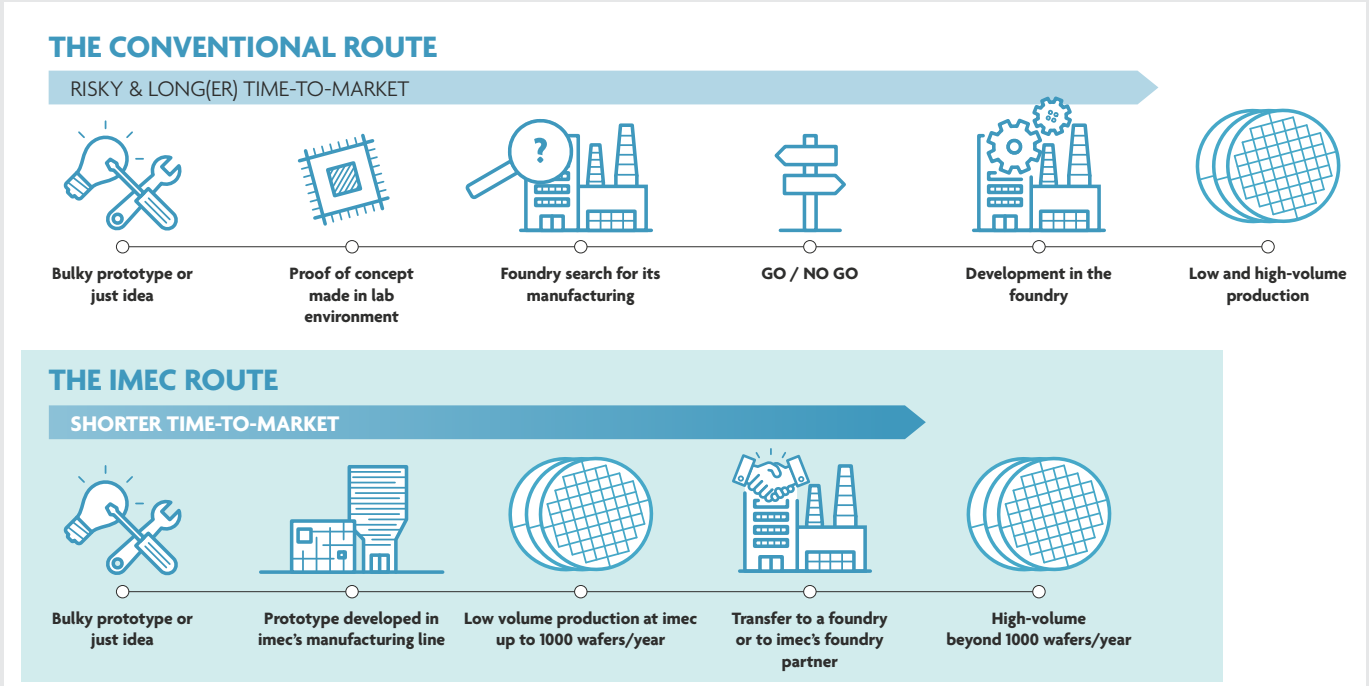
Imec as a post-processing partner

In this whitepaper we will discuss various functional layers, materials and techniques, that imec uses to make true monolithic microsystems for **industry, startups, research labs etc.** It showcases our expertise and the examples that are given are excellent illustrations of the **immense knowledge and engineering capabilities** of our team. Imec offers:

- state-of-the-art infrastructure, both for **200mm and 300mm wafers**
- the most **advanced lithography** tools with sub-5nm overlay capabilities i.e. the precision and accuracy with which multiple layers of patterns are aligned on top of each other
- **high flexibility** in terms of process flow and materials
- a **broad range of expertise** under one roof, enabling cross-disciplinary exchange of ideas.
- access to the **complete trajectory**, from concept idea to prototype, and access to low-volume manufacturing (up to 1,000 wafers per year); and access to high-volume manufacturing – via our network of preferred partners – with a seamless transfer of the process flow knowhow. Find more info here: www.imec-int.com/en/what-we-offer/development and www.imeciclink.com

Imec's patterning options are unique in the world, covering a broad range of tools for both micro and nanostructures. This includes:

- **200mm:**
  - I-line 1X
  - I_line stepper
  - DUV 248nm lithography
  - Dry 193nm lithography
  - Nano Imprint lithograhy
- **300mm:**
  - I-line 1X
  - DUV 248 lithography
  - Immersion 193nm lithography
  - EUV lithography
  - Nano Imprint lithograhy
  - E-beam



Tools for monolithic microsystems, available in imec's 200mm and 300mm semiconductor pilot line

200mm cleanroom

Imec's 200mm cleanroom is equipped with advanced semiconductor manufacturing equipment for processing 200mm/8inch wafers. It is operated in a flexible way, both in terms of process flows and materials. The ideal environment for heterogeneous integration of all kinds of components – CMOS, photonics, fluidics, and other functional layers – into compact systems.

FACTS

- Flexible platform to fabricate prototypes: process steps that are not available off-the-shelf in a foundry
- Low-volume production
- Silicon pilot line with a 130nm TLM CMOS baseline process on 200mm wafers
- Processing on Si and on alternative substrates such as III-V materials, organic semiconductors, SiGe ...
- 3D-IC and 3D-WLP stacking IC baseline flows: Die-to-die bonding, Die-to-wafer, Wafer-to wafer-bonding
- All processes for heterogeneous integration: Bonding, Grinding, Thick Cu plating, Deep Si etch, Litho with back-to-front alignment
- GaN-on-Si capabilities to process power devices
- Bay & chase type of cleanroom
- 5,200m^2 of which 1,750m^2 in class 1 area

300mm cleanroom

Imec's 300mm/12inch cleanroom is focused on researching and developing very advanced sub-2nm CMOS nodes. In the context of monolithic microsystems with on top of CMOS functionalities, this environment is ideally suited for making very small structures such as nanopores, nanoelectrodes etc.

FACTS

- Advanced Lithography centered around ASML scanner equipment
- EUV – Extreme ultraviolet lithography
- DSA: Directed Self Assembly
- State-of-the-art etch, implant, clean, metrology, deposition, ... equipment from leading-edge OEMs
- Ballroom type of cleanroom
- Class 1,000
- Operational 24/7
- Process monitoring, cycle time improvement, quality control
- Total area: 12,000m^2

Functional layers on top of CMOS

1. Integrated photonics

Just as electronics uses electrons to generate, transmit and process signals, photonics uses **light as a carrier of information**. Thanks to advanced miniaturization processes it is now possible to make compact optical components – such as waveguides, modulators, detectors and light sources – that can manipulate and control light on a small scale, on a chip.

The advantage of using light is a **higher transmission speed, larger bandwidth, energy efficiency, signal integrity** etc. The best-known integrated photonics applications are the optical interconnects for tele- and datacom. Other applications are biosensing, quantum computing and 3D sensing (e.g. lidar).

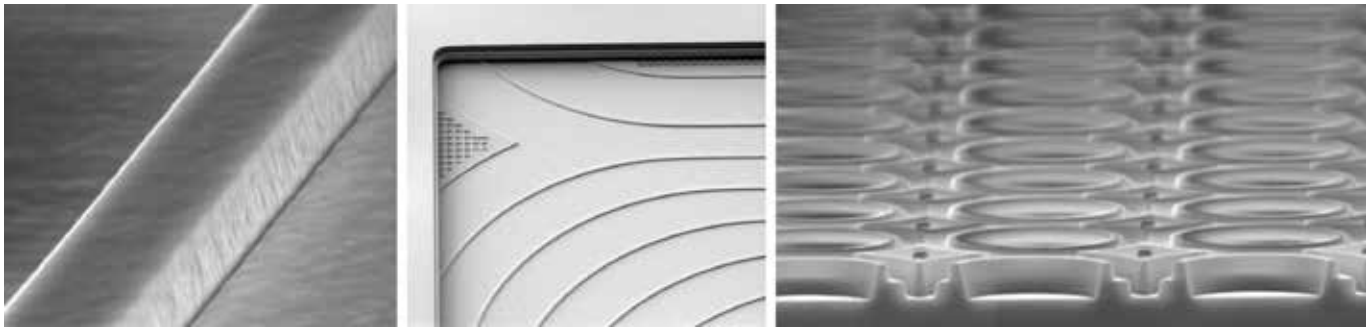
Components

Integrated photonics uses passive and active components **to guide and manipulate light**. They can be combined into a **photonic integrated circuit or PIC** to perform specific functions such as optical switching, signal routing or sensing.

For some applications, it can be feasible to post-process photonic building blocks on top of CMOS. Some examples of photonic components:

- waveguides to guide light waves from one point to another
- modulators to alter light waves (amplitude, phase, frequency) to encode data onto the light waves
- non-silicon detectors for short-wave infrared (SWIR) sensing
- filters to selectively transmit or block specific wavelengths
- different type of lenses (fresnel lens, metalens, ...)
- couplers or splitters to combine or distribute optical signals

A light source (e.g. laser) can be heterogeneously integrated, via flip-chip bonding or transfer printing.



From left to right: Tilted view of SiN waveguide; Array of waveguides where one part is exposed to air; Array of lenses processed on top of CMOS imagers.

Materials

There are different material platforms for integrated photonics. These are silicon-based which allows to reuse the technology maturity and existing infrastructure of the CMOS fab, including the use of 300mm wafers, a high yield, co-integration with CMOS and 3D integration techniques.

The main material platform is **silicon-on-insulator (SOI) or silicon (Si) photonics**. It allows the propagation of light with wavelengths in the 1 to 2 µm range, which are actually the same wavelengths that are used in glass optical fibers for tele- and data-communication applications.

Another material platform is **silicon nitride photonics (SiN)** which has lower light losses and a broader spectral coverage (including visible and near-infrared). This is important for life science applications such as spectroscopy, cytometry, optical coherence tomography (OCT) etc. that make use of visible light. This platform can be used to post-process photonic components on top of CMOS, provided that a low-temperature process is used.

Both SOI/Si and SiN photonic components can be combined in one integrated circuit, allowing to have the best characteristics for each component. The challenge of this **co-integration** is to overcome the difference in processing temperature, which is higher for SiN than for Si-based photonics. One approach is to do a separate processing and bond the wafers together with wafer-to-wafer bonding.

A third material platform uses **III-V materials** for laser integration. The lack of an integrated light source was long a challenge in integrated photonics. III-V based light sources are used such as Indium Phosphide or Gallium Arsenide, depending on the required wavelength. These lasers can be integrated via micro-transfer printing or flip chip.

Imec SiN photonics platforms

Imec has developed several mature platforms for SiN photonics to meet the toughest customer requests for monolithic microsystems. It includes:

- **Ultra-low-loss SiN**, based on low-pressure chemical vapor deposition (LPCVD)
    - for ultra-low loss applications such as data- and telecommunication, AR/VR, life sciences, quantum computing
    - available on 200mm wafers
    - wide wavelength range from 450nm to 2400nm
    - extremely low waveguide loss: < 0.1 dB/cm down to 2 dB/m
- **Low-temperature CMOS-compatible SiN**, based on plasma-enhanced chemical vapor deposition (PECVD)
    - for integrated photonics on top of CMOS imagers and flat optics
    - available on 200mm wafers (BioPIX150 for 400nm – 700nm applications; BioPIX300 for 700nm – 1000nm applications) and 300mm wafers
    - Wide wavelength range from 450nm to 2400nm
    - Low waveguide loss: < 2 dB/cm down to 0.3 dB/cm

Next to this, imec also has SOI, co-integrated Si/SiN and III-V-on-Si(N) material platforms available. The uniqueness of its expertise lies in the fact that different disciplines can be combined with the integrated photonics capabilities.

Project example

TRL

Integrated photonic nanopore devices

Silicon-nitride based photonics is a valuable platform for life science and sequencing applications. For example, the **combination of solid-state nanopores and waveguides** results in a fast, scalable, optofluidic device for **highly sensitive single-molecule detection**. In this device, the molecules travelling through the nanopores are measured optically, taking advantage of the sensitivity and spatial resolution of optical detection methods.

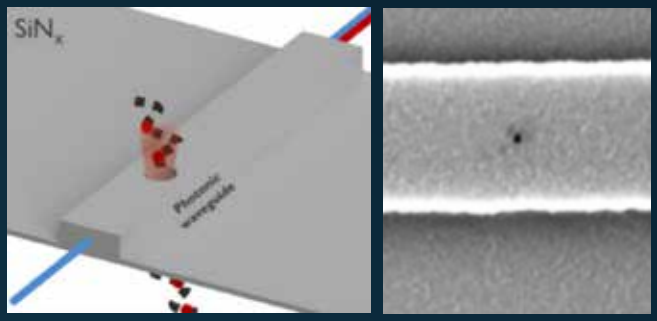


Illustration and SEM image of an integrated photonic nanopore device for fast, scalable single-molecule fluorescence-based detection.

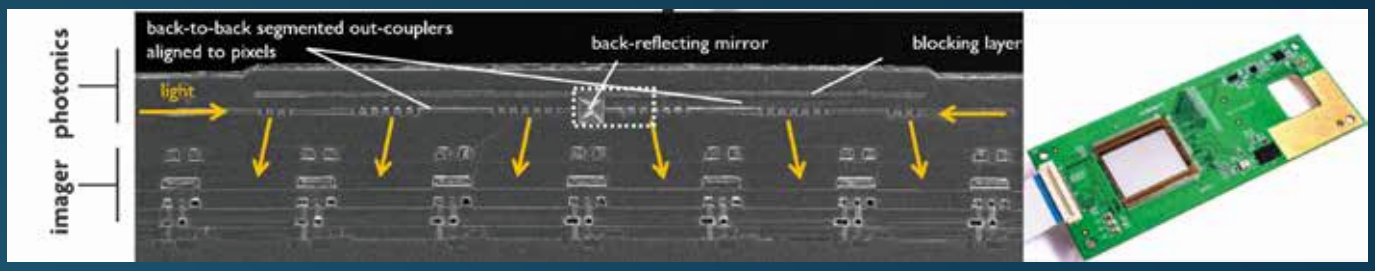
Project example

TRL

High-optical-throughput integrated spectrometer

Raman spectroscopy is a powerful technique, most often used to determine chemical material compositions, for example for quality control. These spectrometers are typically expensive tabletop tools.

Imec made an on-chip solution which is 1000 times smaller with a similar or even improved optical throughput. This patented concept uses **integrated photonics on top of CMOS imagers**. Rather than using classic dispersive optics, imec bases its technology on interference-based spectroscopy, which is used in well-known Fourier transform (FT) spectroscopy. The interferometers are implemented on-chip using integrated waveguide photonics. To match the optical throughput and to avoid moving parts, the waveguide interferometers are massively parallelized monolithically on top of a CMOS image sensor. In this way, both high optical throughput and high spectral resolution can be reached in a miniaturized device. The whole system is free of mechanical components and is built in imec's **PECVD SiN platform**, which guarantees robustness and compatibility with high-volume (low-cost) manufacturing.



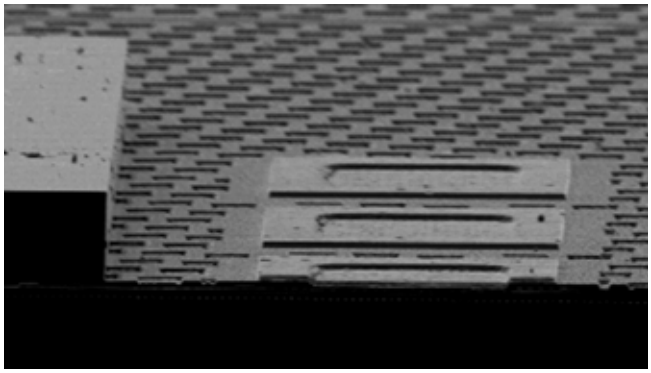
On-chip spectrometer, using PECVD SiN integrated photonics on top of CMOS imager.

2. Functional layers for imagers and LED displays

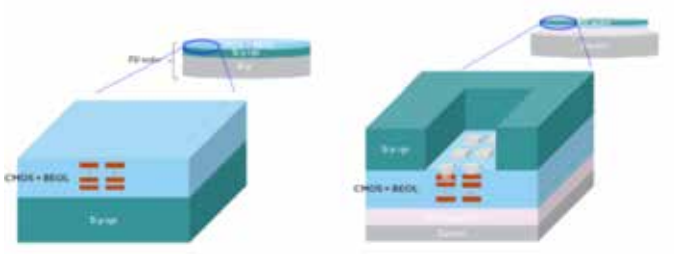
Various post-processed layers can be added on top of CMOS image sensors to **enhance the performance or enable specific functionalities**. Think of color filters, micro-lenses, or anti-reflective coatings. Here we discuss two innovative imager types that are enabled by specific post-processing.

Back-side illuminated imagers

Backside-illuminated imagers (BSI) receive the **light input on the backside** – the opposite side of where the electronics and metal connections are located. This is done by doing post-processing on the standard CMOS image sensor wafer: flipping the wafer upside down, thinning or grinding most of the silicon substrate, and processing of the backside contacts to the front. This results in **improved light sensitivity and reduced pixel crosstalk** because the light is not hampered by the metal and oxide layers of the frontside electronics. BSIs are typically used in applications that demand for **improved image quality and low-light performance** such as digital cameras, smartphones and other consumer electronics.



SEM detail of a thinned wafer. To make BSI imagers, a CMOS wafer with imagers is flipped, the back-side is thinned, openings are created with lithography and etching, and re-metallization is performed to enable e.g. wire bonding. In this detail you see at the right these re-metallization aluminum pads, surrounded by the dielectric area and at the left the thinned wafer.



Concept of front-side illuminated imager (left) and back-side illuminated imager (right).

Project example

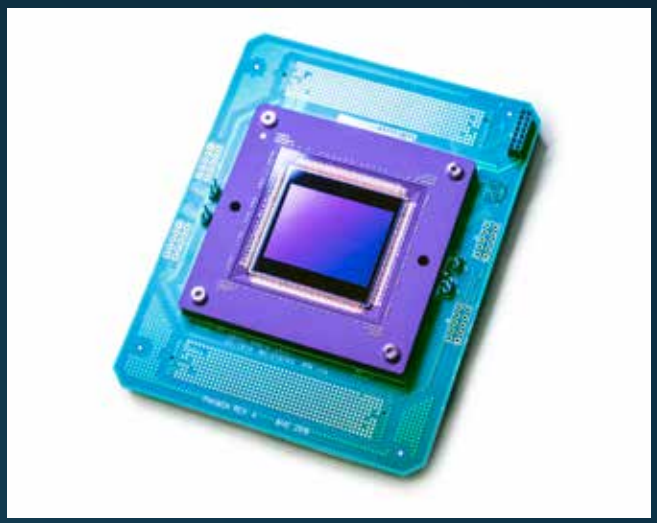
TRL

Backside-illuminated CMOS imager for light-sensitive ultra-high-speed camera

The E9•100S camera of Pharsighted is the world's most light-sensitive ultra-high-speed camera. It reaches 326,000 frames per second (full frame: 640x480 pixels) and up to 2,720,000 frames per second at lower frame size (640x32 pixels). The light sensitivity is ISO 160,000 (monochrome). This outstanding performance is primarily enabled by the backside-illuminated CMOS imager which is developed and manufactured by imec.

The challenge was to combine a large pixel area with high imaging speeds, supported by a massive output data rate. To tackle this, imec developed a BSI CMOS imager process that's dedicated to high-speed imaging, and dedicated pixel and readout circuits integrated on a single die to output digital image data at high speed.

Imec also serves Pharsighted by managing the sensor supply chain from silicon processing to delivery, including testing.



CMOS imager for light-sensitive ultra-high-speed camera.

Spectral imagers

Hyper- and multi-spectral image sensors are devices that can capture light – also beyond the visible range – at **very narrow and specific wavelengths**. These wavelength bands are narrower as compared to the red, green and blue wavelengths of standard image sensors. In this way, spectral imagers capture detailed spectral information on materials and objects out of which '**spectral signatures**' can be identified that translate into **material and object properties**. It is used in applications such as environmental monitoring, precision agriculture, medical diagnostics, surgical imaging and material analysis.

Project example

TRL

On-chip spectral filters enable compact spectral imagers

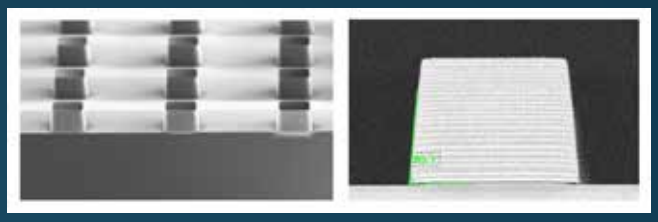
Imec has set up a unique process for fabricating spectral sensors that relies on the deposition of alternating thin layers in specific patterns, to create **optical interference filters on top of the pixels of standard CMOS image sensor wafers**. Imec offers two types of spectral sensors: snapshot and snapscan. Snapshot sensors use a Bayer-like mosaic pattern for **video-rate spectral imaging**, ideal for applications where the studied object is moving. Snapscan sensors entail a striped pattern for **high-resolution spectral imaging**, perfect for proof-of-concept studies or lab settings. More info: www.imechyperspectral.com

Imec develops a range of spectral sensors, each with specific capabilities. They are a clear demonstration of imec's post-processing capabilities to **accurately deposit and pattern thin layers on top of pixels**.

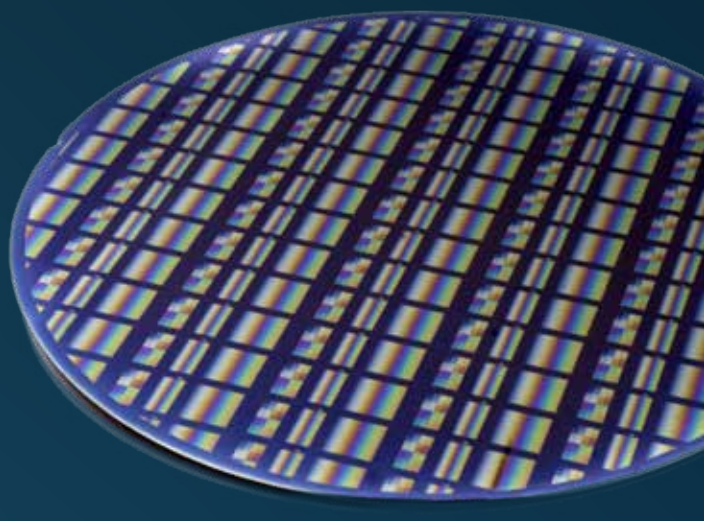
Imec can design and manufacture filters to capture:

- more than 100 narrow wavelength bands in the visible wavelength 450-800nm
- selective wavelengths in the visible and infrared range, according to the needs of the application

And combine this with traditional color filters and micro lenses to have visible and infrared capabilities on the same chip.



Imec's on-chip solution for spectral imagers is based on Bragg filters. At the left is a SEM of such Bragg filters with a detail of its layered structure at the right. It clearly shows how accurately and uniformly the material layers are deposited on the surface of an imager wafer.



The spectral filters are deposited and patterned at wafer-scale. They can be fabricated on a 200/300mm CMOS image sensor wafer directly or on a transparent substrate to be diced and assembled afterwards at chip scale.

Highlight

Unique deposition tool for spectral filters

Imec closely works with material and tool suppliers to have the best and newest options at hand in its 200mm and 300mm cleanroom, even alpha and beta tools that are not yet on the market. A nice example of tool co-development in the field of spectral imagers is the HELIOS 800 tool of Bühler. This company made coatings for all types of glass – solar, architectural, automotive – but was not yet active in the semiconductor industry. Thanks to an intense collaboration with imec, Bühler was able to make a CMOS-compatible tool to deposit thin layers accurately and uniformly across wafers. It is the work horse for imec's spectral image program.

Flat optics & metamaterials

Flat optics refers to the design and fabrication of optical components that are thin and planar, rather than bulky and three-dimensional like traditional lenses and mirrors. These components are typically composed of **metasurfaces**, which are two-dimensional **arrays of nanostructures** engineered to manipulate light in specific ways.

Metamaterials play a crucial role in flat optics because they enable precise control over the properties of light at the nanoscale. By patterning metamaterials into metasurfaces, it is possible to control the phase, amplitude, and polarization of light with high precision. This allows for the creation of **ultrathin optical elements** such as lenses, polarizers, beam deflectors, and waveplates.

One of the key advantages of flat optics is its ability to achieve functionalities that are difficult or impossible with conventional optics. For example, metasurface lenses can be designed to focus light with **subwavelength resolution**, enabling **compact imaging systems** and reducing the overall size and weight of optical devices. Additionally, metasurface-based components offer **flexibility in design**, allowing for the integration of multiple functions into a single device. for applications such as **display, holography, AR/VR and imaging**.

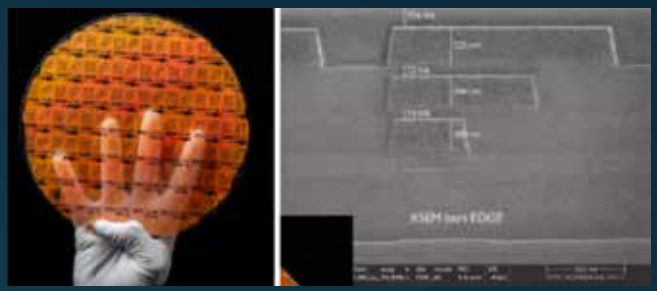
Project example

TRL

LiDAR with nanostructures

Imec can design and post-process metamaterials on top of e.g. standard CMOS or imagers, using advanced lithography to create structures at the subwavelength scale. It is crucial to choose the appropriate materials, typically these are metallic and dielectric materials arranged in specific patterns. The challenge is to work out a process that can rely on one lithography option to make all the vertical layers that make up the specific structure.

One specific project that showcases imec's capabilities in metamaterials is a LiDAR sensor in which the conventional optics was replaced by a nanostructured metamaterial. Pillars of 150nm in diameter and ≥550nm height were fabricated based on metal and amorphous silicon. Note that this example is processed on a glass substrate, not on CMOS.



Glass substrate with LiDAR sensors based on nanostructured metamaterials, and SEM of processing stack.

3. Precision fluidics

Microfluidics involves the **manipulation and control of small amounts of liquids, at the microscale**. Through miniaturized channels, chambers, valves and pumps, the fluid is directed along a defined pathway for a specific purpose. The microfluidic structures can be post-processed on top of CMOS or be integrated with photonics. Possible applications are chemical or biological analysis, diagnostic tests, lab-on-chip devices, environmental monitoring, etc. In short, **all applications that need a more automated and precisely controlled process flow**.

The design and fabrication of microfluidic components is **challenging** and has to deal with:

- finding a good fit between the microfluidic material and the fluids inside, so-called chemical compatibility
- the occurrence of air bubbles
- achieving precise and reliable fluid control, especially at low flow rates
- long-term stable integration of 'wet' fluidics with electronics
- lack of standardization

Another important challenge is the design of 'interposers' or intermediate components that facilitate the **transition of millimeter** fluidic volumes (typical for biological samples) **to micro- or even nanoliter** volumes (used in the microfluidic circuit).

Passive and active microfluidics

A microfluidic circuit can consist of various components: micro-channels, -pumps, -valves, -mixers, -reactors, -chambers, -filters, -heaters, -droplet generators etc. The simplest fluidic circuits are passive ones, without an active control of the fluid flow (e.g. using **capillary forces**). True active microfluidics use **pneumatic, mechanical, or electrical actuation** mechanisms to very precisely control the fluid flow. Such systems have a more complex design but are **highly dynamic – rapid fluid switching, precise dosing, real-time adjustments**.

Most of today's microfluidic systems are hybrid systems, using a passive microfluidic circuit on chip, driven by external pumps and valves.

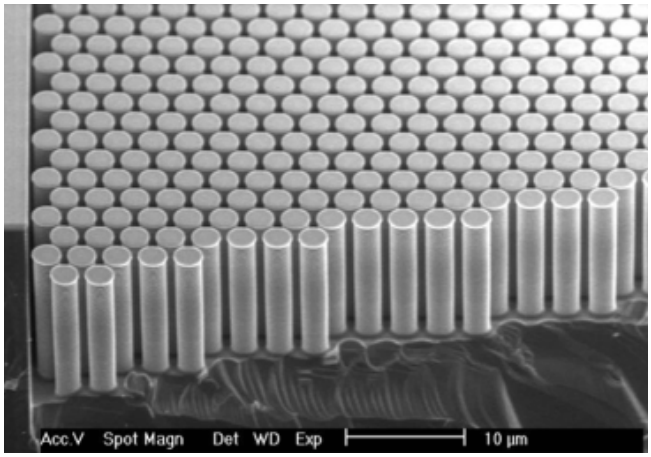
Silicon-based microfluidics

Microfluidic devices can be fabricated from various materials, including polymers, glass, and silicon. The simple passive circuits are mostly done in polymer because of its low-cost advantage. Glass and silicon are more costly but allow to make more detailed structures, with smaller dimensions.

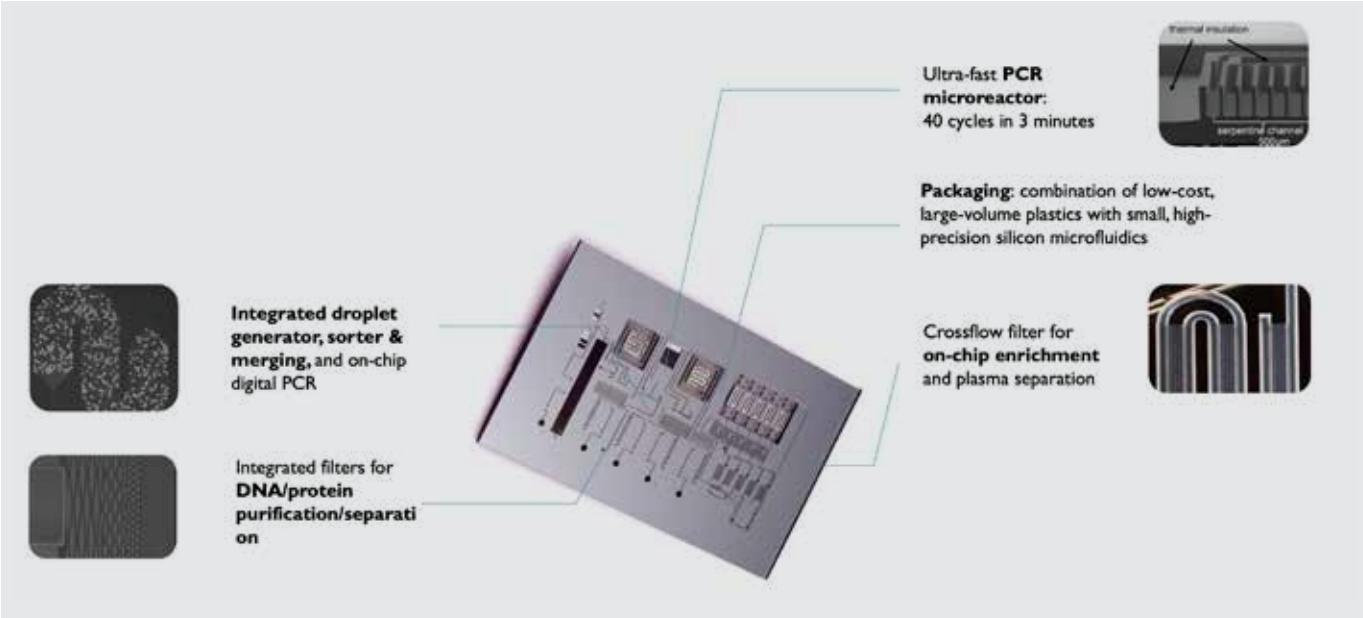
Glass is chosen for (optical) applications where transparency is needed. Silicon has the advantage that it can be patterned and processed with chip manufacturing processes, in a **very precise, accurate and reproducible way, also on a large scale**.

Silicon-based microfluidics is the best option:

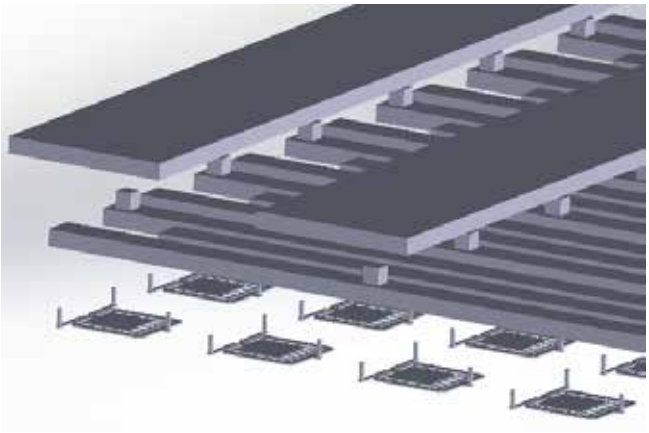
- for complex fluidic circuits
- for complex structures or structures with high aspect ratios such as pillars
- when integration of fluidics and electronics / electrodes is important
- when transfer to production phase is important



Silicon-based microfluidics is the best option for structures with high aspect ratio such as this array of highly ordered micropillars for superior separation resolution.



Examples of silicon-based microfluidic components developed by imec.



Example of complex microfluidics in which case a silicon-based platform is more advantageous: an array of miniaturized multilayered flow cells for faster reagent exchange and sensor delivery.

Surface functionalization

Surface functionalization is closely linked to microfluidics, enhancing the performance and functionality of microfluidic devices. It involves modifying the surfaces of microfluidic channels or components to achieve specific properties or interactions with fluids and biomolecules:

- **Controlled wettability**: using surface chemistry to create hydrophobic or hydrophilic regions, influencing the flow behavior of liquids within the channels.
- **Preventing biofouling**: using surface chemistry to prevent the unwanted adsorption of biological materials onto microfluidic surfaces. This is important for long-term stability and reliability of the structures.
- **Selective binding and capture**: functionalizing surfaces with specific ligands for selective binding and capture of target molecules.

Imec can develop and fabricate silicon-based microfluidic components, with focus on complex structures, active microfluidics and accurate process control.

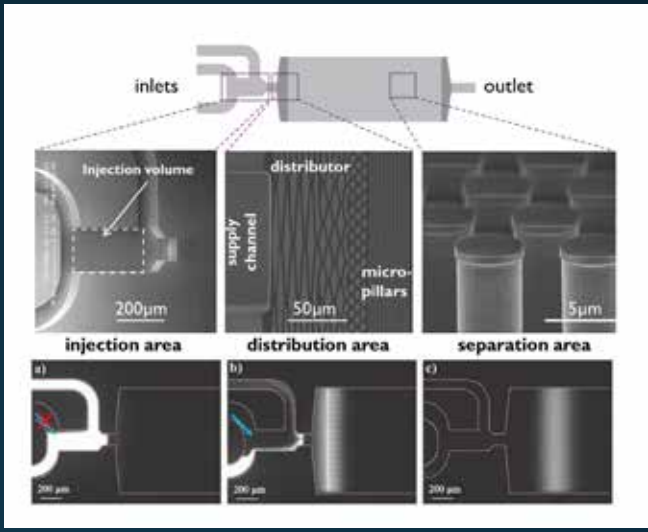
Project example

TRL

On-chip high-performance length-based DNA separation

Imec designed and fabricated silicon-based microfluidic structures for high-resolution length-based DNA separation. It uses silicon micropillar-array chips in the separation area. The challenge in this project was to combine both small – sub-micron to a few micron – and large – a few hundred micron – structures. The use of silicon-based microfluidics was key to make the high-aspect ratio fine pillar structures. Also, expert knowledge in surface chemistry was essential to make this on-chip.

In the first project, high temperatures were used which were not CMOS-compatible. In a next phase, a two-step etch was developed which made the process compatible with CMOS.



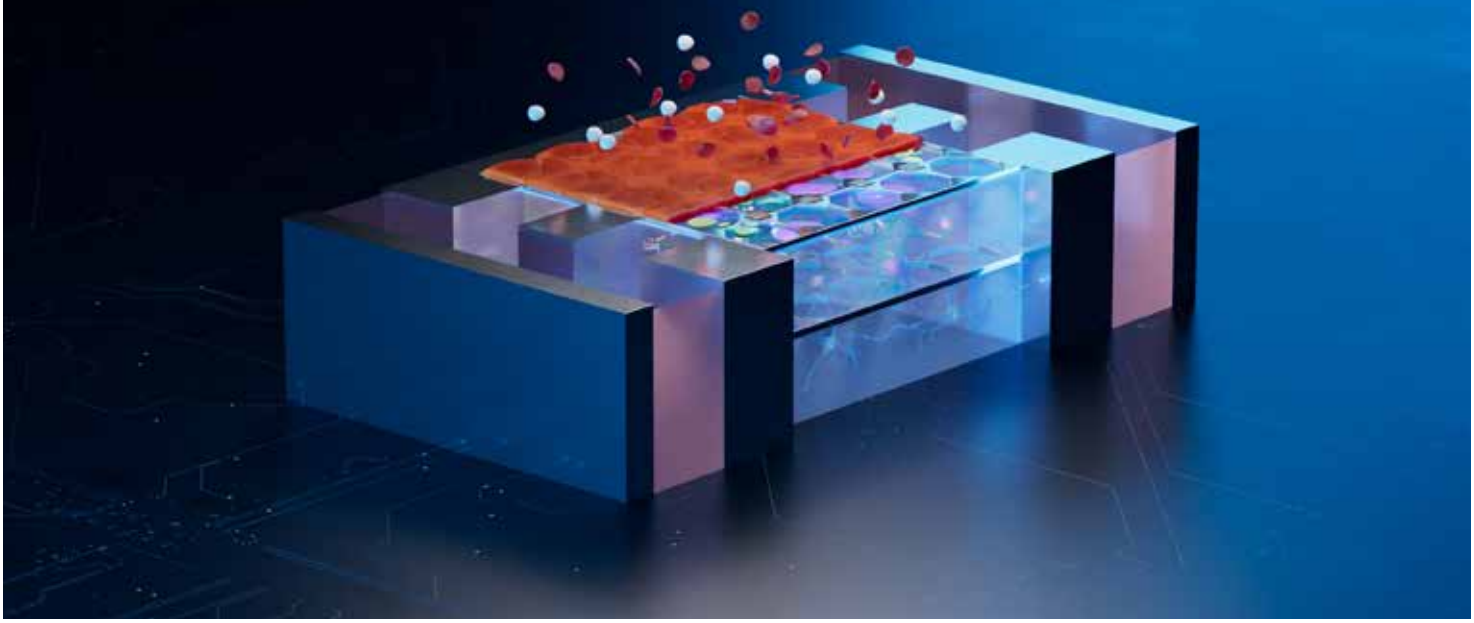
System concept and SEMs of microfluidic components of chip-based DNA separation.

Project example

TRL

Blood-brain-barrier chip

An example of advanced microfluidics and surface functionalization is the blood-brain-barrier on chip that imec is developing. It's a **model system** to better understand this complex biological structure that restricts delivery of many pharmaceuticals and therapeutic antibodies to the central nervous system. The microfluidics consists of three channels, separated from each other by pillars. The gel to cultivate the cells in is contained in the middle channel by special microfluidic engineering techniques.

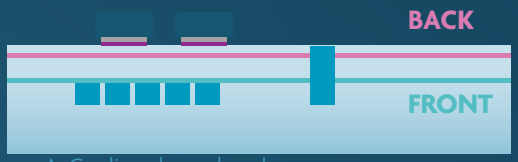


Project example

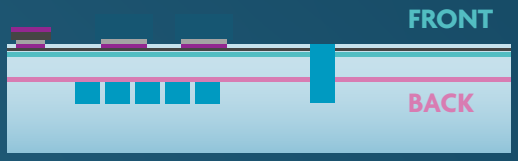
TRL

Chip with integrated cooling fluids

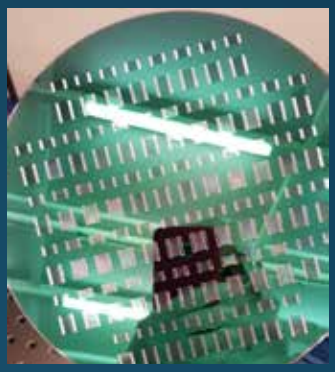
Microfluidics can be used also outside the life sciences domain. Imec developed a silicon-based microfluidics concept for active cooling of dies with co-integration of the dies and cooling liquid. Silicon is used in this case because it is a good conductor to guide the heat from the chip to the cooling liquid. The microfluidics is processed on top of a wafer, next a second wafer is put on top via wafer-to-wafer bonding to close the channels. After grinding of the top surface, the power amplifier dies are put on top.



A: Cooling channels only



B: Device compatible channels
Requires fusion bonding in presence of glue



Concept & picture of the front-side etched wafer with inlet and microfluidic channels.

Project example

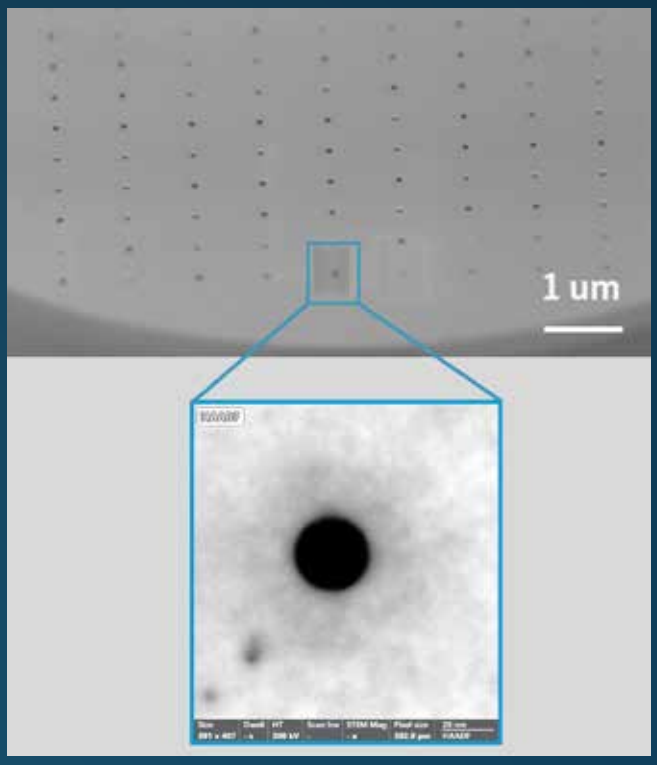
TRL

Nanopore chip for protein sequencing

Compact, high-throughput devices for protein sensing and sequencing are in demand as an alternative for the bulky mass spectrometers. Imec is developing a chip based on solid-state nanopores for the proteomics era.

To be able to make **stable and extremely small – below 20nm – nanopores**, imec relies upon its expertise in silicon-based micro/nanofluidics, surface functionalization and its 300mm cleanroom infrastructure. It's the feature size and the yield that make this a very challenging project. Imec engineers developed an in-line metrology tool to assess the yield.

More info: www.imec-int.com/en/expertise/health-technologies/solid-state-nanopores/digiome-realizing-promise-nanopore-protein



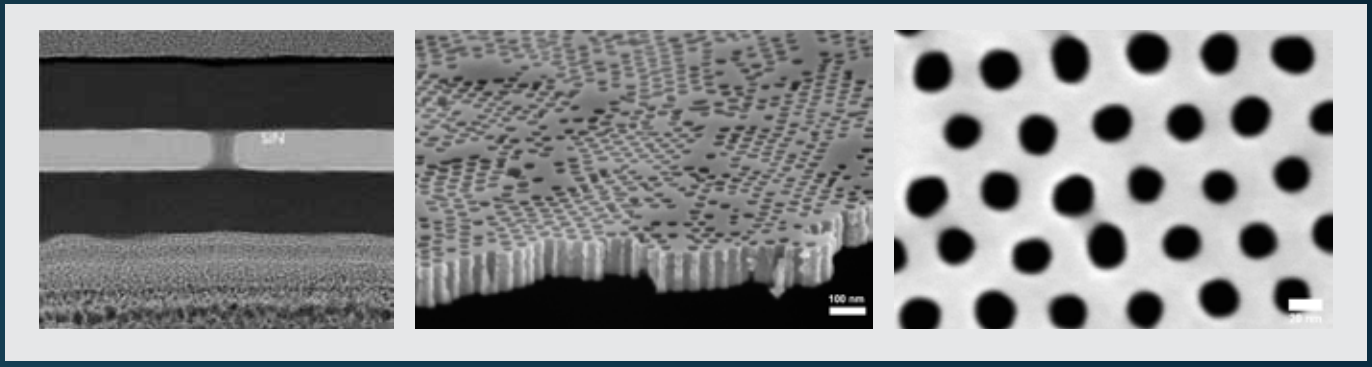
Solid-state nanopores.

Project example

TRL

Nanopore-based filtration chip

Nanopores can also be used to make a specialized filtration structure. Imec is developing such a structure in the framework of an **artificial kidney project** which envisions a bioartificial kidney with on-board sensors to detect in real time the onset of problems, and on-board actuators to perform corrective action, as well as wireless charging. One of the key components are high-selectivity filters which can efficiently filter and purify blood. These **nanoporous haemofilters** are fabricated with imec's state-of the art cleanroom fabrication technologies.



SEM image of 20nm silicon nanopore filter membrane (cross section, top view and detailed top view).

4. Novel materials

Non-silicon materials become more and more important for new applications because of their unique properties, beyond the capabilities of silicon. We will discuss three groups: transition metals, 2D materials and quantum dots.

Transition metals

Especially for structures such as **electrodes** – conductive structures that can be used for sensing or actuation – new materials such as transition metals are important. When electrodes are made with CMOS-compatible processes, it is possible to make **large and regular arrays** of electrode structures. This can be beneficial when a **high degree of parallelization** is wanted, for sensing and actuation. Also, working in a CMOS environment, the electrodes can be made at the micro and nanoscale, enabling the **sensing or steering of single cells**, growing on the electrodes.

There are different material platforms that can be used for electrode arrays: platinum, titanium nitride, ruthenium, aluminum, or a combination of these materials in an advanced electrode stack. The choice of materials depends on the type of fluid, tissue, or cells it will be used with.

Some examples of materials with their unique properties:

- **Ru (Ruthenium)**: chemical stability, corrosion resistance, and catalytic activity.
- **Pt (Platinum)**: high conductivity, corrosion resistance, and catalytic activity.
- **TiN (Titanium Nitride)**: high thermal stability, and corrosion resistance.
- **ITO (Indium Tin Oxide)**: high electrical conductivity, and optical transparency.

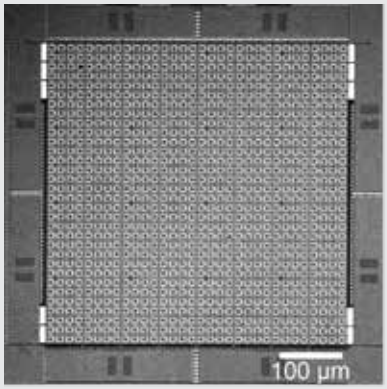
Micro-electrode arrays are often used in combination with **well structures**. It's in these cavities, for example, that the biological or chemical reaction can take place. Electrodes can be made solely on the bottom of these wells, or they can be used in combination with electrodes at different levels in the well (**multilevel electrodes**). These then typically work as anode and cathode.

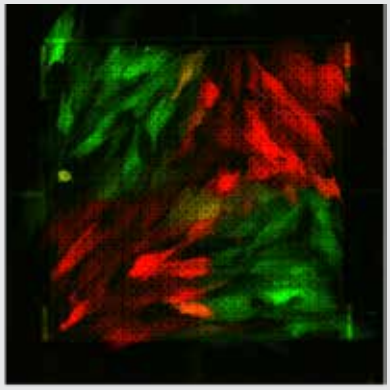
Applications range from DNA synthesis to spatial transcriptomics.

Advanced lithography capabilities for electrode arrays

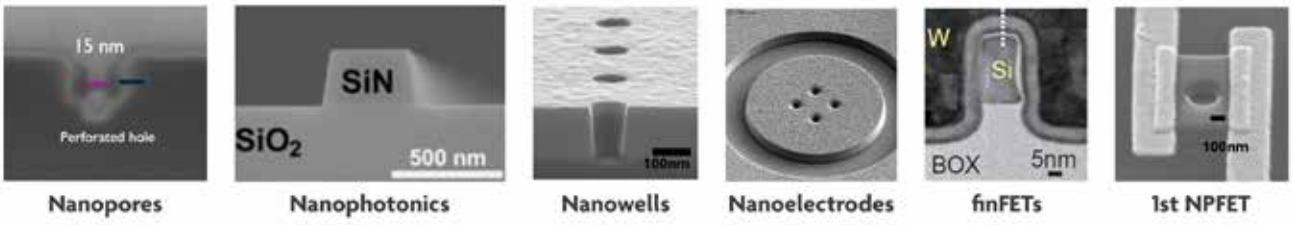
The challenge when making an electrode array on top of a CMOS chip is to make the pixel size, also defined as the pitch of the electrode array, as small as possible. For example, for DNA synthesis applications this is very relevant since every pixel is a unique site on top of which a DNA strand can be synthesized. The more pixels, the more throughput.

Thanks to imec's advanced lithography capabilities (193nm immersion and EUV lithography) the electrode pixel size can be made even smaller, which is as small as the footprint of the logic (transistors and capacitors) on the CMOS chip that is needed to control one pixel.





Close-up of imec's microelectrode array showing a cluster of 1,024 circular, individually addressable electrodes. It is used for high-efficiency, spatially-resolved transfection of human fibroblasts (fluorescence microscopy image of a cells transfected with EFGP- (green) or mCherry- (red) encoding mRNA).



Examples of nanostructures that clearly demonstrate imec's capabilities to make miniature structures.

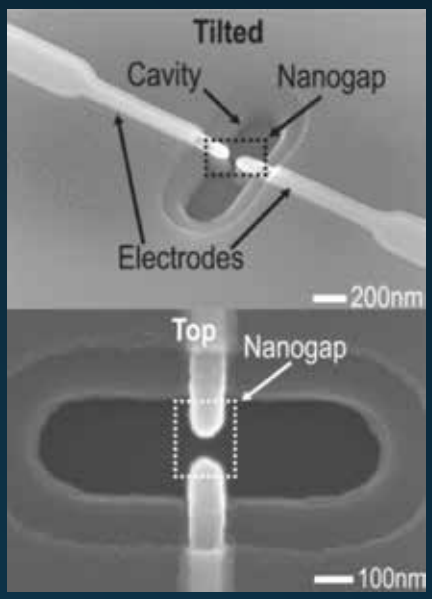
Project example

TRL

Nano-gap ruthenium electrodes for single-molecule biosensing

In this project, a molecular electronics CMOS chip was realized, using single molecules as sensor elements. The sensing element is a 25nm molecular (peptide) wire connected to metal nanoelectrodes which feed into a current monitoring circuit. The peptide contains sites for attachment of various probe molecules (e.g. DNA, proteins, enzymes, antibodies). The current through the molecular wire is monitored and provides direct, real-time observation of the single-molecule interaction kinetics.

The challenge was to make the gap between the electrodes extremely small – to fit in the molecular wire – and to make them electrochemically stable in ionic solutions. After a detailed material compatibility study, ruthenium was chosen due to foundry compatibility, robustness, and electrochemical performance. Using conventional photolithography, 50nm wide electrodes with less than 20nm gaps were realized. The post-processing techniques that were developed allow to fabricate nanoelectrodes in a scalable way, e.g. to create assays with high levels of multiplexing, rapid response on the scale of seconds and a limit of detection down to a single molecule.



SEM images of the nano-gap electrodes for single-molecule bio-sensing REFERENCE

Project example

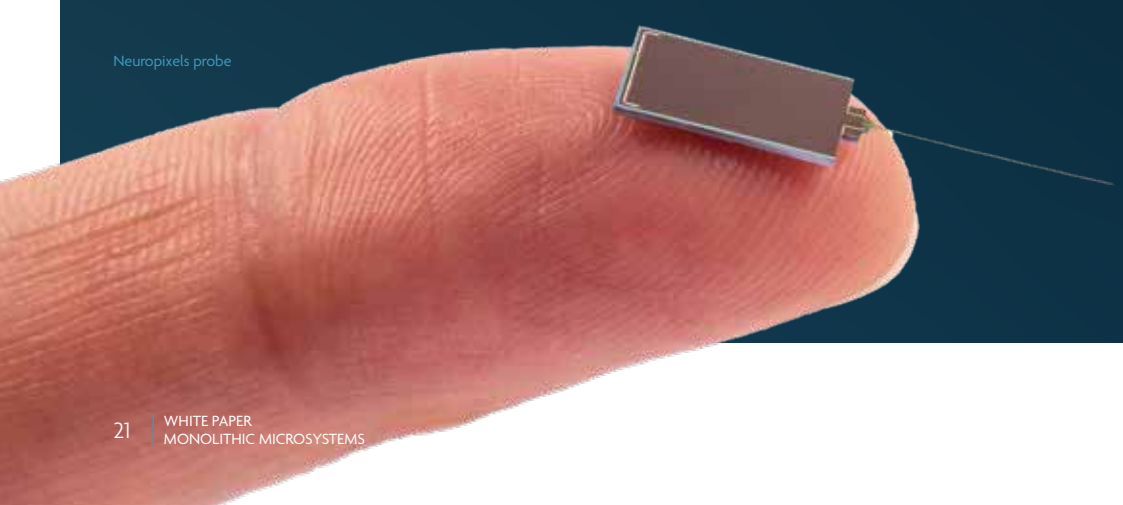
TRL

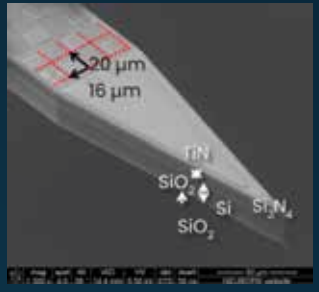
Neuropixels, ultra-high-resolution implants for functional whole-brain activity mapping

Imec has a strong expertise in making micro- and nanoelectrode arrays, in different materials and with the option of multilevel electrodes. For example, electrodes are used for the development of *Neuropixels* probes. These are advanced neural recording devices developed in collaboration with the Howard Hughes Medical Institute (HHMI), the Allen Institute for Brain Science, and University College London (UCL).

The neural probes use an array of small porous TiN electrodes which are on a long needle-like structure and are seamlessly integrated with CMOS for actuation and sensing of neuron action potential and some local data processing. The Neuropixels 2.0 probe for example has more than 5000 sites. The fabrication of the very narrow silicon shank or needle is very challenging. For example, dimensions of 17 µm-thick, 70 µm-wide and 1cm-long shanks are realized. More info: www.neuropixels.org

Neuropixels probe

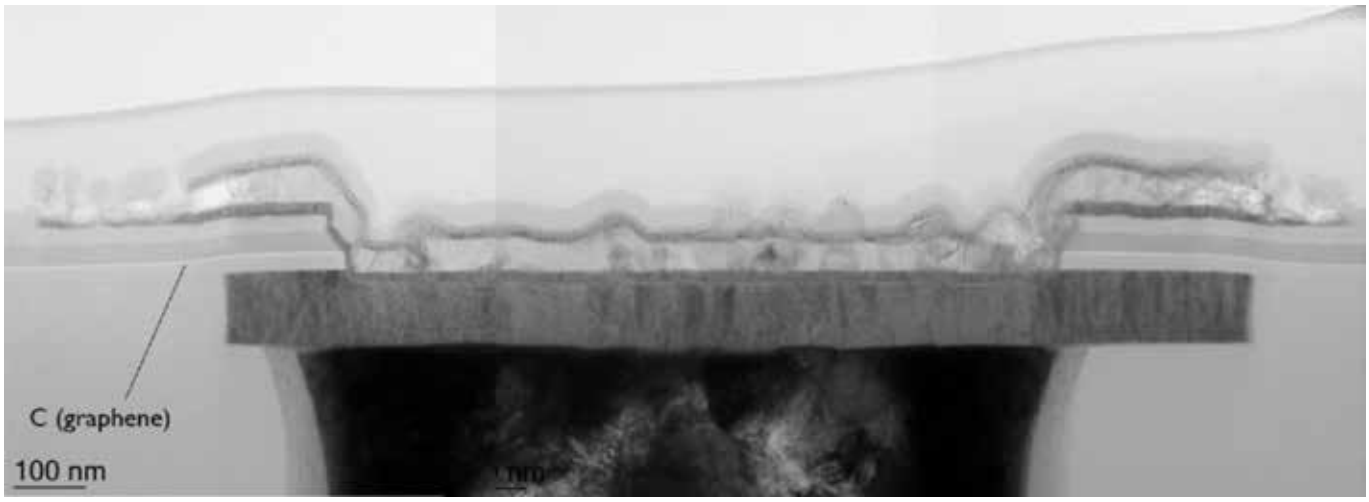




Graphene: integration of 2D materials on sensor chips

2D materials (e.g. graphene) are a class of materials that are extremely thin, typically consisting of a single layer or a few layers of atoms arranged in a two-dimensional structure. 2D materials have unique properties such as high mobility and sensitivity that can drastically enhance sensor performance, e.g. quantum-dot infrared sensors.

Imec works with the dedicated graphene foundry *Graphenea Semiconductor SLU* for the supply of graphene wafers. Imec has set up a CMOS-compatible integration flow to combine graphene layers in a stable way onto CMOS.



TEM image of a graphene layer contacted through an aluminum later and tungsten plug (black) with on top a planarized TiN plate for contacting to underlying CMOS. As there is no physical or chemical adhesion to the substrate, the graphene layer is anchored using dielectric encapsulation layers on top with proprietary imec process.

Quantum dots

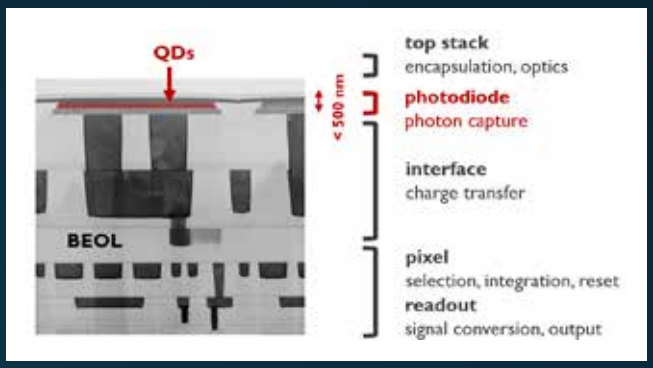
Quantum dots are semiconductor nanocrystals with unique optical and electronic properties that arise from quantum confinement effects. Depending on their size, quantum dots can exhibit different optical properties, for example resulting in tunability of the absorption spectrum and cut-off wavelength. QDs are already used in display applications, where they enable screens with excellent color control. Nowadays, a lot of interest goes into image sensors where the QD photodiode allows sensitivity beyond the band edge of silicon, yielding high resolution and high pixel density imagers, for example, for short-wave infrared (SWIR) wavelength range.

Project example

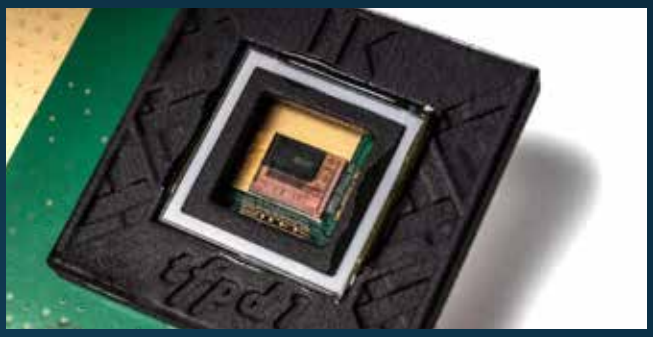
TRL

Monolithically integrated quantum-dot based SWIR image sensor

Imec is developing photodetector stacks based on novel thin-film absorbers, such as organic, perovskites and quantum dots (QD). QDs are especially interesting for wavelengths not accessible by silicon (above 1100 nm). Monolithic integration directly on the readout circuit makes it possible to scale up the resolution (for multi-megapixel arrays) and scale down the pixel pitch (for diffraction-limited imaging). Imec is also working on fab-friendly process flows to enable wafer-level fabrication that is an opener for mass production. With that, SWIR imaging can be envisioned for high-volume applications such as consumer and automotive. Additionally, the QD platform allows for a high level of customization, which is interesting for lower volume applications such as industrial machine vision, space and remote sensing.



Imec also demonstrated successful incorporation of a pinned photodiode (PPD) structure in the readout circuit of thin-film-based image sensors. It's the first of its kind, showing the path towards imagers using thin-film absorbers with low noise. In the first demonstration, an organic photodetector was monolithically hybridized with an indium-gallium-zinc oxide (IGZO)-based thin-film transistor into a PPD pixel. This array was subsequently processed on a CMOS readout circuit to form a superior thin-film NIR image sensor. Combining imec's expertise in IGZO TFTs in the back-end of line (BEOL) with know-how of TFPD stacks and image sensor integration, resulted in this first-of-a-kind proof of concept imager.



Imec's pinned photodiode structure integrated in thin-film image sensors

Techniques for 3D integration of chip functionalities

Although the focus of this white paper is post-processing of functionalities on top of CMOS, there are situations in which 'standard' post processing or monolithic 3D integration is not possible. For example, in case of temperature restrictions, different available wafer sizes or mechanical stress. Here is an overview of the most commonly used 3D integration techniques. It really depends on the specific application, how to translate the specifications into a post-processing stack, or to turn to other specialized methodologies to make the 3D integration work.

Through-silicon via technology

TSV technology involves etching vertical channels (vias) through the silicon substrate of CMOS wafers and filling them with conductive material (typically copper) to create vertical electrical connections between different layers of integrated circuitry. TSVs enable high-density interconnects, reduce signal propagation delays, and allow for efficient heat dissipation. It's used to connect multiple chips or wafers, in a very compact way.

Wafer-to-wafer bonding

Wafer-to-wafer bonding techniques facilitate the stacking of multiple CMOS wafers to create 3D integrated structures. After post-processing steps on individual wafers, such as TSV fabrication, metallization, and insulation, the wafers are aligned and bonded together. Wafer bonding methods include direct bonding, adhesive bonding, and hybrid bonding, depending on the materials and surface properties involved.

Die-to-wafer bonding

Die-to-wafer bonding is a technique used to integrate individual semiconductor dies onto a larger wafer substrate. The semiconductor dies are aligned and bonded onto the wafer substrate using a bonding technique such as adhesive bonding, solder bonding, or thermo-compression bonding. Alignment is critical to ensure proper electrical and mechanical connections between the dies and the wafer.

Layer transfer

Layer transfer techniques enable the transfer of processed device layers from one substrate to another, allowing for heterogeneous integration of materials and functionalities. Post-processing steps involve bonding, thinning, and separation of the transferred layers. Layer transfer methods include wafer bonding with subsequent thinning, ion-cut techniques, and laser-induced lift-off.

Conclusion

In this white paper, we have explored **the potential of post-processing functionalities on top of foundry-fabricated CMOS wafers** to enhance chip-based applications. Imec offers a comprehensive range of capabilities in this domain, spanning **from design to low-volume manufacturing**, leveraging our **state-of-the-art infrastructure and broad expertise**.

Throughout the paper, we have presented **numerous project examples showcasing imec's capabilities in post-processing**, illustrating our ability to seamlessly integrate diverse functionalities onto a single chip. Our lithography capabilities, including **advanced processing techniques like EUV lithography**, enable us to achieve **extremely small pixel sizes** for applications such as DNA synthesis, ensuring high throughput and efficiency.

Furthermore, imec's cleanroom facilities, both for **200mm and 300mm wafers**, provide a **flexible environment for heterogeneous integration** of components, from CMOS and photonics to fluidics and other functional layers. Our expertise in monolithic microsystems offers unique advantages, enabling the seamless integration of diverse functionalities into compact, efficient systems.

In conclusion, imec serves as **a valuable partner** for those involved in the development of innovative chip-based applications, offering cutting-edge technology, extensive expertise, and a collaborative approach to bring ideas from concept to realization. We invite you to explore further and discover how imec can help unlock the full potential of your chip-based innovations.

This white paper was written in collaboration with:

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