DIRECT WRITE ELECTRON BEAM LITHOGRAPHY: A HISTORICAL OVERVIEW

Hans C Pfeiffer
HCP Consulting, Monterey, CA 93940

ABSTRACT

Maskless pattern generation capability in combination with practically limitless resolution made probe-forming electron beam systems attractive tools in the semiconductor fabrication process. However, serial exposure of pattern elements with a scanning beam is a slow process and throughput presented a key challenge in electron beam lithography from the beginning. To meet this challenge imaging concepts with increasing exposure efficiency have been developed projecting ever larger number of pixels in parallel.

This evolution started in the 1960s with the SEM-type ***Gaussian beam*** systems writing one pixel at a time directly on wafers. During the 1970s IBM pioneered the concept of ***shaped beams*** containing multiple pixels which led to higher throughput and an early success of e-beam direct write (EBDW) in large scale manufacturing of semiconductor chips. EBDW in a mix-and match approach with optical lithography provided unique flexibility in part number management and cycle time reduction and proved extremely cost effective in IBM's Quick-Turn-Around-Time (QTAT) facilities. But shaped beams did not keep pace with Moore's law because of limitations imposed by the physics of charged particles: Coulomb interactions between beam electrons cause image blur and consequently limit beam current and throughput. A new technology approach was needed.

Physically separating beam electrons into multiple beamlets to reduce Coulomb interaction led to the development of ***massively parallel*** projection of pixels. Electron projection lithography (***EPL***) - a mask based imaging technique emulating optical steppers - was pursued during the 1990s by Bell Labs with SCALPEL and by IBM with PREVAIL in partnership with Nikon. In 2003 Nikon shipped the first NCR-EB1A e-beam stepper based on the PREVAIL technology to Selete. It exposed pattern segments containing 10 million pixels in single shot and represented the first successful demonstration of massively parallel pixel projection. However the window of opportunity for EPL had closed with the quick implementation of immersion lithography and the interest of the industry has since shifted back to ***maskless*** lithography (***ML2***).

This historical overview of EBDW will highlight opportunities and limitation of the technology with particular focus on technical challenges facing the current ML2 development efforts in Europe and the US. A brief status report and risk assessment of the ML2 approaches will be provided.

Keywords: Electron beam lithography, throughput, shaped beams, massively parallel pixel exposure, Coulomb interaction, multi-beams, maskless lithography.

1. INTRODUCTION

The beginning of electron beam lithography coincided closely with the invention of the integrated circuit by Cilby and Noyce [1]. In 1960 Möllenstedt and Speidel from the University of Tübingen in Germany, published results obtained with an electron optical microrecorder writing 'fine lines' and 0.5um size characters with a 20nm electron beam in a 100nm thick collodium film [2]. This work 50 years ago started the successful evolution of direct write electron beam lithography in support of the unparalleled miniaturization trend in the semiconductor industry.

1965 Gordon Moore [3] published his observation with a semi-logarithmic plot showing the number of components per chip doubling every 18 month. He boldly extrapolated the chart into the future and it since has become Moore's Law still governing the density increases of microprocessors and other semiconductor devices more than four decades later. The

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explosive growth in the performance of semiconductor devices has been largely made possible by the advances in lithography. Progressive miniaturization enabled both the number of transistors on a chip and the speed of the transistors to be increased while the production cost per transistor decreased by many orders of magnitude over this period. Electron beam lithography has plaid an important role in this development of the semiconductor industry and has been used at the leading edge of micro- and nano-fabrication. Starting in the 1960s modified SEM's with pattern generation capability have been used to fabricate exploratory devices of micron and sub-micron dimensions [4] exploiting the superior resolution capability of electron beams exposing one pixel at a time. However, the first large scale manufacturing application of e-beam exposure systems did not make use of high resolution; instead it exploited the pattern generation capability. With the advent of Very Large Scale Integration (VLSI) in the late 1970s, probe-forming Gaussian e-beam systems began to replace the slow opto-mechanical pattern generators and became the technology of choice in mask houses of the semiconductor industry [5].

In the early 1970s IBM decided to use electron beam direct write lithography in their bi-polar fab lines and developed systems with the more efficient exposure technique of shaped beams [6]. During this time shaped beam techniques and systems were also independently invented and developed by Carl Zeiss Jena behind the 'iron curtain' in former East Germany [7].

Figure 1 illustrates the evolution of electron beam exposure techniques highlighting the improvement in exposure efficiency as measured in pixels/shot as a function of time. The first step toward parallel pixel exposure was a series of shaped beams. The fixed shaped beam projected 25 pixels in parallel and was the technique employed in IBM's EL-1 systems [8]. Variable shaped beams projecting on average several hundred pixels per shot were implemented in IBM's next tool generations El-2 and EL-3 [9]. By 1978 IBM had also built a first character projection system with up to 1000 parallel pixels in support of a bubble memory program which was using patterns of non-orthogonal features [10].

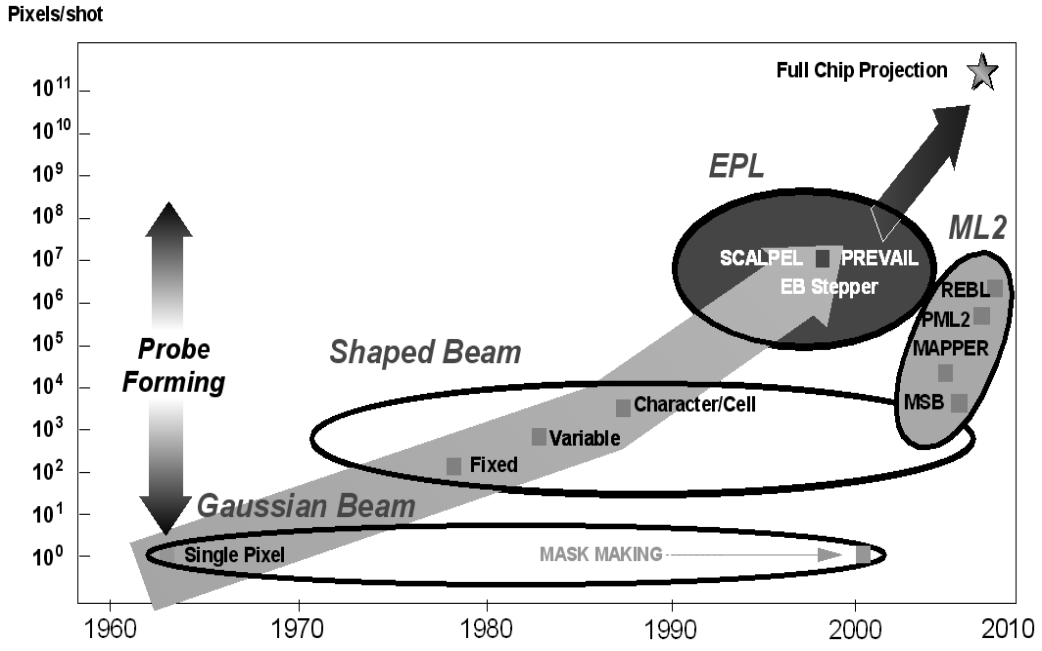


Fig.1. Electron Beam Lithography Evolution

Shaped beams were quickly adopted by the semiconductor industry and to this day are used for both mask writing and direct write on wafers. However their exposure efficiency has not kept pace with Moore's Law and by the early 1990s it was obvious that a quantum leap in parallelism was needed to meet the industry's requirements. This led to the development of *massively parallel* imaging techniques: First to electron-beam projection lithography or EPL which has demonstrated projecting up to 10 million pixels in a single shot [11] and more recently to ML2, a maskless lithography based on massively parallel pixel projection which is currently pursued by teams in Europe [12, 13, 14] and the US [15].

2. EARLY SUCCESSES OF ELECTRON BEAM LITHOGRAPHY

During the 1970s, IBM led the industry in the development and application of high throughput e-beam direct write systems [16]. The IBM EL-1 system had achieved a record throughput of 22 57mm diameter wafers per hour (wph) in the quick turnaround-time (QTAT) manufacturing facility of the IBM Microelectronic Division in East Fishkill, NY. By the 1980s, IBM had installed 30 additional EL-3 variable shaped beam systems worldwide in its semiconductor fabrication facilities. Figure 2 shows installations of several EL-3 systems in the highly automated QTAT line [17] which operated 24/7. Wafers arrived from other processing stations on air tracks and were individually moved in and out of the vacuum under computer control. Pattern information was routed from large buffers and cued to write up to 32 different chips on a single wafer. The primary incentive for this direct write strategy was management of a large number of bipolar logic chip designs through an optical and e-beam mix and match lithography approach. All chip components (transistors, resistors, capacitors) were fabricated on a 'master-slice' wafer using optical lithography. Only the personality defining metallization layers were exposed by e-beam direct write. Master-slice wafers and thousands of chip designs were resident in QTAT for quick response to chip orders from IBM's large system manufacturing sites.

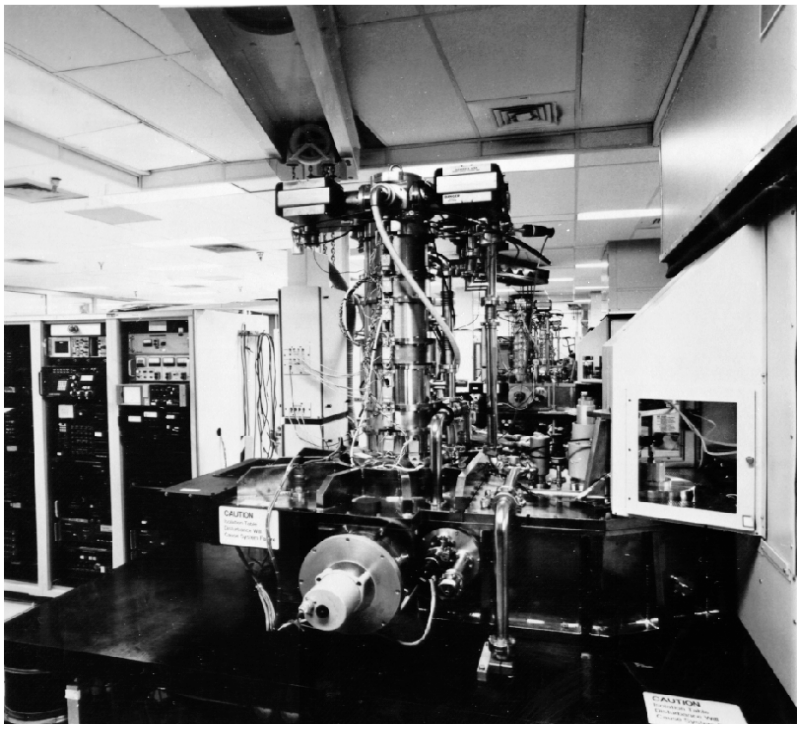


Fig. 2. EL-3 e-beam systems in IBM's QTAT facility (1980s)

E-beam direct write provided IBM with the capability to significantly reduce cycle time during system development by quickly providing the many hundreds of different chips needed for a single mainframe. Mixing different part-numbers on a single wafer drastically cut cost through improved yield and serviceability of orders. During this period the maskless lithography approach of e-beam direct write proved to be very cost effective and extremely valuable in managing logistics of IBM's semiconductor manufacturing lines. QTAT became the showcase of EBDW for the industry.

The shift from bipolar to CMOS-based chip designs at IBM in the early 1990s reduced the required part numbers by several orders of magnitude and made the use of e-beam direct write unnecessary and impractical. This brought to an end the first and only large-scale industrial application of e-beam lithography for direct wafer exposure which had exploited the maskless pattern-generation capability rather than the superior resolution in SC manufacturing. The experience of this era and the incentives for this approach still are valid today: Reducing the use of time consuming and very expensive masks, speeding up the cycle time and providing quick turnaround during development, early prototyping ultimately reducing cost and the time to product introduction.

3. THROUGHPUT CHALLENGES IN ELECTRON BEAM LITHOGRAPHY

Figure 3 illustrates another reason why e-beam direct write was discontinued and why maskless lithography faces a serious throughput challenge again. The chart shows the EL-tool throughput trend in wph and in pixels per second. As previously mentioned, the first EL-1 tool generation had a throughput of 22 wph in 1975. By 1995, after two decades and significant innovation and investment the throughput of EL-4 had declined to 1 wph. The pixel rate of exposure had increased from $2x10^7$ to $2x10^9$ resulting in a two order of magnitude improvement in writing speed. However, the minimum feature size went from 2um to o.25um and the wafer size went from 57mm to 200mm increasing the number

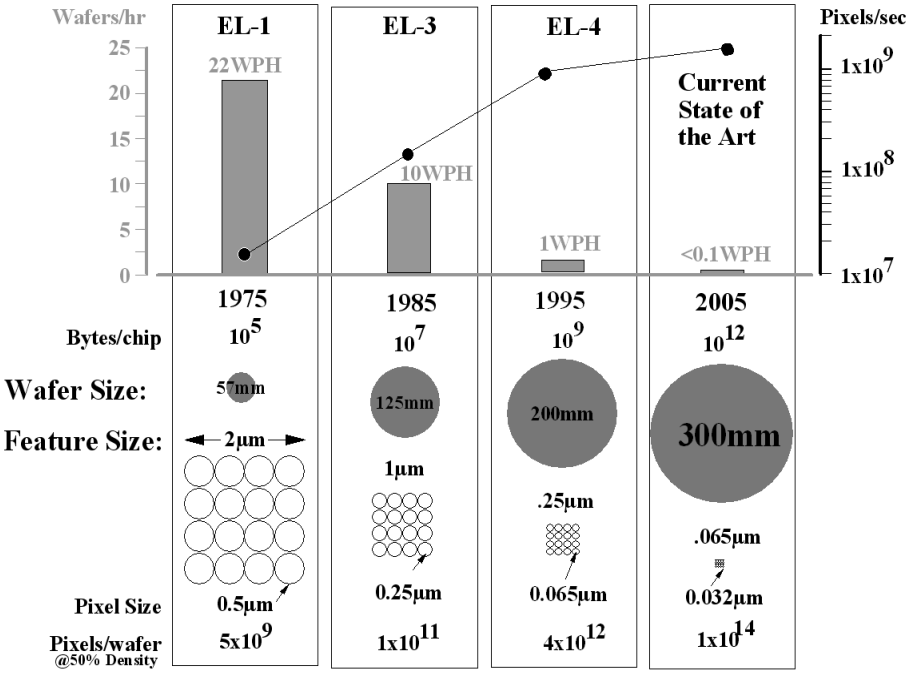


Fig. 3. Throughput trend in wafers per hour and in pixels per second with feature and wafer size trends

of pixels to be exposed by 3 orders of magnitude. E-beam direct write technology clearly had not kept pace with the pixel growth in the semiconductor industry. This trend is continuing today, more than a decade later, the fastest commercially available e-beam direct write tools require many tens of hours for the exposure of a single 300mm wafer. The fact that some semiconductor companies still use e-beam direct write tools [18] under these conditions indicates a very strong demand for maskless lithography. The superior resolution capability of e-beam systems is an additional feature that is exploited during prototyping. However, for e-beam lithography to become a viable alternative to optical lithography in manufacturing of future IC nodes a very significant increase in exposure efficiency was needed.

4. ELECTRON PROJECTION LITHOGRAPHY (EPL)

During the early 1990s Bell Laboratories invented and pioneered SCALPEL [19] - a technique which eliminated mask related problems encountered with earlier electron projection lithography systems [20,21]. The EPL e-beam stepper approach which has been pursued by Nikon [22] in cooperation with IBM [23] was based on the imaging concept of PREVAIL - **P**rojection **R**eduction **E**xposure with **V**ariable **A**xis **I**mmersion **L**enses. It is combining the advantages of a scanning e-beam probe forming system with the exposure efficiency of massively parallel pixel projection. Probe-forming electron beam systems provide the opportunity to dynamically correct for off-axis aberrations while scanning the beam. The VAIL technique exploits this opportunity by shifting the electron optical axis electronically together with the deflected beam so that the beam remains *on-axis* throughout the entire deflection range - effectively eliminating all off-axis aberrations [24]. The PREVAIL e-beam stepper used a 4x membrane stencil mask as reticle containing an entire

chip pattern. The electron beam illuminated 1x1mm^2 subfields in the reticle which were selected electronically by a +/- 10mm beam deflection. The subfield were imaged in 1/4 demagnification onto the wafer where they formed a 5 mm effective imaging field containing 20 stitched subfields. The effective imaging field or 'paint brush' is scanned mechanically in the orthogonal direction in a serpentine pattern stitching together subfields to expose one chip and ultimately the entire wafer sequentially.

In 2003 Nikon shipped the first NCR-EB1A e-beam stepper tool to Selete where its performance was thoroughly tested and improved until 2006 [25]. It met all its key specifications regarding placement accuracy, distortion control, stitching and overlay specifications in a mix and match exposure strategy with optical steppers. The exposure results demonstrated a resolution of 10^7 pixel elements in each subfield. The window of opportunity had been defined as the resolution gap between early 193 DUV steppers perceived to be limited to >70nm and the later EUV tools with resolution of < 22nm. The quick and successful development and implementation of 193 immersion lithography in combination with double exposure etc. had closed this window for EPL. The joint efforts at IBM, where the electron optics technology was developed, and at Nikon, where the precision, high speed and vacuum compatible air bearing stages were developed together with overall systems integration had succeeded in producing a remarkable electron optical lithography capability - but it proved unnecessary and consequently was not adapted by the semiconductor industry. The interest in the meantime has returned to maskless lithography.

5. MASKLESS LITHOGRAPHY (ML2)

Figure 4 shows a parameter matrix of the key ML2 projects currently pursued in Europe and the US. The common technical approach is based on parallel beams to achieve higher throughput. The ultimate goal is *massively parallel*

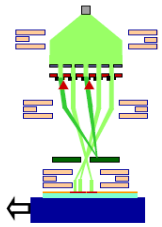
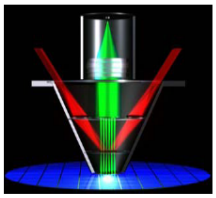
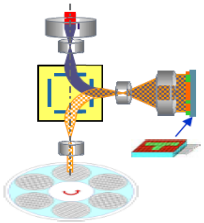
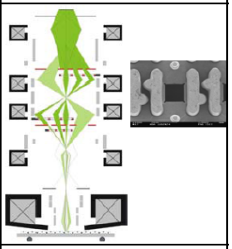
IMS Nanofabrication	MAPPER Lithography	KLA-Tencor	Vistec Electron Beam
PML2	MAPPER	REBL	MSB
			
Massive parallel			Multi VSB
50kV	5kV	50kV	50kV
Point beam/Gray scale			VSB / CP
~10M beams	13k beams	Reflective (REBL) >1M pixels	64 shaped beams for mask writing
5wph [≤22nm hp] (50wph by 10 tools)	10wph [≤22nm hp] (100wph by 10 tools)	40wph (Via), 2wph (Metal) [45nm node]	~4wph [≤22nm node] (1024 beams)
2012	2011	2013	2012
EU FP7 MAGIC project		DARPA/KLA-Tencor	TBD in November '09

Fig. 4. ML2 projects in Europe, US and Japan based on massively parallel beams [26]

projection of pixels. The separation of beam electrons into individual beamlets significantly reduces Coulomb interactions between them and allows for much higher total beam current without additional beam blur. The total beam current projected onto the wafer represents the most important figure of merit for exposure speed and systems throughput. The number of parallel beams quoted in Fig. 4 ranges from 64 shaped beams with about 6400 pixels to millions of beamlets. The projected throughput figures for a single tool are between 4 and 40 wafers per hour. However, all these projects are currently in early phases of development and levels of demonstrated performance with proof of concept (POC) systems are orders of magnitude below the stated throughput goals. To realize these goals and establish credibility for the various approaches significant investments and very significant technological progress will be

required. Encouraging progress has been demonstrated in fabricating the various forms of programmable aperture arrays using MEMS technology in combination with integrated CMOS. A key challenge remaining is the demonstration of reduced Coulomb interaction between beam electrons at the high total beam current which ultimately has to be delivered to the wafer in support of the high throughput goals. Separating electrons into beamlets reduces interaction blur but collective crossovers formed in most systems still will limit throughput. Top priority should be given to efforts demonstrating high total beam current at the required resolution.

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