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To cite this article: Shaoying Ke *et al* 2020 *J. Phys. D: Appl. Phys.* **53** 323001

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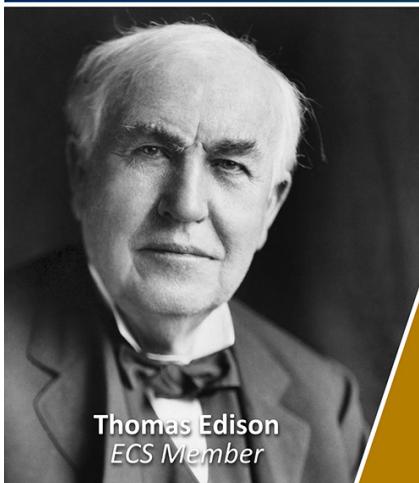
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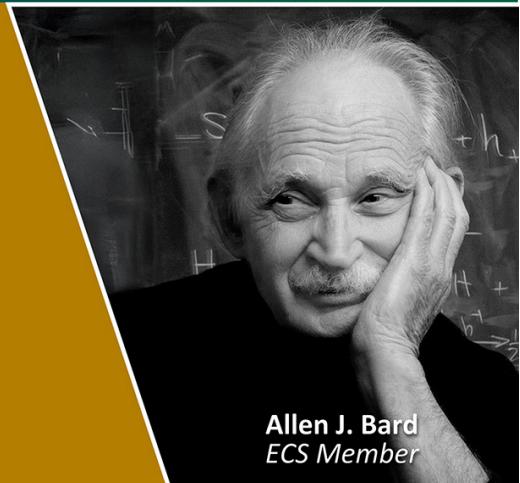
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Topical Review

A review: wafer bonding of Si-based semiconductors

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Received 4 October 2019, revised 10 January 2020

Accepted for publication 7 April 2020

Published 3 June 2020



Abstract

Wafer bonding techniques, which are very different from epitaxial growth techniques, can be used not only for the fabrication of micro-electromechanical systems (MEMS), silicon on insulator (SOI), and Si-based device integration, but have recently been applied to the achievement of high-quality homojunctions and heterojunctions in the photoelectric field. That is, carrier transport at the interface of the wafer-bonded junction should be unimpeded and carrier recombination at the bonded interface should be restrained. For Si/Si wafer bonding, although a high bonding strength and a bubble-free bonded interface are needed for the fabrication of the MEMS and SOI, a perfect Si/Si bonded interface which is expected to be bubble-free, oxide-layer-free, and dislocation-free is needed for the achievement of high-performance photoelectric devices, such as Ge/Si single-photon avalanche photodiodes. On the other hand, for Ge/Si heterogeneous hybrid integration (high lattice mismatch), threading dislocations (TDs) in the Ge film can be eliminated by low-temperature heterogeneous wafer bonding, due to the lower diffusion rate of misfit dislocations (MDs) at the Ge/Si bonded interface. This is very different from epitaxial growth, in which high-density TDs form in the integrated Ge layer due to the threading of MDs at high-temperature. In this paper, we review the wafer bonding of Si-based semiconductors based on different bonding methods. The advantages and disadvantages of different bonding methods are pointed out for comparison. We focus on the illustration of the fabrication of Si/Si and Ge/Si wafer pairs with TD-free, bubble-free, and oxide-layer-free bonded interfaces. Finally, the outlook for the development of Si/Si and Ge/Si wafer bonding and devices based on the wafer bonding technique is considered. We trust that this work may provide guidance for the low-temperature heterogeneous hybrid integration of different group materials with ultrahigh lattice mismatch, such as GeSn on Si and III–V materials on Si.

⁵ These authors contributed equally to this work.

Keywords: wafer bonding, hydrophilic reaction, oxide layer, bonding strength, bubbles, on/off ratio

(Some figures may appear in colour only in the online journal)

1. Introduction

With the development of microelectronics [1–5] and optoelectronics [6–10], the information era and the big data era have arrived successively on schedule. It is worth mentioning that the Moore's law [11–15] was first proposed over 50 years ago. Although many people have attempted to predict an end date for this law over the years, new revolutionary techniques, such as the fin field-effect transistor (FinFET) technique [16–18], the fully-depleted silicon-on-insulator (FD-SOI) technique [19–21], and the gate-all-around (GAA) technique [22–24] have been proposed, which allowed this law to continue to hold true. However, the number of transistors on a chip cannot possibly increase indefinitely, due to the fact that the size of transistors cannot possibly decrease indefinitely. The main factor limiting the decrease in size of the transistor has been suggested to be the physical difficulty in the Si-based fabrication process [25–27]. When the channel length of the transistor decreases to several nanometers, the thickness of the gate oxide decreases by several atomic layers. The electrical characteristics of the small transistor are difficult to control due to the increased leakage current induced by the quantum tunneling effect [28–30]. However, a further decrease in the size of the transistor is an important issue for the development of the integrated circuit.

The development of the Si complementary metal oxide semiconductor (CMOS) circuit triggers a further investigation of micro-electro-mechanical systems (MEMS) [31–33]. MEMS is a micro-system which contains several micromodules (micro-devices), such as a power source, sensor, control circuit, and processor. At present, MEMS has a wide range of applications in the field of material science, energy science, biomedicine, etc [34–37]. The development of MEMS has been accompanied by the rise of the study of MEMS packaging techniques. The packaging of MEMS can not only protect the micro-device from mechanical and environmental damage, but can also solve the problem of the heat dissipation of the chip. Many MEMS packaging techniques have been proposed to package the micro-system, such as the flip chip packaging technique [38, 39], multichip component technique [40, 41], multichip packaging technique [42, 43], wafer level packaging technique [44, 45], and three-dimensional (3D) integration packaging technique [46, 47].

The wafer level packaging technique based on Si/Si wafer bonding, and the 3D integration packaging technique based on Si/Si wafer bonding and through silicon via (TSV) technique [48–50] are two popular and important packaging techniques for the application of MEMS. Wafer level packaging is commonly used in the vacuum packaging of MEMS [51–55]. Vacuum packaging based on Si/Si wafer bonding provides a vacuum cavity for the MEMS device, to protect the movable structures in some specific MEMS devices, such as

the accelerometer [56, 57], gyroscope [58, 59], and pressure sensor [60, 61]. With the development of the integration of MEMS, 2D packaging based on photolithography is unable to meet market demands due to the fact that the feature size of semiconductor devices is gradually reaching its physical limits. That is, the number of integrated devices cannot be further increased in the future. Although some emerging techniques, such as the interposer technique [62–64] to achieve 2.5 D packaging, and the wire-bonding interconnect technique [65] to achieve quasi-3D packaging, have been proposed to increase the number of integrated devices, the integration level and the reliability of these techniques need to be further considered. 3D integration of the MEMS device based on wafer bonding and TSV techniques can achieve genuine device integration in the vertical direction. Overall, Si/Si wafer bonding plays an important role in the integration of MEMS.

Furthermore, Si/Si wafer bonding has potential application prospects in the fabrication of photoelectric devices. Currently, the fabrication of the Si avalanche layer of Ge/Si avalanche photodiodes (APD) is based on the traditional Si/Si homoepitaxy technique [66–69]. Due to the existence of lattice vacancies during Si/Si homoepitaxy, the Si avalanche layer commonly exhibits weak n-type doping (10^{15} – 10^{16} cm $^{-3}$). In addition, the residual P atom in the pipeline and on the chamber wall (or heater strip) from a previous run can diffuse into the epitaxial intrinsic Si layer during homoepitaxy of intrinsic Si. This leads to a high concentration of P atoms (10^{17} cm $^{-3}$ [70]) in the epitaxial intrinsic Si layer. On the other hand, the Si/Si homoepitaxy is commonly carried out at high temperature (>850 °C), thus the P atoms in the heavily-doped Si substrate can also diffuse into the epitaxial intrinsic Si layer due to the high diffusion rate of P atoms in Si [71–73]. When the P concentration in the Si avalanche layer increases, the electric field in the Si avalanche layer decreases and that in the Ge layer increases, as shown in figure 1(a), leading to the pre-breakdown of the device, as shown in figure 1(b). Thus, the fabrication of an impurity-free and vacancy-free Si avalanche layer is very important for the achievement of high-performance Ge/Si APD. Potential methods for the fabrication of a high-quality Si avalanche layer include the low-temperature Si/Si wafer bonding technique and the Smart-Cut technique. Based on these two techniques, the quasi-bulk-Si layer can be transferred to the heavily-doped Si substrate at low temperature. Thus, the achievement of a Si/Si bonded interface which shows perfect electrical properties is also very important.

On the other hand, in the past few years, Ge/Si photoelectric devices drew the attention of researchers due to the fact that these devices can not only respond to infrared light, but they can also be directly integrated with the CMOS circuit. It is well-known that the fabrication of Ge/Si photoelectric devices is based on established and mature epitaxial

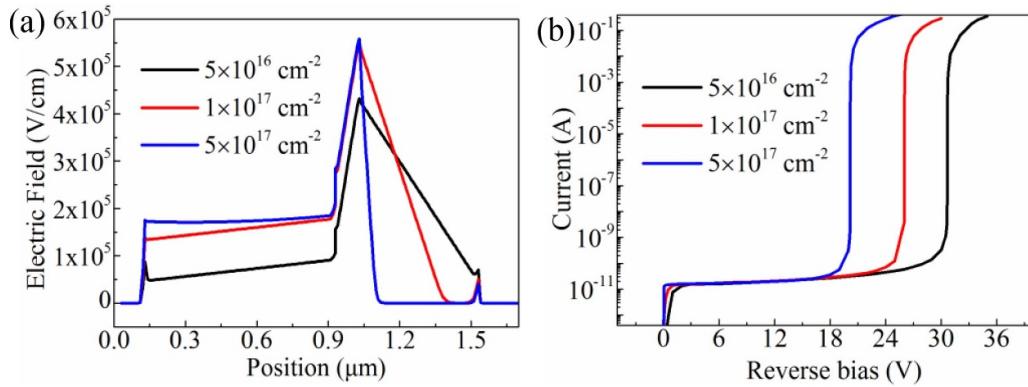


Figure 1. (a) I–V curves and (b) electric fields of Ge/Si APDs with different doping concentrations of Si avalanche layer.

techniques, such as reduced pressure chemical vapor deposition (RPCVD) [74, 75], ultra-high vacuum chemical vapor deposition (UHV-CVD) [76, 77], and molecular beam epitaxy (MBE) [78, 79]. However, epitaxial growth of the Ge film by these devices commonly requires ultrahigh vacuum (10^{-8} Pa) and high temperature (600 °C– 800 °C). In addition, the Ge/Si heterogeneous epitaxial growth produces high-density threading dislocations (TDs) (10^8 – 10^9 cm^{-2} [80, 81]) in the Ge film due to a 4.2% lattice mismatch between Ge and Si. Furthermore, after Ge growth, high-temperature cyclic annealing (700 °C– 900 °C) should be carried out to decrease the TD density (TDD) to 10^6 – 10^7 cm^{-2} [82–84]. This may lead to serious Ge/Si intermixing at the Ge/Si interface and the blue shift of the absorption wavelength of the photoelectric devices. It has been reported that the TDs in Ge film act as acceptor-like defects at the middle of bandgap [85, 86], leading to the increase of the dark current of the device.

Many modified Ge/Si epitaxial methods were proposed to decrease the TDD, such as the two-step Ge layer growth [80], Ge/SiGe multiple quantum well segregation [87, 88], graded SiGe buffer layer growth [89], and selective growth [90, 91]. It was reported that each method can lead to a decrease in the size of the TDD to 10^6 cm^{-2} . However, the dark current density of the Ge/Si photoelectric devices based on these epitaxial methods is still too high (10 – 50 mA cm^{-2} [92–99]) due to the fact that the distribution of the TDs is nonuniform in the epitaxial Ge film. It was reported in our previous works [80] that the TDD near the Ge/Si interface (within 100 nm) is as high as $>10^8 \text{ cm}^{-2}$. With the increase of Ge film thickness, the TDD decreases. Thus, further lowering the epitaxial growth temperature to <400 °C and the TD density to $<10^5 \text{ cm}^{-2}$ are two challenges for heterogeneous Ge/Si epitaxial growth. However, it is obvious that these two indicators are problematic in attempting to achieve Ge/Si epitaxial growth, due to the fact that the quality of epitaxial Ge film is low when lower epitaxial temperature is applied, and the epitaxial growth process cannot avoid the 4.2% lattice mismatch. One potential method for further decreasing the TDD is the heterogeneous Ge/Si wafer bonding and Smart Cut™ technique. It was reported that low-temperature Ge/Si wafer bonding can eliminate the TDs in Si-based Ge film. The Ge/Si wafer bonding and Smart Cut™ technique are considered to be an alternative for

Ge/Si epitaxial growth and the fabrication of Ge/Si photoelectric devices.

As described above, Si/Si wafer bonding and Ge/Si wafer bonding are two important techniques for improving of the quality of the Si avalanche layer and the elimination of TDs in Si-based Ge film, respectively. In this paper, we review the progress of Si/Si wafer bonding and Ge/Si wafer bonding to provide guidance for further understanding the importance of Si-based wafer bonding techniques in microelectronics and optoelectronics.

2. The process of Si/Si wafer bonding

The investigation of Si/Si wafer bonding starts from the direct bonding technique proposed by Shimbo *et al* in 1986 [100]. Compared to the epitaxial growth and ion implantation techniques in the semiconductor fabrication process, the Si/Si wafer bonding technique was receiving more and more attention in the field of MEMS and photoelectric devices because of its unique advantages. The most popular and common Si/Si wafer bonding method is direct wafer bonding. Two Si wafers with a root-mean-square (RMS) below 0.5 nm can directly contact each other in atmosphere or in vacuum without the bonder or metal transition layer after the wafers have been cleaned. Then post-annealing of the contacted wafers is conducted to enhance bonding strength. Popular methods for Si/Si wafer bonding include wet chemical surface-activated bonding, plasma-activated bonding, high-vacuum surface-activated bonding, ultraviolet-activated bonding, and semiconductor interlayer bonding.

2.1. Wet chemical surface-activated method

The wet chemical surface-activated method contains two techniques. One is wet chemical hydrophilic bonding, and the other is wet chemical hydrophobic bonding. For wet chemical hydrophilic bonding, during the RCA cleaning of Si wafers, each cleaning step can activate the Si surface due to the introduction of H_2O_2 , leading to the formation of a thin SiO_2 layer on the Si surface. The existence of the SiO_2 layer represents the hydrophilicity of the Si surface. For wet chemical hydrophobic bonding, H bonds should be introduced to passivate the Si

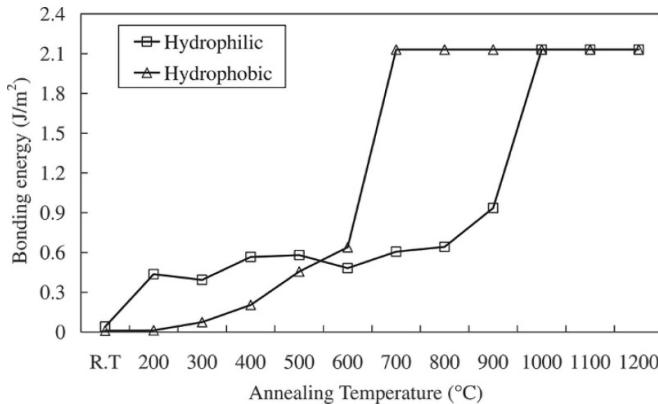


Figure 2. Bonding energy as a function of annealing temperature for hydrophilic and hydrophobic direct Si wafer bonding.
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surface. Commonly, the treatment of the HF solution of the cleaned Si surface can achieve H bond passivation.

Toyoda *et al* [101] and Plach *et al* [102] systematically investigated the wet chemical surface-activated method for Si/Si wafer bonding. For hydrophilic and hydrophobic bonding, a $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:10:60$ solution and a 5% HF solution were used to activate the Si surface, respectively. The effect of the annealing temperature on the bonding energy of bonded Si wafers in these two methods is shown in figure 2. One can see that the bonding energy of Si wafer pairs increases with the increase in the annealing temperature. The annealing of the wafer pairs should be carried out at 1000 °C in order to achieve a high bonding energy of 2.1 J m^{-2} for hydrophilic bonding, while an annealing temperature of 700 °C is required for hydrophobic bonding. Note that the bond energy of -OH groups is stronger than that of -H groups. Thus, hydrophilic bonding is easier to achieve than hydrophobic bonding.

The bonding mechanism of hydrophilic bonding is shown in figure 3. One can see that H bonding occurs at the interface when the temperature is below 200 °C. In addition, the S-O-Si bonds and H_2O bubbles begin to form at the bonded interface when the temperature is above 200 °C. Note that when the temperature is increased to >700 °C, the hydrophilic reaction ($\text{Si} + 2\text{H}_2\text{O} = \text{SiO}_2 + 2\text{H}_2$) occurs, and the H_2O bubbles at the bonded interface turn into H_2 bubbles. Finally, H_2 gas diffuses into the Si wafer when the temperature is increased to >900 °C, leading to the disappearance of H_2 bubbles.

For hydrophobic bonding, as shown in figure 4, when the wafer pairs are annealed at <300 °C, the wafers are weakly held by van der Waals force. When the temperature is increased to >300 °C, the Si-H₂ bond converts into Si-H bond and H_2 , and the Si-Si bond begins to form. When the temperature is raised to >700 °C, the H_2 begins to diffuse into Si wafers, resulting in the disappearance of H_2 bubbles. TEM images of bonding interfaces are shown in figure 5. One can see that an obvious oxide layer appears at the bonded interface for hydrophilic direct bonding due to the hydrophilic reaction at the bonded interface. However, the oxide clusters appear at the bonding interface due to the aggregation of O atoms in the Si wafer at the bonded interface.

Overall, hydrophilic and hydrophobic direct wafer bonding are two easy methods of Si/Si wafer bonding. Both methods can achieve a high bonding strength of Si wafer pairs and bubble-free bonded interfaces. However, the annealing temperature of wafer pairs must be high enough. In addition, the oxide layer originating from the hydrophilic reaction and the oxide clusters originating from the aggregation of O atoms are difficult to eliminate.

2.2. Plasma-activated bonding

As described above, the annealing temperature of Si/Si wafer pairs should be increased to at least 700 °C to enhance the Si/Si bonding strength. This is close to the fracture strength of bulk Si for wet chemical surface-activated bonding. However, for the packaging of MEMS and the prevention of the diffusion of impurities in the substrate into the intrinsic layer, the bonding temperature of Si wafer pairs should be decreased to ≤ 400 °C. In order to decrease the annealing temperature of Si wafer pairs, some researchers propose to introduce plasmas for the activation of the Si surface. Howlader *et al* and Suga *et al* [103–109] systematically studied the effect of sequential plasma activation on the bonding strength, bubble density, bonded interface, and electrical properties of Si bonded wafer pairs. The plasmas used in the experiment are O plasma in the RIE system and N microwave plasma radicals. The surface treatment process is shown in figure 6. Firstly, the Si wafer surface was exposed to the O plasma, and then the wafers were treated with N microwave plasma radicals. After that, the treated Si wafers were contacted to achieve the pre-bonding of the wafer pairs.

Note that, as shown in figure 7(a), when the wafers were just contacted to each other, a low bonding energy of $\sim 0.2 \text{ J m}^{-2}$ was achieved. However, when the wafer pairs were stored in air for 24 h, the bonding energy increased to $\sim 2.2 \text{ J m}^{-2}$. This is attributed to the formation of Si-O-Si bonds at the Si/Si bonding interface during the storing of the wafer pairs. The bonding mechanism of the sequential plasma activation method can be described as follows: Firstly, the O plasma treatment in the RIE system, which is similar to the O ion bombardment process, removed contaminants on the Si surface and formed a porous oxide layer on the Si surface. These porous structures are beneficial for the migration of H_2O and H_2 . After that, the Si surface was treated by energy-free N microwave plasma radicals to produce a chemical-metastable oxynitride thin film on the Si surface. Thus, the Si surface after the O and N plasma treatment becomes extremely hydrophilic. Some H_2O molecules can diffuse into this oxynitride to form the Si-O-Si bonds, resulting in an increase in bonding strength at room temperature.

The temperature dependence of the bonding strength of the wafer pairs is shown in figure 7(b). One can see that for wet chemical hydrophilic bonding, the bonding strength of ~ 16 Mpa was achieved when the temperature reached 1100 °C. However, for sequential plasma activation method, the bonding strength of ~ 16 Mpa was achieved at room temperature. However, with the increase in annealing temperature, the bonding strength slightly increases at first, and then decreases.

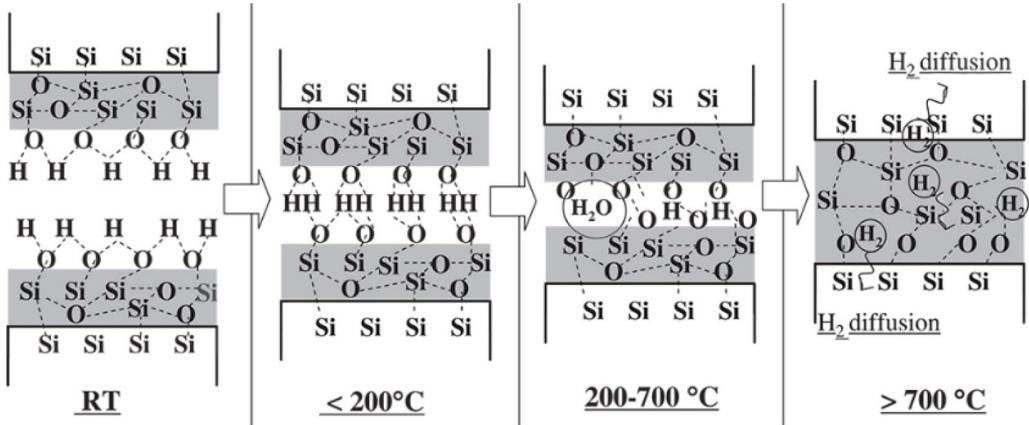


Figure 3. Bonding mechanism of hydrophilic direct Si wafer bonding. Reproduced from [101]. © IOP Publishing Ltd. All rights reserved.

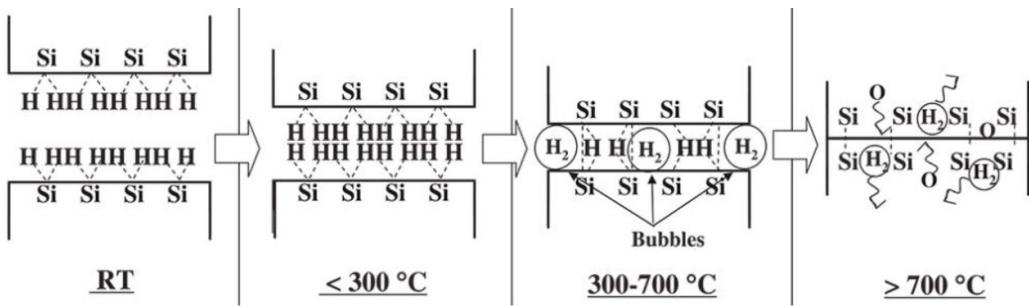


Figure 4. Bonding mechanism of hydrophobic direct Si wafer bonding. Reproduced from [101]. © IOP Publishing Ltd. All rights reserved.

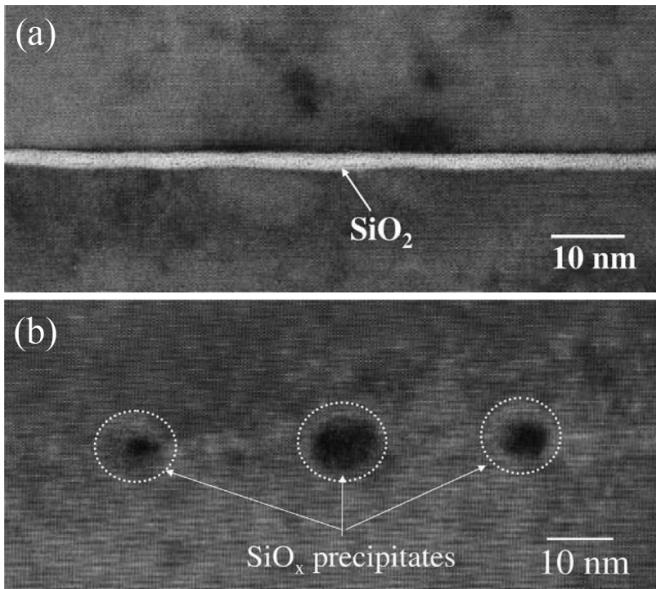


Figure 5. TEM images of the bonding interfaces. Reproduced from [101]. © IOP Publishing Ltd. All rights reserved. (a) Hydrophilic direct wafer bonding and (b) hydrophobic direct wafer bonding.

This feature can be explained by the increase of the bubble density at the bonded interface, as shown in figure 8.

This is a common phenomenon for hydrophilic wafer bonding and is due to the increase of hydrophilic reactions at the bonded interface when higher annealing temperatures were

applied, leading to the decrease of the bonding strength of the wafer pairs. In other words, the Si/Si wafer pairs produced by sequential plasma-activated bonding cannot suffer from high-temperature annealing. On the other hand, with the increase of the annealing temperature, the oxide layer thickness at the bonded interface increases, as shown in figure 9. When the temperature increases to 600 °C, the oxide layer thickness reaches ~13 nm. This is also attributed to a serious hydrophilic reaction at the bonded interface. The existence of the oxide layer at the bonded interface produces a high barrier at the bonded interface, leading to the nonlinearity of the I-V curves, as shown in figure 10.

Overall, sequential plasma-activated bonding can achieve a high bonding strength of Si/Si wafer pairs and a near-bubble-free bonded interface at room temperature due to the appearance of the chemical bonds at the bonded interface after storing. However, with the increase of the annealing temperature, the bubble density increases, leading to a decrease in bonding strength. In addition, with the increase of the annealing temperature, the oxide layer thickness at the bonded interface increases, leading to the nonlinearity of the I-V curves. That is, the transport of the carriers at the bonded interface is restrained by the interface barrier.

2.3. High-vacuum surface-activated bonding

As illustrated above, chemical reactions occur at the Si/Si bonded interface in wet chemical surface activation and plasma surface activation, due to the introduction of -OH and -H

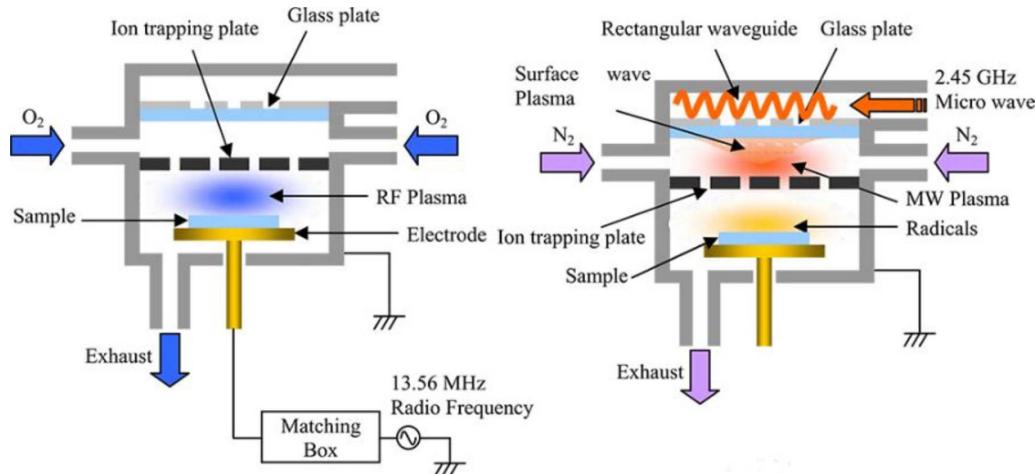


Figure 6. Schematic diagram of the sequential plasma-activated bonding. Reproduced from [103]. © IOP Publishing Ltd. All rights reserved.

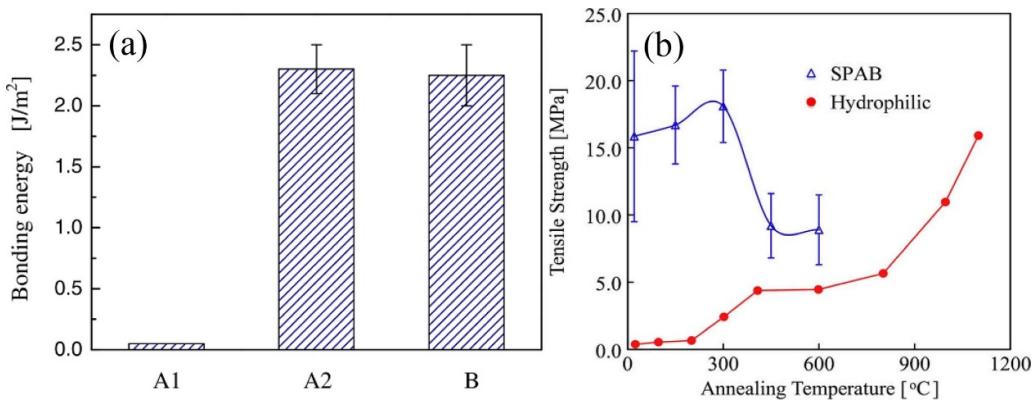


Figure 7. (a) Bonding energy versus stored time of the bonded wafer pairs. Reproduced from [103]. © IOP Publishing Ltd. All rights reserved. (b) Bonding strength versus annealing temperature for sequential plasma-activated bonding and hydrophilic direct bonding. © (2010) IEEE. Reprinted with permission from [104].

groups on the Si surface to enhance bonding strength. The bonding of the wafers in these two methods takes place in atmosphere. The absorption of -OH groups in atmosphere cannot be avoided. In order to eliminate -OH groups on the Si surface completely, high-vacuum surface-activated bonding was proposed. The surface-activated bonding was conducted in high vacuum. Thus, the molecules in the atmosphere cannot absorb on the Si surface after surface activation. The surface-activated bonding process is shown in figure 11. Firstly, Si wafers were loaded into the vacuum chamber after cleaning. Note that an oxide layer and adsorbed molecules exist on the Si surface after cleaning. Ar atom beam etching was carried out when the pressure of the vacuum chamber decreased to $< 5 \times 10^{-5}$ Pa to activate the Si surface. The surface oxide layer and adsorbed molecules can be totally removed after Ar atom beam treatment, leaving Si dangling bonds on the Si surface. The Si surface is difficult to reoxidize in high-vacuum conditions. Thus, the Si surface can maintain high activity and achieve the bonding of Si dangling bonds. Finally, the treated Si wafers were directly bonded by the Si-Si bonds, achieving high bonding strength.

Suga *et al* [110–116] started to investigate Si/Si wafer bonding using high-vacuum surface-activated bonding in the

1990 s. They not only studied the effect of different conditions, such as annealing temperature, processing time of the Ar atom, and vacuum degree, on the bonding quality of Si/Si wafer pairs, but also achieved Ge/Ge [117] and GaAs/Si wafer bonding [118] by this method. For Si/Si wafer bonding, they revealed the dependence of bonding strength on the annealing temperature, as shown in figure 12(a). One can see that the bonding strength of the wafer pairs fabricated by this method is greater than that fabricated by wet chemical surface-activated bonding and plasma surface-activated bonding. This indicates that the bond energy of the Si-Si bond is higher than that of the Si-O-Si bond. With the increase in annealing temperature, a decrease in bonding strength was not observed. Bonding strength can reach ~18 Mpa when the treated wafers were direct contacted at room temperature. This is ascribed to the fact that only Si-Si bonds form at the Si/Si bonded interface, and other elements were not introduced. Thus, with an increase in temperature, chemical reactions are absent at the bonded interface, leading to the stabilization of bonding strength.

They also studied the effect of pressure applied on the wafer pairs on bonding strength, as shown in figure 12(b). One can see that the bonding strength of the wafer pairs is almost unchanged with the increase in applied load. This implies

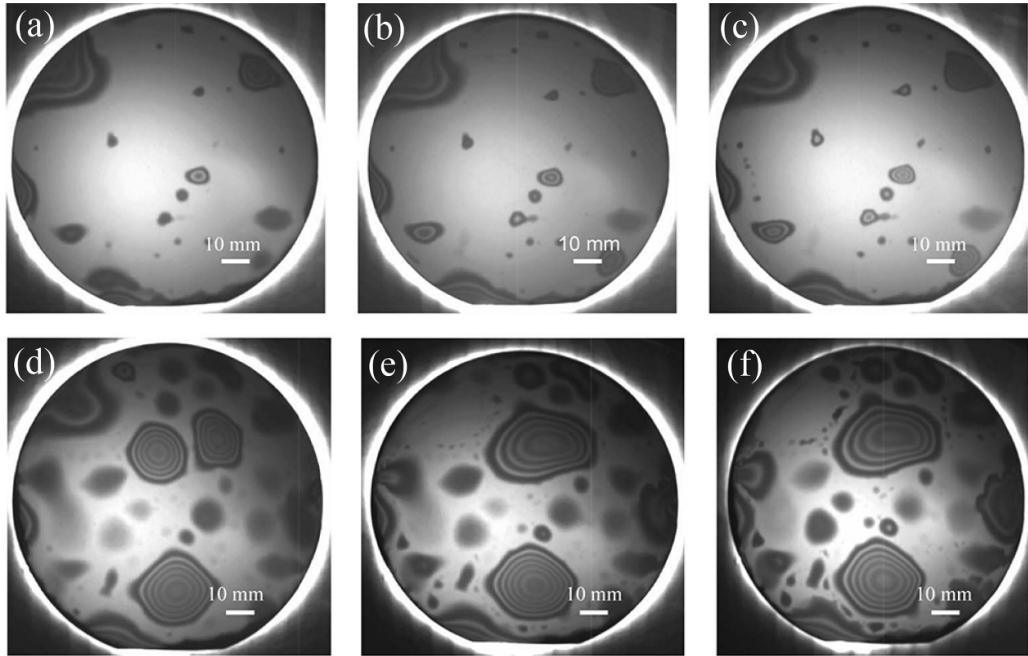


Figure 8. (a)–(f) Infrared images of the Si/Si bonded interfaces annealed at 100 °C, 200 °C, 300 °C, 400 °C, 500 °C, and 600 °C. © (2010) IEEE. Reprinted with permission from [104].

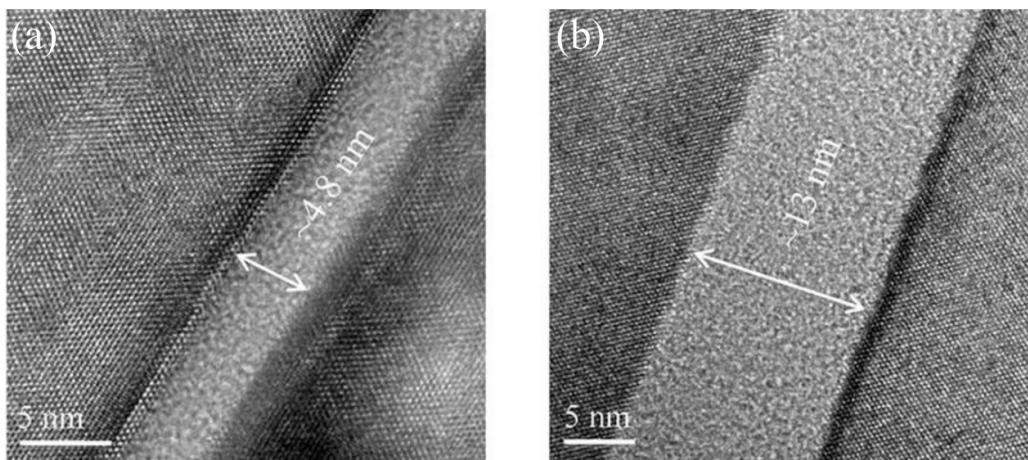


Figure 9. TEM images of Si/Si bonded interfaces (a) before annealing and (b) after annealing at 600 °C. Reproduced from [105]. © IOP Publishing Ltd. All rights reserved.

that once the activated Si wafers are contacted together, high bonding strength can be achieved without the applied load. Figure 13(a) shows the effect of the etching time of the Ar beam on the bonding strength of the wafer pairs. It is shown that bonding strength increases at first, then stabilizes at ~ 12 MPa, and finally decreases with the increase in etching time. The increase of the bonding strength is due to the activation of the Si surface, while the decrease of the bonding strength results from the increase of the RMS of the Si surface with the increase of the etching time, as shown in figure 13(b).

It is known that the vacuum level is an important factor in this method. They also investigated the effect of the vacuum level on bonding strength and bubble density. As shown in figure 14(a), bonding strength increases with the increase of the vacuum level. When the pressure decreases to 5×10^{-5} Pa, a bonding energy of 2.5 J m^{-2} can be achieved. Figures

14(b) and (c) show infrared images of the wafer pairs bonded in a vacuum chamber with a pressure of 2×10^{-5} and 5×10^{-4} Pa, respectively. One can see that no bubbles can be observed at the bonded interface when the pressure was set to 2×10^{-5} Pa, while some bubbles appear at the bonded interface when the pressure was increased to 5×10^{-4} Pa. This is ascribed to the fact that the particles and molecules were adsorbed on the activated Si surface when the pressure was set to a higher value, leading to the appearance of hydrophilic reactions at the bonded interface. Thus, the bubbles appear at the bonded interface. In order to achieve a satisfied Si/Si bonded interface, a pressure of as low as 10^{-7} Pa should be applied.

Note that a thin amorphous Si (a-Si) layer appears at the Si/Si bonded interface after wafer bonding by this method, due to the bombardment effect of the Ar atom beam, as shown in figure 15(a). This is similar to the ion implantation effect.

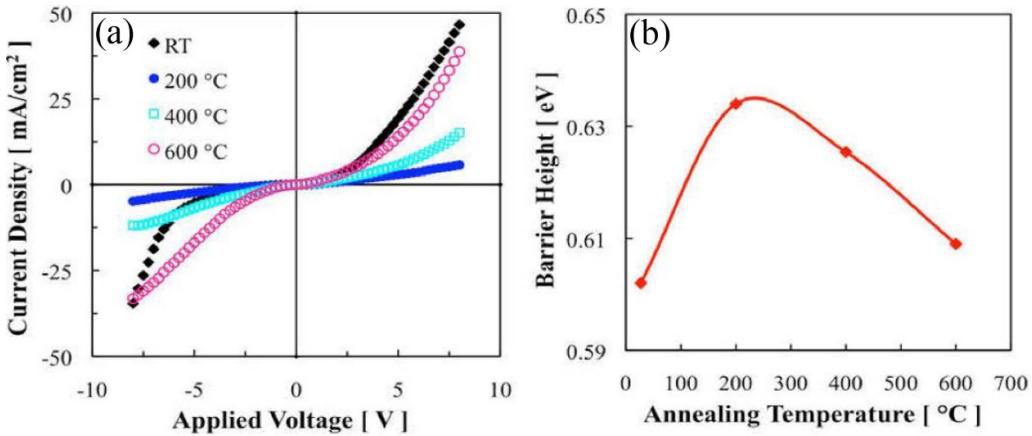


Figure 10. (a) I-V curves of the bonded wafer pairs annealed at different temperatures. (b) Barrier height at the bonded interface versus annealing temperature. (a), (b) Reproduced from [105]. © IOP Publishing Ltd. All rights reserved.

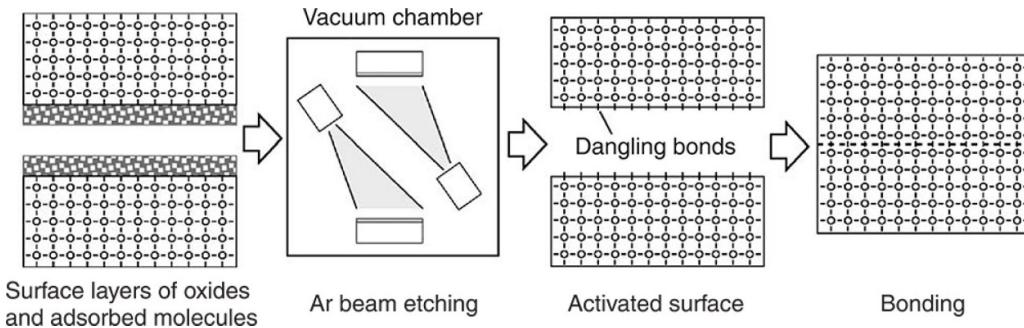


Figure 11. Bonding process of high-vacuum surface-activated bonding. Reprinted from [110], Copyright (2006), with permission from Elsevier.

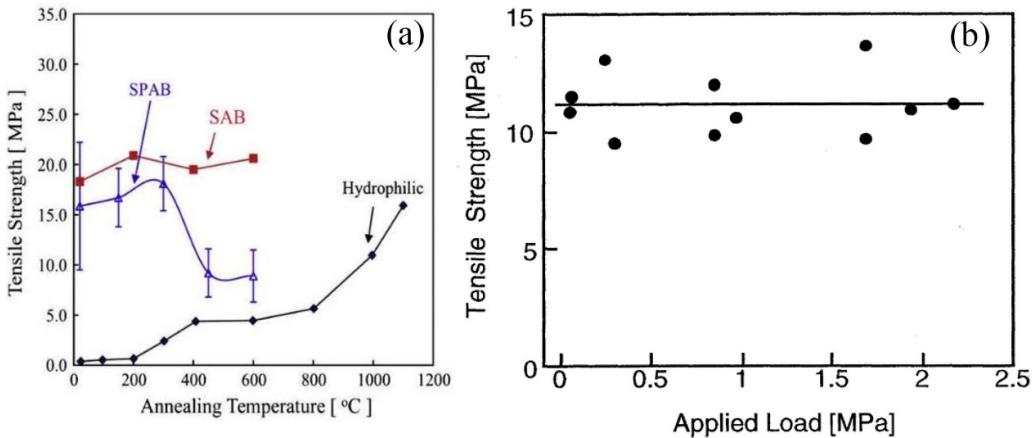


Figure 12. (a) Bonding strength versus annealing temperature. Reprinted from [111], Copyright (2010), with permission from Elsevier. (b) Bonding strength versus applied load. Reproduced from [112]. © IOP Publishing Ltd. All rights reserved.

The thin a-Si layer can be totally repaired after annealing at 700 °C for 3 h, as shown in figure 15(b). On the other hand, the n-Si/n-Si junction fabricated by this method can achieve a linear electrical property at room temperature, as shown in figure 15(c). However, the current densities of the n-Si/n-Si and p-Si/p-Si junctions irregularly change with the increase of the annealing temperature, as shown in figures 15(d) and (e). The potential barrier at the bonded interface is shown in figure 15(f). One can see that the potential barrier of the n-Si/n-Si junction is smaller than that of the p-Si/p-Si junction.

In addition, the potential barrier at the bonded interface fabricated by this method is smaller than that fabricated by the plasma-activated method.

Overall, due to the absence of -OH groups adsorbed on the activated Si surface, the oxide layer and the interface bubbles at the bonded interface can be eliminated and high bonding strength can be achieved. However, a thin a-Si layer appears at the bonded interface. High-temperature annealing (700 °C) should be conducted to repair this layer. In addition, although the linear I-V curve can be achieved for the sample bonded

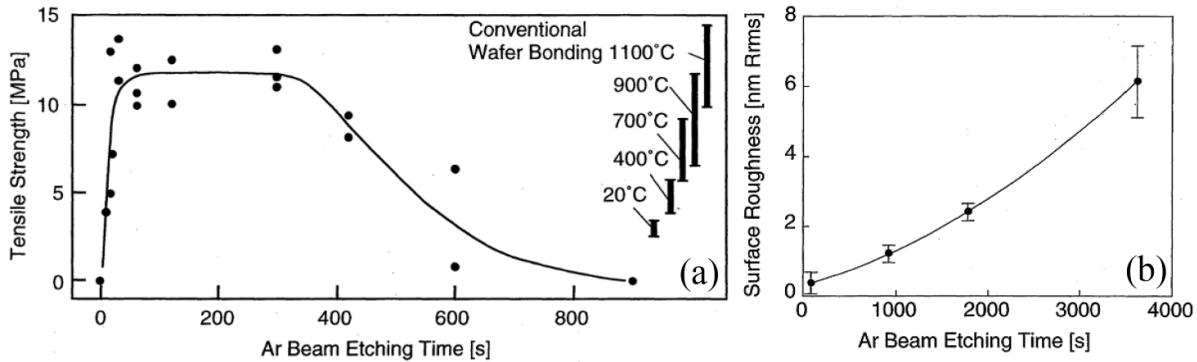


Figure 13. (a) Bonding strength versus Ar beam etching time. (b) Surface roughness versus Ar beam etching time. (a), (b) Reproduced from [112]. © IOP Publishing Ltd. All rights reserved.

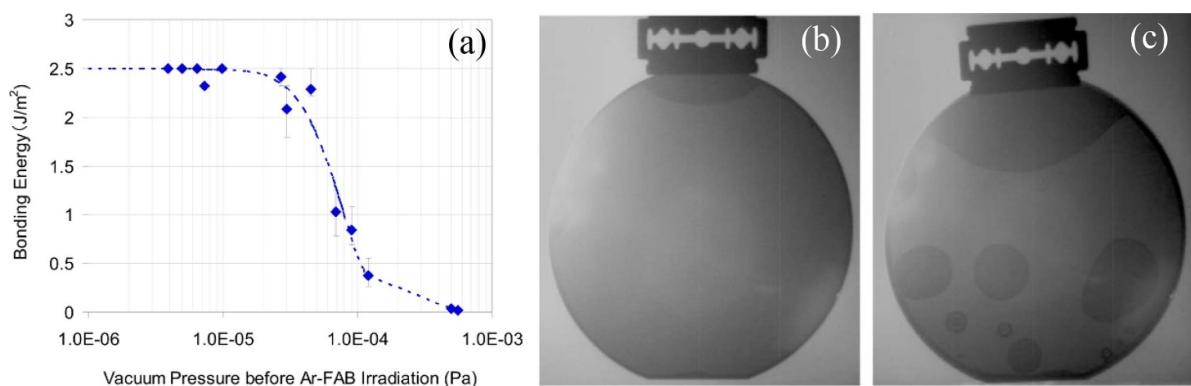


Figure 14. (a) Bonding energy versus vacuum pressure. Infrared images of the samples bonded at a pressure of (b) 2×10^{-5} Pa and (c) 5×10^{-4} Pa. (a)–(c) © (2010) IEEE. Reprinted with permission from [113].

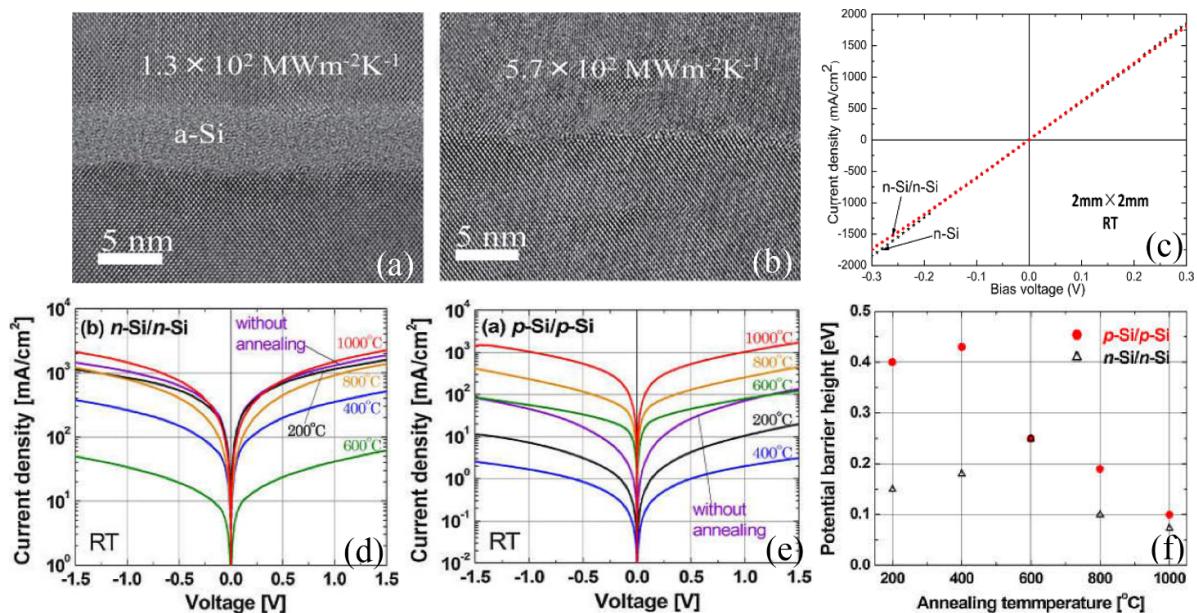


Figure 15. TEM images of the bonded interfaces (a) before annealing and (b) annealed at 700 °C for 3 h. Reproduced from [114], with the permission of AIP Publishing. I–V curves of (c) the n-Si/n-Si wafer pairs bonded at room temperature. Reproduced from [115], with the permission of AIP Publishing. (d) The n-Si/n-Si wafer pairs annealed at different temperature, (e) p-Si/p-Si wafer pairs annealed at different temperature. Reproduced figure from [116], with the permission of IOP Publishing. (f) Potential barrier height versus annealing temperature. (d)–(f) Reproduced from [116]. © IOP Publishing Ltd. All rights reserved.

at room temperature, the I-V curve is still sensitive to the annealing temperature. High-temperature annealing should be conducted for achieving low potential barrier height at the bonded interface.

2.4. Ultraviolet-activated bonding

Dry activation, such as plasma activation and Ar atom beam activation, can lower the annealing temperature of bonded Si wafer pairs. However, as described above, the mechanism for low-temperature Si/Si wafer bonding is different. Ultraviolet (UV)-activated bonding is another low-temperature Si/Si wafer bonding technique. Before Si/Si wafer bonding, the Si wafers were exposed to the UV light to activate the Si surface. The Si surface is extremely hydrophilic after activation. The mechanism for the UV-activated bonding can be divided into two parts: surface cleaning, and surface activation. The UV irradiation can further clean the Si surface, as shown in figure 16. Some organic molecules may absorb on the Si surface after wet cleaning. When UV irradiation at a wavelength of 185 nm is conducted on the Si surface, the C-C bonds and C = C bonds in hydrocarbon break to form ions, free atoms, and active molecules. On the other hand, UV irradiation (185 nm) can decompose O₂ into O₃ and O (2O₂ = O₃ + O). The O₃ can be absorbed again by UV irradiation with the wavelength of 254 nm to form O₂ and O. This continuous photosensitized reaction leads to an increase of active O atoms on the Si surface. The O atoms bond with the C atoms to form CO₂ and CO, leading to a cleaning of the Si surface.

UV irradiation can activate the Si surface, as shown in figure 17. High-energy UV irradiation can break the bonds of water molecules to form -OH and -H bonds on the Si surface. The -H bonds can further bond with the surrounding O atoms to form -OH bonds. In addition, UV irradiation can break the Si-O bonds in the Si oxide to form Si- and Si-O-bonds, then the Si- bonds can bond with the -OH bonds to form Si-OH bonds and the Si-O- bonds can bond with the -H bonds to form Si-OH bonds, leading to an increase in the hydrophilicity of the Si surface.

Shi *et al* and Kub *et al* [119–123] systematically studied the effect of UV irradiation on Si/Si wafer bonding. The effect of UV irradiation time on the RMS of the Si surface and on bonding strength was investigated, as shown in figure 18. One can see that when a UV irradiation time of 5 min was applied, the RMS of the Si surface reaches lowest value and the bonding strength reaches highest value (~15 Mpa). With the increase of UV irradiation time, the RMS increases and the bonding strength decreases. This is similar to the outcomes in high-vacuum surface-activated bonding. They also studied the dependence of bubble density on UV irradiation time, as shown in figure 19. It is shown that no bubbles were observed in the infrared image when a UV irradiation time of 5 min was applied. When increasing the irradiation time to 10 min, some bubbles appear at the bonded interface. This may be due to the increase of the RMS, as shown in figure 18(a).

Bonding strength as a function of annealing temperature and annealing time is shown in figure 20. One can see that the bonding strength increases with the increase of the annealing

temperature. This is explained by the increase of the Si-O-Si bonds formed by the hydrophilic reaction at the bonding interface when higher temperature was applied. In addition, the bonding strength increases at first, and then tends to become stable with the increase of the annealing time. The increase of the bonding strength at first is attributed to the increase of the hydrophilic reaction when short-time annealing was conducted, while the stabilization of the bonding strength is due to the absence of the hydrophilic reaction when long-time annealing was conducted.

Figures 21(a) and (b) show scanning acoustic microscope (SAM) images of bonded interfaces with and without UV irradiation for 5 min, respectively. It is important to note that although the infrared images show that no bubbles were observed at the bonded interface when a UV irradiation time of 5 min was applied, the SAM images show that some small bubbles still exist at the bonded interface. This indicates that the resolution of SAM is higher than that of infrared transmission. It is more suitable to evaluate interface bubbles using SAM. One can see that the bubbles in the sample with UV irradiation are smaller than that in the sample without UV irradiation. On the other hand, although the authors did not show the TEM image of the bonded interface, we can speculate that the bonding interface contains an oxide layer due to the fact that the UV-activated method is a hydrophilic bonding method, so Si-O-Si always exists at the bonded interface.

2.5. Semiconductor interlayer bonding

In order to achieve a real bubble-free bonded interface, some researchers have attempted to construct a porous semiconductor interlayer between two Si wafers to exhaust by-products produced at the bonded interface. This is known as semiconductor interlayer bonding. In this method, a smooth semiconductor interlayer, which is formed by film deposition, ion implantation, or ion etching, was inserted between two Si wafers to achieve interlayer bonding. Tong *et al* [124] and our colleagues [125–129] systematically studied Si/Si wafer bonding based on an a-Si layer and on amorphous Ge (a-Ge), respectively. Tong *et al* studied the effect of a-Si interlayers fabricated by sputtering, ion implantation, RIE etching, and B₂H₆ plasma treatment on the bonding strength and interface characteristics of Si/Si wafer pairs. The HF solution was used to achieve hydrophobic bonding. As described above, the annealing temperature for hydrophobic bonding should be increased to >700 °C for the achievement of high bonding strength. Thus, in order to lower the annealing temperature of Si/Si hydrophobic bonding, the dehydrogenation of the Si surface was carried out at low temperature. Van de Walle *et al* and Tong *et al* [130, 131] reported that the H atoms on the a-Si surface can be released at a lower temperature (200 °C) than that on the bulk Si surface (300 °C). Thus, Si wafer bonding based on a-Si can be achieved at a lower temperature. On the other hand, a-Si exhibits a porous structure; it can absorb and release H atoms when post-annealing is conducted.

Firstly, the As⁺ implantation was applied to form 150 nm thick a-Si layer on the Si surface. The ion implantation of one wafer and two wafers were both conducted for wafer

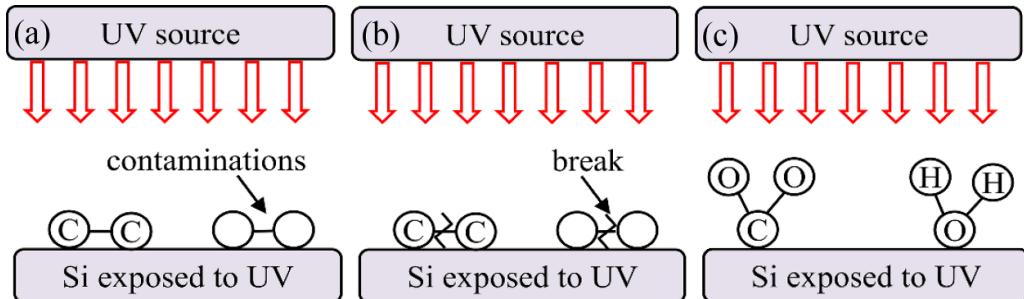


Figure 16. Mechanism of UV surface cleaning. (a) UV radiation forms active O atoms. (b) UV radiation breaks down hydrocarbon contaminations on wafer surface. (c) Gaseous byproducts form and escape from the surface. [119] (2018) © (Springer Nature Switzerland AG. Part of Springer Nature.) With permission of Springer.

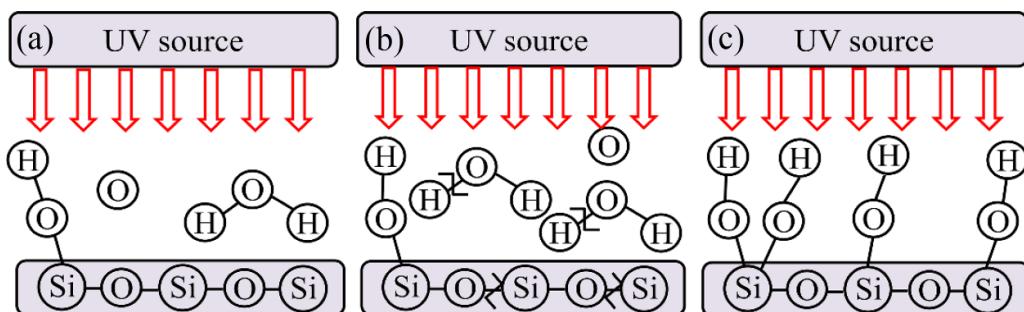


Figure 17. Mechanism of UV surface modification. (a) UV exposure on the silicon surface. (b) UV radiation breaks down H₂O and Si-O-Si, then forms H-, -OH, Si- and Si-O-. (c) Silicon surface acquires considerable Si-OH and becomes hydrophilic. [119] (2018) © (Springer Nature Switzerland AG. Part of Springer Nature.) With permission of Springer.

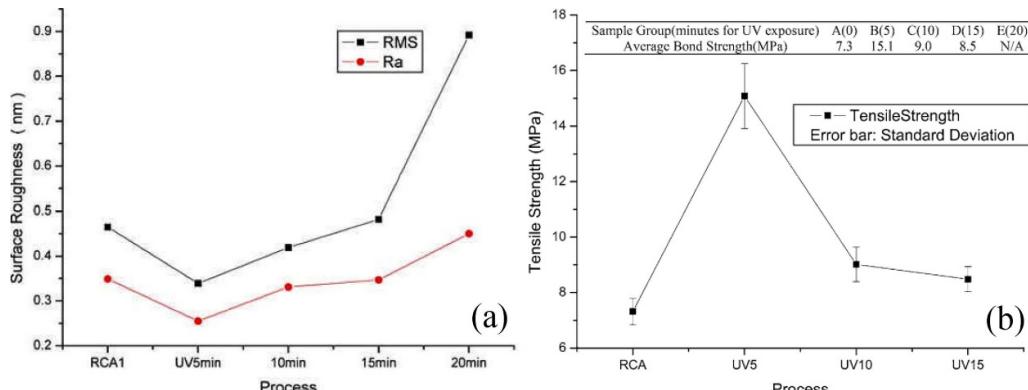


Figure 18. (a) Surface roughness versus UV exposure time. (b) Bonding strength versus UV exposure time. (a), (b) [119] (2018) © (Springer Nature Switzerland AG. Part of Springer Nature.) With permission of Springer.

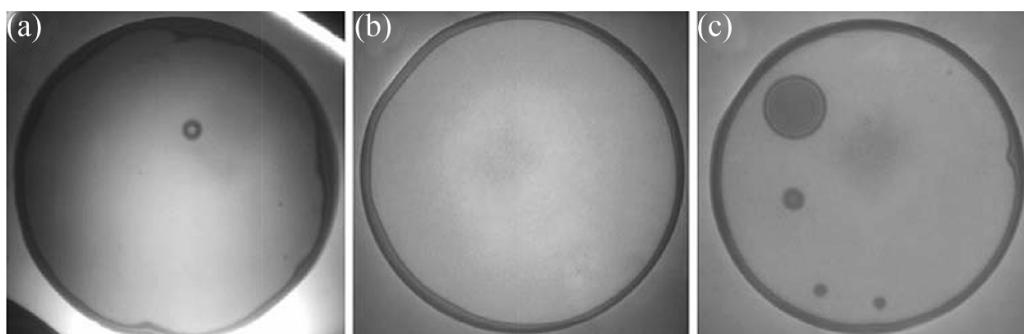


Figure 19. Infrared images of the bonded samples (a) without UV irradiation, (b) with UV irradiation for 5 min, and (c) with UV irradiation for 10 min. [119] (2018) © (Springer Nature Switzerland AG. Part of Springer Nature.) With permission of Springer.

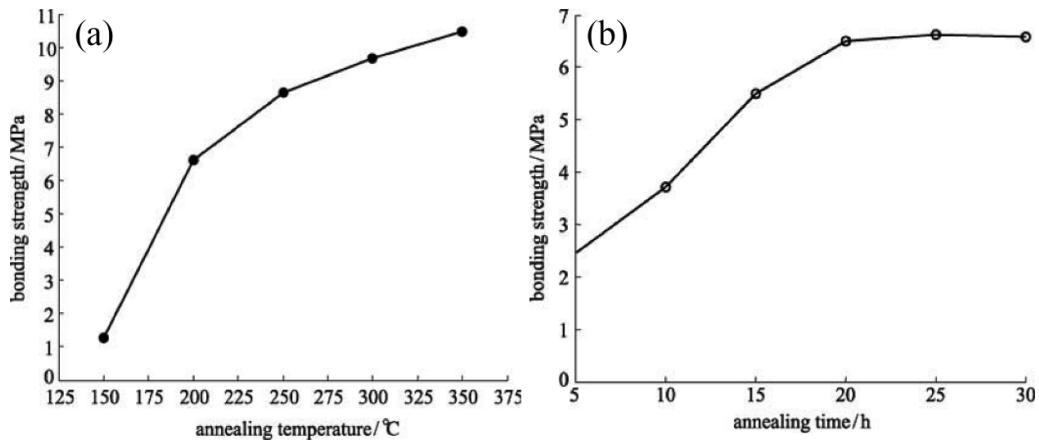


Figure 20. (a) Bonding strength versus annealing temperature. (b) Bonding strength versus annealing time. (a), (b) [120] (2009) © (Springer Nature Switzerland AG. Part of Springer Nature.) With permission of Springer.

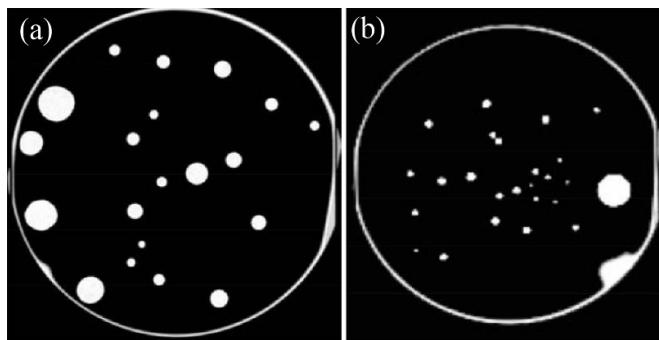


Figure 21. Scanning acoustic microscopy images of the bonded interfaces (a) without UV radiation and (b) with UV radiation for 5 min. Reproduced from [121]. © IOP Publishing Ltd. All rights reserved.

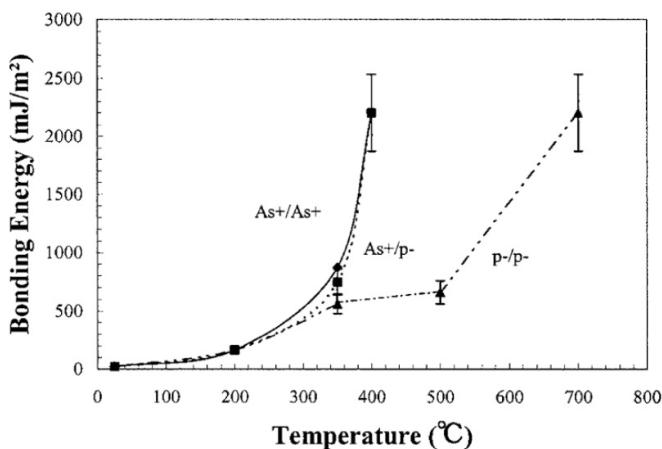


Figure 22. Bonding energy versus annealing temperature. Reprinted from [124], with the permission of AIP Publishing.

bonding. Bonding energy as a function of annealing temperature is shown in figure 22. One can see that for direct wafer bonding, the wafer pairs should be annealed at 700 °C to achieve a bonding energy of $\sim 2.2 \text{ J m}^{-2}$. However, for the sample with As^+ implantation, only 400 °C annealing needs to be applied for the achievement of a bonding energy of $\sim 2.2 \text{ J m}^{-2}$.

m^{-2} . Figure 23(a) shows the TEM image of the bonded interface for the as-bonded sample. The a-Si/a-Si bonded interface can be clearly observed, and a $\sim 300 \text{ nm}$ thick a-Si layer exists at the bonded interface. After annealing at 450 °C for 24 h, as shown in figure 23(b), most of the a-Si has crystallized, leaving a $\sim 10 \text{ nm}$ thick a-Si layer at the bonded interface. After annealing at 450 °C for 28 h, the a-Si has completely crystallized (not shown here).

They also fabricated a $1 \mu\text{m}$ thick a-Si layer on the Si wafer using sputtering and CMP techniques for wafer bonding. The bonding strength of the Si wafer pairs reached the fracture strength of bulk Si when the annealing temperature was set to 300 °C. In addition, bubbles were not observed at the bonded interface due to the absorption of H by the a-Si film. This indicates that a thick a-Si layer can further decrease the bonding temperature. They also fabricated a 1–3 nm thick a-Si layer onto the Si by RIE etching for wafer bonding. An annealing temperature of 400 °C needs to be applied to achieve high bonding strength. Finally, B_2H_6 plasma was used to form a 2 nm thick a-Si layer on the Si wafer surface. The effect of annealing temperature on bonding strength is shown in figure 24. One can see that bulk fracture strength was achieved when the temperature was increased to 350 °C. The lower annealing temperature of the wafer pairs results from the fact that after treatment with B_2H_6 plasma, the B in Si weakens Si-H_x bonds, leading to the breakage of the Si-H_x bonds at a lower temperature.

Our colleagues introduced a thin a-Ge layer between two Si wafers to achieve Si/Si wafer bonding with a high bonding strength and a bubble-free bonded interface. Firstly, we investigated the RMS of a sputtered a-Ge layer on the Si substrate versus input power and operation pressure, as shown in figure 25(a). One can see that the RMS of the a-Ge film is small ($<0.4 \text{ nm}$) and is almost static at lower power (3–120 W), while it increases sharply at a higher power setting ($>120 \text{ W}$). In addition, the RMS of the a-Ge film also shows little change at low pressure, while it increases sharply when the pressure exceeds 0.4 Pa. Finally, an a-Ge film with an RMS of 0.28 nm (power = 20 W and pressure = 0.3 Pa) was selected for bonding experiments. Before a-Ge wafer bonding, we studied the

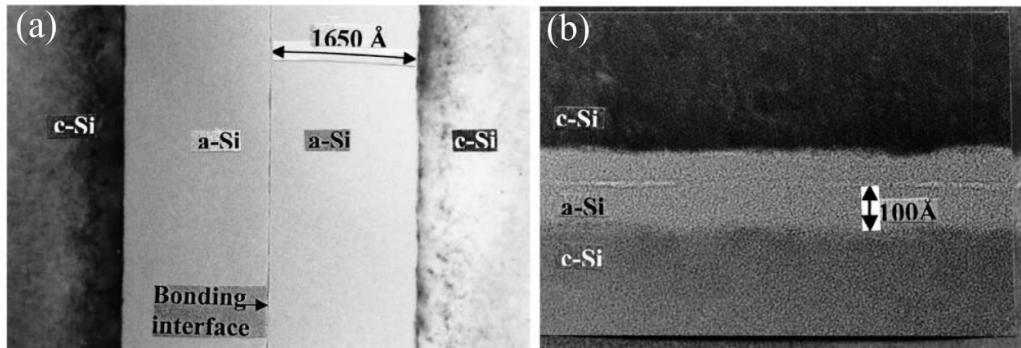


Figure 23. TEM images of the bonded interfaces for (a) the as-bonded sample and (b) the sample further annealed at 450 °C for 24 h. Reprinted from [124], with the permission of AIP Publishing.

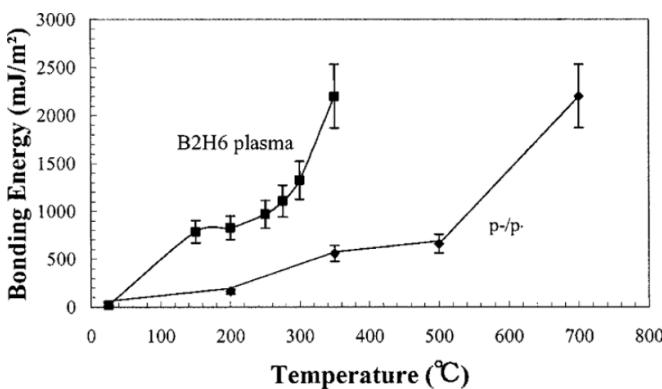


Figure 24. Bonding energy versus annealing temperature. Reprinted from [124], with the permission of AIP Publishing.

effect of a-Ge layer thickness on the hydrophilicity of the Ge film, as shown in figure 25(b). One can see that with an increase in the thickness of the a-Ge layer, the contact angle decreases at first, and then trends towards stability ($\sim 3^\circ$). This indicates that the sputtered a-Ge film (>2 nm) exhibits extremely hydrophilic behaviour. The inset shows the effect of sputtering power on contact angle. It demonstrates that the contact angle remains static with the increase of sputtering power. We also investigated the contact angle of the a-Ge versus exposure time, as shown in figure 25(c). One can see that with the increase of the exposure time, the contact angle increases, indicating a decrease in the level of hydrophilicity. This is due to the oxidation and carbonization of the a-Ge surface when the a-Ge film is exposed to air, as shown in the inset of figure 25(c).

We also investigated the effect of the secondary annealing temperature on bubble density and bonding strength, as shown in figures 26 and 27(a). One can see that with the increase in secondary annealing temperature, bubble density increases at first, and then decreases. In addition, bonding strength increases with the increase of the annealing temperature. The increase in bubble density at first results from residual hydrophilic reactions at the bonded interface, and the decrease in bubble density is attributed to the crystallization of the a-Ge film at the bubble position when higher a annealing temperature was applied (as discussed below).

Figures 27(b)–(e) show metalloscope images of the Si surfaces of the samples with secondary annealing after a pulling test of the bonded wafers. One can see that the Ge pit position is the bubble position. When the sample is annealed at higher temperature, the color of the bubble position, which is yellow at a lower annealing temperature, turns black. This is due to the crystallization of the a-Ge film at the bubble position, as shown in figure 28. When the sample is annealed at 350 °C, the a-Ge at the bubble position starts to crystallize and the a-Ge film out of the bubble position still shows amorphous phase. When the annealing temperature increases to 400 °C, the entire Ge film at the bonded interface has crystallized.

Figure 29 shows the TEM images of the Si bonded interface with a 90 nm thick Ge layer annealed at 400 °C for 20 h. One can see that the a-Ge at the a-Ge/a-Ge bonded interface crystallizes to poly-Ge and the a-Ge at the a-Ge/Si interface still shows amorphous phase. This indicates that the poly-Ge film at the Si/Si bonded interface can absorb the by-products (H_2 and H_2O) in the bubbles, leading to the disappearance of the bubbles at a higher annealing temperature (figure 26). We also simulated stress in the bonded wafer pairs, as shown in figure 30(a). One can see that the stress symmetrically distributes in the wafer pairs, and that the largest stress appears at the a-Ge/a-Ge interface. This reveals that the crystallization of the a-Ge starts from the a-Ge/a-Ge interface and extends to the a-Ge/Si interface, as shown in the inset of figure 30(a), due to the stress-induced crystallization of the a-Ge.

On the other hand, we cannot observe an oxide layer at the bonded interface, as shown in figure 29(b). The O element cannot be detected by the TEM energy dispersion spectrum (EDS), as shown in figure 30(b). This suggests that the bonded interface is an oxide-layer-free interface. The mechanism for the absence of the oxide layer at the bonded interface is shown in figure 31. Firstly, the oxide layer forms at the bonded interface due to the hydrophilic reaction. When the crystallization of the a-Ge occurs at the bonded interface, the atom migration becomes serious, the Ge atoms migrate into the oxide layer and the O atoms migrate into the Ge film, leading to the decomposition of the oxide layer.

We also investigated bubble density as a function of a-Ge layer thickness at 350 °C and 400 °C, as shown in figures 32 and 33. One can see that when the samples were annealed at

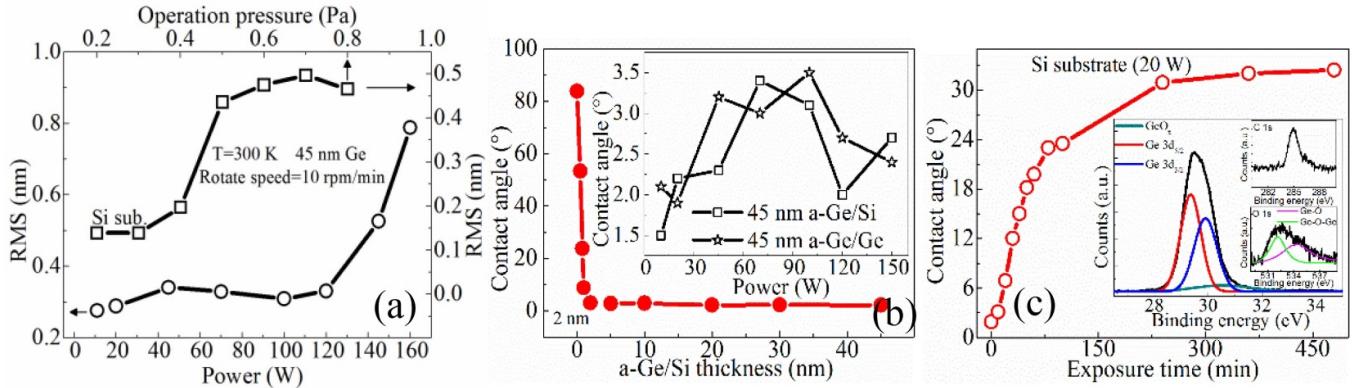


Figure 25. (a) RMS of a-Ge layer versus sputtering power and operation pressure. (b) Contact angle versus a-Ge layer thickness. Inset shows the contact angle versus sputtering power. (c) Contact angle versus exposure time. Inset shows the x-ray photoelectron spectroscopy (XPS) curves of the a-Ge surface. (a)–(c) Reprinted from [125], with the permission of AIP Publishing.

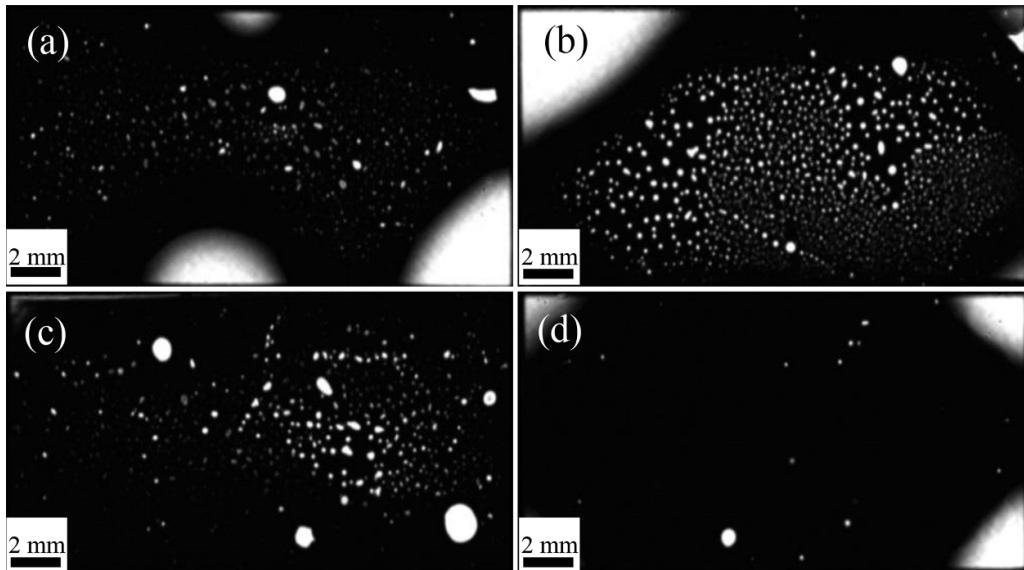


Figure 26. SAM images of Si bonded wafer pairs annealed at (a) 350 °C for 10 h, (b) 350 °C for 10 h/300 °C for 10 h, (c) 350 °C for 10 h/350 °C for 10 h, and (d) 350 °C for 10 h/400 °C for 10 h. Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

350 °C for 20 h, the bubble density decreases slightly with the increase of the a-Ge layer thickness. However, bubbles still exist at the bonded interface, even for the sample with a 100 nm thick a-Ge layer. Only small bubbles (0–0.01 mm² and 0.01–0.1 mm²) were observed at 350 °C with the increase of the a-Ge layer thickness, as shown in figure 34(a). In addition, as shown in figure 34(b), the bonding strength (7–8 Mpa) remains almost unchanged with the increase in a-Ge layer thickness. This is due to the fact that the crystallization of the a-Ge film is insufficient at 350 °C, so the bubbles cannot be totally absorbed, leading to lower bonding strength in the Si wafer pairs. For the samples annealed at 400 °C for 20 h, the bubble density decreases with the increase in a-Ge layer thickness. The bubbles almost disappear when the a-Ge layer thickness reaches 30 nm. Not only the smaller bubbles, but also the large bubbles (>0.1 mm²), as shown in figure 34(a), can

be totally absorbed at 400 °C with the increased a-Ge layer thickness, due to sufficient crystallization of the a-Ge at 400 °C. The crystallization of the a-Ge also leads to an increase in bonding strength (16–18 Mpa).

In order to reveal the repair process of bubbles during annealing, a pulling test was conducted for the sample annealed at 350 °C for 20 h, as shown in figure 35(a). One can see that some bubbles have crystallized and some bubbles still show amorphous phase. The Raman shift of the bubble in figure 35(c) is shown in figure 35(e). It shows that the crystallization of the a-Ge film begins at the center of the bubbles and expands to the edge of the bubble. This is consistent with the bubble evolution shown in figure 36. The bubble starts to darken from the center in the SAM image, until finally the entire bubble becomes a bonded region.

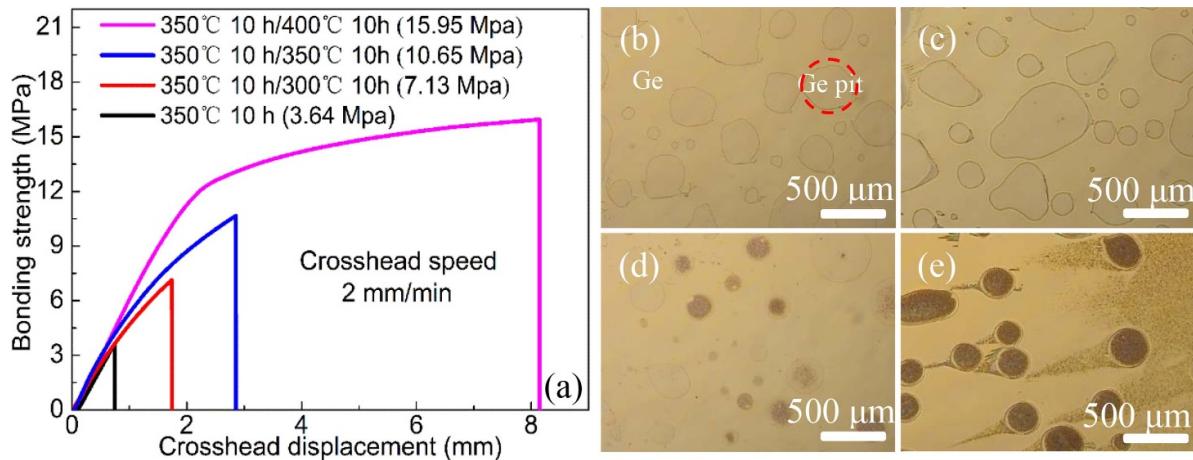


Figure 27. (a) Bonding strength of Si bonded wafer pairs annealed at different temperatures. Metalloscope images of the bonded interfaces of the samples annealed at (b) 350 °C for 10 h, (c) 350 °C for 10 h/300 °C for 10 h, (d) 350 °C for 10 h/350 °C for 10 h, and (e) 350 °C for 10 h/400 °C for 10 h after the pull test. Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

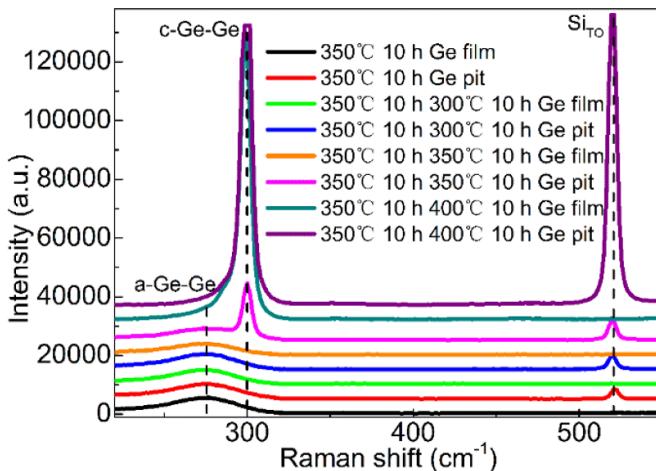


Figure 28. Raman spectrum of the bonded interfaces of the Si bonded wafer pairs annealed at different temperatures. Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

The sputtered a-Ge film was immersed into DI water and was then spin-dried before bonding in the experiments shown above. We also fabricated bonded Si/Si samples using the direct contact method in which the sputtered a-Ge was not immersed in DI water, as shown in figure 37. One can see that after annealing at 350 °C for 20 h, lots of bubbles appear at the bonded interface in the sample whose a-Ge film was immersed in DI water, while no bubbles appear at the bonded interface for the sample whose a-Ge film was not immersed in DI water. This is attributed to the fact that the a-Ge surface absorbed few -OH groups when the a-Ge film was not immersed in DI water, leading to a decrease in hydrophilic reactions at the bonded interface, and the disappearance of bubbles.

We also studied the effect of annealing temperature on the I-V curves of n-Si/n-Si bonded wafer pairs, as shown in figure 38(a). One can see that the I-V curves of the wafer pairs are all linear. This indicates that the barrier at the bonded

interface is low enough for carrier transport. With an increase in the annealing temperature, the current increases, indicating a decrease in resistance at the bonded interface. When the annealing temperature reaches 400 °C, the current of the bonded wafer pairs is close to that of bulk n-Si. This is attributed to the crystallization of the a-Ge film with an increase in annealing temperature. This is suggestive of low resistance at the n-Si/n-Si bonded interface.

We also studied the effect of a-Ge layer thickness on the I-V curves of p-Si/n-Si junction annealed at 350 °C for 20 h and 400 °C for 20 h, as shown in figures 38(b) and (c), respectively. One can see that the I-V curves all exhibit rectification characteristics. This indicates that the carriers at the bonded interface can transport well at the bonded interface. With an increase in the thickness of the a-Ge layer, both reverse current and forward current decrease. This is attributed to an increase in resistance at the bonded interface due to the insertion of the thick a-Ge layer. On the other hand, the reverse current for the sample annealed at 400 °C for 20 h is higher than that annealed at 350 °C for 20 h. This can be ascribed to the increase in electrical conductivity induced by the crystallization of the a-Ge film.

Overall, the semiconductor interlayer bonding technique can achieve Si/Si wafer bonding with a high bonding strength and a bubble-free bonded interface. This method is low-cost and easy to accomplish. In addition, the interface oxide layer formed by the hydrophilic reaction can be totally decomposed due to the crystallization of the semiconductor interlayer. The bonded homojunction can achieve a linear I-V curve comparable to that of bulk material. However, due to the insertion of the semiconductor interlayer, the resistance at the bonded interface increases, leading to a decrease in the reversed current and forward current of the device. Although the crystallization of the semiconductor interlayer may lead to a decrease in interface resistance, the thickness of the semiconductor interlayer should be as low as possible.

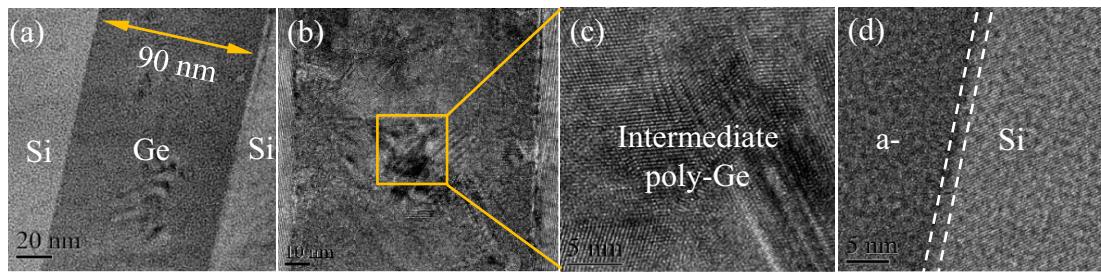


Figure 29. TEM images of the Si/Si bonded interfaces with 45 nm a-Ge layer. Reprinted from [125], with the permission of AIP Publishing.

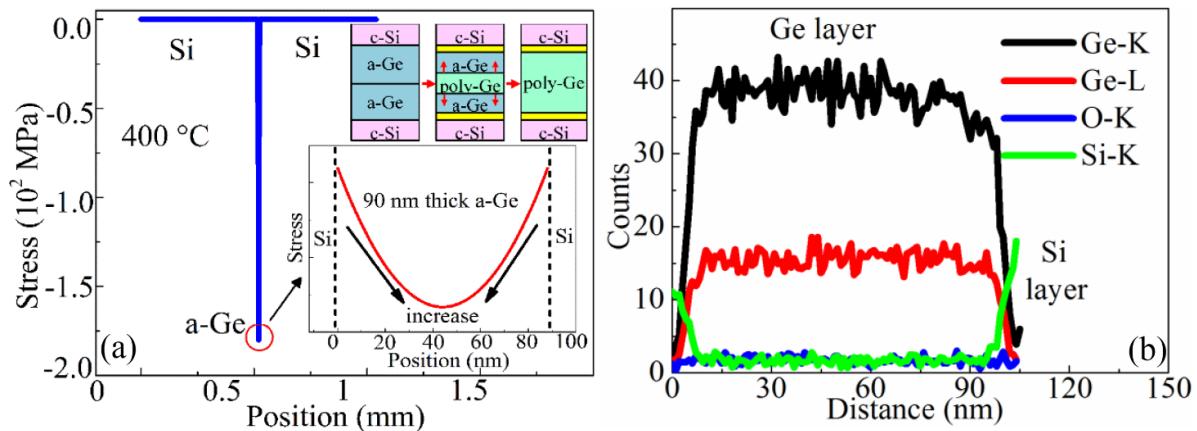


Figure 30. (a) Simulation results of the stress distribution in Si/Si bonded wafers annealed at 400 °C. (b) EDS curves of the Si/Si bonded interface. (a), (b) Reprinted from [125], with the permission of AIP Publishing.

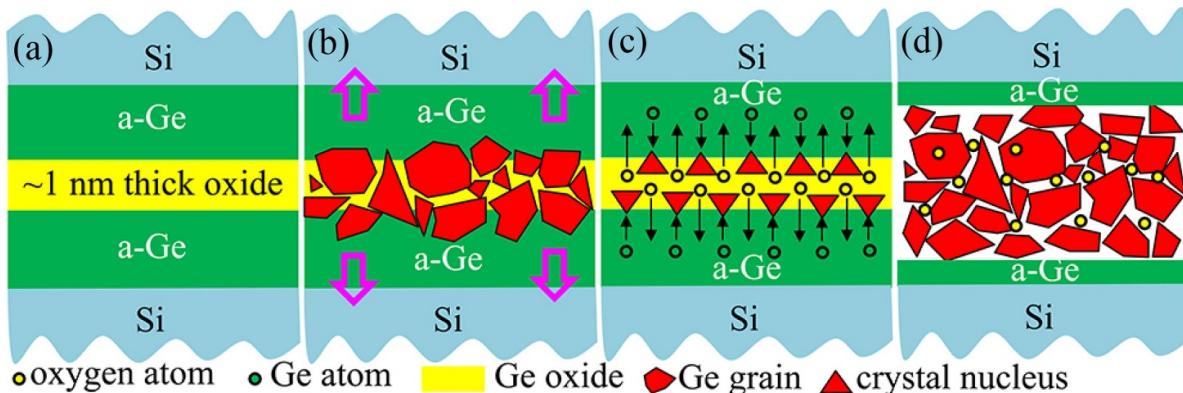


Figure 31. (a), (b) Crystallization process of a-Ge at the Si/Si bonded interface. (c), (d) Kinetic process of the Ge and oxygen atoms at the Si/Si bonded interface. (a)–(d) [127] (2019) © (Springer Nature). With permission of Springer.

3. The process of Ge/Si wafer bonding

Compared to homogeneous Si/Si wafer bonding, the investigation of heterogeneous Ge/Si wafer bonding is relatively recent, and few groups have focussed on the study of Ge/Si wafer bonding and its applications in the photoelectric field. Si-based Ge film fabrication is mainly based on epitaxial growth. Thus, the wafer bonding technique is not widely used in the semiconductor technology. The reason for fewer available works on the subject of Ge/Si wafer bonding can be ascribed to the following five reasons: (1) there is a 4.2% lattice mismatch between Ge and Si materials. If Si and

Ge wafer surfaces are not properly treated before bonding, misfit dislocations may diffuse into the Ge wafer. (2) There is a thermal expansion coefficient mismatch between Ge and Si materials (Ge [132]: $5.5 \times 10^{-6} \text{ K}^{-1}$ and Si [133]: $2.6 \times 10^{-6} \text{ K}^{-1}$). If the annealing temperature is not well controlled, the thermal stress may be large enough to trigger separation or to crack the bonded sample during annealing due to the thickness of the bulk wafer (hundreds of micrometers). (3) The unstable oxides of Ge materials, such as GeO and Ge₂O, form easily on the clean Ge surface, leading to instability in the Ge/Si bonded interface. Although the HF solution can remove most stable Ge oxide (GeO₂) on the Ge surface, the

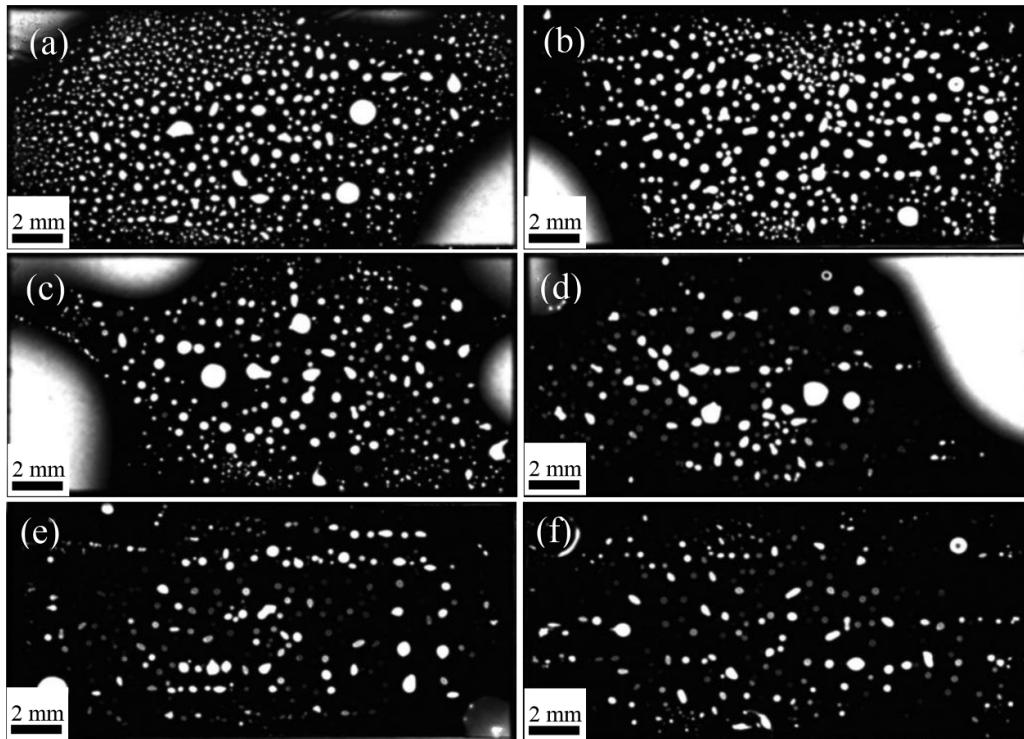


Figure 32. SAM images of the Si bonded wafer pairs with (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 30 nm, (e) 45 nm, and (f) 70 nm thick a-Ge layer annealed at 350 °C for 20 h. Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

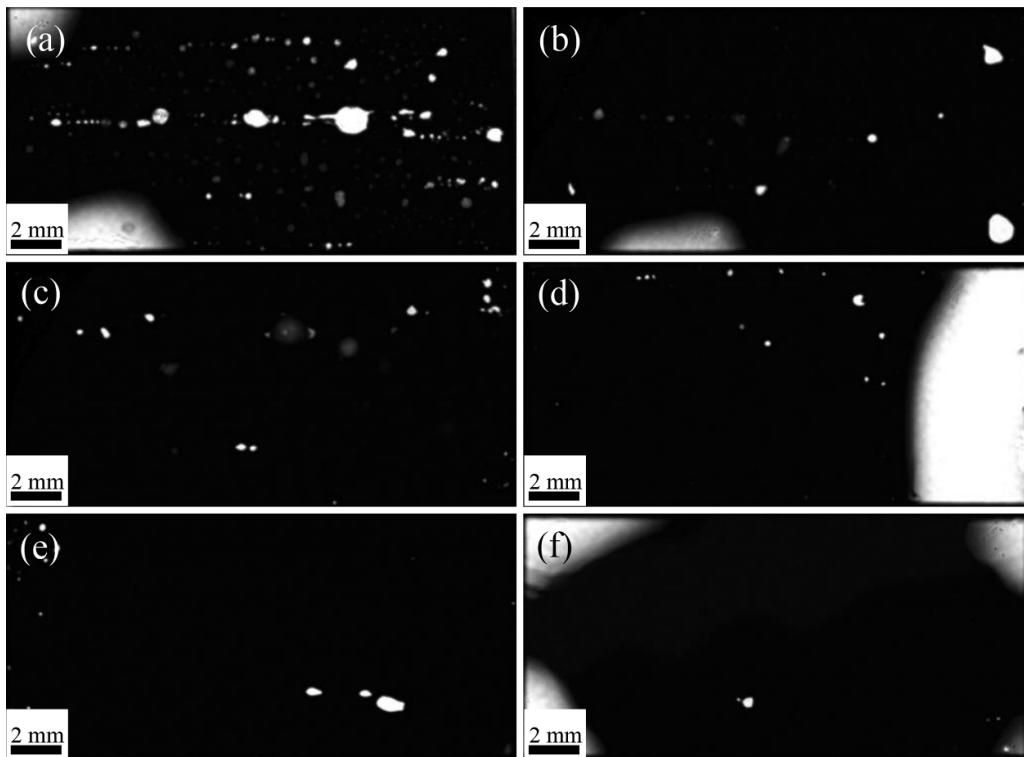


Figure 33. SAM images of the Si bonded wafer pairs with (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 30 nm, (e) 45 nm, and (f) 70 nm thick a-Ge layer annealed at 350 °C for 20 h. Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

unstable oxide is difficult to remove cleanly. The unstable oxide can evaporate and break existing Ge/Si bonds during higher temperature annealing (≥ 400 °C), resulting in the

formation of interface bubbles. (4) Although bonding strength may increase when high-temperature annealing is conducted, the wafers may separate or crack during annealing, and

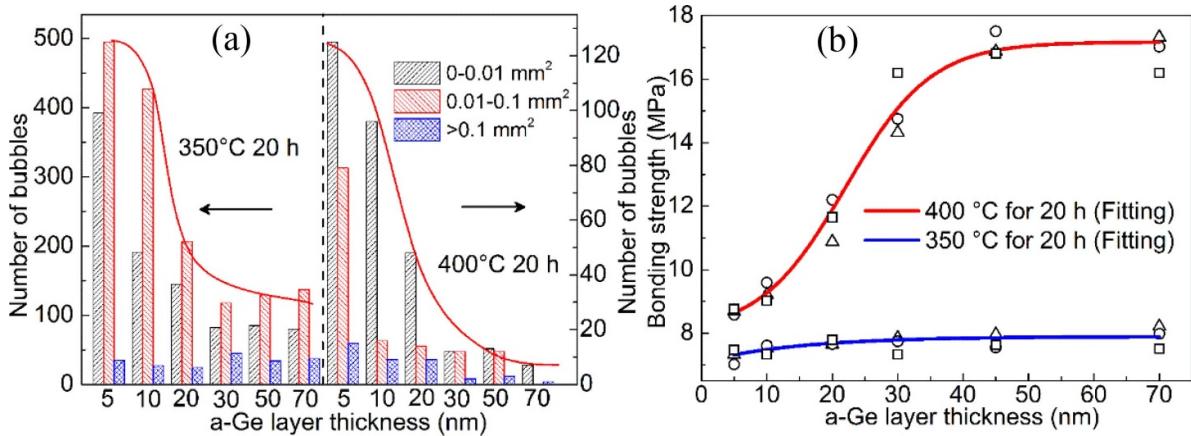


Figure 34. (a) Statistical histogram of the area of all the bubbles annealed at different temperatures. (b) Bonding strength of three sets of wafer pairs with different a-Ge layer thicknesses, annealed at 350 °C and 400 °C for 20 h. (a), (b) Reproduced from [126]. © IOP Publishing Ltd. All rights reserved.

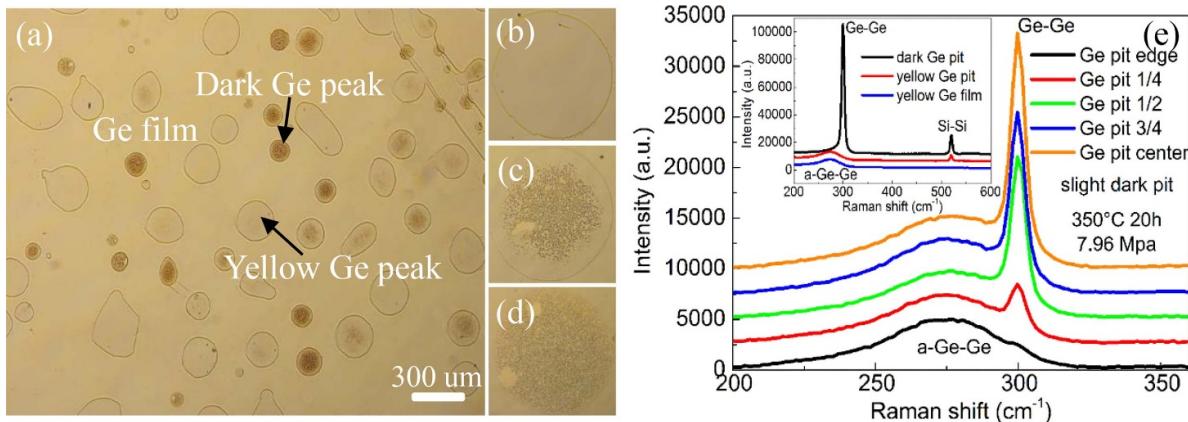


Figure 35. (a) Optical microscope image of the bonded interface of the sample annealed at 350 °C for 20 h. (b)–(d) Enlarged drawing of (a). (e) Raman spectrum of the Ge pit at different places shown in (d). Inset shows the Raman spectrum of the Ge film and Ge pit shown in the figure. (a)–(e) Reprinted from [128], Copyright (2018), with permission from Elsevier.

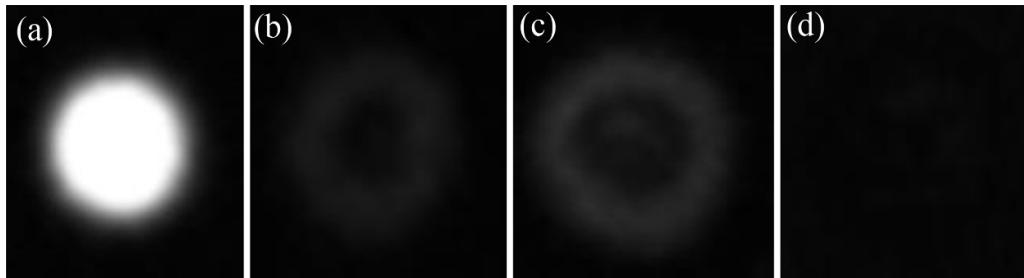


Figure 36. SAM image of a single bubble at different crystalline stages. Reprinted from [128], Copyright (2018), with permission from Elsevier.

Ge/Si interdiffusion is serious at high temperature. Thus, it is difficult to obtain a desired Ge/Si bonding interface at higher annealing temperatures. However, the bonding strength of the Ge/Si wafer pairs annealed at a lower temperature is relatively lower than that annealed at higher temperatures. This leads to unsatisfied electrical properties at the bonded interface. (5) The most important reason is that an oxide layer formed by

hydrophilic or hydrophobic reactions exists at the Ge/Si interface in most Ge/Si wafer bonding techniques. The existence of the oxide layer at the bonded interface restricts carrier transport at the bonded interface and leads to an increase in the RC time constant. Thus, the 3 dB-bandwidth may decrease. This factor limits the use of this wafer bonding technique in the optoelectronic field.

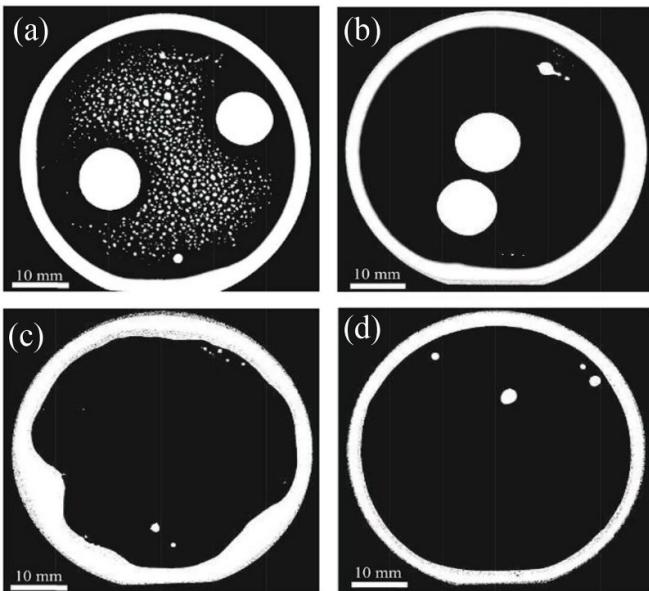


Figure 37. SAM images of bonded wafer pairs annealed at (a) 350 °C for 20 h with DI water immersion, (b) 400 °C for 20 h with DI water immersion, (c) 350 °C for 20 h without DI water immersion, and (d) 400 °C for 20 h without DI water immersion. Reproduced from [129]. © IOP Publishing Ltd. All rights reserved.

Although many challenges need to be overcome with regard to Ge/Si wafer bonding at present, there are four distinct advantages of this technique which show potential as an alternative to the traditional epitaxy technique. (1) Ge/Si wafer bonding can be carried out at low temperatures ≤ 300 °C. This is much lower than those used in the epitaxy technique (deoxygenation of the Si substrate at >850 °C and epitaxial growth of the Ge film at ~ 600 °C). (2) Low-temperature Ge/Si wafer bonding can achieve a TD-free Ge/Si bonded interface due to the restriction of nucleation and the diffusion of misfit dislocations at low temperature. (3) Ge/Si wafer bonding retains the crystalline quality and photoelectric characteristics of bulk Ge. (4) Ge/Si wafer bonding may be combined with the Smart-Cut technique to fabricate an Si-based Ge film whose quality may be considered comparable with bulk Ge.

Proposed techniques for achieving Ge/Si wafer bonding currently include: wet wafer bonding, which is divided into hydrophilic wet wafer bonding and hydrophobic wafer bonding, plasma-activated bonding, dry wafer bonding, high-vacuum surface-activated bonding, and semiconductor interlayer bonding.

3.1. Hydrophilic wet wafer bonding

For hydrophilic wet wafer bonding, after cleaning the Ge and Si wafers, they were bonded in DI water and post-annealed for wafer bonding. Similar to Si/Si wafer bonding, high-temperature annealing of Ge/Si wafer pairs was investigated by Kanbe *et al* [134–137] firstly. After cleaning the Si and Ge wafers in the organic solution, the wafer surfaces were deoxidized using the HF solution. Then the wafers were further

cleaned using $H_2SO_4:H_2O_2:H_2O$ and $HCl:H_2O$ solutions, respectively. After cleaning, the Si and Ge wafer surfaces both exhibit hydrophilic qualities. Subsequently, the wafers were contacted to each other in DI water and annealed at 880 °C in H_2 atmosphere for 90 min to enhance bonding strength. TEM images of the Ge/Si bonded interface are shown in figures 39(a) and (b).

One can see that a transition layer with the thickness of several tens of nanometers appears at the Ge/Si bonded interface and some island-like structures appear in the transition layer. These island-like structures result from the interdiffusion of Ge and Si atoms at the bonded interface during high-temperature annealing. In addition, dislocation lines along the [110] direction exist in the island-like structures, and distortion of the lattice at some positions on the bonded interface was observed. These abnormal features are attributed to the lattice mismatch and the thermal mismatch between Ge and Si. On the other hand, an obvious oxide layer appears at the Ge/Si bonded interface, as shown in figures 39(b) and (c). Moreover, a serious interdiffusion exists at the bonded interface; a diffusion depth of ~ 50 nm was detected. The EDS curve presents a O atom distribution at the Ge/Si bonded interface, indicating the existence of Si and Ge oxide layers at the bonded interface.

Kanbe *et al* fabricated a Ge/Si device based on this Ge/Si bonding method, as shown in figure 40(a). Although the device achieves a quantum efficiency of 40% at near-infrared wave range, the dark current of the device is too large, as shown in figure 40(b). The dark current reaches 0.5 mA when the reverse bias increases to 10 V. The large dark current of the device may be attributed to the interdiffusion and the formation of dislocations at the bonded interface.

Following their study of high-temperature Ge/Si wet wafer bonding, Kanbe *et al* also study the low-temperature annealing of wet-bonded Ge/Si wafer pairs at 250 °C and 350 °C for 12–48 h. TEM images of the Ge/Si bonded interface are shown in figure 41(a). One can see that compared to the Ge/Si interface annealed at high temperature, the quality of the bonded interface annealed at low-temperature was improved. Misfit dislocations and TDs cannot be observed clearly at the bonded interface. Only a 3–5 nm thick amorphous transition layer appears at the bonded interface. In addition, this layer is non-uniform. This may be due to the introduction of excessive H_2O at the bonded interface. C and O atoms were detected at the bonded interface, as shown in figure 41(b), indicating the existence of contaminants and an oxide layer at the bonded interface. In addition, interdiffusion was observed at the bonded interface. The Ge/Si device based on this wafer bonding method also exhibits large dark current, as shown in figure 41(c). This may be due to low bonding strength when annealed at low temperature, and the existence of contaminants at the bonded interface.

Overall, whether high-temperature annealing or low-temperature annealing, the hydrophilic Ge/Si wet wafer bonding cannot achieve a good Ge/Si bonded interface. A thick oxide layer appears at the Ge/Si bonded interface due to bonding in DI water, and excessive hydrophilic reactions at the Ge/Si bonded interface. High-temperature annealing triggers the formation of TDs and Ge/Si intermixing at the bonded

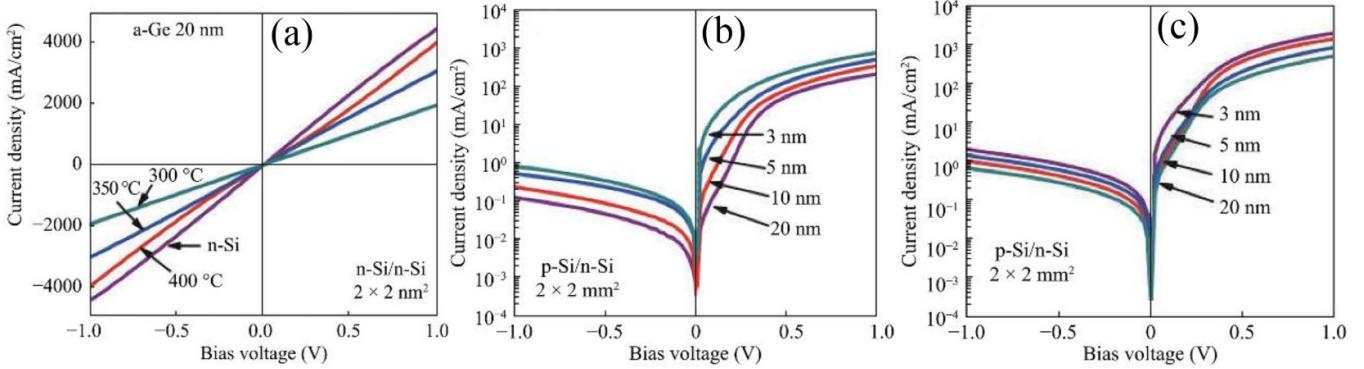


Figure 38. (a) I-V characteristics of n-Si/n-Si bonded wafers (20 nm) annealed at different temperatures. I-V curves of the Si-based PN junction with different a-Ge interlayer thicknesses, annealed at (a) 350 °C for 20 h and (b) 400 °C for 20 h. Reproduced from [129]. © IOP Publishing Ltd. All rights reserved.

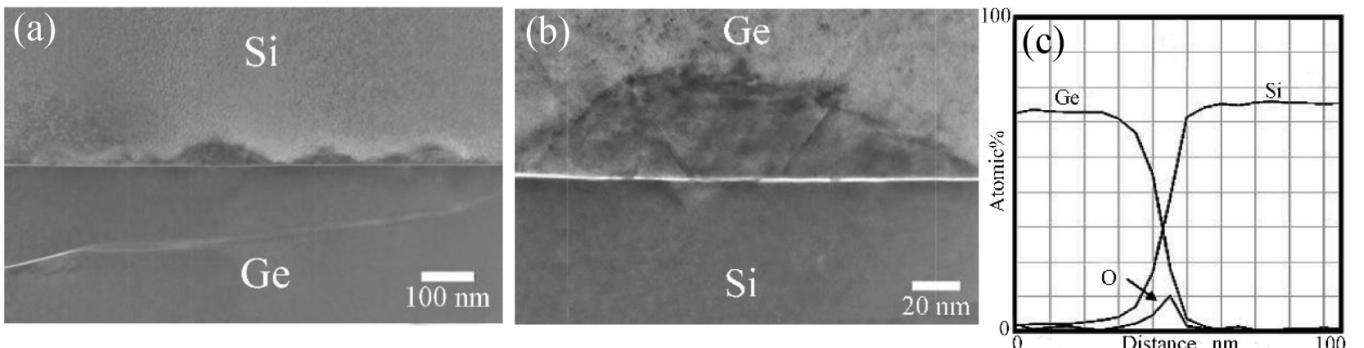


Figure 39. (a), (b) TEM images of the Ge/Si bonded interface annealed at high temperature. (c) EDS curves of the Ge/Si bonded interface. Reprinted from [134], with the permission of AIP Publishing.

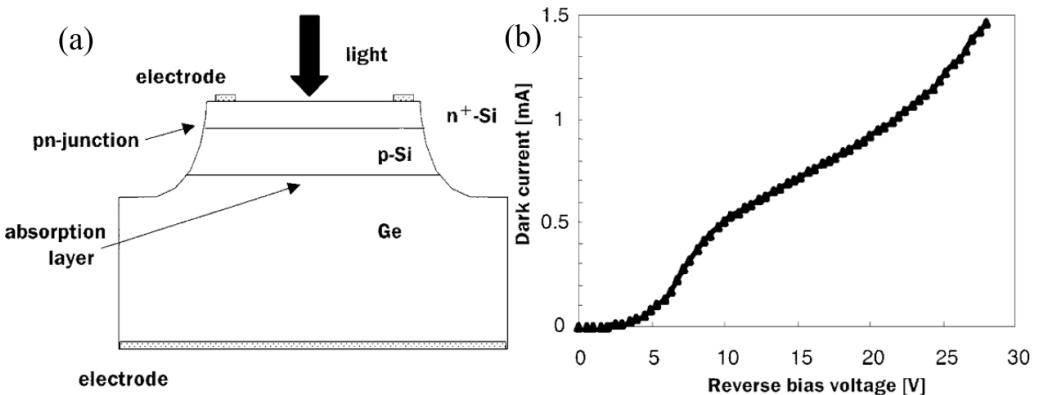


Figure 40. (a) Ge/Si device fabricated based on the Ge/Si wafer pairs annealed at high temperature. (b) I-V curve of this device. (a), (b) Reproduced from [135]. © IOP Publishing Ltd. All rights reserved.

interface, while low-temperature annealing suffers from low bonding strength, resulting in the large dark current of the Ge/Si device.

3.2. Hydrophobic wet wafer bonding

In recent years, Lee *et al* [138, 139] investigated the crystallization of the a-Ge film on a SiO₂ isolation layer induced by the Si window to achieve Ge/Si wafer bonding in a BOE solution.

The induction process of the a-Ge film and the Ge/Si wafer bonding process are shown in figure 42. Firstly, a SiO₂ isolation layer was deposited on the Si substrate. Then, a seed Si window for the crystallization of the a-Ge was opened on the SiO₂ isolation layer. After that, a 300 nm thick a-Ge layer was deposited on the Si substrate and then a SiO₂ capping layer was deposited on the a-Ge layer. Finally, the Si substrate was annealed at 950 °C for 4 s using rapid thermal annealing to trigger the crystallization of the a-Ge film.

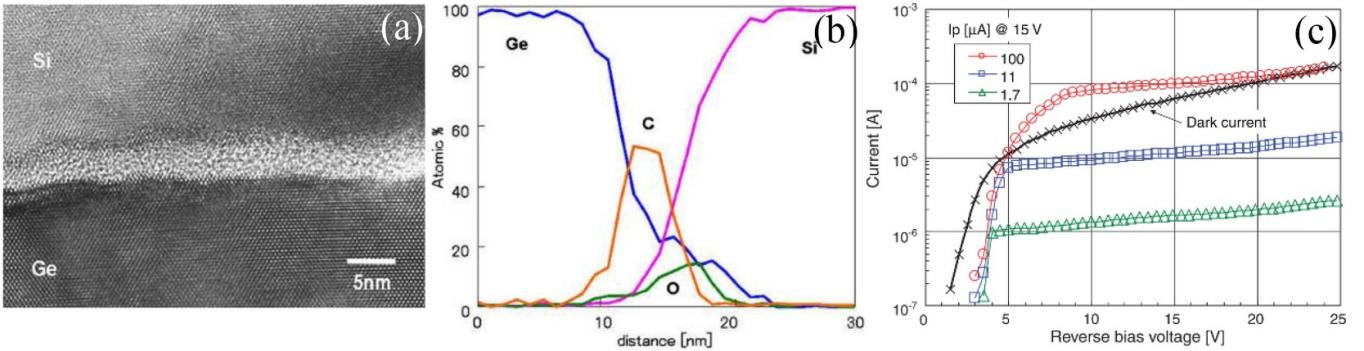


Figure 41. (a) TEM image of Ge/Si wafer pairs annealed at low temperature. (b) EDS curves of the bonded interface. (a), (b) [136] (2010) © (Springer Nature). With permission of Springer. (c) I-V curves of the Ge/Si device. (a), (b) Reproduced from [137]. © IOP Publishing Ltd. All rights reserved.

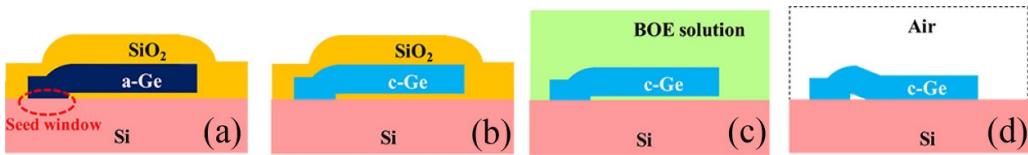


Figure 42. Process of Ge/Si hydrophobic wet wafer bonding. © (2012) IEEE. Reprinted with permission from [139].

After annealing, the Si substrate was immersed into the BOE solution to remove all the SiO_2 on the substrate. The Ge film was attached to the Si substrate by van der Waals force in the BOE solution. Finally, the Si substrate was taken out of the BOE solution and annealed at 400 °C for 1 h to achieve Ge/Si bonding. Figure 43 shows TEM images of the Ge/Si bonded interface. One can see that a 7 nm thick amorphous transition layer appears at the bonded interface. The element distribution in the transition layer is Si:54%, Ge:14%, and O:32%. This indicates that the transition layer is an oxide layer. In addition, the a-Ge turns into a single-crystal Ge after annealing. Note that the crystallization of the a-Ge film not only appears at the Si window, but also in the Ge film on the SiO_2 layer. The Ge film on the SiO_2 layer is demonstrated to be TD-free; misfit dislocations and TDs only exist at the Si window.

Lee *et al* fabricated a waveguide Ge/Si p-i-n photodiode based on this bonding method, as shown in figure 44(a). The dark current of this photodiode is shown in figure 44(b). One can see that the I-V curve shows rectification characteristics. However, the dark current sharply increases with the increase in the reverse bias, and the saturation characteristic is not so satisfied. In addition, the forward current is lower, indicating the existence of large series resistance. This may be due to the poor quality of the Ge layer and the unsatisfied Ge/Si bonded interface. The responsivity of the photodiode is shown in figure 44(c). At -2 V reverse bias, the responsivity of the device at a wavelength of 1310 nm is only 0.3 A W^{-1} . In addition, the Ge film thickness is 300 nm, and the calculated 3 dB-bandwidth is dozens of GHz [140]. However, the 3 dB-bandwidth of this device is only 16 GHz, as shown in figure 44(d), which is much lower than that of the epitaxial waveguide Ge/Si p-i-n photodiode [141].

Overall, although hydrophobic wet wafer bonding can restrict the occurrence of TDs in the Si window, the point

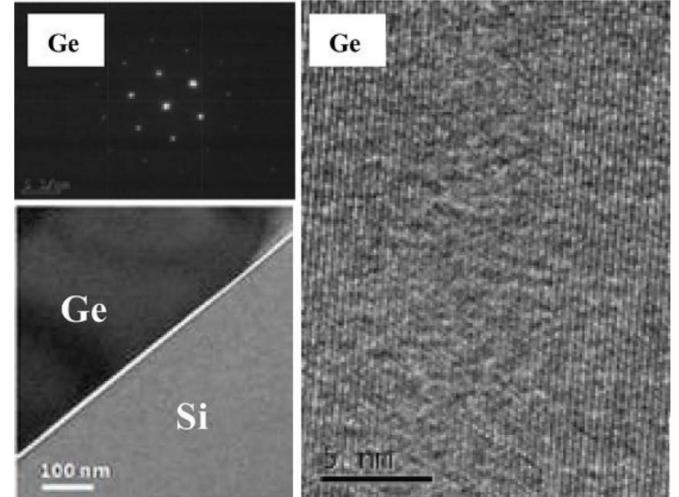


Figure 43. TEM images of the Ge/Si bonded interface fabricated by hydrophobic wet wafer bonding. © (2012) IEEE. Reprinted with permission from [139].

defects in the re-crystalline Ge layer on the SiO_2 isolation layer cannot be eliminated, leading to a deterioration in device performance.

3.3. Plasma-activated bonding

Byun *et al* [142–144] and Gity *et al* [145–147] systematically investigated low-temperature Ge/Si wafer bonding based on a free radical surface treatment. O and N free radicals were used to activate wafer surfaces to be hydrophilic. The wafer bonder for the hot-pressed treatment of contacted wafer pairs was used to enhance bonding strength and achieve pre-bonding. Firstly, after Si and Ge wafers had been cleaned, the wafer surfaces

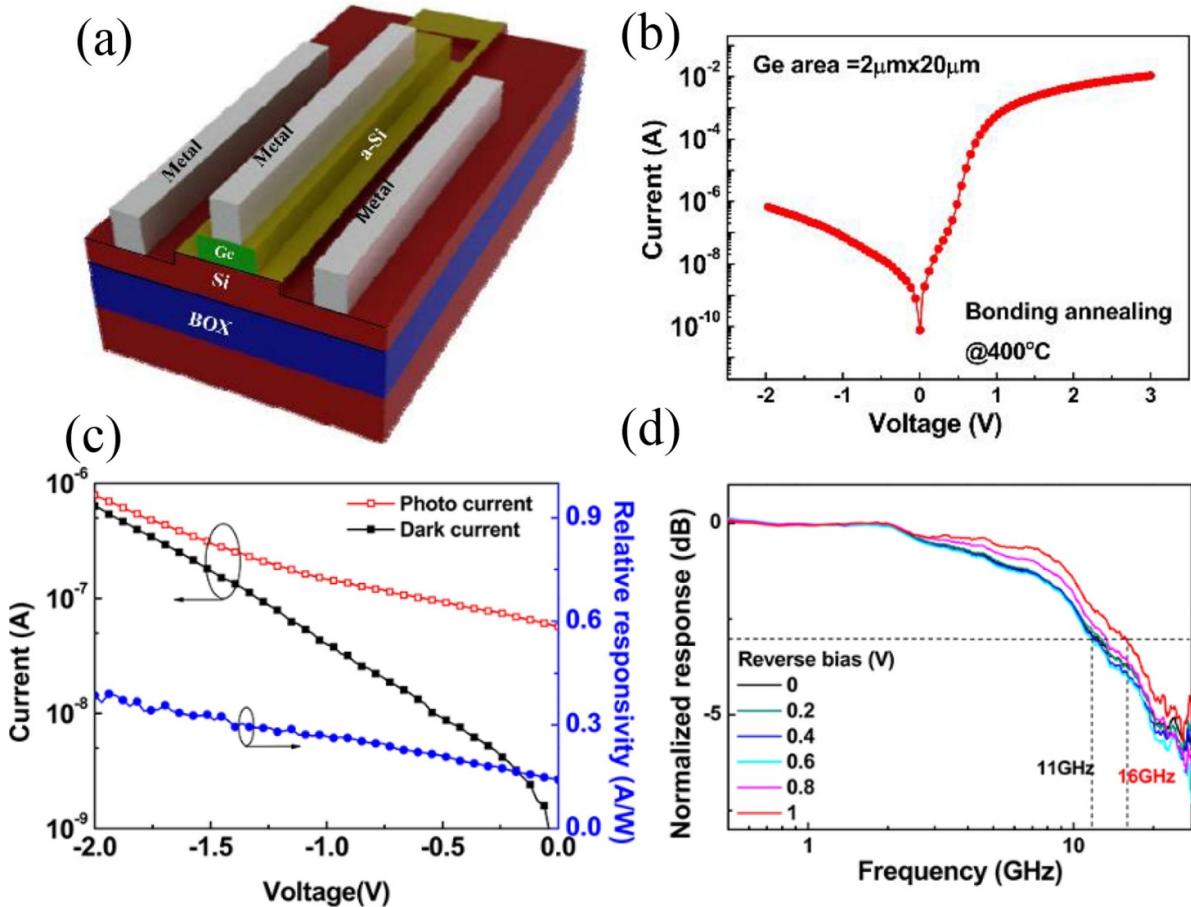


Figure 44. (a) Schematic diagram of the Ge/Si p-i-n photodiode based on hydrophobic wet wafer bonding. (b) Dark current of the device. (c) Photocurrent of the device. (d) 3 dB-bandwidth of the device. (a)–(d) © (2012) IEEE. Reprinted with permission from [139].

were activated by the O or N free radicals. Next, the wafers were contacted to each other and put into the wafer bonder for hot-pressed treatment. The wafers were firstly bonded under a force of 1 kN (5 min) at a chamber pressure of 10^{-5} mbar, and they were then annealed *in situ* at 100 °C for 1 h under a force of 500 N. Finally, an ex situ annealing at 200 °C and 300 °C for 24 h was conducted to achieve Ge/Si wafer bonding with a high bond strength. O and N free radical surface treatment can form stable GeO₂ on the Ge wafer due to the oxidation of the Ge surface, and enhance hydrophilic qualities, respectively, as shown in figure 45.

SAM images of Ge/Si wafer pairs treated by different free radicals are shown in figure 46. One can see that lots of bubbles appear at the Ge/Si bonded interface in the sample without free radical treatment, while an obvious decrease in bubble density was observed at the Ge/Si bonded interface with both O and N free radical treatment. In addition, the bubble density at the Ge/Si bonded interface treated by N free radicals is lower than that treated by O free radicals. As is well-known, the oxide layer at the bonded interface can transfer by-products out of the wafer pairs; that is, the thicker the oxide layer at the bonded interface, the fewer the by-products trapped at the bonded interface. Figure 47 shows the TEM images of the Ge/Si bonded interface treated by different free radicals. One can see that

the oxide layer thickness at the bonded interface without the plasma treatment is 1.3 nm, and that treatment with the O and N free radicals gives a thickness of 1.6 and 2.2 nm, respectively. Thus, bubble density at the Ge/Si bonded interface in the sample treated by the N free radical is lowest. This is consistent with the SAM images.

Gity *et al* exfoliated a 700 nm thick Si-based Ge film by means of plasma-activated Ge/Si wafer bonding and the Smart-Cut technique. They also fabricated a p⁻Ge/n⁺-Si heterojunction based on this exfoliated Ge film, as shown in figure 48(a). The dark current of this p⁻Ge/n⁺-Si heterojunction is shown in figure 48(b). One can see that although the p⁻Ge/n⁺-Si heterojunction shows the rectification characteristic, the forward current is lower, indicating the existence of high resistance at the bonded interface. In order to enhance the forward current, the heterojunction was annealed at 400 °C for 30 min. As shown in figure 48(b), the forward current increases after post-annealing, while the dark current slightly increases. The on/off current ratio of the p⁻Ge/n⁺-Si heterojunction with 100 μm diameter mesa at -0.5 V reaches 5×10^4 , and ideality factors of 5.48 and 2.28 were achieved before and after post-annealing.

The activation energies before and after post-annealing are shown in figure 49(a). One can see that the activation energy

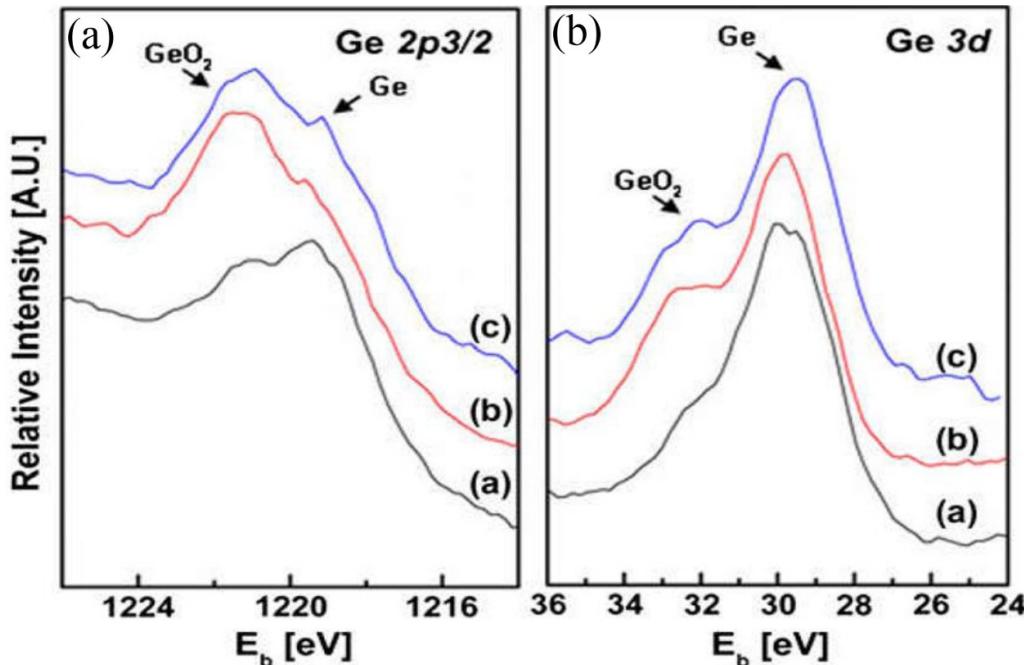


Figure 45. XPS curves of Ge surfaces treated by (a) O and (b) N free radicals. Reprinted from [142], Copyright (2012), with permission from Elsevier.

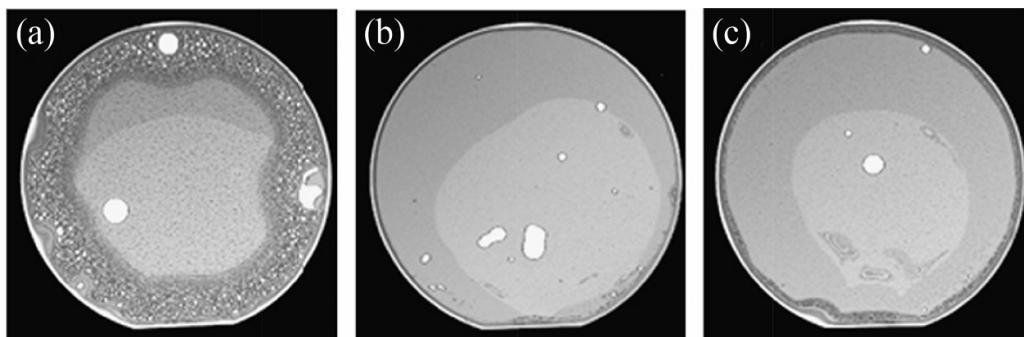


Figure 46. SAM images of the Ge/Si bonded interfaces (a) without free radical treatment, (b) with O free radical treatment, and (c) with N free radical treatment. Reprinted from [142], Copyright (2012), with permission from Elsevier.

of 0.33 eV of the heterojunction was obtained before post-annealing. This value is close to half of the Ge band gap. Thus, the mechanism for the generation and recombination of the carriers is dominant in the p⁻Ge/n⁺-Si heterojunction before post-annealing. However, the activation energy of the heterojunction is ~0.013 eV after post-annealing. This is much lower than that of the Ge band gap. Thus, the band-to-band tunneling (BBT) mechanism may be responsible for carrier transport at the heterojunction after post-annealing, as shown in figures 49(b) and (c).

Overall, the bubble density at the Ge/Si bonded interface can be decreased using plasma-activated Ge/Si wafer bonding, while the bubbles cannot be totally eliminated due to the hydrophilic reaction at the bonded interface. More importantly, the oxide layer still exists at the bonded interface even if surface activation is applied. The carriers at the bonded interface can only transport by tunneling. This is not good for the fabrication of high-performance Ge/Si devices.

3.4. Dry wafer bonding

The Ge and Si wafers were contacted in a BOE solution using the wet wafer bonding method described above. In other words, the bonded Si wafer is the original Si substrate after the corrosion of the SiO₂. However, in dry wafer bonding, after the corrosion of the SiO₂, thermal release tape was used to transfer the thin film on the original Si substrate to a new substrate. Dry wafer bonding can be divided into two parts. One is direct thin film transfer, and the other is aligned thin film transfer. Kiefer *et al* [148] investigated direct thin film transfer for Ge/Si wafer bonding. They intended to transfer a 200 nm thick Si thin film in SOI substrate to a Ge wafer surface. Firstly, the Si thin film was defined and etched, and then the SOI wafer was immersed into the HF solution to corrode the BOX layer. After corrosion, the Si thin film was attached to the Si substrate by weak van der Waals force. Next, the Si thin film was peeled off from the Si substrate using thermal release tape, and transferred to the Ge

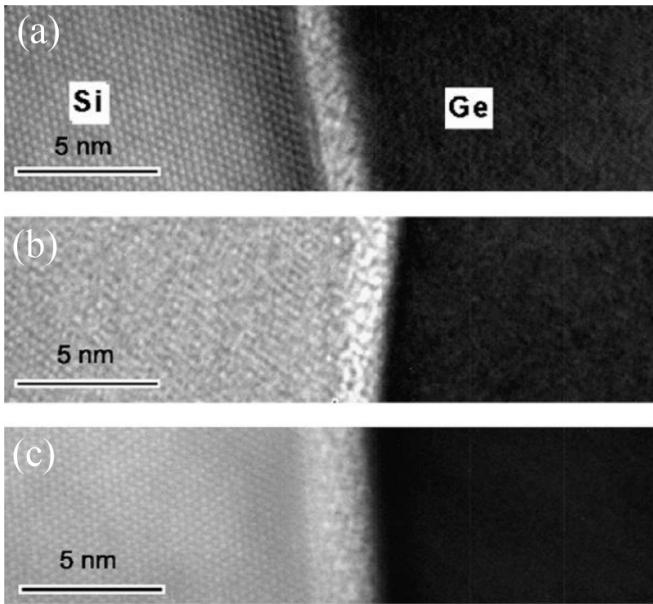


Figure 47. TEM images of the Ge/Si bonded interfaces (a) without free radical treatment, (b) with O free radical treatment, and (c) with N free radical treatment. Reprinted from [142], Copyright (2012), with permission from Elsevier.

substrate after the wafer was removed from the HF solution. Finally, the Ge wafer was annealed at 400 °C for 30 min to enhance bonding strength.

This bonding method is also a form of hydrophobic bonding due to the fact that the Si thin film surface was passivated by H bonds before bonding. The optical microscope image of the transferred Si thin film is shown in figure 50(a). The TEM image of the Ge/Si bonded interface is shown in figure 50(b). One can see that no TDs were observed at the Ge/Si bonded interface. Only a thin amorphous transition layer (1.2 nm) appears at the bonded interface. The absence of TDs can be attributed to the thin Si film and the low temperature annealing. However, the 1.2 nm thick amorphous transition layer introduces a barrier at the Ge/Si bonded interface, restricting the transport of carriers, as shown in figure 51. One can see that the carrier transport mechanism at the bonded interface is the barrier tunneling mechanism. This is similar to that of the Ge/Si bonded interface fabricated by plasma-activated bonding.

Liu *et al* [149, 150] recently achieved Ge/Si micro-ribbon bonding by means of aligned thin film transfer. The bonding process is shown in figure 52. Firstly, the SOI substrate with 70 nm thick n⁺-top Si and the GOI with 60 nm thick p⁻-top Ge were defined and etched to form Si and Ge ribbons on the SiO₂, respectively. After that, the SOI and GOI were put into the HF solution to remove all the SiO₂, leaving Si and Ge ribbons on the Si substrate. Next, thermal release tape was used to transfer the Si ribbons onto the Ge ribbons to achieve the Ge/Si micro-ribbon bonding. Micro-ribbon alignment was conducted for this bonding method. This bonding method is also considered to be a hydrophobic bonding.

The TEM image of the Ge/Si bonded interface is shown in figure 53(a). One can see that TDs were not observed in the

Ge or Si thin film, while an oxide layer with a thickness of 3 nm was clearly observed at the Ge/Si bonded interface. This can also be identified from the EDS curves shown in figure 53(b). Liu *et al* fabricated a p⁻Ge/n⁺-Si heterojunction using this bonding method, as shown in figures 53(c) and (d). The dark current of this p⁻Ge/n⁺-Si heterojunction is shown in figures 54(a) and (b). One can see that the threshold voltage of this heterojunction is only 0.3 V, which is much lower than that for the Ge/Si heterojunction fabricated by the plasma-activated bonding. An ideality factor of 2.15 was achieved for this ribbon heterojunction, which is also much lower than that for the wafer-bonded heterojunction (5.48). However, the forward current of this device does not improve effectively. Due to the existence of the oxide layer at the bonded interface, the tunneling effect is dominant at the bonded interface, as shown in figure 54(c).

3.5. High-vacuum surface-activated bonding

High-vacuum surface-activated bonding method has been used in Si/Si wafer bonding. As described above, an Ar atom beam was emitted to clean and activate the Si surface. However, for high-vacuum surface-activated Ge/Si wafer bonding, an Ar ion beam was applied to activate the Si and Ge surface. The fabrication process is shown in figure 55. The surface activation of Ge and Si surfaces in high-vacuum was conducted after cleaning the wafers. Next, the wafers were aligned and bonded together in high vacuum ($\sim 10^{-6}$ Pa). Finally, the bonded wafer pairs were post-annealed to enhance bonding strength.

The TEM image of the Ge/Si bonded interface in the sample annealed at 150 °C for 2 h is shown in figure 56(a). One can see that TDs are absent at the Ge/Si bonded interface. Only a 0.9 nm thick amorphous transition layer appears at the Ge/Si bonded interface. The amorphous transition layer at the Ge/Si bonded interface is thinner than that occurring in Si/Si wafer bonding. This may be due to the fact that the damage to a surface bombarded by an Ar ion beam is less extensive than that caused by bombardment from an Ar atom beam. The SAM image of the Ge/Si bonded interface annealed at 150 °C for 2 h is shown in figure 56(b). One can see that few bubbles appeared at the bonded interface when low-temperature annealing was conducted. Razek *et al* also studied the effect of annealing temperature on the I-V curve of the Ge/Si heterojunction, as shown in figure 56(c). One can see that the threshold voltage of this heterojunction is only 0.3 V and an ideality factor of 1.1 for the heterojunction was achieved after post-annealing, indicating the excellent performance of the Ge/Si heterojunction.

3.6. Semiconductor interlayer bonding

Our group focused on the investigation of Ge/Si wafer bonding and Ge/Si layer exfoliation based on an a-Ge interlayer between Ge and Si wafers [125, 127, 152, 153]. Before bonding, we investigated the RMS of the a-Ge on the Ge substrate as a function of input power, as shown in figure 57(a). One can see that the variation trend of the curve is similar to that for the a-Ge film on the Si substrate. Finally, the a-Ge with RMS of

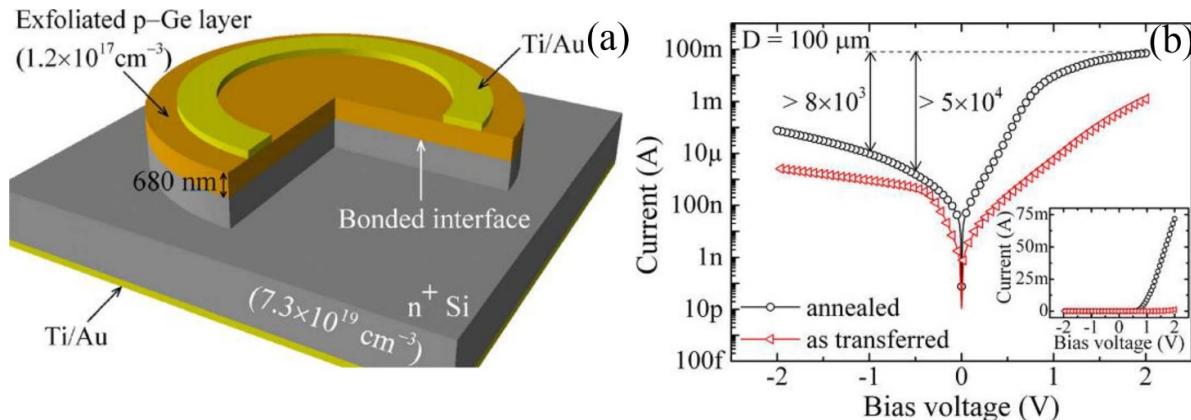


Figure 48. (a) p^- -Ge/ n^+ -Si heterojunction fabricated by plasma-activated Ge/Si wafer bonding. (b) I-V curves of the p^- -Ge/ n^+ -Si heterojunction. (a), (b) Reprinted from [145], with the permission of AIP Publishing.

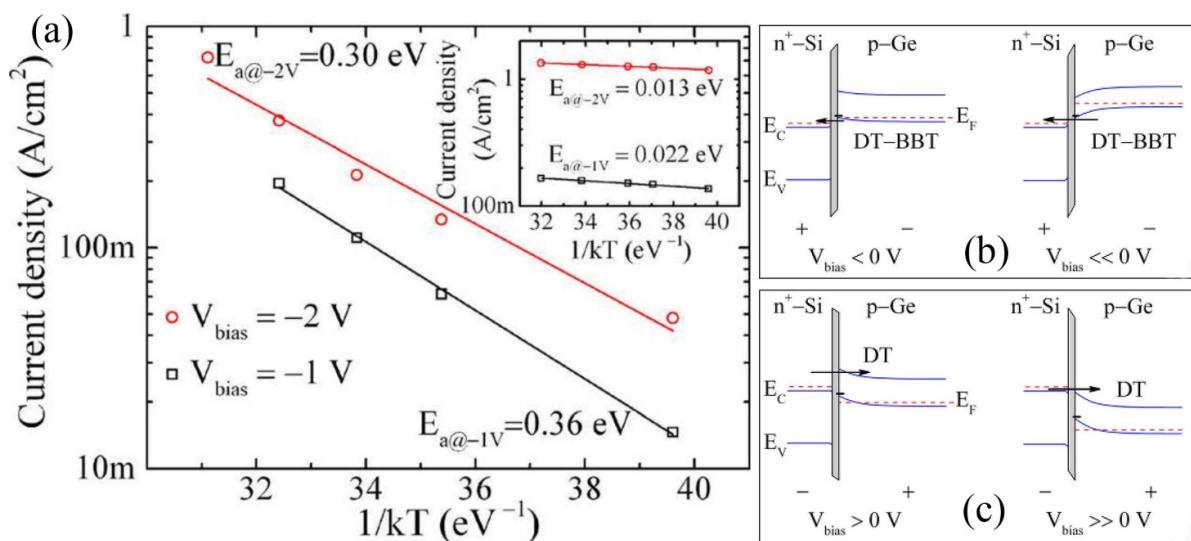


Figure 49. (a) Activation energies of the p^- -Ge/ n^+ -Si heterojunction before and after post-annealing. Carrier transport mechanisms at the Ge/Si bonded interface (b) under reverse bias and (c) forward bias. (a)–(c) Reprinted from [145], with the permission of AIP Publishing.

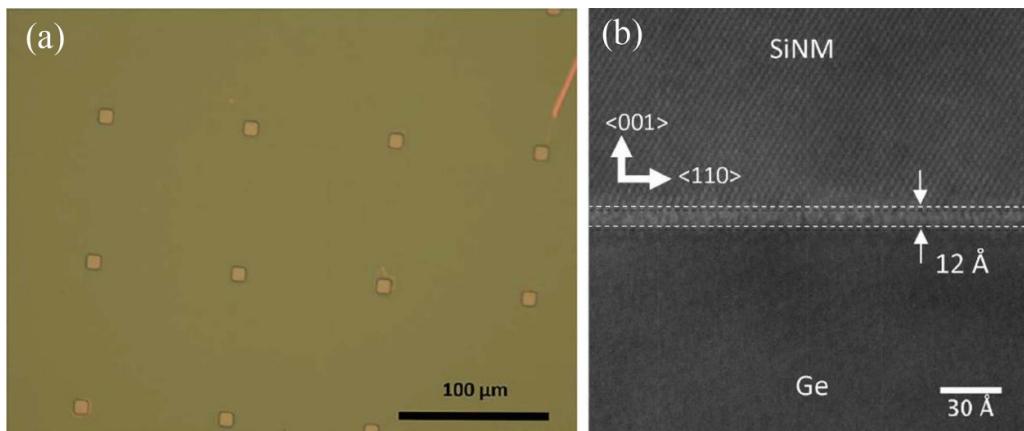


Figure 50. (a) Optical microscope image of the transferred Si thin film. (b) TEM image of the Ge/Si bonded interface fabricated by the direct thin film transfer. (a), (b) Reprinted with permission from [148]. Copyright (2011) American Chemical Society.

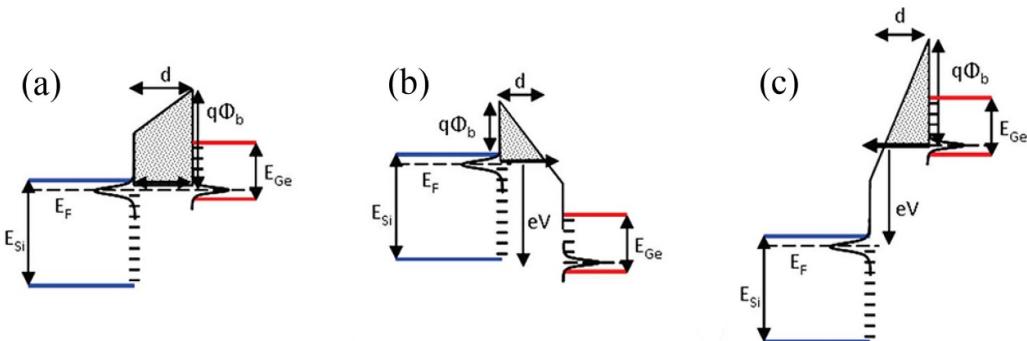


Figure 51. Carrier transport at the Ge/Si bonded interface fabricated by direct thin film transfer. Reprinted with permission from [148]. Copyright (2011) American Chemical Society. (a) At equilibrium. (b) At high forward bias. (c) At high reverse bias.

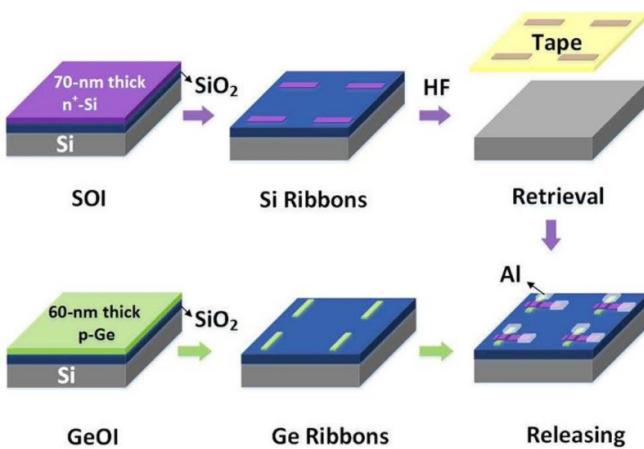


Figure 52. Fabrication process of Ge/Si micro-ribbon bonding. © (2017) IEEE. Reprinted with permission from [149].

0.46 nm was selected for Ge/Si wafer bonding. In addition, the contact angles versus the thickness and the exposure time of the a-Ge layer on the Ge substrate were also investigated, as shown in figures 57(b) and (c), respectively. One can see that the a-Ge layer on the Ge substrate, whose thickness is larger than 2 nm, exhibits extremely hydrophilic characteristics. In addition, the hydrophilia also increases with an increase in exposure time.

For Ge/Si wafer bonding, we firstly studied the effect of a-Ge layer thickness on bubble density. After deposition of the a-Ge layer, the Ge and Si wafers were taken out of the chamber and directly bonded (~1 min). After that, the contacted wafers were annealed at 300 °C for 20 h. The CSAM images of the Ge/Si bonded interface are shown in figure 58. One can see that with the increase of the a-Ge layer thickness, the bubble density slightly increases. This is attributed to the increase of the -OH groups absorbed on the a-Ge layer with the increase of the a-Ge layer thickness.

We also studied the dependence of the bubble density of Ge/Si bonded wafers on the annealing time, as shown in figures 59(a) and (b). One can see that with the increase of the annealing time, the bubble density shows no change. This indicates that the by-products at the bonded interface are difficult to transfer outside the wafer. In addition, when the

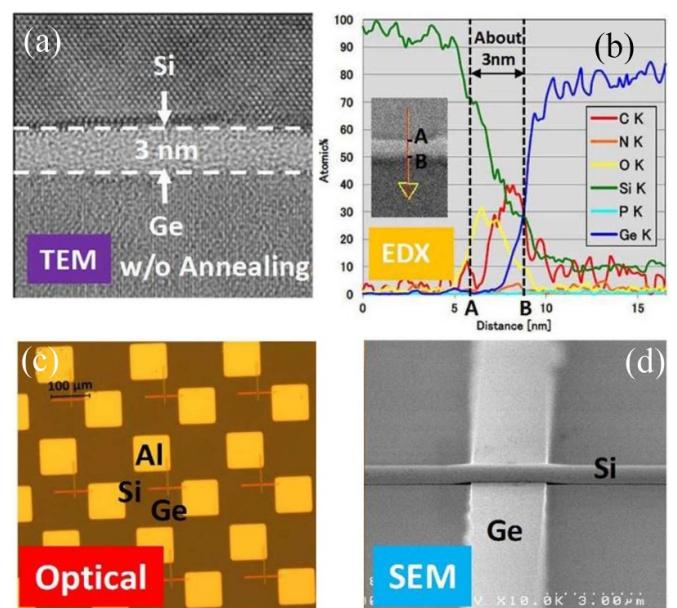


Figure 53. (a) TEM image of the Ge/Si bonded interface fabricated by Ge/Si micro-ribbon bonding. (b) EDS curves of the Ge/Si bonded interface. (c) Optical microscope image of the p-Ge/n⁺-Si heterojunction. (d) SEM image of the Ge/Si micro-ribbon. (a)-(d) © (2017) IEEE. Reprinted with permission from [149].

temperature increases to 350 °C, as shown in figure 59(c), the bubble density slightly decreases and some small bubbles turn dark and dim. This may be due to the enhanced absorption of by-products by the a-Ge film before crystallization when the annealing temperature was increased. However, bubbles still exist at the bonded interface. In order to investigate the bubble density when the sample was annealed at 400 °C, we decreased the thickness of the Ge wafer to 20 μm before annealing due to the fact that if the contacted wafers were directly annealed at 400 °C, the wafers might separate due to the large thermal mismatch between Ge and Si. The SAM image of the Ge/Si bonded interface after annealing at 400 °C is shown in figure 59(d). One can see that bubbles still exist at the bonded interface. High-temperature annealing still cannot significantly decrease bubble density.

In order to further decrease the bubble density, we studied bubble density as a function of exposure time (the time

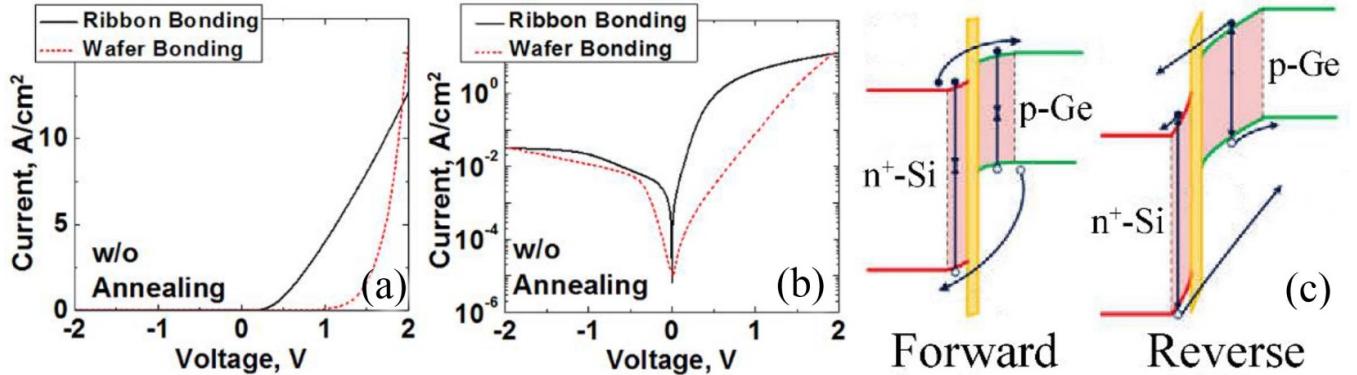


Figure 54. (a), (b) I–V curves of the Ge/Si heterojunction fabricated using Ge/Si micro-ribbon bonding. (c) Carrier transport mechanism at the Ge/Si bonded interface. © (2018) IEEE. Reprinted with permission from [150].

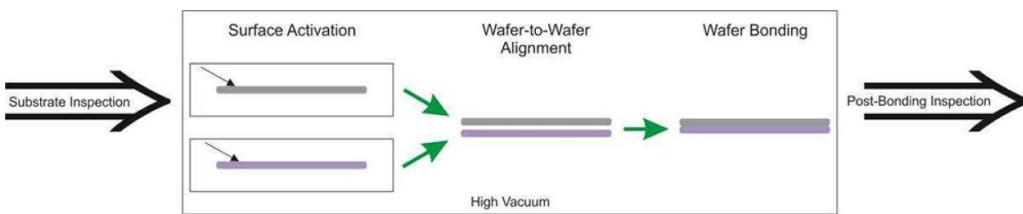


Figure 55. Fabrication process of Ge/Si wafer pairs using high-vacuum surface-activated bonding. Reproduced from [151]. © IOP Publishing Ltd. All rights reserved.

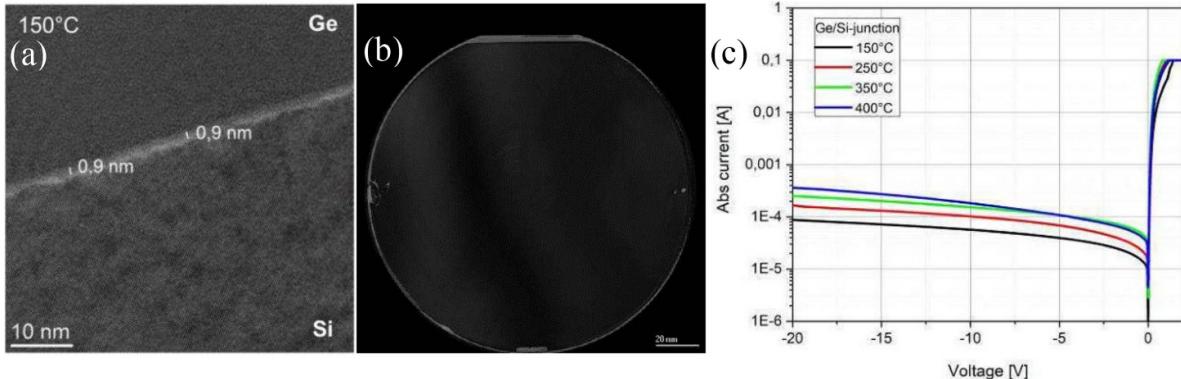


Figure 56. (a) TEM image of the Ge/Si bonded interface fabricated using high-vacuum surface-activated bonding annealed at 150 °C for 2 h. (b) SAM image of the Ge/Si bonded interface annealed at 150 °C for 2 h. (c) I–V curves of the Ge/Si heterojunction. (a)–(c) Reproduced from [151]. © IOP Publishing Ltd. All rights reserved.

that the a-Ge layer was exposed to the air after sputtering and being taken out of the chamber), as shown in figure 60. One can see that with a decrease in exposure time, bubble density decreases. This is due to the fact that with the decrease of the exposure time, the -OH absorbed on the a-Ge layer decreases, leading to a decrease in the hydrophilic reaction (decrease of H₂) at the bonded interface. When the exposure time was set to 3 s, a near-bubble-free Ge/Si bonded interface was achieved.

We fabricated a p[−]Ge/n⁺-Si heterojunction diode based on the Ge/Si interlayer wafer bonding method, as shown in figure 61. The Ge wafer was chemical thinned and polished to 10 μm before the fabrication of the heterojunction diode. The effect of the annealing condition on the diode performance was investigated. The annealing condition of diode A is 300 °C for

20 h, that of diode B is 300 °C for 20 h and further 300 °C for 10 h, and that of diode C is 300 °C for 20 h and further 400 °C for 10 h. The IV curves of the heterojunction diodes are shown in figure 62(a). One can see that these three diodes all show rectification characteristics, and a high on/off ratio of 3.4×10^5 was achieved for diode B. This is higher than that of the p[−]Ge/n⁺-Si heterojunction diode fabricated by means of plasma-activated bonding and dry bonding. This indicates that the quality of the Ge/Si bonded interface fabricated by means of interlayer bonding is higher. The dependence of the I–V curve of the heterojunction diode is shown in figure 62(b). One can see that when the temperature decreases to 250 K, the dark current decreases sharply. This indicates that most of the recombination mechanism is restricted near-room

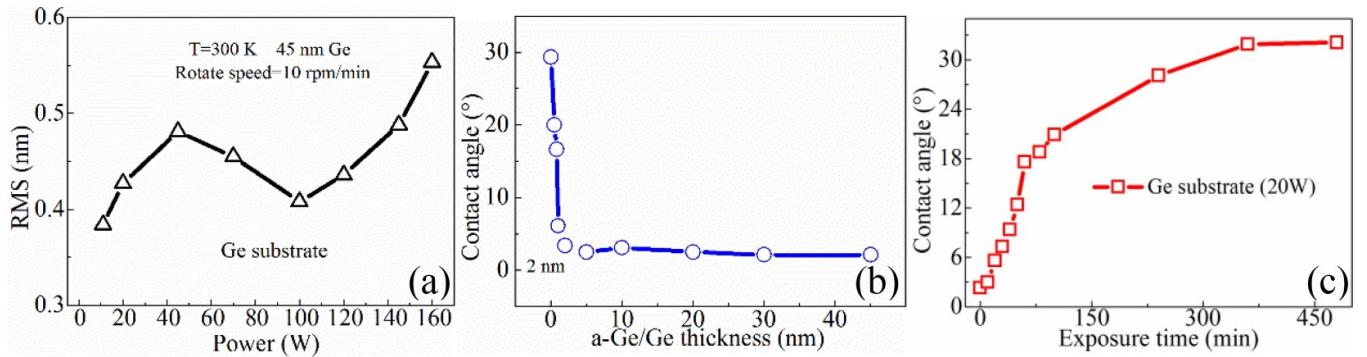


Figure 57. (a) RMS of the a-Ge film on the Ge substrate versus input power. (b) Contact angle versus a-Ge layer thickness. (c) Contact angle versus exposure time. (a)–(c) Reprinted from [125], with the permission of AIP Publishing.

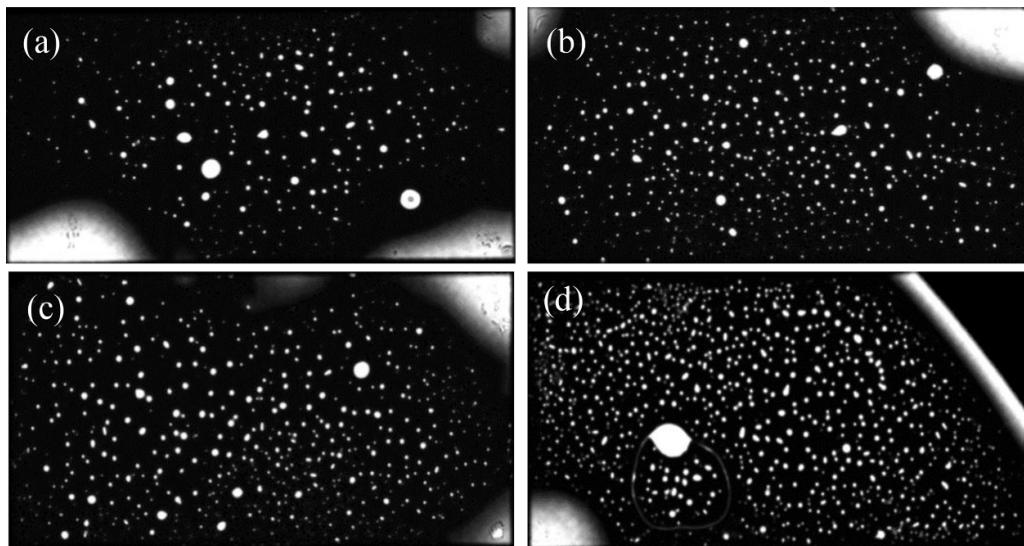


Figure 58. SAM images of the Ge/Si bonded interface with different a-Ge layer thicknesses. (a) 2 nm. (b) 5 nm. (c) 10 nm. (d) 20 nm.

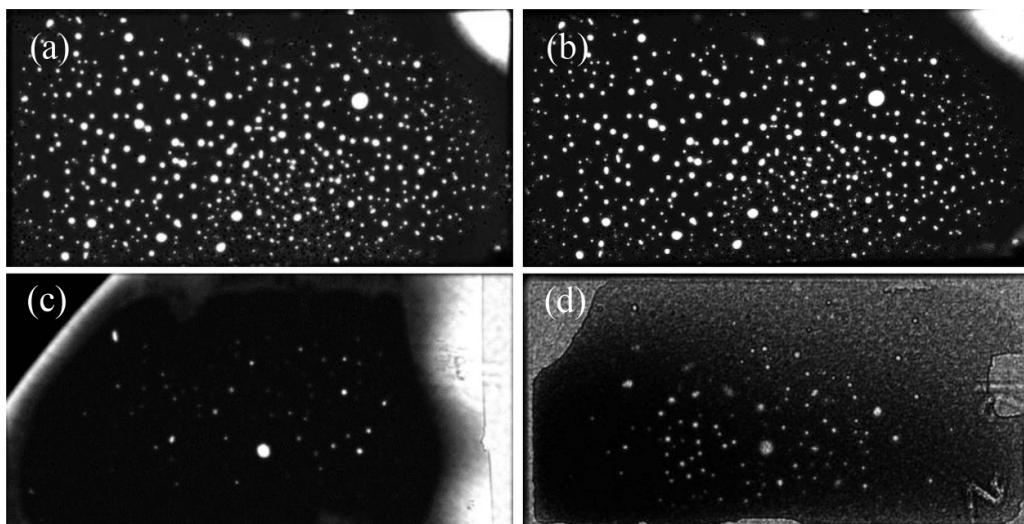


Figure 59. SAM images of the Ge/Si bonded interface annealed at 300 °C for (a) 20 h and (b) 60 h. SAM images of the Ge/Si bonded interface annealed at (c) 350 °C for 20 h and (d) 400 °C 20 h. (a)–(d) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

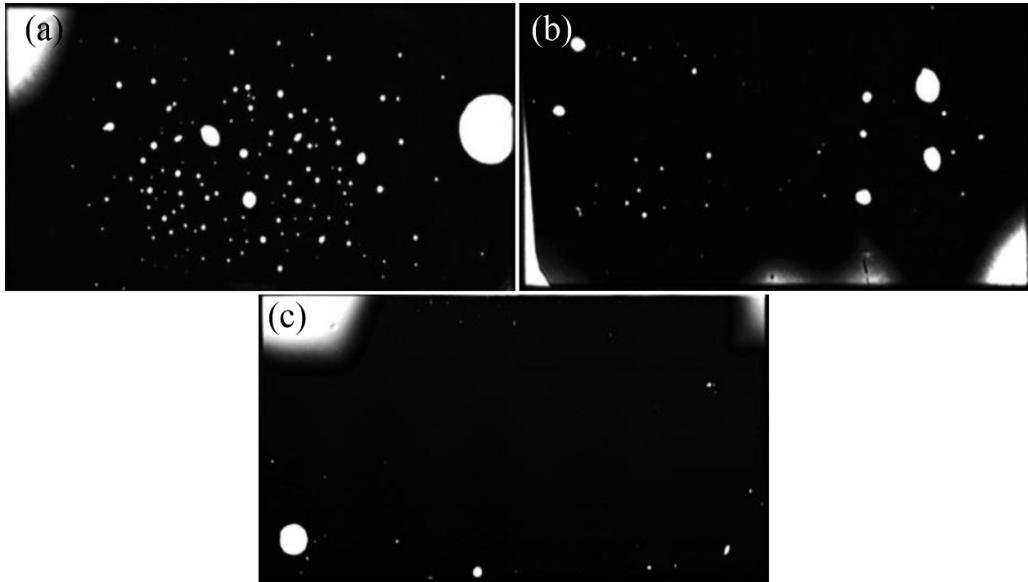


Figure 60. SAM images of the Ge/Si bonded interface bonded with the exposure time of (a) 20 s, (b) 10 s, and (c) 3 s. (a)–(c) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

temperature. This is very important for the fabrication of sensitive detectors (such as single-photon avalanche photodiodes) operated at near-room temperature. On the other hand, a lower ideality factor was achieved for diode B (1.75 at 300 K and 1.02 at 150 K), as shown in figure 62(c).

In order to reveal the different electrical properties of the different diodes, a TEM examination of the Ge/Si bonded interface was conducted, as shown in figure 63. One can see that after annealing at 300 °C for 20 h, as shown in figures 63(a)–(d), the a-Ge at the Ge side has turned into single-crystal Ge (c-Ge), and that at the Si side still exhibits amorphous phase. In addition, an oxide layer appears at the Ge/Si bonded interface. More importantly, TDs were not observed in the Ge wafer at the bonded interface. After further annealing at 300 °C for 10 h, as shown in figures 63(e)–(h), almost all of the a-Ge has turned into c-Ge, leaving a 1–2 nm amorphous layer at the bonded interface. Note that the oxide layer disappears at the bonded interface and that TDs also cannot be observed after annealing. After further annealing at 400 °C for 10 h, as shown in figures 63(i)–(l), the a-Ge has almost completely turned into c-Ge, although some distorted atoms appear at the bonded interface. Similarly, an oxide layer also cannot be observed at the bonded interface.

In order to investigate TDs in the Ge layer, the etch pit method was applied, as shown in figure 64. The TDs in diode B were extracted to be $2.8 \times 10^3 \text{ cm}^{-2}$, as shown in figure 64(a), and those in diode C were extracted to be $2.1 \times 10^5 \text{ cm}^{-2}$, as shown in figure 64(b). Thus, the deterioration of the performance of diode C is due to the increase of the TDs in the Ge layer. In order to investigate the carrier mechanism at the bonded interface, the activation energy of the heterojunction diode was extracted, as shown in figure 64(c). One can see that the activation energy of diode B is 0.32 eV, thus the generation and recombination mechanism is dominant in diode B. The activation energy of diode C is 0.05, thus the BBT mechanism

can be responsible for carrier transport. The activation energy of diode A is 0.19 eV, thus the carrier migration at the bonded interface is a mixed mechanism of both recombination and the BBT mechanisms. The schematic diagrams of carrier transport at the Ge/Si bonded interface are shown in figure 65.

We also investigated the crystallization mechanism of the a-Ge film and the oxide layer evolution at the bonded interface. When the Ge/Si wafer pairs were annealed at 300 °C for 20 h, the a-Ge layer at the unbonded region still shows amorphous phase, as shown in figures 66(a)–(c), while that at the bonded region has crystallized, as shown in figures 66(d)–(f). We believe that the stress-induced crystallization of the a-Ge film at the bonded region may be responsible for this phenomenon. In order to reveal the crystallization process of the a-Ge film at the bonded interface, Ge/SiO₂ wafer bonding with the a-Ge interlayer was also investigated. The TEM image of the Ge/SiO₂ bonded interface is shown in figures 66(g)–(i). One can see that the a-Ge crystallizes from the Ge substrate. This is consistent with Ge/Si wafer bonding.

In addition, no oxide layer was observed at the a-Ge/a-Ge bonded interface. Thus, the crystallization of the a-Ge film and the oxide layer evolution were drawn, as shown in figure 67. One can see that when the a-Ge shows amorphous phase, a thin oxide layer formed by the hydrophilic reaction appears at the a-Ge/a-Ge bonded interface. When the Ge/Si wafer pairs were annealed at 300 °C for 20 h, a-Ge starts to crystallize from the Ge substrate and turns into c-Ge induced by the Ge substrate. Due to the crystallization of the a-Ge, the atom migration becomes serious at the bonded interface, the Ge atoms migrate into the oxide layer and the O atoms migrate into the Ge layer, leading to the decomposition of the oxide layer at the bonded interface. Finally, the a-Ge completely crystallizes when 400 °C-annealing was conducted.

We also fabricated a p⁻Ge/n⁺-Si heterojunction diode with 1 μm thick Ge layer: the XRD examination of the Ge(004)

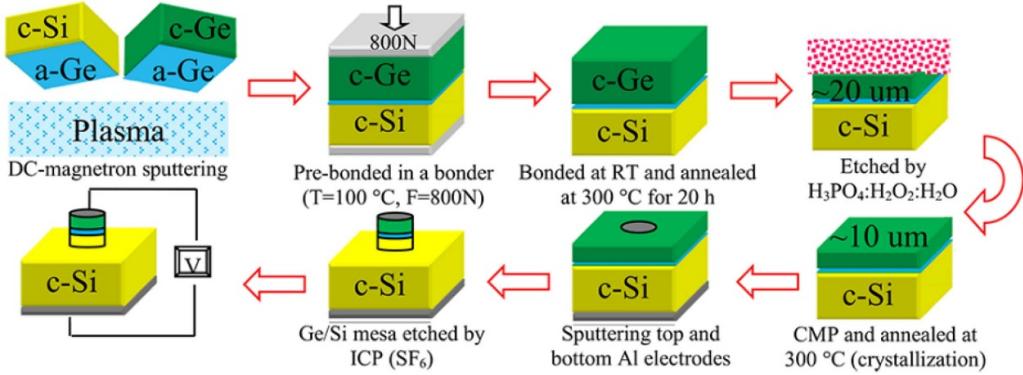


Figure 61. Fabrication process of the p^- -Ge/ n^+ -Si heterojunction diode based on Ge/Si interlayer wafer bonding. Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

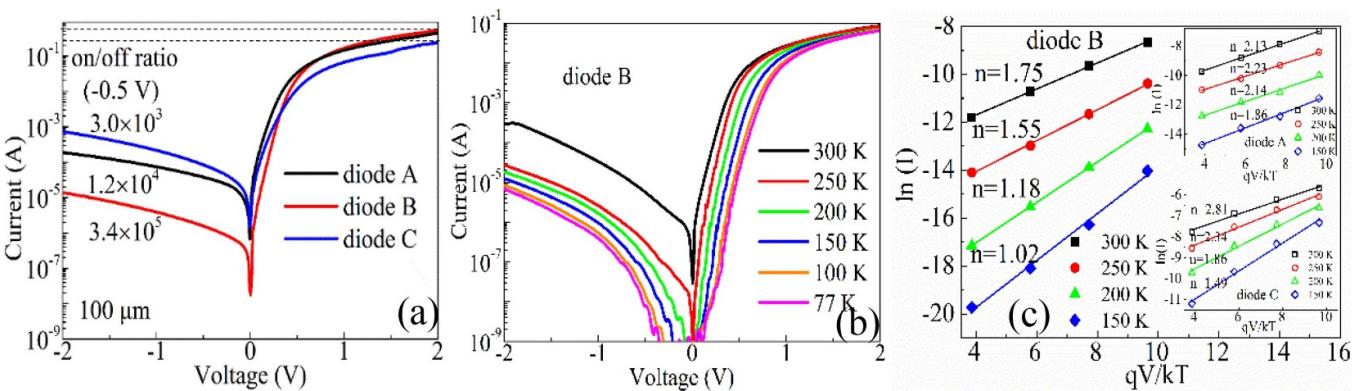


Figure 62. (a) I-V curves of the p^- -Ge/ n^+ -Si heterojunction diode ($100 \mu\text{m}$) based on Ge/Si interlayer wafer bonding. (b) Temperature dependence of the I-V curve of diode B ($200 \mu\text{m}$). (c) Ideality factors of the heterojunction diodes. (a)–(c) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

peak is shown in figure 68(a). One can see that the FWHM of the wafer-bonded Ge film is only $34''$, which is much smaller than that of the epitaxial Ge film ($375''$). This indicates that the quality of the wafer-bonded Ge film is higher than that of the epitaxial Ge film. Figure 68(b) shows the I-V curve of wafer-bonded Ge/Si photodetectors with diameters of 32 and $100 \mu\text{m}$. It can be seen that all the devices show good rectification characteristics. Responsivities of 0.49 and 0.61 A W^{-1} were achieved for photodiodes with diameters of 32 and $100 \mu\text{m}$, respectively, at 1310 nm . In addition, a responsivity of 0.16 and 0.24 A W^{-1} was obtained at 1550 nm for these two devices, respectively. Figure 68(c) shows the responsivity of the heterojunction diode as a function of wavelength. One can see that the responsivity of both photodiodes extends to 1560 – 1630 nm , which is beyond the absorption edge of the bulk Ge. This results from the Ge bandgap narrowing induced by the 0.205% tensile strain. The responsivity at 1630 nm is 94 and 17 mA W^{-1} for these two devices, respectively. This indicates that the wafer-bonded Ge/Si heterojunction photodiode is suitable for optical communication in all WDM bands, including the L-band and the entire C band.

We also attempted to fabricate the Si-based Ge film using the interlayer wafer bonding and Smart-Cut technique. H^+ implantation (at a dose of $5 \times 10^{16} \text{ cm}^2$ and energy of 150 keV) was applied to create a defective blistered region below

the Ge surface. Before Ge/Si wafer bonding, a 2 nm thick a-Ge layer was deposited on the substrate. The exposure time of 3 s was set for near-bubble-free wafer bonding. After contact, the wafer pairs were successively annealed at 150°C under a force of 2 MPa for 1 h, 250°C under a force of 0.5 MPa for 1 h, 350°C without force for 1 h, and 400°C without force for 1 h to trigger the exfoliation of Ge film. The whole bonding process took place under a chamber pressure of 10^{-5} mbar .

The camera image of the exfoliated Ge film is shown in figure 69(a). One can see that most of the Ge film was transferred onto the Si substrate. Only one bubble bursts on the Si substrate. The SAM image and SEM image of the Ge/Si bonded interface are shown in figures 69(b) and (c), respectively. One can see that few bubbles appear at the Ge/Si bonded interface, indicating that less hydrophilic reactions appear at the bonded interface due to the short exposure time of a-Ge. The Ge film is uniformly located on the Si substrate and no cracks were observed at the bonded interface.

The XRD peak of the Ge film is shown in figure 70(a). One can see that the exfoliated Ge film exhibits 0.275% compression strain and the FWHM of the exfoliated Ge film is $96''$, which is also smaller than that of the epitaxial type, while it is slightly larger than that of the thinning type shown above. There is a shoulder peak at the left side of the Ge(004) peak

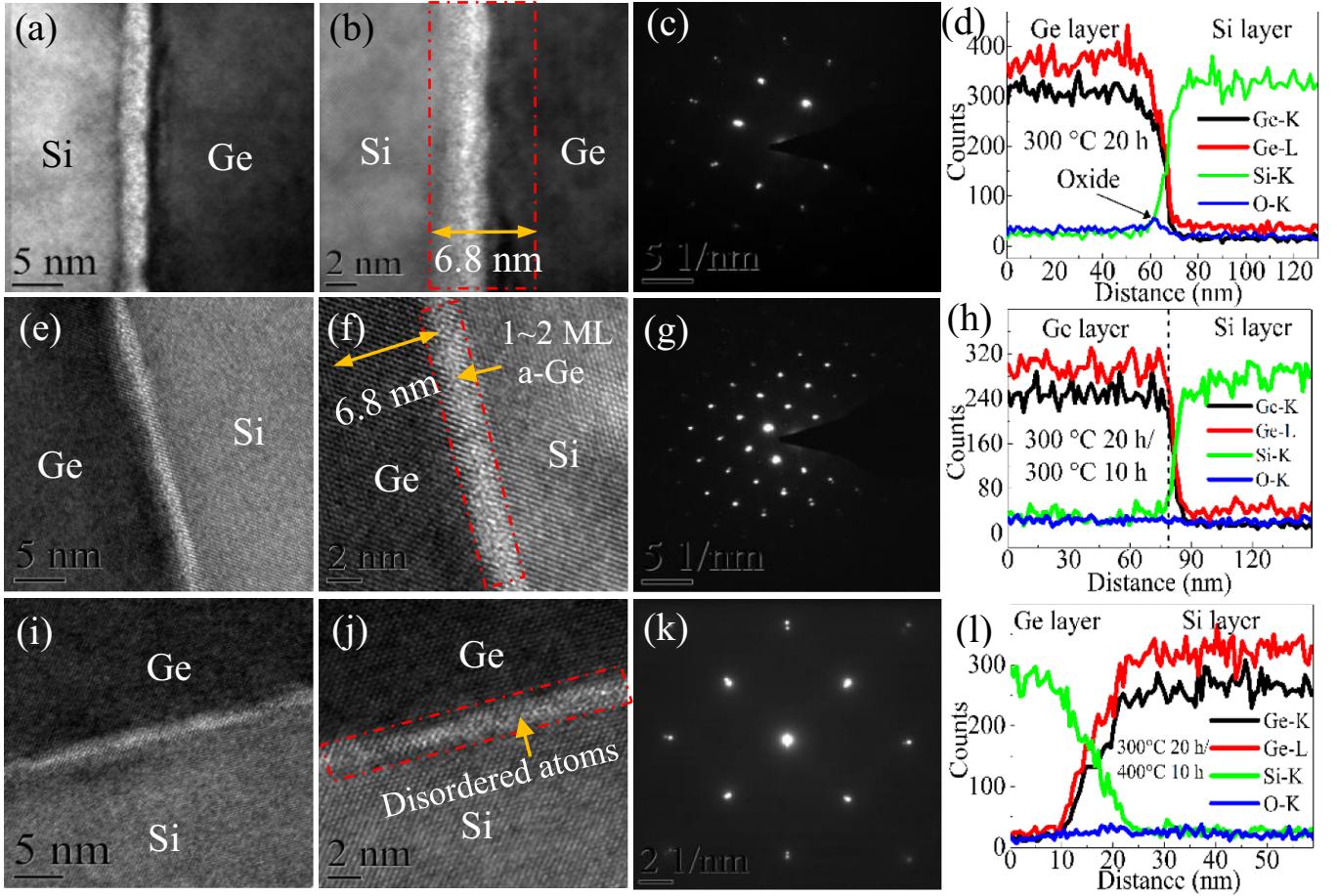


Figure 63. TEM images, electron diffraction, and EDS curves of (a)–(d) diode A, (b) diode (b), and diode (c). (a)–(d) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

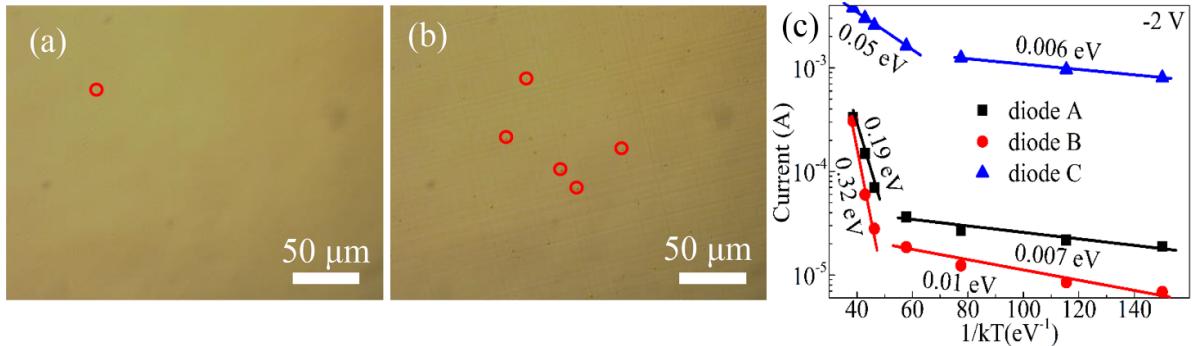


Figure 64. Optical microscope image of the Ge surface in (a) diode B and (b) diode C etched in secco solution for 60 s. (c) Activation energies of the three diodes at -2 V. (a)–(c) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

which results from the interference effects between the substrate and the strained layers created by the H⁺ implantation [154–156]. This indicates that the strain in the Ge film is nonuniform. In addition, the shape of the Ge peak of the as-exfoliated Ge film is unusual. The upper half of the Ge peak is sharp, while the bottom half is broad. This is due to point defects in the as-exfoliated Ge film induced by the H⁺ implantation. In order to eliminate the point defects, high-temperature annealing (500 °C) was conducted for 1 h. The XRD peak is shown in figure 70(a). One can see that after

post-annealing, the shape of the Ge peak becomes symmetrical and the bottom half of the Ge peak becomes narrow, indicating the relaxation of the nonuniform strain and the repair of the point defects in the Ge film. However, the FWHM of the Ge film (104°) slightly increases. This is due to an increase in TDs when high-temperature annealing was conducted, as shown in figures 70(b) and (c). One can see that the number of TDs in the as-exfoliated Ge film is less than 10⁵ cm⁻², and that in the post-annealed Ge film this number increases to 10⁶ cm⁻². More importantly, the peak position shows right-shift after

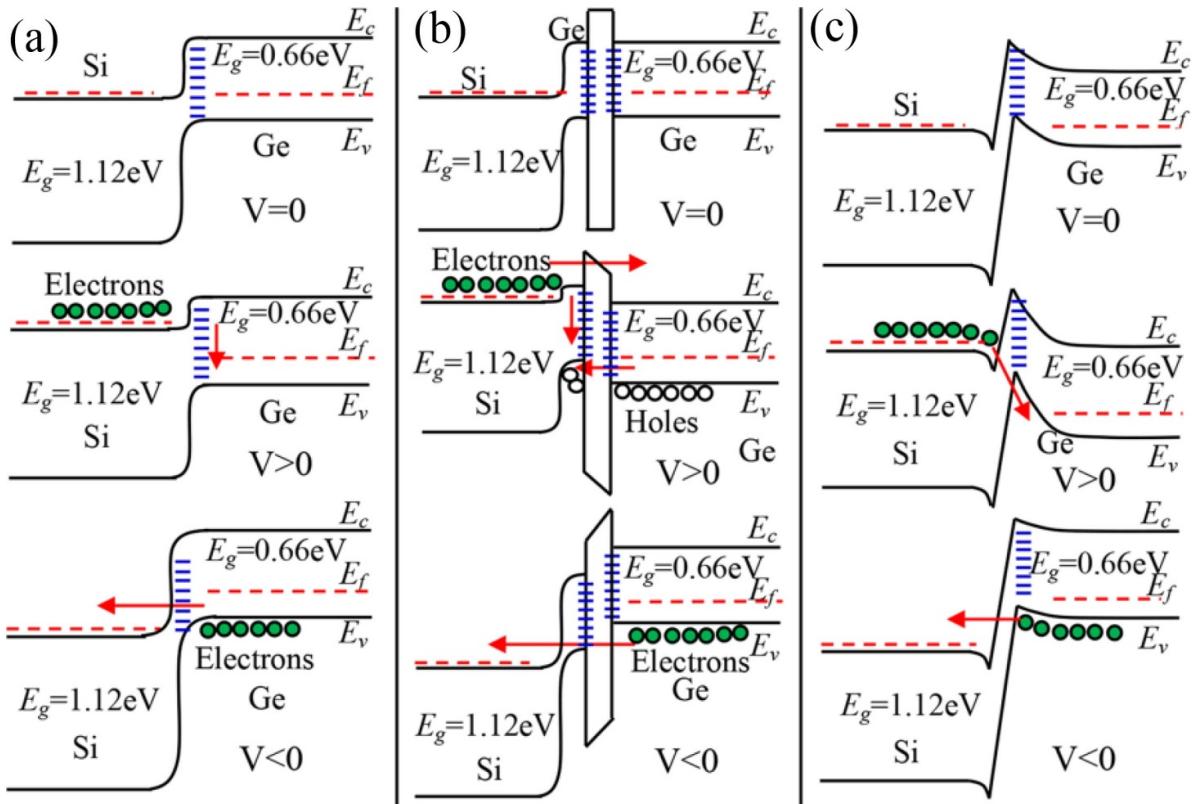


Figure 65. Schematic diagram of carrier transport in (a) diode B, (b) diode A, and (c) diode C. (a)–(c) Reproduced from [152]. © IOP Publishing Ltd. All rights reserved.

post-annealing, and the compression strain turns into tensile strain (0.392%) after post-annealing.

We fabricated two wafer-bonded Ge/Si p-i-n photodiodes using the exfoliated Ge film. The dark current of the p-i-n photodiode based on the as-exfoliated Ge film is shown in figure 71(a). One can see that a low dark current of 5.97 mA cm^{-2} was achieved for the $24\text{ }\mu\text{m}$ -diameter mesa at -1 V and that a dark current of 14.1 mA cm^{-2} was achieved for the $32\text{ }\mu\text{m}$ -diameter mesa. These values are comparable with the epitaxial Ge/Si p-i-n photodiode. A dark current of 207.6 mA cm^{-2} was achieved for the p-i-n photodiode based on the exfoliated Ge film annealed at $500\text{ }^\circ\text{C}$ for 1 h with the $24\text{ }\mu\text{m}$ -diameter mesas. The increase of the dark current of the post-annealed p-i-n photodiode is attributed to the increase of TDs in the Ge film. The increase in TDs leads to the increase in bulk current density, as shown in figures 71(b) and (e). The activation energy of the photodiode was also extracted, as shown in figure 71(c) and (f). One can see that the activation energies of both photodiodes are close to 0.33 eV , indicating that the recombination mechanism is dominant in both photodiodes.

The photocurrents of the photodiodes are shown in figures 72(a) and (b). One can see that the responsivities of the photodiode based on the as-exfoliated Ge film at 1310 and 1550 nm were obtained to be 0.304 and 0.221 A W^{-1} , respectively, and that based on the exfoliated Ge film annealed at $500\text{ }^\circ\text{C}$ for 1 h increase to 0.475 and 0.381 A W^{-1} , respectively. The increase in responsivity is ascribed to the 0.392%

tensile strain in the Ge film after post-annealing. The ideality factors of these two devices are shown in figure 72(c). It is shown that an ideality factor of 1.19 of the device without post-annealing was achieved, and that this increases to 1.56 after post-annealing. The deterioration of the performance of the device is due to an increase in TDs in the Ge film after post-annealing.

4. Outlooks for Si/Si wafer bonding and Ge/Si wafer bonding

The investigation of Si/Si wafer bonding is currently mature. We can easily achieve Si/Si bonded wafer pairs with high bonding strength, low bonded temperature, and a bubble-free bonded interface. These features are basic requirements in MEMS. However, it is difficult to apply Si/Si wafer bonding techniques to the photoelectric field at present. Due to the fact that the carriers must transport through the Si/Si bonded interface for photoelectric devices, it is sufficient to lower the potential barrier at the bonded interface for carrier transport and to restrict carrier recombination. The difficulties inherent in the application of Si/Si wafer bonding in the photoelectric field may be categorised as follows: (1) the oxide layer at the Si/Si bonded interface should be totally eliminated at the bonded interface. (2) The Si/Si bonded interface should exhibit the electrical properties of bulk Si. (3) Small bubbles (several nanometers), which are difficult to detect using the IR transmission technique or the CSAM technique, should be

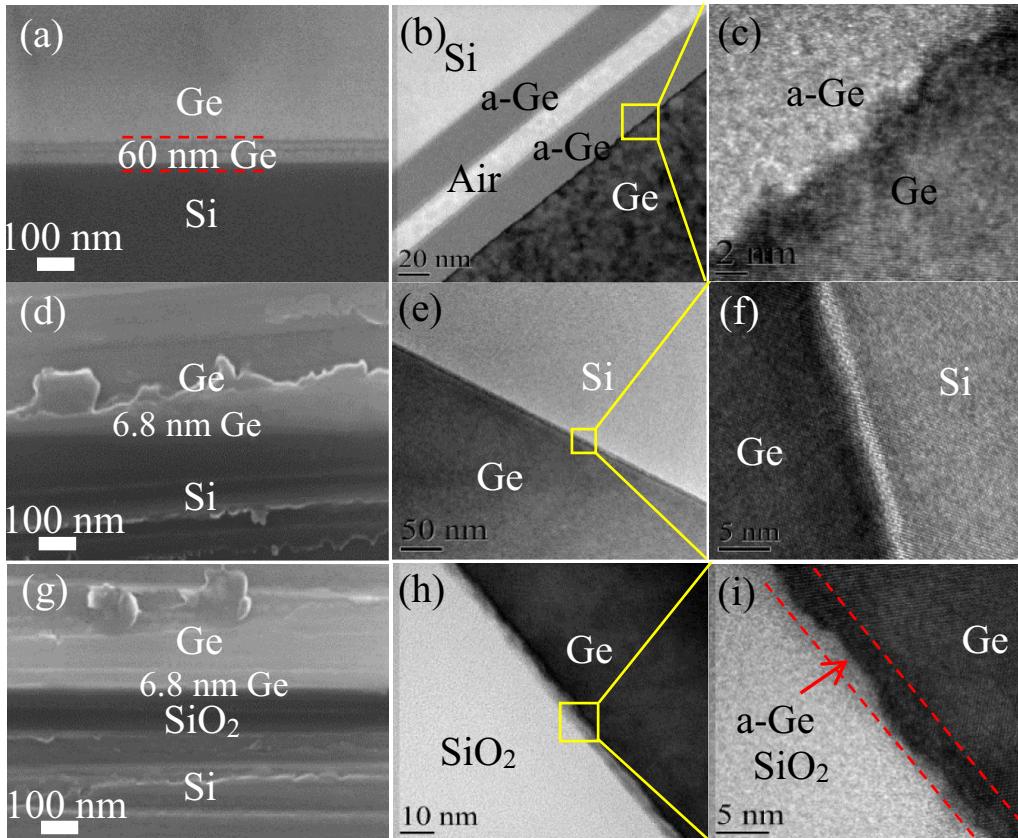


Figure 66. SEM images of (a) unbonded region of the Ge/Si bonded interface, (d) bonded region of the Ge/Si bonded interface, and (g) bonded region of the Ge/SiO₂ bonded interface. TEM images of (b), (c) unbonded region of the Ge/Si bonded interface, (e), (f) bonded region of the Ge/Si bonded interface, and (h), (i) bonded region of the Ge/SiO₂ bonded interface. [127] (2019) © (Springer Nature). With permission from Springer.

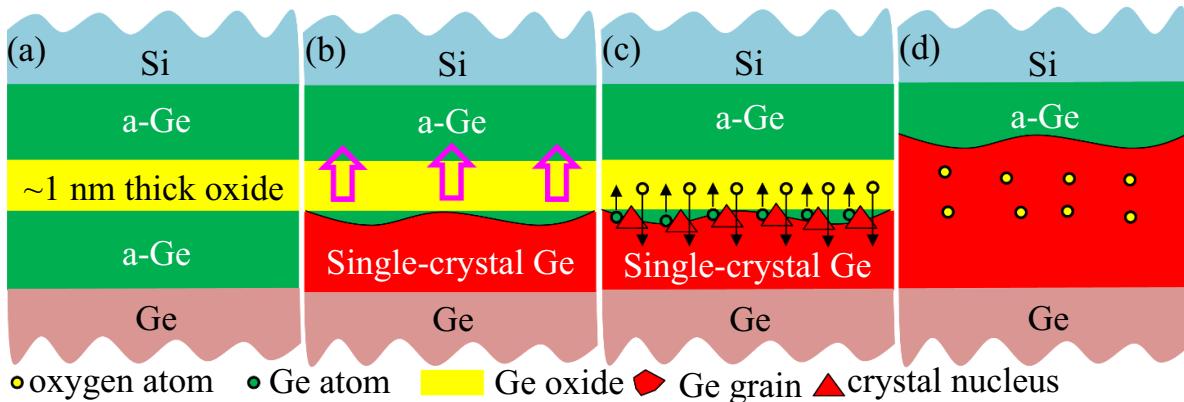


Figure 67. (a), (b) Crystallization process of a-Ge at the Ge/Si bonded interface. (c), (d) Kinetic process of Ge and oxygen atoms at the Ge/Si bonded interface. (a)–(d) [127] (2019) © (Springer Nature). With permission from Springer.

eliminated. These small bubbles may lead to leakage current at the Si/Si bonded interface. The research direction for Si/Si wafer bonding in the future should focus on the replacement of the epitaxial Si layer with a wafer-bonded (exfoliated) Si layer. For example, the epitaxial Si multiplication layer in the Ge/Si avalanche photodiode may be replaced by wafer-bonded Si layer. This may lead to a decrease in the dark current of the device, and the decrease of the dark count rate and afterpulsing

probability of related Ge/Si single-photon avalanche photodiodes.

The study of Ge/Si wafer bonding and photoelectronic devices based on this technique is still incomplete. Using the above techniques, we can fabricate a Si-based Ge film without TDs at low temperature. The quality of wafer-bonded Ge film will hopefully be higher than that of epitaxial varieties. This is due to a low-temperature achievement of the covalent bond at

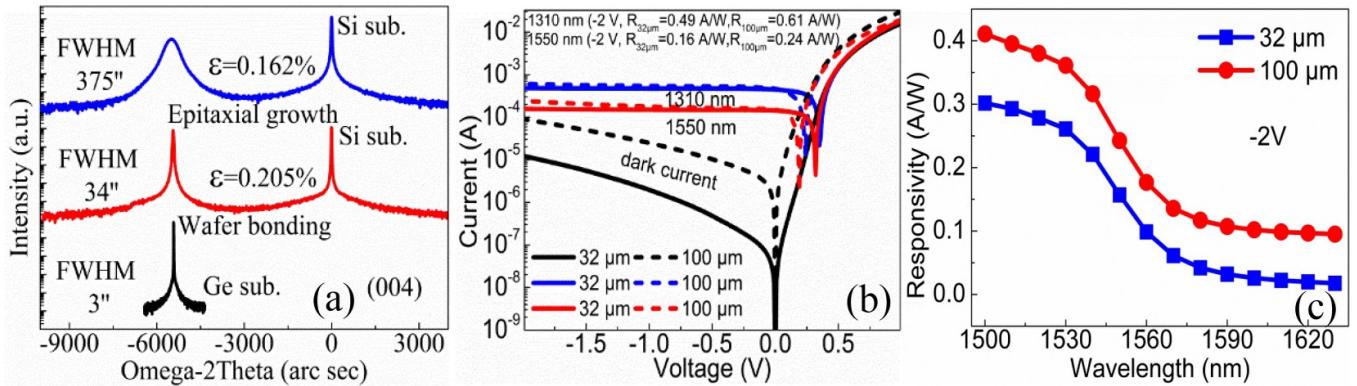


Figure 68. (a) XRD examination of the Ge(004) peak. (b) Photocurrent of the heterojunction diode. (c) Responsivity of the heterojunction diode versus wavelength. (a)–(c) [127] (2019) © (Springer Nature). With permission from Springer.

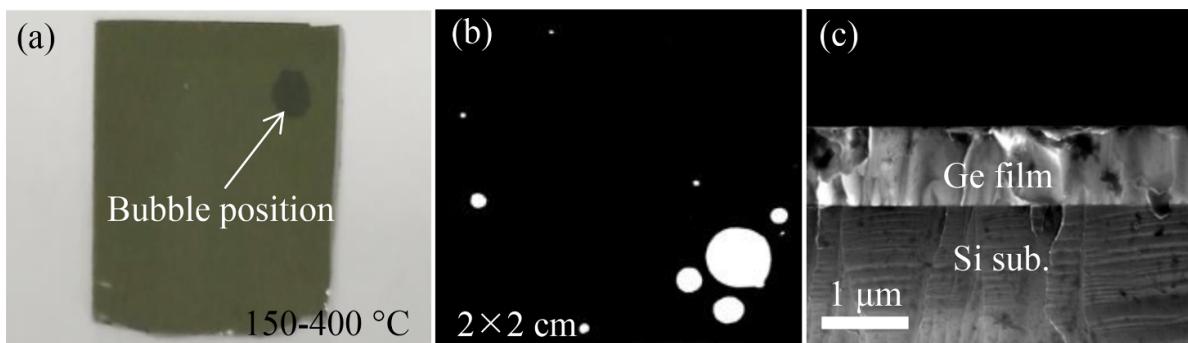


Figure 69. (a) Camera image of the exfoliated Ge film. (b) SAM image of the Ge/Si bonded interface. (c) SEM image of the Ge/Si bonded interface. (a)–(c) (2019) IEEE. Reprinted with permission from [153].

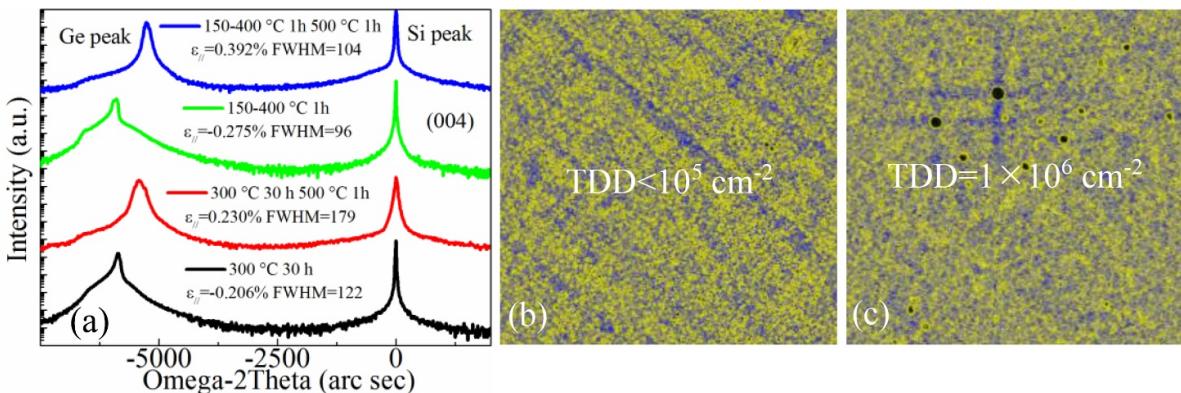


Figure 70. (a) XRD curves of the exfoliated Ge film annealed at different temperature. AFM images of (b) the as-exfoliated Ge film and (c) the exfoliated Ge film post-annealed at 500 °C for 1 h etched in secoco solution for 10 s. (a)–(c) (2019) IEEE. Reprinted with permission from [153].

the bonded interface. Low-temperature annealing can eliminate TD nucleation and diffusion at the bonded interface. However, many problems still need to be solved in the bonding process, such as how to further lower the bonding temperature, how to totally eliminate small bubbles at the bonded interface, how to fundamentally eliminate misfit dislocation, how to exfoliate the whole Ge film on the Si substrate, and how to effectively repair the point defects in the Ge film without the introduction of TDs.

The research direction of Ge/Si wafer bonding can be identified as follows. (1) Introduction of porous materials at the Ge/Si bonded interface to absorb by-products at the bonded interface. (2) Increasing the implantation dose of the H⁺ to further decrease the exfoliation temperature of the Si-based Ge film. (3) Introduction of amorphous material or polycrystalline material at the Ge/Si bonded interface to eliminate misfit dislocations. (4) Etching the implantation damage in Ge film to further enhance Ge film quality. (5) The application of short-time

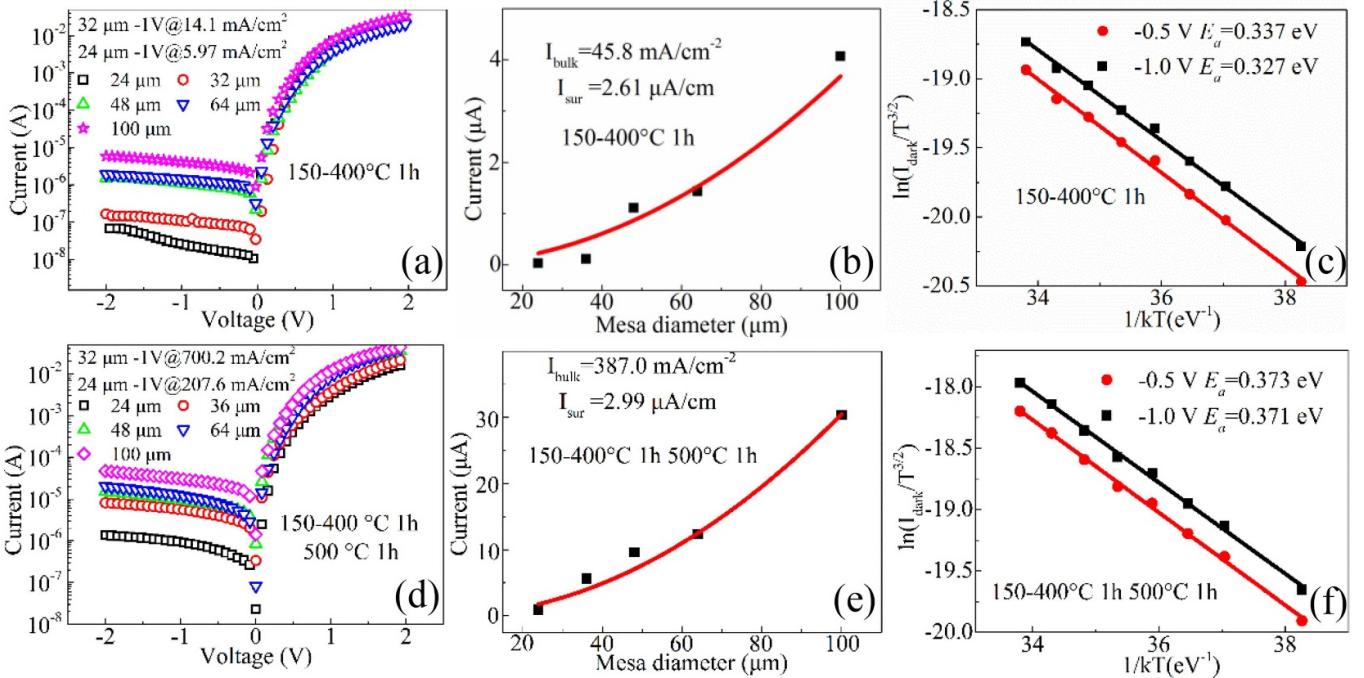


Figure 71. (a) IV-curves, (b) current versus mesa diameter, and (c) activation energy of the Ge/Si p-i-n photodiode based on the as-exfoliated Ge film. (d) IV-curves, (e) current versus mesa diameter, and (f) activation energy of the Ge/Si p-i-n photodiode based on the exfoliated Ge film annealed at 500°C for 1 h. (a)–(f) (2019) IEEE. Reprinted with permission from [153].

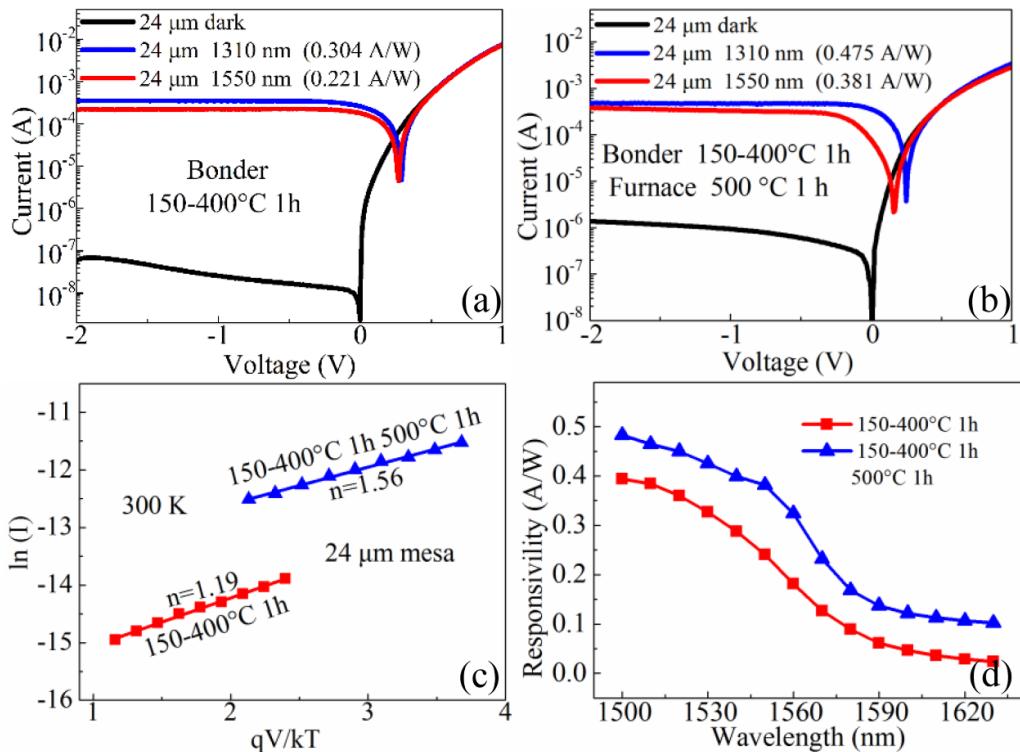


Figure 72. (a), (b) Photocurrent of the Ge/Si p-i-n photodiode based on the as-exfoliated Ge film and the exfoliated Ge film annealed at 500°C for 1 h, respectively. (c) Ideality factor and (d) responsivity versus wavelength of the photodiode. (a)–(d) (2019) IEEE. Reprinted with permission from [153].

high-temperature annealing methods to improve the Ge film quality, such as nanosecond-pulsed laser annealing.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (61534005, 61974122 and 11673019), General Armaments Department of China (6140721040411), National Key Research and Development Program of China (2018YFB2200103), Presidential Research Fund of Minnan Normal University (KJ19014), Natural Science Research Project of Huaian (HAB201909), Jiangsu Shuangchuang program for Doctor.

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References

- [1] Wu S-Y, Yang C, Hsu W and Lin L 2015 *Microsyst. Nanoeng.* **1** 15013
- [2] Karnaushenko D, Muenzenrieder N, Karnaushenko D D, Koch B, Meyer A K, Baunack S, Petti L, Troester G, Makarov D and Schmidt O G 2015 *Adv. Mater.* **27** 6797–805
- [3] Poulton C V, Zeng X, Wade M T, Shainline J M, Orcutt J S and Popovic M A 2015 *IEEE Photonics Technol. Lett.* **27** 665–8
- [4] Eckstein R, Alt M, Roedlmeier T, Scharfer P, Lemmer U and Hernandez-Sosa G 2016 *Adv. Mater.* **28** 7708–15
- [5] Wade M T, Pavanello F, Orcutt J, Kumar R, Shainline J M, Stojanovic V, Ram R and Popovic M A 2015 *CLEO: Sci. Innovations SW4N* 1
- [6] Mak K F and Shan J 2016 *Nat. Photonics* **10** 216–26
- [7] Wu W and Wang Z L 2016 *Nat. Rev. Mater.* **1** 16031
- [8] Wang G *et al* 2015 *Sci. Adv.* **1** e1500613
- [9] Chen Y, He M, Peng J, Sun Y and Liang Z 2016 *Adv. Sci.* **3** 1500392
- [10] Jarrahi M 2015 *IEEE Trans. Terahertz Sci. Technol.* **5** 391–7
- [11] Schaller R R 1997 *IEEE Spectrum* **34** 52–9
- [12] Waldrop M M 2016 *Nature* **530** 144
- [13] Lundstrom M 2003 *Science* **299** 210–1
- [14] Thompson S E and Parthasarathy S 2006 *Mater. Today* **9** 20–5
- [15] Theis T N and Wong H S P 2017 *Comput. Sci. Eng.* **19** 41
- [16] Hisamoto D, Lee W C, Kedzierski J, Takeuchi H, Asano K, Kuo C, Anderson E, King T J, Bokor J and Hu C M 2000 *IEEE Trans. Electron Devices* **47** 2320–5
- [17] Yu B *et al* 2002 *Int. Electron Devices Meeting* pp 251–4
- [18] Choi Y K, King T J and Hu C M 2002 *IEEE Electron Device Lett.* **23** 25–7
- [19] Trivedi V P and Fossum J G 2005 *IEEE Electron Device Lett.* **26** 26–8
- [20] Zhang G, Shao Z and Zhou K 2008 *IEEE Trans. Electron Devices* **55** 803–9
- [21] Shimada H, Ohshima I, Ushiki T, Sugawa S and Ohmi T 2001 *IEEE Trans. Electron Devices* **48** 1619–26
- [22] Singh N *et al* 2006 *IEEE Electron Device Lett.* **27** 383–6
- [23] Bangsaruntip S *et al* 2009 *IEEE Int. Electron Devices Meeting* 1–4
- [24] Yang B, Buddharaju K D, Teo S H G, Singh N, Lo G Q and Kwong D L 2008 *IEEE Electron Device Lett.* **29** 791–4
- [25] Keyes R W 2005 *Rep. Prog. Phys.* **68** 2701
- [26] Keyes R W 2001 *Proc. IEEE* **89** 227–39
- [27] Fuechsle M, Miwa J A, Mahapatra S, Ryu H, Lee S, Warschkow O, Hollenberg L C L, Klimeck G and Simmons M Y 2012 *Nat. Nanotechnol.* **7** 242
- [28] Shokri Kojori H, Yun J H, Paik Y, Kim J, Anderson W A and Kim S J 2015 *Nano Lett.* **16** 250–4
- [29] Cao X and Guo J 2014 *IEEE Trans. Electron Devices* **62** 659–65
- [30] Jin L and Li L 2015 *Opt. Lett.* **40** 1798–801
- [31] Zang X, Zhou Q, Chang J, Liu Y and Lin L 2015 *Microelectron. Eng.* **132** 192–206
- [32] Kan T, Isozaki A, Kanda N, Nemoto N, Konishi K, Takahashi H, Kuwata-Gonokami M, Matsumoto K and Shimoyama I 2015 *Nat. Commun.* **6** 8422
- [33] Arbabi E, Arbabi A, Kamali S M, Horie Y, Faraji-Dana M and Faraon A 2018 *Nat. Commun.* **9** 812
- [34] Pitchappa P, Manjappa M, Ho C P, Singh R, Singh N and Lee C 2016 *Adv. Opt. Mater.* **4** 541–7
- [35] Ciuti G, Nardi M, Valdastri P, Menciassi A, Fasolo C B and Dario P 2014 *Urology* **84** 976–81
- [36] Ciuti G, Pateromichelakis N, Sfakiotakis M, Valdastri P, Menciassi A, Tsakiris D P and Dario P 2012 *Sensors Actuators A* **186** 270–6
- [37] Sgandurra G, Bartalena L, Cioni G, Greisen G, Herskind A, Inguaggiato E, Lorentzen J, Nielsen J B and Sicola E 2014 *BMC Pediatr.* **14** 268
- [38] Boustedt K, Persson K and Stranneby D 2002 *52nd Electronic Components & Technology Conf.* pp 124–8
- [39] Mercado L L, Goldberg C, Kuo S M, Lee T Y and Pozder S K 2003 *IEEE Trans. Device Mater. Reliab.* **3** 111–18
- [40] Butler J T, Bright V M and Comtois J H 1998 *Sensors Actuators A* **70** 15–22
- [41] Butler J T, Bright V M, Chu P B and Saia R J 1998 *1998 Int. Conf. on Multichip Modules and High Density Packaging* pp 106–11
- [42] Wang Z, Wang L, Nguyen N T, Wien W A H, Schellevis H, Sarro P M and Burghartz J N 2006 *IEEE Trans. Adv. Packag.* **29** 615–22
- [43] Balde J W 2003 Springer Science & Business Media
- [44] Esashi M 2008 *J. Micromech. Microeng.* **18** 073001
- [45] Yang H A, Wu M C and Fang W L 2005 *J. Micromech. Microeng.* **15** 394–9
- [46] Topol A W, Furman B K, Guarini K W, Shi L, Cohen G M and Walker G F 2004 *54th Electronic Components & Technology Conf.* pp 931–8
- [47] Wunderle B, Mrossko R, Wittler O, Kaulfersch E, Ramm P, Michel B and Reichl H 2006 *MRS Online Proc. Libr.* **970** 1–8
- [48] Garrou P, Bower C and Ramm P 2011 *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits* (New York: Wiley)
- [49] Kim J *et al* 2011 *IEEE Trans. Compon., Packag., Manuf. Technol.* **1** 181–95
- [50] Marinissen E J, Verbree J and Konijnenburg M 2010 *28th VLSI Test Symp. (VTS)* pp 269–74
- [51] Do C D, Erbes A, Yan J, Soga K and Seshia A A 2016 *J. Microelectromech. Syst.* **25** 851–8
- [52] Cheng Y T, Hsu W T, Najafi K, Nguyen C C and Lin L 2002 *J. Microelectromech. Syst.* **11** 556–65
- [53] Topalli E S, Topalli K, Alper S E, Serin T and Akin T 2009 *IEEE Sens. J.* **9** 263–70
- [54] Lin L 2000 *IEEE Trans. Adv. Packag.* **23** 608–16
- [55] Sparks D R, Massoud-Ansari S and Najafi N 2003 *IEEE Trans. Adv. Packag.* **26** 277–82
- [56] Seshia A A, Palaniapan M, Roessig T A, Howe R T, Gooch R W, Schimert T R and Montague S 2002 *J. Microelectromech. Syst.* **11** 784–93
- [57] Seok S, Kim H and Chun K 2004 *Sensors (IEEE)* pp 654–7

- [58] Alper S E, Azgin K and Akin T 2007 *Sensors Actuators A* **135** 34–42
- [59] Choa S H 2005 *Microelectron. Reliab.* **45** 361–9
- [60] Mailly F, Dumas N, Pous N, Latorre L, Garel O, Martincic E and Nouet P 2009 *Sensors Actuators A* **156** 201–7
- [61] Lefevre E, Martincic E, Woytasik M, Leroux X, Edmond S, Pellet C, Nouet P and Dufour-Gergam E 2009 *Procedia Chem.* **1** 782–5
- [62] Oi K, Otake S, Shimizu N, Watanabe S, Kunimoto Y, Kurihara T, Koyama T, Tanaka M, Aryasomayajula L and Kutlu Z 2014 *IEEE 64th Electronic Components and Technology Conf. (ECTC)* pp 348–53
- [63] Murayama K, Aizawa M, Hara K, Sunohara M, Miyairi K, Mori K, Charbonnier J, Assous M, Bally J-P and Simon G 2013 *IEEE 63rd Electronic Components and Technology Conf.* pp 879–84
- [64] Sturcken N, O'Sullivan E J, Wang N, Herget P, Webb B C, Romankiw L T, Petracca M, Davies R, Fontana R E and Decad G M 2013 *IEEE J. Solid-State Circuits* **48** 244–54
- [65] Patti R S 2006 *Proc. IEEE* **94** 1214–24
- [66] Duan N, Liow T Y, Lim A E J, Ding L and Lo G Q 2012 *Opt. Express* **20** 11031–6
- [67] Dong Y *et al* 2014 *IEEE Trans. Electron Devices* **62** 128–35
- [68] Martinez N J, Gehl M, Derose C T, Starbuck A L, Pomerene A T, Lentine A L, Trotter D C and Davids P S 2017 *Opt. Express* **25** 16130–9
- [69] Huang M, Li S, Cai P, Hou G, Su T I, Chen W, Hong C-Y and Pan D 2017 *IEEE J. Sel. Top. Quantum Electron.* **24** 1–11
- [70] Li C, Xue C, Guo X and Liu Z 2014 *Asia Communications and Photonics Conf.* pp 1–3
- [71] Fahey P M, Griffin P B and Plummer J D 1989 *Rev. Mod. Phys.* **61** 289
- [72] Liu X Y, Windl W, Beardmore K M and Masquelier M P 2003 *Appl. Phys. Lett.* **82** 1839–41
- [73] Mathiot D and Pfister J C 1982 *J. Phys., Lett.* **43** 453–9
- [74] Kinoshita D, Qian R, Irby J, Hsu T, Anthony B, Banerjee S, Tasch A, Magee C and Grove C L 1991 *Appl. Phys. Lett.* **59** 817–9
- [75] Chen D, Xue Z, Wei X, Wang G, Ye L, Zhang M, Wang D and Liu S 2014 *Appl. Surf. Sci.* **299** 1–5
- [76] Luan H C, Lim D R, Lee K K, Chen K M, Sandland J G, Wada K and Kimerling L C 1999 *Appl. Phys. Lett.* **75** 2909–11
- [77] Colace L, Masini G, Assanto G, Luan H C, Wada K and Kimerling L C 2000 *Appl. Phys. Lett.* **76** 1231–3
- [78] People R, Bean J C, Lang D V, Sergeant A M, Störmer H L, Wecht K W, Lynch R T and Baldwin K 1984 *Appl. Phys. Lett.* **45** 1231–3
- [79] Maree P M J, Nakagawa K, Mulders F M, Van der Veen J F and Kavanagh K L 1987 *Surf. Sci.* **191** 305–28
- [80] Huang S, Li C, Zhou Z, Chen C, Zheng Y, Huang W, Lai H and Chen S 2012 *Thin Solid Films* **520** 2307–10
- [81] Shah V A, Dobbie A, Myronov M and Leadley D R 2011 *Thin Solid Films* **519** 7911–7
- [82] Liu Z, Hao X, Ho-Baillie A, Tsao C Y and Green M A 2015 *Thin Solid Films* **574** 99–102
- [83] Ghosh A, Clavel M B, Nguyen P D, Meeker M A, Khodaparast G A, Bodnar R J and Hudait M K 2017 *AIP Adv.* **7** 095214
- [84] Chong H, Wang Z, Chen C, Xu Z, Wu K, Wu L, Xu B and Ye H 2018 *J. Cryst. Growth* **488** 8–15
- [85] Masini C, Calace L, Assanto G, Luan H-C and Kimerling L C 2001 *IEEE Trans. Electron Devices* **48** 1092–6
- [86] Wei Y, Cai X, Ran J and Yang J 2012 *Microelectron. Int.* **29** 136–40
- [87] Currie M, Samavedam S, Langdo T, Leitz C and Fitzgerald E A 1998 *Appl. Phys. Lett.* **72** 1718–20
- [88] Oh J, Campbell J C, Thomas S G, Bharatan S, Thoma R, Jasper C, Jones R E and Zirkle T E 2002 *IEEE J. Quantum Electron.* **38** 1238–41
- [89] Chen C, Li C, Huang S, Zheng Y, Lai H and Chen S 2012 *Int. J. Photoenergy* **2012** 1–8
- [90] Li Q, Han S M, Brueck S R, Hersee S, Jiang Y-B and Xu H 2003 *Appl. Phys. Lett.* **83** 5032–4
- [91] Park J-S, Bai J, Curtin M, Adekoré B, Carroll M and Lochtefeld A 2007 *Appl. Phys. Lett.* **90** 052113
- [92] Colace L, Balbi M, Masini G, Assanto G, Luan H-C and Kimerling L C 2006 *Appl. Phys. Lett.* **88** 101111
- [93] Osmond J, Isella G, Chrustina D, Kaufmann R and von Känel H 2008 *Thin Solid Films* **517** 380–2
- [94] Xue C, Xue H, Cheng B, Hu W, Yu Y and Wang Q 2009 *J. Lightwave Technol.* **27** 5687–9
- [95] Balbi M, Sorianello V, Colace L and Assanto G 2009 *Phys. E* **41** 1086–9
- [96] Yu H-Y, Kim D, Ren S, Kobayashi M, Miller D A, Nishi Y and Saraswat K C 2009 *Appl. Phys. Lett.* **95** 161106
- [97] Zhou Z, He J, Wang R, Li C and Yu J 2010 *Opt. Commun.* **283** 3404–7
- [98] Yang H D, Kil Y-H, Yang J-H, Kang S, Jeong T S, Choi C-J, Kim T S and Shim K-H 2014 *Mater. Sci. Semicond. Process.* **22** 37–43
- [99] Chen L-Q, Huang X-Y, Li M, Huang Y-H, Wang Y-Y, Yan G-M and Li C 2015 *Optoelectron. Lett.* **11** 195–8
- [100] Shimbo M, Furukawa K, Fukuda K and Tanzawa K 1986 *J. Appl. Phys.* **60** 2987–9
- [101] Toyoda E, Sakai A, Isogai H, Senda T, Izunome K, Nakatsuka O, Ogawa M and Zaima S 2009 *Japan. J. Appl. Phys.* **48** 011202
- [102] Plach T, Hingerl K, Tollabimazraehno S, Hesser G, Dragoi V and Wimplinger M 2013 *J. Appl. Phys.* **113** 094905
- [103] Wang C, Higurashi E and Suga T 2008 *Japan. J. Appl. Phys.* **47** 2526
- [104] Howlader M M, Kagami G, Lee S H, Wang J G, Kim M J and Yamauchi A 2010 *J. Microelectromech. Syst.* **19** 840–8
- [105] Kibria M, Zhang F, Lee T, Kim M and Howlader M 2010 *Nanotechnology* **21** 134011
- [106] Howlader M R, Itoh H, Suga T and Kim M 2006 *ECS Trans.* **3** 191–202
- [107] Howlader M M R, Suga T, Itoh H and Kim M J 2006 *ECS Trans.* **3** 191–202
- [108] Howlader M, Wang J and Kim M J 2010 *Mater. Lett.* **64** 445–8
- [109] Howlader M M, Zhang F and Kim M J 2011 *J. Microelectromech. Syst.* **20** 17–20
- [110] Takagi H and Maeda R 2006 *J. Cryst. Growth* **292** 429–32
- [111] Howlader M and Zhang F 2010 *Thin Solid Films* **519** 804–8
- [112] Takagi H, Maeda R, Chung T R, Hosoda N and Suga T 1998 *Japan. J. Appl. Phys.* **37** 4197
- [113] Wang Y-H and Suga T 2010 *Proc. 60th Electronic Components and Technology Conf. (ECTC)* pp 435–9
- [114] Sakata M, Oyake T, Maire J, Nomura M, Higurashi E and Shiomi J 2015 *Appl. Phys. Lett.* **106** 081603
- [115] Liang J, Miyazaki T, Morimoto M, Nishida S and Shigekawa N 2013 *J. Appl. Phys.* **114** 183703
- [116] Morimoto M, Liang J, Nishida S and Shigekawa N 2015 *Japan. J. Appl. Phys.* **54** 030212
- [117] Higurashi E, Sasaki Y, Kurayama R, Suga T, Doi Y, Sawayama Y and Hosako I 2015 *Japan. J. Appl. Phys.* **54** 030213
- [118] Essig S, Moutanabbir O, Wekkeli A, Nahme H, Oliva E, Bett A and Dimroth F 2013 *J. Appl. Phys.* **113** 203512
- [119] Lin X, Liao G, Tang Z and Shi T 2009 *Microsyst. Technol.* **15** 317–21

- [120] Liao G, Zhang X, Lin X, Ma C, Nie L and Shi T 2010 *Front. Mech. Eng.* **5** 87–92
- [121] Breninford M, Colinge C, Holl S, Hobart K and Kub F J 2009 *J. Electrochem. Soc.* **156** H303–6
- [122] Holl S, Colinge C, Hobart K and Kub F J 2006 *J. Electrochem. Soc.* **153** G613–6
- [123] Lin X, Shi T, Liao G, Tang Z, Liu S and Nie L 2007 7th IEEE Conf. on Nanotechnol. (IEEE NANO) pp 754–8
- [124] Tong Q-Y, Gan Q, Hudson G, Fountain G, Enquist P, Scholz R and Gösele U 2003 *Appl. Phys. Lett.* **83** 4767–9
- [125] Ke S, Ye Y, Lin S, Ruan Y, Zhang X, Huang W, Li C and Chen S 2018 *Appl. Phys. Lett.* **112** 041601
- [126] Ke S, Lin S, Ye Y, Mao D, Huang W, Xu J, Li C and Chen S 2017 *J. Phys. D: Appl. Phys.* **50** 405305
- [127] Ke S, Ye Y, Wu J, Ruan Y, Zhang X, Huang W, Li C and Chen S 2019 *J. Mater. Sci.* **54** 2406–16
- [128] Ke S, Lin S, Ye Y, Mao D, Huang W, Xu J, Li C and Chen S 2018 *Appl. Surf. Sci.* **434** 433–9
- [129] Lin S, Ke S, Ye Y, Huang D, Wu J, Chen S, Li C and Huang W 2018 *J. Semicond.* **39** 113001
- [130] Van de Walle C G and Tuttle B R 2000 *IEEE Trans. Electron Devices* **47** 1779–86
- [131] Tong Q Y, Schmidt E, Gösele U and Reiche M 1994 *Appl. Phys. Lett.* **64** 625–7
- [132] de Lima M Jr, Lacerda R, Vilcarromero J and Marques F C 1999 *J. Appl. Phys.* **86** 4936–42
- [133] Tamaki T, Watanabe W and Itoh K 2006 *Opt. Express* **14** 10460–8
- [134] Kanbe H, Miyaji M, Hirose M, Nitta N and Taniwaki M 2007 *Appl. Phys. Lett.* **91** 142119
- [135] Kanbe H, Komatsu M and Miyaji M 2006 *Japan. J. Appl. Phys.* **45** L644
- [136] Kanbe H, Hirose M, Ito T and Taniwaki M 2010 *J. Electron. Mater.* **39** 1248–55
- [137] Kanbe H, Miyaji M and Ito T 2008 *Appl. Phys. Express* **1** 072301
- [138] Na N, Tseng C-K, Kang Y and Lee M-C M 2014 *Proc. SPIE* **8990** 899014
- [139] Tseng C-K, Tian J-D, Hung W-C, Ku K-N, Tseng C-W, Liu Y-S, Na N and Lee M-C M 2012 9th Int. Conf. on Group IV Photonics (GFP) pp 1–3
- [140] Li C, Xue C, Liu Z, Cheng B, Li C and Wang Q 2013 *IEEE Trans. Electron Devices* **60** 1183–7
- [141] Liu Z, Yang F, Wu W, Cong H, Zheng J, Li C, Xue C, Cheng B and Wang Q 2017 *J. Lightwave Technol.* **35** 5306–10
- [142] Byun K Y and Colinge C 2012 *Microelectron. Reliab.* **52** 325–30
- [143] Byun K Y, Fleming P, Bennett N, Gity F, McNally P, Morris M, Ferain I and Colinge C 2011 *J. Appl. Phys.* **109** 123529
- [144] Byun K Y, Ferain I, Fleming P, Morris M, Goorsky M and Colinge C 2010 *Appl. Phys. Lett.* **96** 102110
- [145] Gity F, Yeol Byun K, Lee K-H, Cherkaoui K, Hayes J M, Morrison A P, Colinge C and Corbett B 2012 *Appl. Phys. Lett.* **100** 092102
- [146] Gity F, Byun K Y, Lee K, Cherkaoui K, Hayes J M, Morrison A P, Colinge C and Corbett B 2012 *ECS Trans.* **45** 131–9
- [147] Gity F, Daly A, Snyder B, Peters F H, Hayes J, Colinge C, Morrison A P and Corbett B 2013 *Opt. Express* **21** 17309–14
- [148] Kiefer A M, Paskiewicz D M, Clausen A M, Buchwald W R, Soref R A and Lagally M G 2011 *ACS Nano* **5** 1179–89
- [149] Liu T C, Kabuyanagi S, Nishimura T, Yajima T and Toriumi A 2017 *IEEE Electron Device Lett.* **38** 716–9
- [150] Liu C, Toriumi A and Sun D 2018 *IEEE Int. Conf. on Electron Devices and Solid State Circuits (EDSSC)* pp 1–2
- [151] Razek N, Dragoi V, Jung A and von Känel H 2018 *ECS Trans.* **86** 191–7
- [152] Ke S, Ye Y, Wu J, Lin S, Huang W, Li C and Chen S 2018 *J. Phys. D: Appl. Phys.* **51** 265306
- [153] Ke S et al 2019 *IEEE Trans. Electron Devices* **66** 1353–60
- [154] Ruan Y, Liu R, Lin W, Chen S, Li C, Lai H, Huang W and Zhang X 2011 *J. Electrochem. Soc.* **158** H1125–H1128
- [155] Ferain I, Byun K Y, Colinge C, Brightup S and Goorsky M S 2010 *J. Appl. Phys.* **107** 054315
- [156] Miclaus C and Goorsky M S 2003 *J. Phys. D: Appl. Phys.* **36** A177