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Heterogeneous Integration in Co-Packaged Optics

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Abstract—Generative artificial intelligence (GAI) and Large Language Model (LLM) require data center to have higher bandwidth, and better energy efficiency. To achieve this, Co-packaged optics (CPO) is one of the future directions that leverages advanced packaging with integrated photonics. However, this tight integration complicates data center system design and multi-physics interactions, including electrical, optical, thermal, mechanical, and material aspects. In this paper, heterogeneous integration (HI) in CPO is discussed. Multi-physics packaging is exemplified with two cases. Challenges in HI technologies are reviewed and corresponding mitigation methods are provided, including (1) thermal crosstalk within the electrical domain and between the electrical and the optical interaction, (2) SIPI of wide-and-slow and narrow-and-fast channel links, and (3) pros and cons of interposer material. Integrated photonics part is introduced and is composed of (1) light sources, (2) optical coupling strategies, (3) fiber attach schemes with advanced packaging, and (4) integrated optical technologies, e.g. novel microlens, optical TSV, 3D waveguide, and optical 3DIC. This article aims to identify the key HI challenges in CPO and points out the potential solutions for future CPO system advancement.

Index Terms—Co-packaged optics, Data center, Silicon photonics, Multi-physics heterogeneous integration, Wireline communication

I. INTRODUCTION

AI, and LLM speed up the demand of high performance computing with high bandwidth due to the explosive growth of embedded parameters of neural network. In 2013, Alexnet with 60 million of parameters, which is a convolutional neural network (CNN) architecture, marks among the first to reach the training compute era of one Exa-FLOPS. In 2020, GPT-3, which is an autoregressive transformer model with 175 billion of parameters, requires one million Exa-FLOPs of computation. This is followed by GPT-4 with 1.8 trillion of parameters and by GPT-5 with estimated 3 to 5 trillion of parameters, as shown in Fig.1 (a).

The desired scale of computation inevitably generates the same scale of data, up to 90,000 petabits by 2027, as shown in Fig. 1(b). Energy and power consumption are both accelerated upward accordingly. In Fig. 1(c), for example, computing power with GAI alone may increase much faster than 200% in three years as compared to global energy generation ramping up merely 6% in three years. This indicates computing power may soon exceed global energy generation before new computing architectures are massively deployed in data centers.

Within the increased amount of energy, there is around 25% to 50% of consumption is through wired electrical and optical data communication although the transistor scaling is moving toward 1 aJ/b of energy efficiency. Therefore, the direction for future wireline scaling targets higher performance, higher data bandwidth, but at the same time lower power consumption per bit. One of the future solutions is through complex and compact HI that co-designs electrical, optical, thermal, mechanical, and material sub-parts.

Fig. 2 shows a conceptual example of ultimate compact integration of various components, including three-dimensional integrated circuits (3DIC), 3D memory, interposer/substrate, through silicon via (TSV), micro-fluid cooling channel, optical source, waveguide, optical transceiver, fiber attachment, etc. The 3DIC is a lump summation and can refer to any main dies, e.g. application specific integrated circuits (ASIC), switch dies, XPU, etc. The 3D memory can be represented by high bandwidth memory (HBM), etc. This level of integration targets minimizing resistive copper (Cu) electrical communication between the compute part, the memory part, and the optical part.

The challenge, however, is to co-optimize among multi-physics interactions. For instance, regarding the system design consideration between electrical, mechanical: when multiple chipsets are integrated on one substrate, this substrate is required to be large enough with margins to accommodate all the chip area. This large substrate dimension naturally has large warpage due to the material mismatch of various embedded core and build-up layers. Warpage affects the exposure depth of focus of a stepper during a lithography process, limiting minimum resolvable line and space (L/S) of Cu wires and traces. Cu L/S may restrain electrical routing of power, clock, signal, and isolation between chipsets. This requires significant optimization and back-and-forth efforts in electrical place and route, fan-out design, power integrity (PI), signal integrity (SI), loss compensation, etc. Warpage in a large substrate also puts limitation on reliable minimum bump pitch, dimension, and die-to-die spacing across the center and the edge area due to mechanical and reliability challenges. Die spacing, I/O pitch, and Cu L/S constrain fan-out routability and bump-to-bump distance for all the I/Os, affecting reach distance, bandwidth and bandwidth density, energy efficiency in various die-to-die communication protocols

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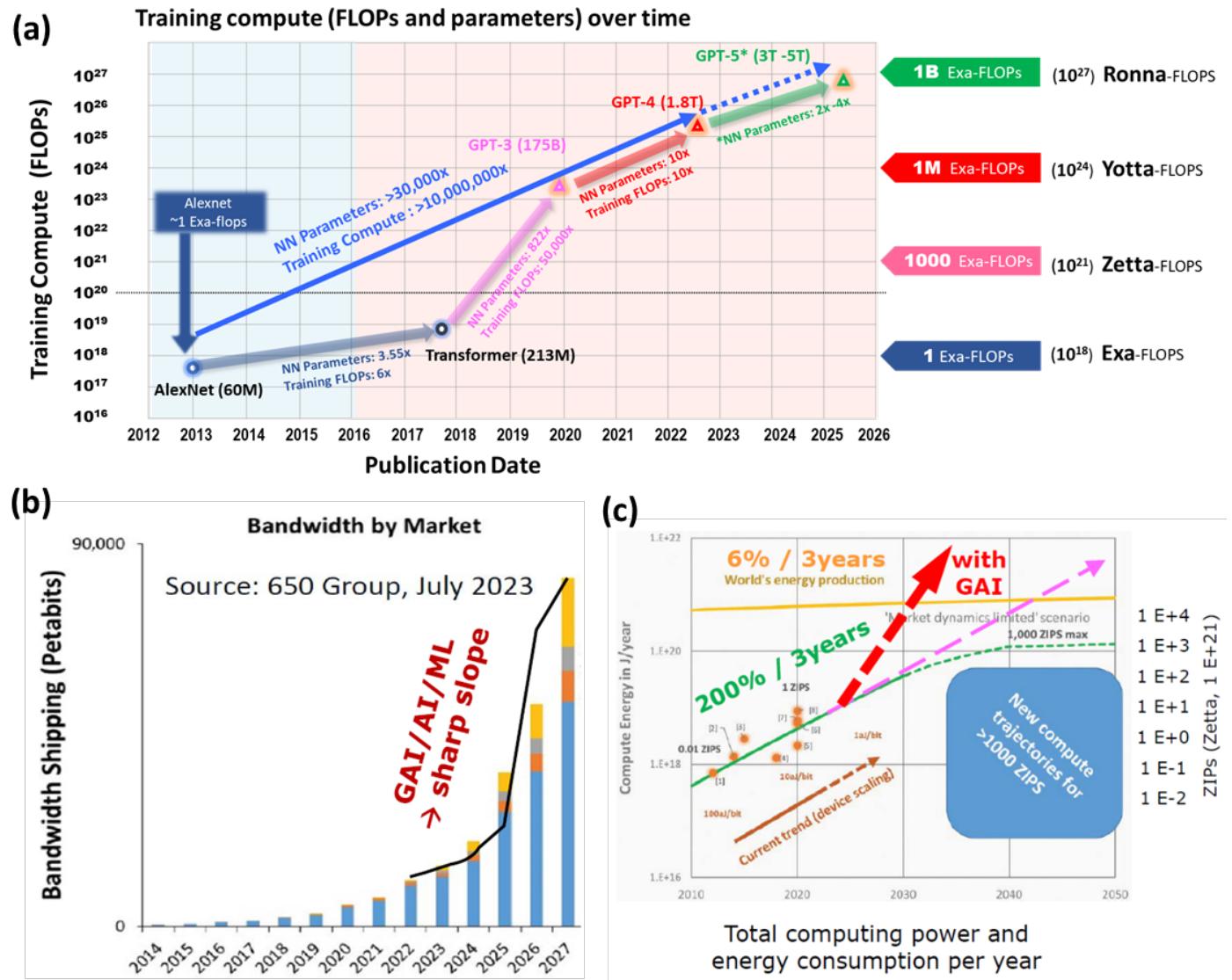


Fig. 1. (a) Growth of AI training and corresponding training compute required in FLOPS, GPT-5 is estimated based on early release [1-3] **(b)** Bandwidth shipping by market [1-3] **(c)** Total computing power and energy consumption per year [1-3]

Another example considering the system design drawing in Fig. 2 among electrical, optical, thermal, and mechanical: after electrical chips place and route optimization, electrical signals can go through vias (TVs) to optical transceivers vertically. This can lead to optimization of place and route for optical chips and waveguide, selection of integrated and standalone laser sources, and choice of optical connectivity and testing through an edge coupling or a grating coupling. The TV in an interposer can be leveraged as electrical TV and thermal TV and the height is related to the interposer/substrate thickness, which leads to tradeoff between SIPI in TV, warpage, and place & route due to keep-out zone constraints. When electrical and optical chipsets operate simultaneously, thermal hotspots are created, putting challenges in thermal crosstalk, including (1) electrical-to-electrical, and (2) electrical-to-optical. The thermal requirements for electrical chipsets are to be cooled under junction temperatures and to deal with a record-high thermal density. For optical chipsets, besides junction temperatures, the extra requirement is thermal stability and thermal-induced

reliability challenges in the component-level lasers, both of which require delicate system design optimization.

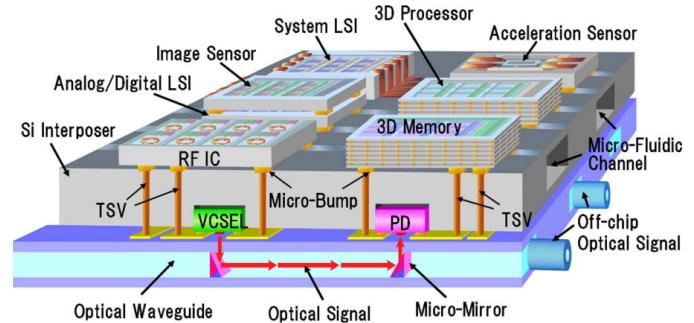


Fig. 2 Conceptual structure of one 3-D heterogeneous electrical and optical integrated system ©2011 IEEE [4]. The Vertical Cavity Surface Emitting Laser (VCSEL) in this figure is to illustrate optical source integration in a future system. For CPO applications, semiconductor lasers (e.g., DFB lasers and comb lasers) are commonly adopted.

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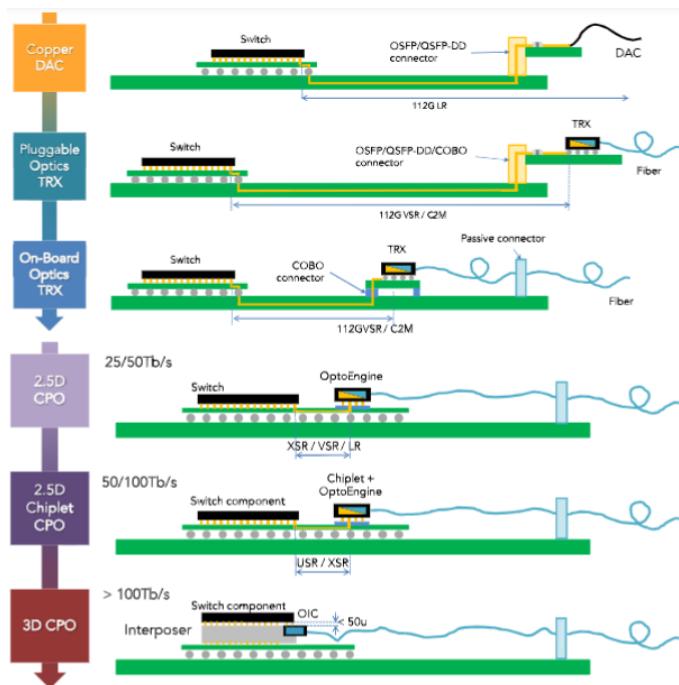


Fig. 3. CPO roadmap with tighter integration of EIC, PIC, and main dies. © 2021 [5]. This figure is openly licensed via CC BY-NC-ND 4.0

Among the real-world HI platforms, CPO is one of the cases that are similar to the integration scheme in Fig. 2 and the light source is replaced with semiconductor lasers. General optical connectivity consists of four major parts: (1) electrical integrated circuit (EIC) dies, including optical driver, transimpedance amplifier (TIA), retimer, (2) photonic integrated circuits (PIC): modulator, photodetector and optional laser source, (3) advanced packaging and integration, (4) fiber attach and optical coupling [6]. As shown in Fig. 3, the technology of CPO brings the front panel pluggable EIC& PIC closer to a main die and co-packages the main die and EIC& PIC on one substrate. Co-packaged schemes can be side-by-side 2.5D CPO, chiplet-based 2.5D CPO, and future on one interposer as stacked-based integration of 3D CPO, all of which are based on the high-bandwidth demand. This significantly reduces lossy and lengthy Cu traces for high-speed Serializer/deserializer (SerDes) application [7-11] and shorter reach of SerDes can be used for communication between optical transceiver dies and main dies. With much less equalizer on-chip design and without retimer chips, power consumption of wired electrical communication can be improved and the electrical beachfront bandwidth density can gradually match the optical counterpart. The technology of CPO has been demonstrated by various industrial companies, including MediaTek [12], Broadcom [13], Intel [14], Cisco [15], Marvell [16], and etc.

In this paper, advanced integration and optical coupling in CPO are the focus, as shown in Fig. 4. The challenges are introduced in section II, including electrical, optical, thermal, mechanical, and material.

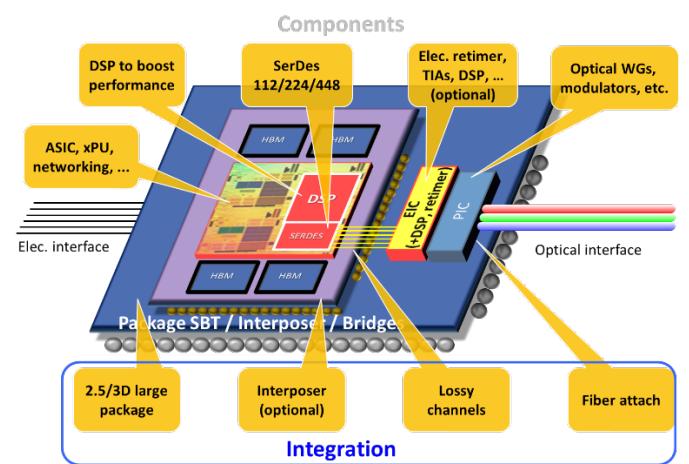


Fig. 4. Anatomy of co-packaged optics system. The integration part is the focus in this paper, including large package, interposer, lossy channel, and fiber attach [17]

II. HI CHALLENGES IN CPO

In this session, HI challenges are discussed as below: A. thermal, B. SI/PI of lossy channels, C. interposer/substrate material, D. light source, E. optical coupling strategy, F. fiber attach, and G. integrated optical technologies.

A. Thermal

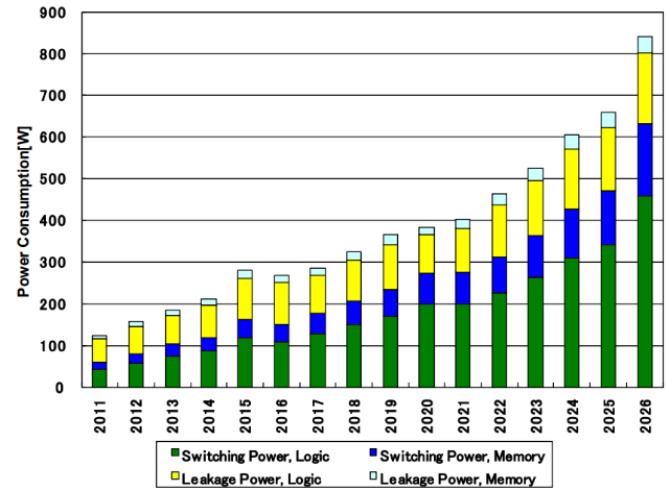


Fig. 5 Predicted power consumption based on logic and memory switching and leakage power ©2011 IEEE [18]

In a data center, a PCB system in a rack box is composed of several main dies (ASIC, XPU), HBM, and optics. With future higher bandwidth chipsets and stacking applications, the power consumption per socket may be much higher than 2 kW based on Fig. 5 and Fig. 6, which can be relaxed with CPO under the same bandwidth. Due to compact integration between high-power main dies, HBM and optics, this amount of power and density is still challenging to be cooled and can cause reliability issues and high failure-in-time rate when not properly addressed. The paragraphs below describe how thermal effect impacts a CPO system from electrical and optical perspectives and propose potential thermal solutions.

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Parameter	Current (2023)	Proposed (2035)
Architecture	Discrete GPU + CPU	xPU (CPU+GPU)
FP64 Flops	10^8	10^{21}
Socket Size (mm ²)	~1,000	~200,000
Silicon Area (mm ²) / Socket	4,000	500,000-1,000,000
Transistors (Billions) / Socket	100	10,000
Nodes	10,000	100
Socket power (kW)	2	100
Exaflops/MW(HPC - FP64)	15	1500
Total System Power (MW)	50-60	100-150

Fig. 6 Potential system attributes for the next era ©2023 IEEE [19]

For the electrical part, besides cooling the chipsets under device junction temperature, the new challenges are dealing with a record-high thermal design power (TDP) and corresponding thermal crosstalk. For example, HBM stacks multiple layers of Dynamic Random Access Memory (DRAM) and DRAM is sensitive to the transistor and capacitor leakage current, both of which can be significantly degraded in a high-temperature system and requires more frequent memory refresh operations. Due to a short-distance proprietary communication IP, HBM is inevitably assembled surrounding main dies with few mm distance, which leads HBM to be the thermal victim of high-power main dies. This thermal crosstalk stems from the lateral thermal transport through interposer, epoxy molding compound (EMC), and heat sink. Corresponding proper thermal isolation is needed: for example, reduced in-plane thermal conductivity of interposer and co-designed thermal isolation structure in heat sink. Besides side-by-side integration, there is a recent growing trend stacking memory directly on top of one main die, either with bare memory dies or with packaged chips. This gives higher bandwidth between memory and compute core but requires tighter thermal specs.

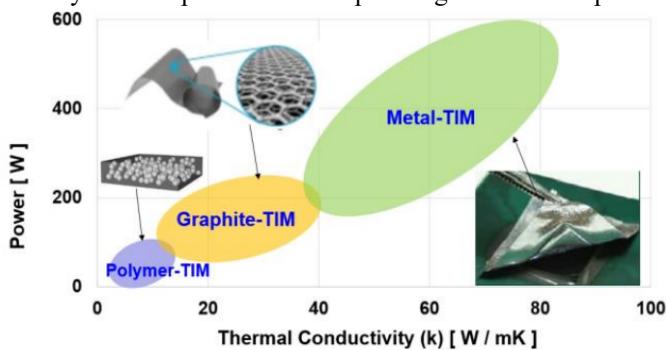


Fig. 7 Different types of TIM with corresponding thermal conductivity and target power usage ©2023 IEEE [21]

For optical chipsets, besides device junction temperature and thermal density in lasers, the new challenge is thermal uniformity and stability when nearby high-power main dies. In PIC, phases and wavelengths are key optical design parameters in waveguides, resonators, and modulators that are sensitive to refractive index change ($\text{dn}/\text{dT} \sim 10^{-4}\text{K}^{-1}$). Depending on multiplexing selections and types of modulators, dynamic

thermal crosstalk from proximal main dies may cause instantaneous temperature variation of a few degrees across modulation area. This can potentially lead to multiplexing instability in a system, which requires effective and timely thermal control to overcome aperiodic heat waves.

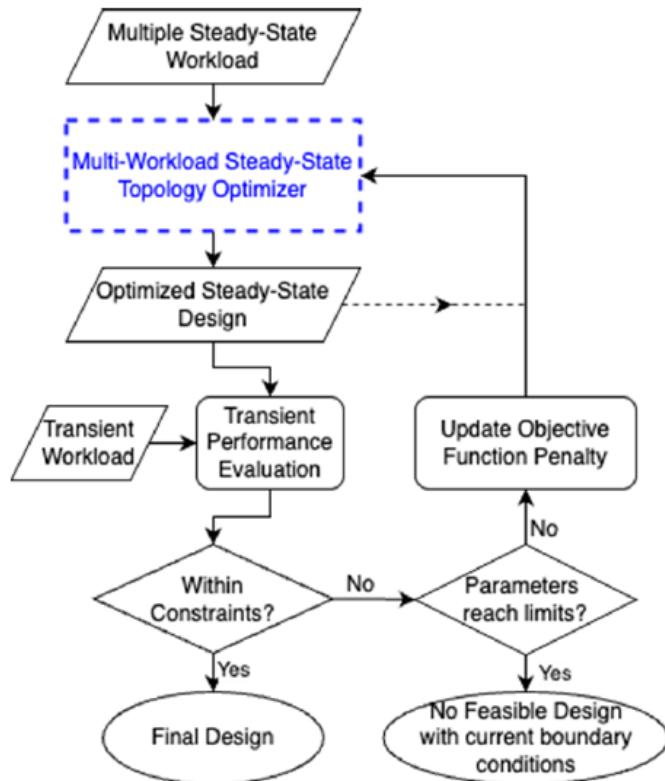


Fig. 8 Transient loads using an objective function penalization method ©2025 IEEE [23]

Considering thermal requirements of record-high TDP, thermal crosstalk, and thermal stability, novel cooling strategies will be needed. Liquid-based cooling technologies may be required for heat flux $>1\text{W/mm}^2$ [20]. Those technologies include two major categories: (1) devices direct contact w/ fluid: immersion cooling, electrowetting, etc; (2) devices indirect contact w/ fluid with thermal interface material (TIM) in between: two-phase heat pipe, jet impingement boiling, thermoelectric cooling, vacuum chamber, phase change material with pin fin heat sink, etc. The TIM layer is an intermediate material that sandwiches and fills out the uneven interface between main chipsets (ASIC, XPU, HBM) and indirect cooling methods. This facilitates thermal conduction flow and reduces thermal resistance along the pathway. The future direction for TIM development is to continue reducing thermal resistance, either through a higher thermal conductivity, k , or through thinner bottom-line thickness that is less than 100 um. As shown in Fig. 7, TIM can be categorized with three types: (1) polymer-based TIM, including grease, adhesive, etc, with k up to 15 W/mK, (2) metal and solder-based TIM, including alloys, metallic foils, etc, with k up to 80 W/mK, (3) carbon-based TIM, including graphite with k up to 40 W/mK [21], carbon nano tube with k up to 50 W/mK [22], diamond with k much higher than 100 W/mK. Besides cooling

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technologies and material innovation, recent research combines liquid-based microchannel heat sink with thermal-aware floor planning and topology optimization for continuous and transient main die workloads, which is one of the directions for future thermal design technology co-optimization, as shown in Fig. 8 [23].

B. SIPI of lossy channels

SIPI is a concept that applies to the quality of signal distortion, signal dispersion and power distribution in electronic systems. It affects the performance of a CPO system in a way that generally can be characterized through channel eye diagram, bit error rate, etc. SIPI is required to ensure reliable and stable operation and communication between main dies, HBM, EIC, and PIC on an interposer and a package substrate. Detailed analysis of SIPI is beyond the scope of the paper and two communication examples are illustrated in the paragraphs below: (a) between main dies and HBM, (b) between main dies and EIC.

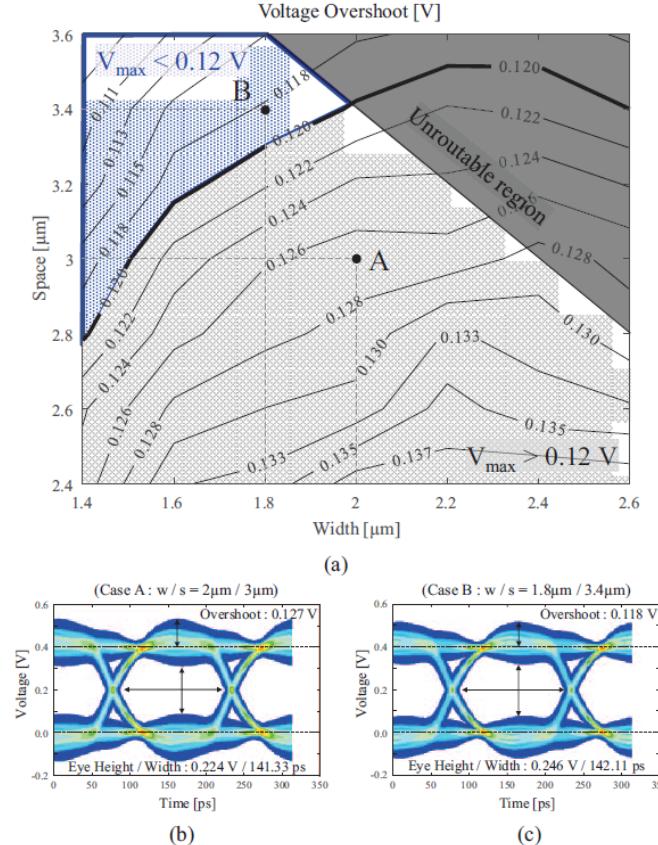


Fig. 9 Example of voltage overshoot based on varying channel dimension and eye diagram of (b) & (c) ©2024 IEEE [24]

Communication between main dies and HBM is through proprietary HBM IP that drives bump-to-bump distance of 5 mm with the frequency range adding margin potentially up to 10 to 15 GHz. SI metrics need to consider insertion/return loss, crosstalk, eye diagram (e.g., eye width and height, rising edge, falling edge, overshoot), timing skew and propagation delay, etc, as shown in Fig. 9. Those metrics are affected by RC,

layout, line and space, interposer, and package stack up (e.g., layers, material dielectric constant, loss tangent, and thickness [25, 26]). As shown in Fig. 10 (a), PI is affected by resistance, inductance, and time-varying current. Those values add up along the pathway, including microbump, Through Silicon Via (TSV), C4 bumps, redistribution layer, Plated Through Hole (PTH), BGA ball, as shown in Fig. 10 (b). The metrics in PI include IR drop, ripple, power droop, power delivery network impedance, as shown in Fig. 10 (c), etc. Electromagnetic interference of neighboring lanes, on the other hand, is growing severe and affects both SI and PI due to constraints of die area and die stacking.

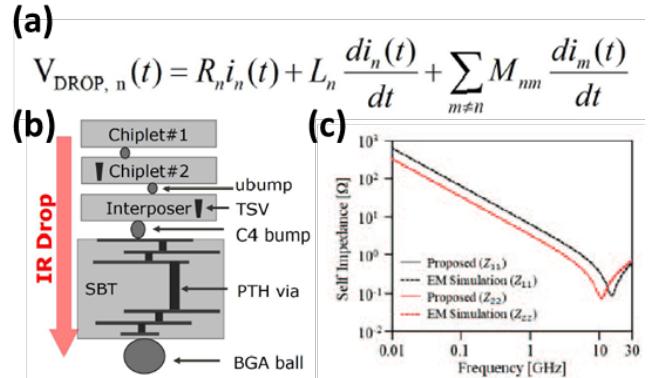


Fig. 10 (a) Voltage drop based on resistance, inductance, and time-varying current [27], (b) Lossy pathway from chiplet to BGA [27], (c) Example of PDN impedance ©2024 IEEE [24]

Communication between main dies and EIC can be through (1) wide-and-slow protocols, e.g., Universal Chiplet Interconnect express (UCIE) that supports bandwidth density up to 10 Tbps/mm, and (2) narrow-and-fast protocols, e.g., SerDes that supports up to 224Gbps per lane and beyond. The challenges for UCIE are similar to HBM protocols therefore not repeating the contents again. For high-speed SerDes beyond 100 Gbps, depending on modulation type, the required Nyquist frequency bandwidth adding margin goes up to 80 GHz or higher, within which frequency range the challenges are different from the UCIE and new mitigation methods are needed. Two examples are brought up as below.

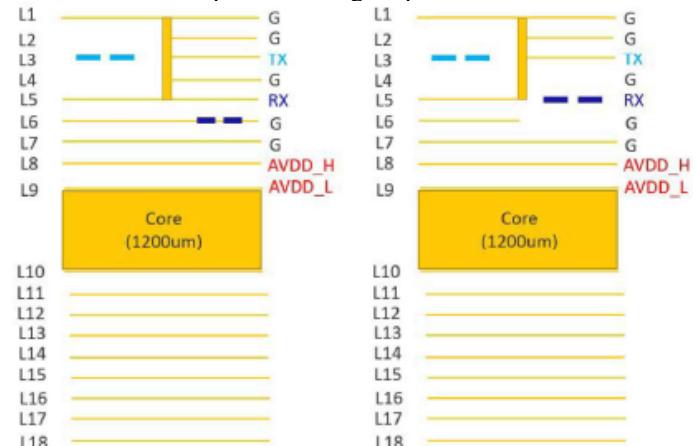


Fig. 11. Example of skip layer design for better SI of TX and RX for high-speed SerDes ©2024 IEEE [28]

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The first example is the package unit insertion loss, which can grow three-fold at Nyquist frequency even with the latest mitigation methods. Those techniques include lower-loss substrate core and build up layer material, thicker ABF film, smoother surface roughness, and skip layer routing design, as shown in Fig. 11. Besides material and substrate stack up, the bump design, e.g., pitch, ball size, pad scheme, wiring breakout style, etc., is another key improvement to reduce unexpected cavity resonance and to avoid additional modes within Nyquist frequency. Design examples include Hex pattern, as shown in Fig. 12 (a), ground fence, via junction, pattern optimization, and different wiring breakout style, as shown in Fig. 12 (b).

Skew tuning, which is another example, results from the length difference of differential signals and trace asymmetry. Skew can reflect on both trace insertion loss and common mode noise, which affecting the system link budget. Generally, 0.3 UI tolerance is allowed for skew and can be allocated for components along signal traces, including on-die, package, PCB, connectors, flyover cables, and environment, e.g., bending, twist, temperature, humidity, etc. The mitigation techniques include serpentine parameters tuned per stack up and impedance control.

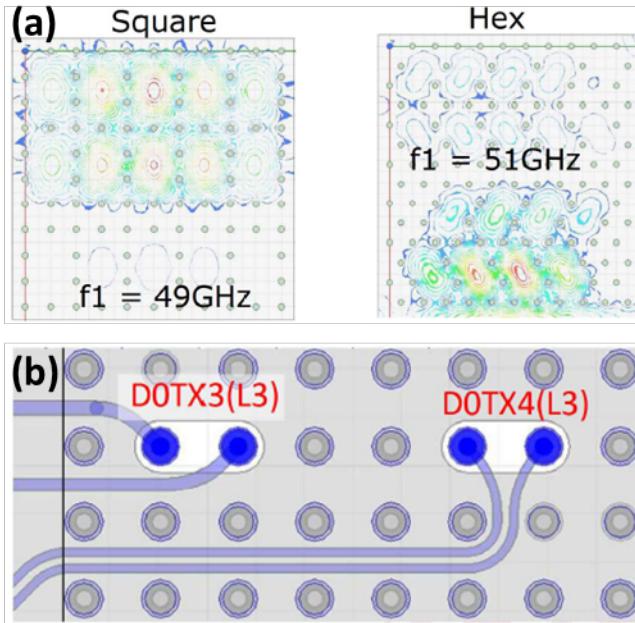


Fig. 12. (a) Example of pad arrangement scheme square vs hex, (b) Wiring breakout style ©2024 IEEE [28]

C. Interposer and substrate material

Interposer and substrate material is important to consider in CPO systems since it affects: (1) loss of communication channels and SIPI, (2) heat conduction and crosstalk, (3) stress and warpage. Paragraphs below briefly describe organic, Si, and glass material and their pros and cons.

Organic material has low-cost process and high-volume manufacturable for 20+ years. It is relative simpler to laminate layers on organic-based cores, through which 11 layers per side has been productized in HPC products [29] and 12 layers and above are under development. The package dimension, however, is limited between 100 mm and 120 mm per side, caused by large warpage across package. This results from

material difference in coefficient of thermal expansion (CTE), young's modulus, Poisson's ratio, and material stiffness. Those various material types include Cu, fiber glass core, ABF, underfill, Si, and bumps. SI of high-speed SerDes beyond 200 Gbps per lane is another challenge using organic material for interposer and substrate due to lossy dielectric material, thick thru-core, and rough surface. There are continuing efforts on pushing high-frequency extreme with organic substrate using lower loss material, e.g., polyphenyl-ethers (PPE), liquid-crystal polymer (LCP), polytetrafluoro-ethylene (PTFE), etc. [30]

Glass material is an emerging technology for low-cost, large-panel, and low-warpage process, which is improved by its tunable CTE and young's modulus that match close to Si dies and Cu traces. Those common glass types include Aluminosilicate, Boro-Aluminosilicate, Borosilicate, etc. Glass provides similar thermal conductivity as organic material, excellent low-loss core, and low surface roughness. Those properties make glass potentially one of material supporting high-speed SerDes beyond 200 Gbps. The integration level and layer count, however, are still under development and verification phase.

Although with much higher material and processing cost, Si interposer is predominantly used for high performance products that assemble main dies and HBMs with proximal hundreds of micrometers due to low-warpage surface. Si is proven to have precise-control and high-reliability process with high-volume manufacturing. Si, however, is an electrical conducting lossy dielectrics and cannot support long-reach high frequency SerDes on a large Si interposer and wafer-scale system [31], which requires new clock-forwarding, re-timing, fault-tolerant mesh network, etc. High thermal conductivity of Si interposer can be good heat spreader but on the other hand, it can cause significant thermal crosstalk when integrating high-power main dies close to HBM and PICs.

D. Light source

Current light sources for optical communication include uLED [32] and laser depending on the reach distance and link budget of intra-rack and inter-rack applications. The uLED light source, as shown in Fig. 13, is an emerging technology and mostly integrated in a large array with transmitters. This large array can provide massive wide-and-slow channels and light source redundancy for required reliability specification.

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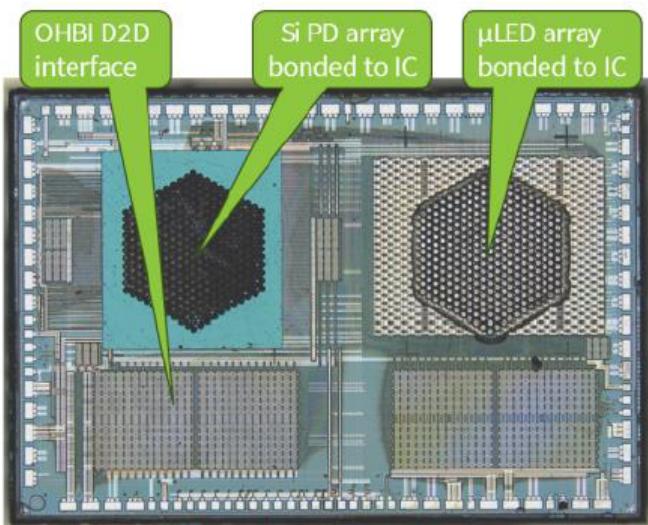


Fig. 13 Example of uLED light source integrated on chip
©2024 IEEE [32]

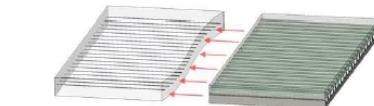
For current optical communication in CPO, the laser light source, including distributed-feedback laser (DFB) lasers and comb lasers, is still required due to much higher pristine optical output power. With wavelength division multiplexing (WDM), multi-lambda optical laser can leverage an array of single-lambda DFB or combs with a pump laser. Adoption of which type of laser involves CPO system and rack design in a data center, which beyond the scope of this paper. Lasers can be sourced internally within a PIC as integrated lasers and externally from a standalone laser module. Based on the III-V material processing before and after integration, integrated lasers can be classified as flip-chip bonded lasers and heterogeneous integrated lasers. The heterogeneous integrated laser has been experimentally proven to be reliable for years [33, 34], while the flip-chip bonded laser is under verification phase. External lasers, on the other hand, couple light into PIC through fiber to on-PIC waveguides. Although this creates higher optical loss due to multiple interfaces and fiber-core-to-waveguide misalignment, separation of laser sources from the main die package may reduce risks of laser reliability and increases multi-source interoperability and serviceability.

E. Optical coupling strategies

TABLE I Fiber coupling methods vs loss, bandwidth, alignment tolerance, and challenges. The coupling methods include grating, edge, evanescent, microlens, photonic wire bonding, vertical coupler [35], detachable coupling [36,37]

	Loss	Bandwidth	1 dB alignment tolerance	Challenges
Grating	>1.5dB	30-80 nm for 1dB	~2 um	High coupling loss
Edge	> 0.5 dB	>100 nm For 3dB		1.Alignment throughput 2.Wafer cleaving 3.Wafer sorting
Evanescent	> 0.1 dB	>300nm For 1 dB	>2.8 um	1.Exposed waveguide 2.precise alignment
Microlens	> 1.7dB		~30 um	1. Alignment 2. Automatic testing
Photonic wireboning	> 0.5dB	300nm For 1 dB		Laser writing time
Vertical coupler	<0.1	>100 nm	~2.5 um in Y & Z >50um in gap	
Detachable	<1.5 dB		+~ 40 um	

Conventional EC



Vertical Coupler

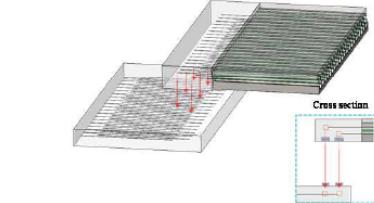


Fig. 14 Vertical coupler ©2024 IEEE [35]

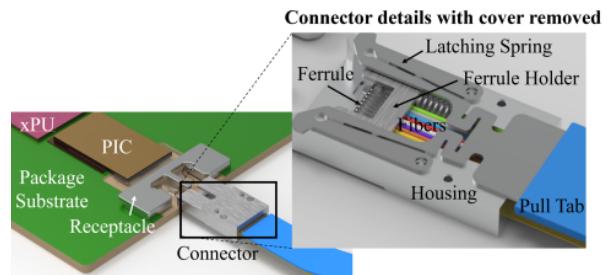


Fig. 15 Example of detachable connector design, including all the mechanical structure ©2023 IEEE [37]

Among all the coupling strategies, grating coupling (GC) and edge coupling (EC) are the main types. When GC is selected, it is limited by multiplexing types, angle of incidence, polarization, narrow bandwidth, and higher coupling losses although higher bandwidth density is possible with multiple rows of fibers. EC has properties of broad multiplexing and broadband capability, negligible polarization dependence and high coupling efficiency but wafer sorting is challenging. GC, EC and variants of EC (e.g. microlenses, evanescent, photonic wire bonding, vertical coupler as shown in Fig. 14) are summarized in the Table 1 [38] with corresponding loss, bandwidth, alignment tolerance and challenges. In the next session of fiber attach, EC will be exemplified.

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F. Fiber attach

TABLE II Fiber first vs. fiber last challenges [39-41]

	Fiber first	Fiber last
Mechanical handling and assembly	Delicate fiber module handling in each assembly process	Standard microelectronics assembly before fiber attach
Planarity during fiber attach	Best condition with Die-level warpage	Substrate-level adding lid-level
Strain relief	No	Yes by metal lid
Test of known-good sub-engines	yes	Not until assembly is done
Reflow compatible fiber and ferrule	Required high temperature ferrule	Not required

Edge coupling fiber attach can be classified in the assembly flow with two categories: fiber-first and fiber-last. In a fiber-first process, fiber arrays are positioned on a stress-free, nearly perfectly flat PIC. The PIC is controlled with uniform thickness, so after the initial setup of the assembly stage, no further adjustments are needed to maintain coplanarity between the V-grooves and fiber planes. In the fiber-last method, on the contrary, the fiber interface area is affected by the substrate warpage due to flip-chip soldering and underfill curing. Minimizing PIC assembly warpage is crucial to ensure that the parallelized fibers are fully inserted into the V-grooves with the pressure applied via the buffer lid. Thoughtful design and the selection of suitable substrate materials help reduce warpage and address optical fiber alignment challenges. The comparison of fiber-first and fiber-last approaches is summarized in Table II

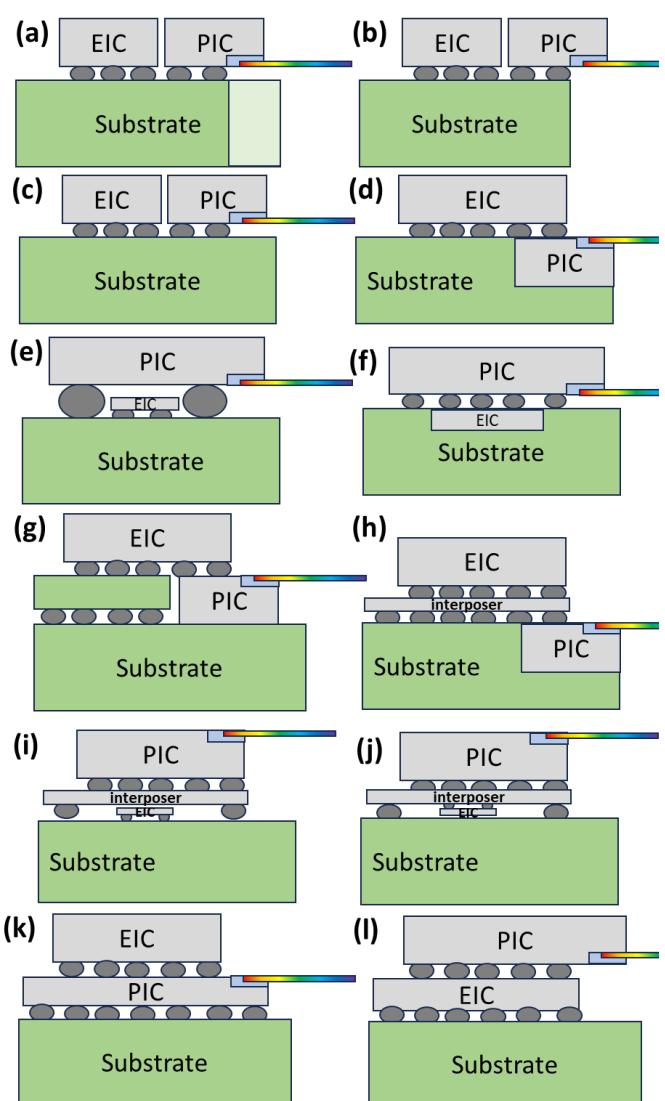


Fig. 16 Integration variants of EIC, PIC, interposer, fiber attach, and substrate [42]. The edge fiber attach can be either v-groove-based attach or multi-microlens-assisted methods.

In the advanced packaging, there are innovations for EIC and PIC assemblies, including side-by-side, embedded in substrate, 2.5D stacked on interposer, and 3D stacked. PIC can face up and face down with EIC and the edge fiber attach can be either v-groove-based attach or multi-microlens-assisted methods. As shown in Fig.16, the integration scheme includes a) to l) and each category is introduced as below:

- (a) Flip-chip EIC and PIC on a substrate with cut off at edge
- (b) EIC and PIC facing down and PIC protruding from the substrate edge
- (c) EIC and PIC facing down on substrate without cutout
- (d) PIC facing up and embedded in a recessed substrate with EIC/PIC direct 3D stacked,
- (e) PIC facing down soldering to a substrate with EIC thinned and solder on the same substrate
- (f) Embedded EIC facing up with PIC face-to-face
- (g) EIC facing down and partially on PIC facing up with another interposer or substrate
- (h) EIC on interposer with PIC embedded in substrate

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- (i) PIC on interposer with thinned EIC below interposer
- (j) PIC on interposer with thinned EIC flipped soldering on the other side of interposer
- (k) EIC on PIC 3D integration with TSV and PIC facing up. (l) PIC on EIC 3D integration with TSV and PIC facing down. The down-selection of those schemes is based on link budget and system design constraints.

G. Integrated optical technologies

Besides advanced packaging with fiber attach, there are integrated optical innovations targeting co-integration with electronics:

- (1) Integrated lens: a) Integrated lensed edge coupler formed by dielectrics, as shown in Fig. 17 [43], and b) Integrated Microlens Coupler (IMC): wafer-scale optical packaging with SU8-based spherical lens adding polymer waveguide [44]
- (2) Optical TSV: a) transmitting optical signals from substrate to PIC through micro-mirror, as shown in Fig. 18(a) [45], and b) interlayers on PIC through layer transfer process, as shown in Fig. 18 (b) [46]
- (3) Optical wafer scale processing: a) die-to-wafer assembly process for optically interconnected System-on-wafer, as shown in Fig. 19 [47], and b) wafer-scale waveguide, which is fabricated with stepper and design of reticle edges [48]
- (4) 3D waveguides: it is through 3D ultrafast laser inscription technologies for realizing arbitrary interfaces between the two different systems, as shown in Fig. 20 [45]
- (5) Conceptual optical 3D IC with electrical and optical co-wiring, as shown in Fig. 21 [49].

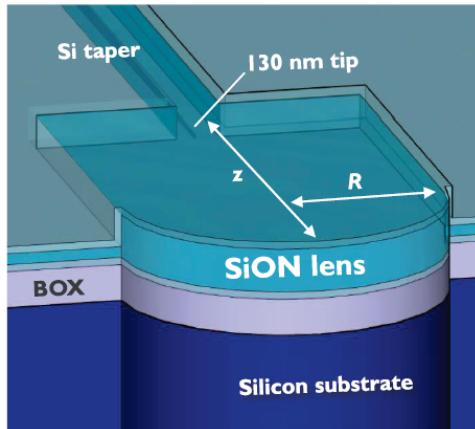


Fig. 17 Integrated lensed edge coupler ©2018 IEEE [43]

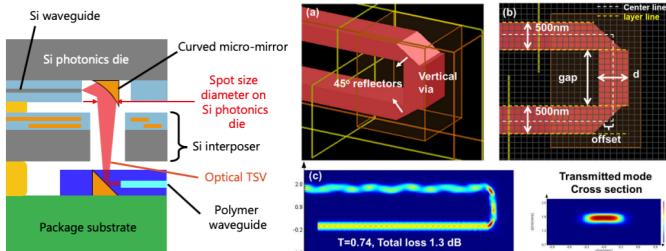


Fig. 18 (a) Optical TSV implemented through curved micro-mirror ©2019 IEEE [45] (b) Optical TSV implemented through angled interconnects and layer transfer ©2020 IEEE [46]

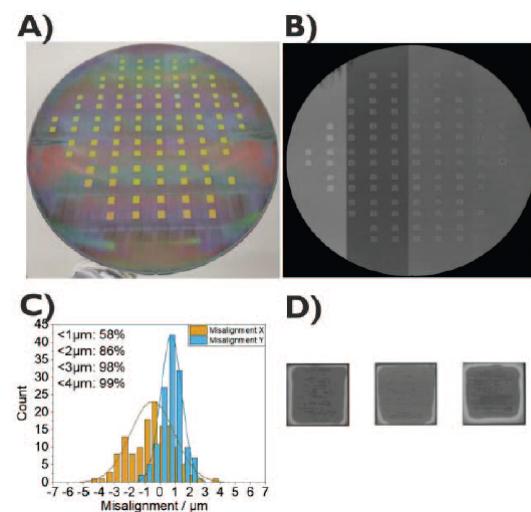


Fig. 19 Die-to-wafer assembly process for optically interconnected System-on-wafer ©2024 IEEE [47]

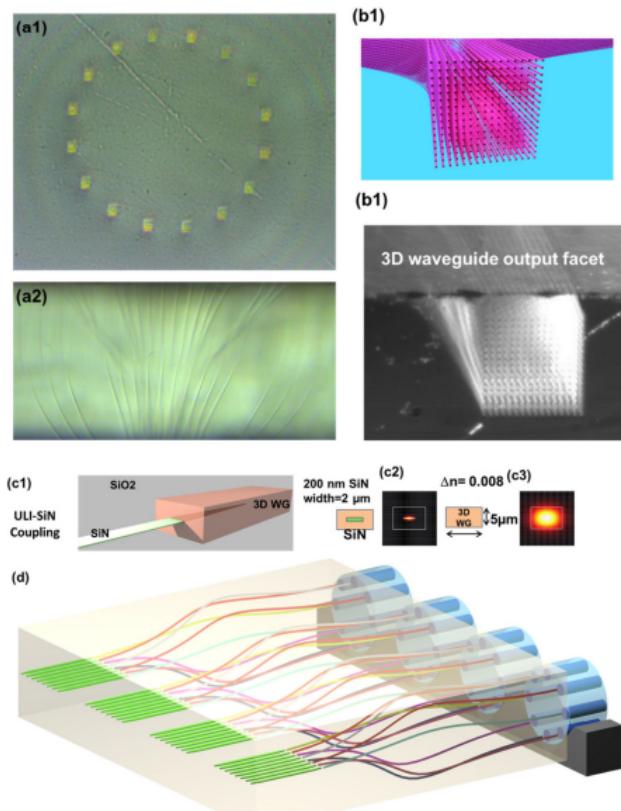


Fig. 20 3D waveguides through 3D ultrafast laser inscription technologies ©2020 IEEE [45]

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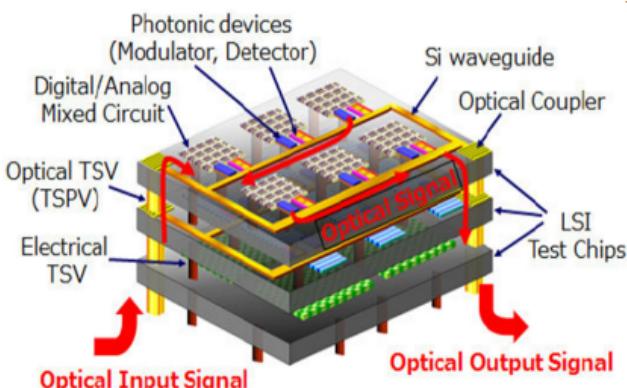


Fig. 21 Conceptual drawing of 3DIC with electrical and optical routing and signaling ©2023 IEEE [49]

V. CONCLUSION

In this paper, heterogeneous integration in CPO is discussed. Multi-physics packaging is exemplified with two cases, including a system design consideration between electrical and mechanical, and another system design consideration between electrical, optical, thermal, and mechanical. Challenges in HI technologies are discussed, and mitigation methods are provided: (1) thermal crosstalk within the electrical domain and between the electrical and the optical interaction, both of which can be minimized with novel cooling methods, TIM development, and cooling adding thermal-aware floor planning and topology optimization, (2) SIPI of wide-and-slow and narrow-and-fast channel links, which can be reduced by better isolation, pad arrangement scheme, new wiring breakout, skip layer stackup, impedance control, and serpentine skew control, (3) analysis of pros and cons of organic, Si and glass as interposer and substrate material. Optical technologies are introduced, including light sources of uLED and laser, coupling of GC and EC and EC variants, fiber attach process innovation with advanced packaging, and integrated optical technologies, e.g. novel microlens, optical TSV, 3D waveguide, and optical 3DIC. This article points out the key HI challenges and the potential solutions in CPO, paving the way for faster development of future CPO technologies.

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