Bridging the information gap....

BERTScope™ Family

BERTScope™ S

- Stress and advanced analysis for complete compliance testing

- High Speed BERT
- Sampling Scope
- Stressed Eye Generator
- Mask Tester
- Jitter Analyzer
- Error Analyzer

- Faster compliance testing
- Faster time to market
- More information you can use

The Vision of a Scope, the Confidence of a BERT, and Clock Recovery you can Count on.

SYNTHESYS RESEARCH, INC.

BERTScope - The Logical Evolution of Test

Ever viewed a performance problem in the waveform, error and jitter domains? Why doesn't the information ever tie together? The BERTScope family is the next generation of signal integrity equipment that provides multiple views to help you find answers more quickly.

The BERTScope family provides a new approach to signal integrity testing to 12.5 Gb/s. The various models comprising the BERTScope family are shown below (new models highlighted in yellow):

Capability	Type	0.1 to 7.5 Gb/s	0.1 to 12.5 Gb/s
Stressed	Generator and Analyzer	BERTScope S 7500B	BERTScope S 12500B
	Generator Only		BERTScope SPG 12500B
Non-stressed	Generator and Analyzer	BERTScope 7500A	BERTScope 12500A

Some of the BERTScope's contributions are:

Usability

Troubleshooting BERT set-ups often used to take longer than the real work of solving design problems. It is very difficult to get lost with the simple graphical layout, and many measurements are one-button.

Carefully matched twin decision points give deep eye diagrams and the ability to easily move between measurement domains from time, jitter and BER and have results correlate together. They also enable parametric measurement of live data signals, an area previously closed to high speed BERTs.

Innovations Providing New Capabilities

Modern analysis needs rely crucially on the precise control of time. The BERTScope's novel automatic delay calibration ensures accurate analysis of jitter, BER Contour etc. at the exact time, temperature and bit rate currently in use.

Patented error analysis uncovers relationships between individual errors to accelerate troubleshooting.

A New Generation

Many legacy instruments are out of support life, and expensive to repair. This new generation instrument has been designed to be more robust, with inputs more resistant to abuse, and exchangeable APC-3.5 front panel connector crowns for user swap-out if damage occurs, or you wish to change connector type.

The flagship BERTScope has everything you will need to perform receiver compliance testing and advanced analysis. Featuring easy and flexible stress testing, physical layer analysis such as BER Contour and Jitter measurements, and the new Compliance Contour view for mask/BER comparison, the BERTScope S represents a breakthrough in insight and saved development time.

New BERTScope "B" Features at a Glance

- ✓ Comprehensive range of differential divided clock outputs for supplying test devices with an instrument-grade clock
- ✓ External clock input upgraded to allow imposition of stress
- ✓ Optional Spread Spectrum clock (SSC) and Data Generation
- ✓ Analysis (using clock recovery if desired) of signals with SSC
- ✓ Analysis of physical layer parameters such as eye diagrams and jitter while the input signal has SSC on it.
- ✓ BER and eye diagram measurements down to 100Mb/s, operable with the internal clock or an external clock.
- ✓ Variable depth eye and mask measurements to allow correlation with shallow sampling scope measurements or a deeper, more revealing view of device performance
- ✓ Optical measurement units for eye diagrams with an external optical reference receiver
- ✓ Active measurement and graphing of BERTScope clock recovery loop bandwidth and peaking
- ✓ Optional jitter tolerance compliance template testing with margin testing
- ✓ Analyzer with greater than 20 GHz bandwidth for superior jitter, Q factor and eye measurement accuracy and fidelity.

BERTScope™ S

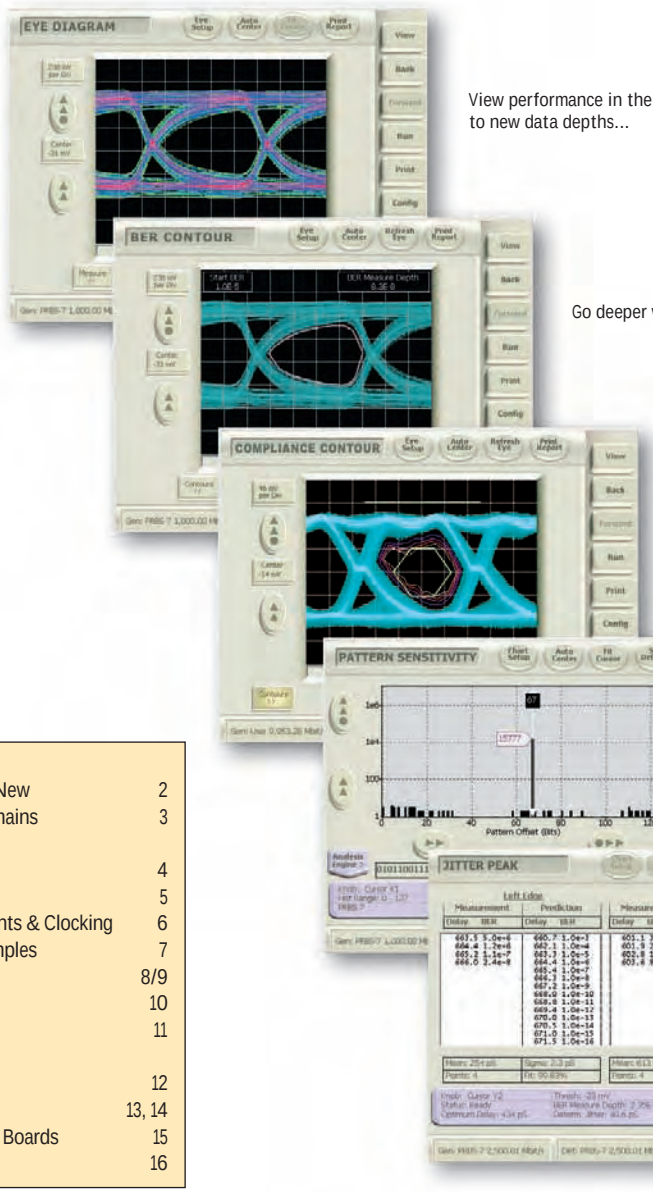
"Having seen customers struggle with testing high-speed components, we realized that a new approach was essential. This new approach, the BERTScope family, precisely ties together eye diagrams with bit error rates to provide the missing link between the time, error and jitter measurement domains. This enables the solving of problems that are 1 in a trillion as easily as solving problems that are 1 bit in 10."

Tom Waschura
Chief Technology Officer
SyntheSys Research Inc.

Linking Domains

Eye diagrams have always provided an easy and intuitive view of digital performance. It has been harder to tie this directly with BER performance, as the instruments that provide views of each have been architected in fundamentally different ways. Eye diagrams have been composed of shallow amounts of data that have not easily uncovered rarer events. BERTs have counted every bit and so have provided measurements based on vastly deeper data sets, but have lacked the intuitive presentation of information to aid troubleshooting. This has lead to an information gap between BERTs and sampling scopes.

Imagine being able to quickly and easily view an eye diagram based on at least two orders of magnitude more data than conventional eyes (see page 5). Seeing a feature that looks out of the ordinary, you are able to place cursors on the item of interest and by simply moving the sampling point of the BERT, use the powerful Error Analysis capabilities to gain more insight into the feature of interest. For example, check for pattern sensitivity of the latest rising edges. Alternatively, use one button measurement of BER Contour to see whether performance issues are bounded or likely to cause critical failures in the field. In each case information is readily available to enhance modeling or aid troubleshooting, and is available for patterns up to 2^{31}-1 PRBS.



View performance in the time domain to new data depths...

Go deeper with one-button BER Contour...

Compare standards specified masks at 10^{-12} levels with measured BER Contour to easily see whether your device complies.

Pick a feature to examine more deeply... and analyze exactly the pattern sequence behind it.

Easily export high quality information to your favorite modeling software.

Brochure Contents

Transmitter Testing Made Easy

Whether you are making electrical or optical measurements, the BERTScope will give you insight that is just not available anywhere else. You get more information that you can actually use. Recent additions to the BERTScope firmware now mean that the depth in eye diagram and mask testing is variable, making it easy to correlate to sampling scope results.

Testing optical transmitters with BERTScope mask testing and a Picometrix® wide wavelength photo-receiver

Data-Rich Eye Diagrams

As shown on the facing page, there is an impressive difference in data depth between conventional eye diagrams taken with a sampling oscilloscope and those taken with a BERTScope. So what does that mean? It means that you see more of what is really going on – more of the world of low probability events that is present every time you run a long pattern through a dispersive system of any kind, have random noise or random jitter from a VCO – a world that is waiting to catch you out when your design is deployed. Adding to this the deeper knowledge that comes from the one-button measurements of BER Contour, Jitter Peak and Q Factor, and you can be confident that you are seeing the complete picture – a picture that doesn't rely on extensive extrapolation from architectures with shallow measurement depth.

Deep Mask Testing

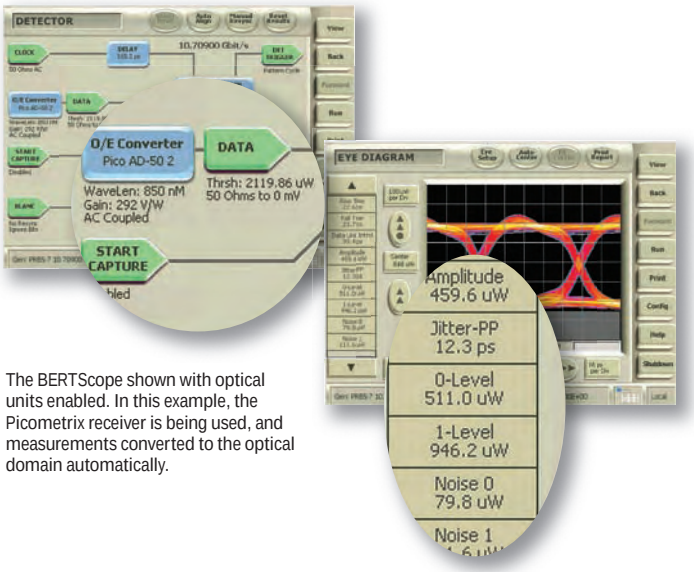
The depth advantage gained for eye diagrams is at least 10 times greater for mask testing. Unlike pseudo-mask testing offered by some BERTs, a BERTScope mask test samples every point on the perimeter of an industry standard mask, including the regions above and below the eye. Not only that, but each point is tested to a depth unseen before. This means that even for a test lasting a few seconds using a mask from the library of standard masks or from a mask you have created yourself, you can be sure that your device has no lurking problems.

Accurate Jitter Testing to Industry Standards

Testing with long or short patterns, the most accurate jitter measurement is likely to come from the methodology that uses little or no extrapolation to get it's result. With the BERTScope, you can quickly measure to levels of $1x10^{-8}$, or wait for the instrument to measure $1x10^{-12}$ directly. Either way, the BERTScope's one-button measurements are compliant to the MJSQ jitter methodology, and because the underlying delay control is the best available on any BERT, you can be sure that the measurements are accurate. Use the built-in calculations for Total Jitter (TJ), Random Jitter (RJ) and Deterministic Jitter (DJ) or easily export the data and use your own favorite jitter model.

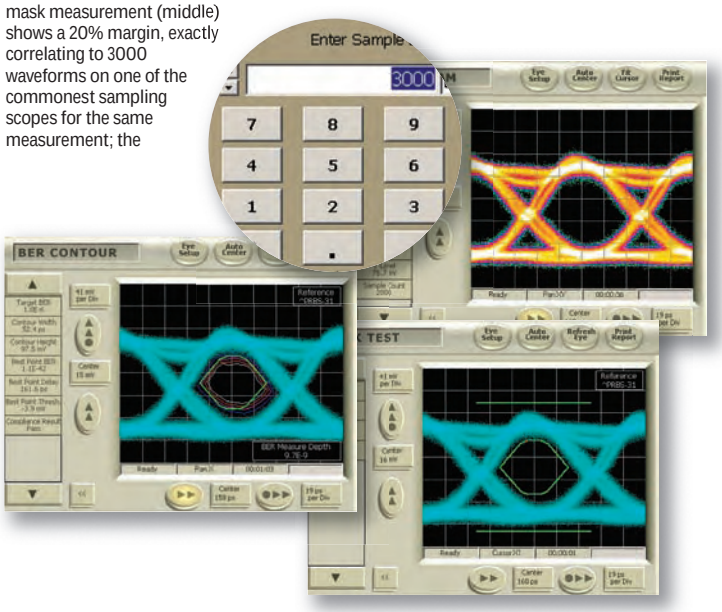
Mask Compliance Contour Testing

Many standards such as XFP/XFI and OIF CEI now specify mask tests intended to assure a specified $1x10^{-12}$ eye opening. New Compliance Contour view makes this easy by taking a mask, and overlaying it on your measured BER contours – so you can immediately see whether you have passed the mask at whatever BER level you decide.

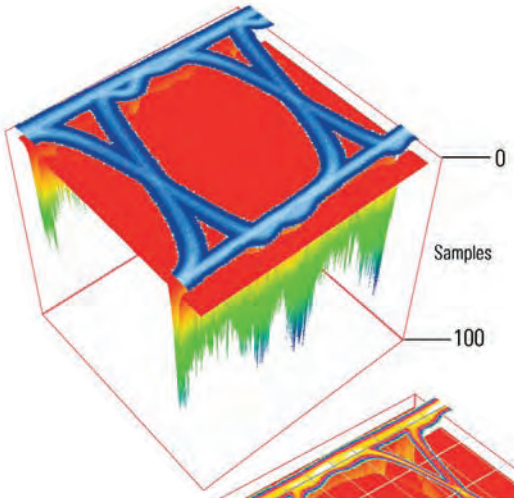


The BERTScope shown with optical units enabled. In this example, the Picometrix receiver is being used, and measurements converted to the optical domain automatically.

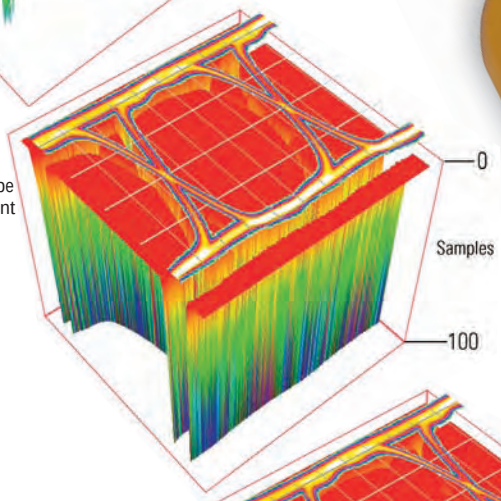
Using variable sample depth, it proves to be very easy to move between revealingly deep measurements, and shallow measurements that match those of a sampling scope. The measurements in this group show an optical transmitter eye diagram (top). With the depth dialed up to 3000 waveforms, the mask measurement (middle) shows a 20% margin, exactly correlating to 3000 waveforms on one of the commonest sampling scopes for the same measurement; the results become even more impressive when measurement time is included – 30 seconds on the sampling scope, 1 second on the BERTScope. The lower screenshot shows the same device being tested against a $1x10^{-6}$ BER mask using Compliance Contour, and showing that it passes with 17% margin even at that depth.



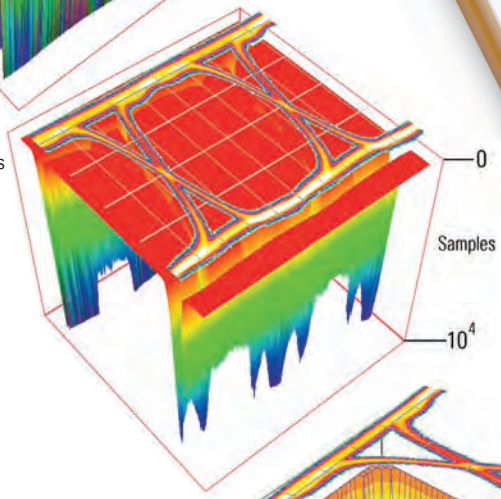
A Question of Depth....



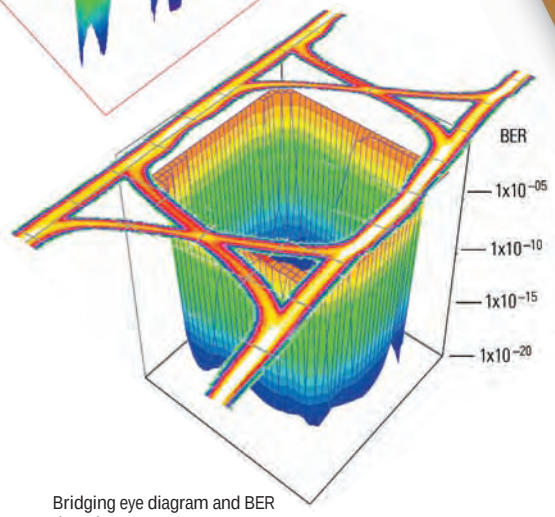
The first photo shows the sample depth of a conventional equivalent-time sampling oscilloscope, measuring for around 10 seconds.



The second picture shows the sample depth of a 10 second BERTScope eye diagram measurement at standard depth, on the same scale as the one above.



Plotting the same data in the second picture on a scale 100 times smaller shows that the depth of measurement of a BERTScope eye is at least 100x the depth of a conventional sampling scope.



Bridging eye diagram and BER domains, a BER Contour measurement gives even greater depth to uncover problematic performance issues.

"We need to understand what's limiting the performance of the devices we are developing. The eye diagram options on the BERTScope are great because they provide so much data depth. To really probe deeply, the BER Contour and Jitter measurements show us what's actually going on. The BERTScope helps us a lot to be more effective in our research."

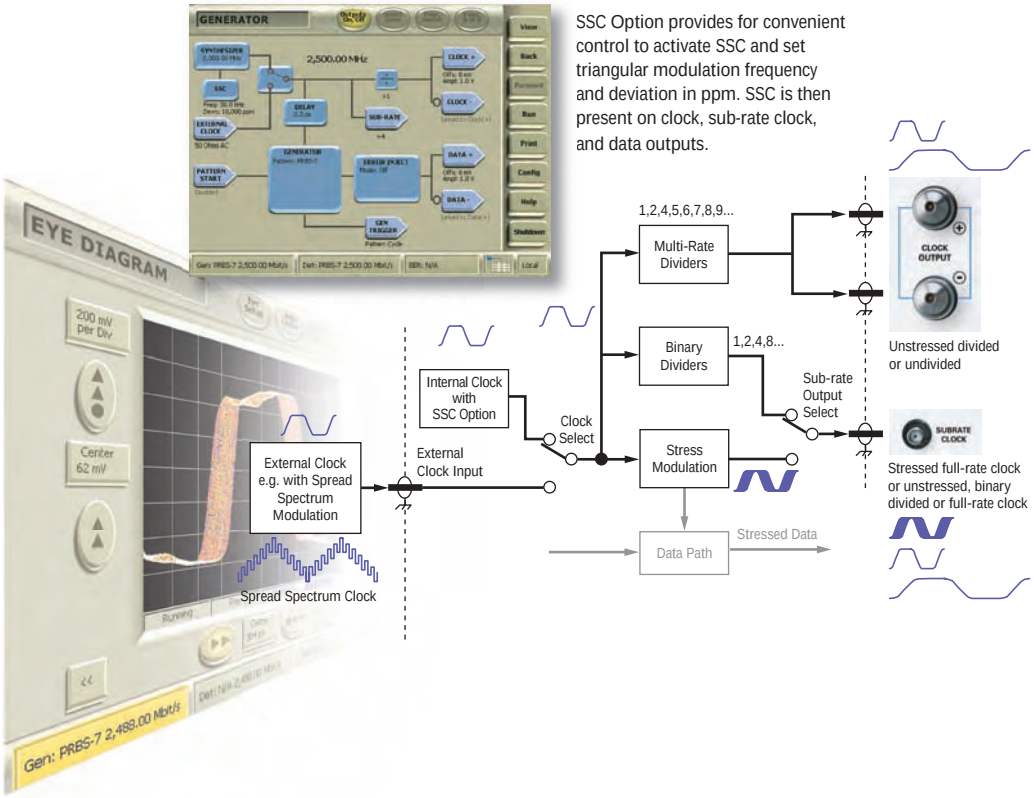
Alexei Glebov
Research Scientist
Fujitsu Labs of America

Flexible Clocking

The new generator clock path features in the BERTScope S and BERTScope SPG provide the test flexibility needed for emerging real-world devices. Whether computer cards or disk drives, it is often necessary to be able to provide a sub rate system clock, such as 100MHz for PCI-Express. To get the target card running may require a differential clock signal with a particular amplitude and offset; this is easily accomplished with the new BERTScope architecture, with many flexible divide ratios available.

Another common need is to synchronize both sides of a transceiver, including any SSC modulation. In combination with a BERTScope CR, the generator external clock input may be used to create a synchronized clock signal to the generator; from this, any of the on-board stress elements may be applied without restriction, or a clean full or divided clock provided.

An additional advantage is measurement of BER and eye diagram analysis down to 100MHz, with either the internal, or an external clock.

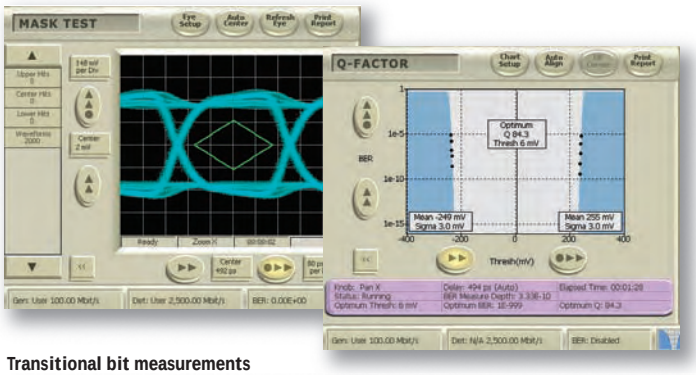


SSC Option provides for convenient control to activate SSC and set triangular modulation frequency and deviation in ppm. SSC is then present on clock, sub-rate clock, and data outputs.

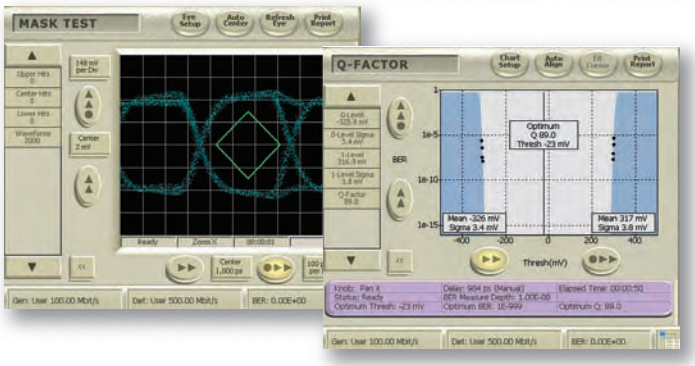
Example: PCI-Express Transmitter Measurements

The screenshots show compliance measurements made with the BERTScope. The PCI-Express card was tested in a compliance test board, and the BERTScope provided a 100MHz differential clock signal with the correct amplitudes and offset. The card output was measured using the required compliant loop bandwidth clock recovery, provided by a BERTScope CR instrument.

De-emphasized bit measurements

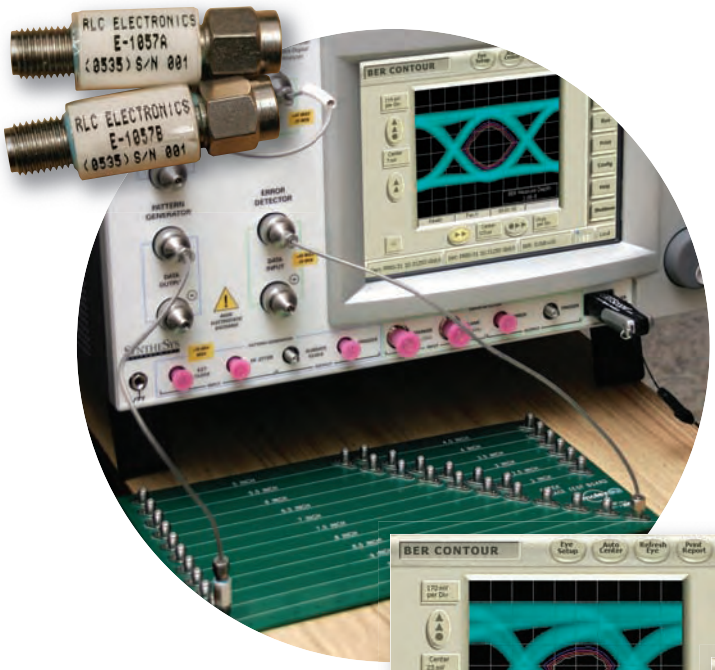


Transitional bit measurements



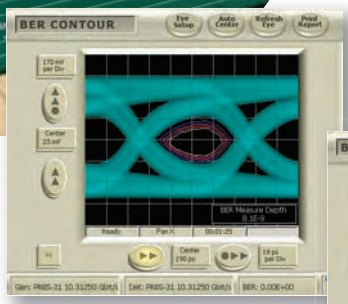
On the upper left is shown the test device passing the appropriate compliance mask. On the upper right, the same signal is measured with Q Factor to get an accurate value for the de-emphasized mean amplitudes. The lower two screenshots show the same measurements for the transitional bit.

There are two things to notice; firstly, the transitional bit was easy to isolate by triggering with a divide-by-5 sub rate clock from the CR – this allows all five bit periods of the data word to be viewed separately as eye diagrams. Secondly, it is straignt forward to calculate the de-emphasis ratio from the means of the two Q Factor measurements.

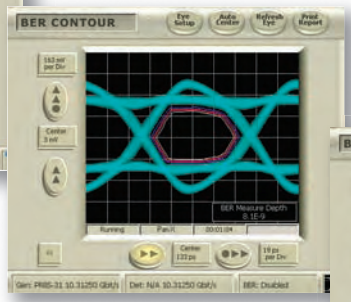


Example: Filter XFI Measurement

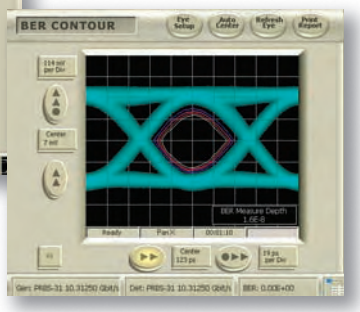
The XFP MSA describes use in some tests of an equalizing filter. In this example, the effectiveness of such a filter to overcome the effects of circuit board dispersion is clearly evident. The BERTScope measurements shown are of BER Contour, showing that the eye opening is significantly improved even at deep BER levels.



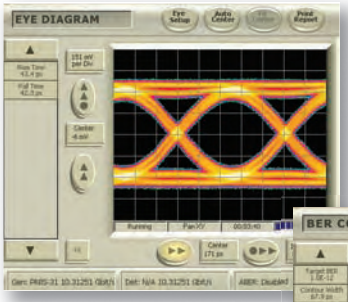
Circuit board dispersion



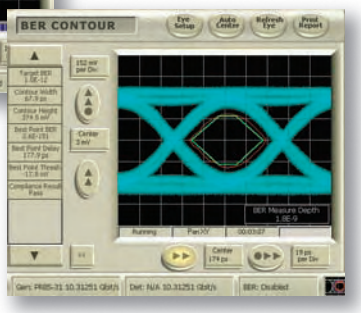
The effect of the filter alone



Filter and circuit board combined



XFI rise/fall time testing



XFI C' (receiver electrical output) mask test at $1x10^{-12}$ depth

Example: XFP Module Measurements

In addition to 10Gb/s optical interfaces, the XFP MSA describes a 10Gb/s serial electrical interface for the circuit board side of the transceiver, known as XFI. The XFP optical receiver has an electrical output, defined as the point C', and it must meet transmitter eye specifications. Two are shown here: the upper one is a rise/fall time measurement on an eye diagram. The second is a mask measurement. The specification states that this test must be passed at a depth of $1x10^{-12}$ - impossible to measure directly on a sampling scope, but easy to accomplish with a BERTScope using Compliance Contour.

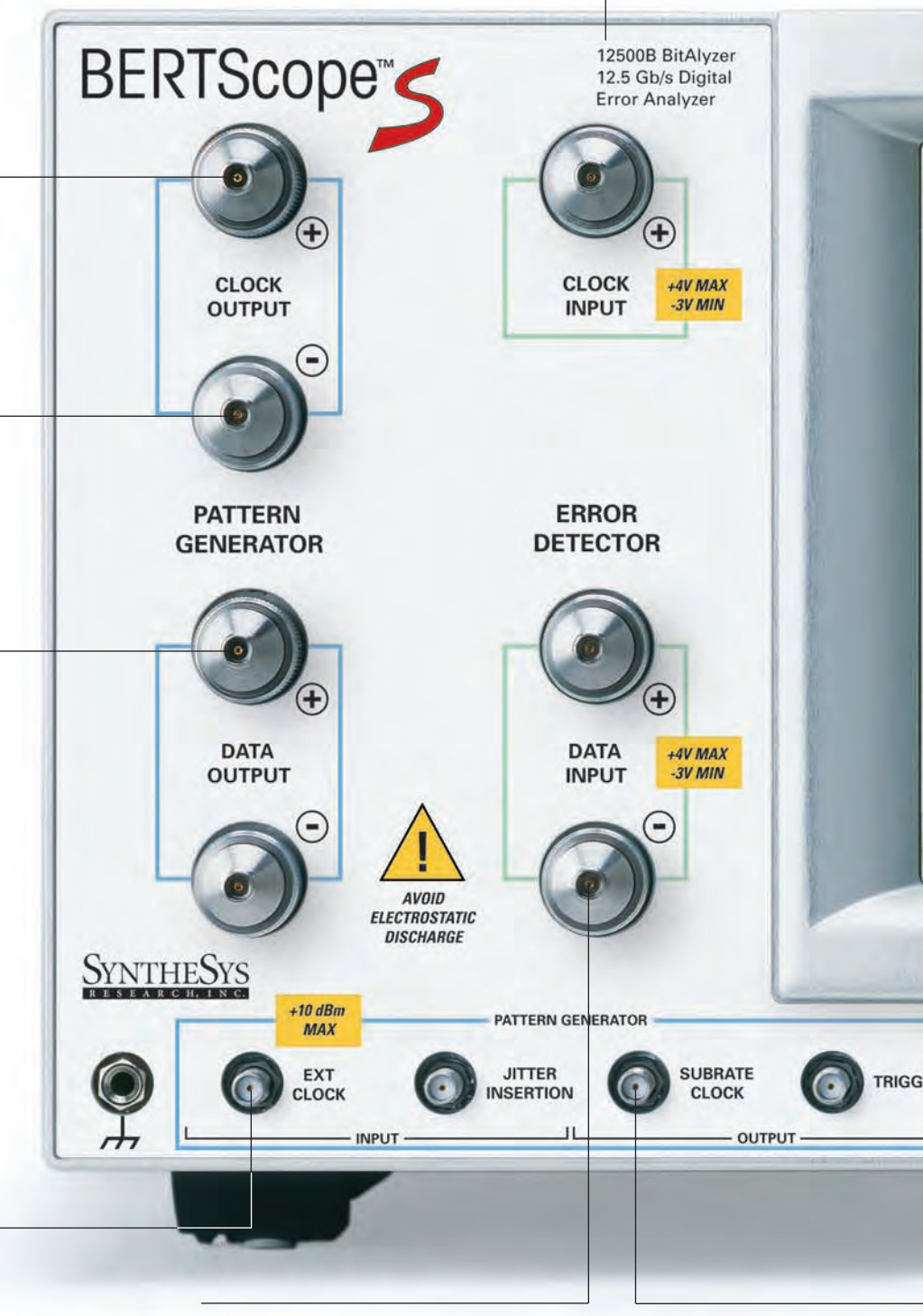
Not Just a Pretty Face

User-replaceable APC-3.5 Planar Crown® connector adapter and unique protection circuitry on high speed interfaces mean your measurement up-time will be in a different league to BERTs you've experienced before.

12.5 Gb/s now or order the 7.5 Gb/s 7500B and upgrade it when your needs grow.

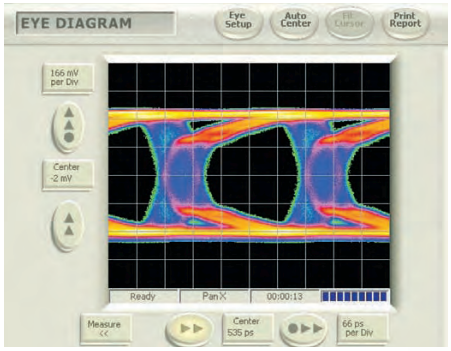
BER and eye diagram measurement down to 100 Mb/s with internal or external clock

Planar Crown connector adapters may be user-exchanged to other connecter types such as N-type.



A formidable list of clock divide ratios are now available from the differential clock output as well as full-rate, with full amplitude, offset and termination control.

High quality, low jitter outputs assure your device is being stimulated by an instrument quality signal.



The BERTScope S makes testing receivers and clock recovery circuits a breeze with the integrated stress generator.

Add stress to clock and data outputs of the BERTScope using an external clock input. This allows the actual SSC clock from the device under test to be used as the source for test signal generation.

Complementary data outputs and inputs to allow characterization of the real world performance of differential devices

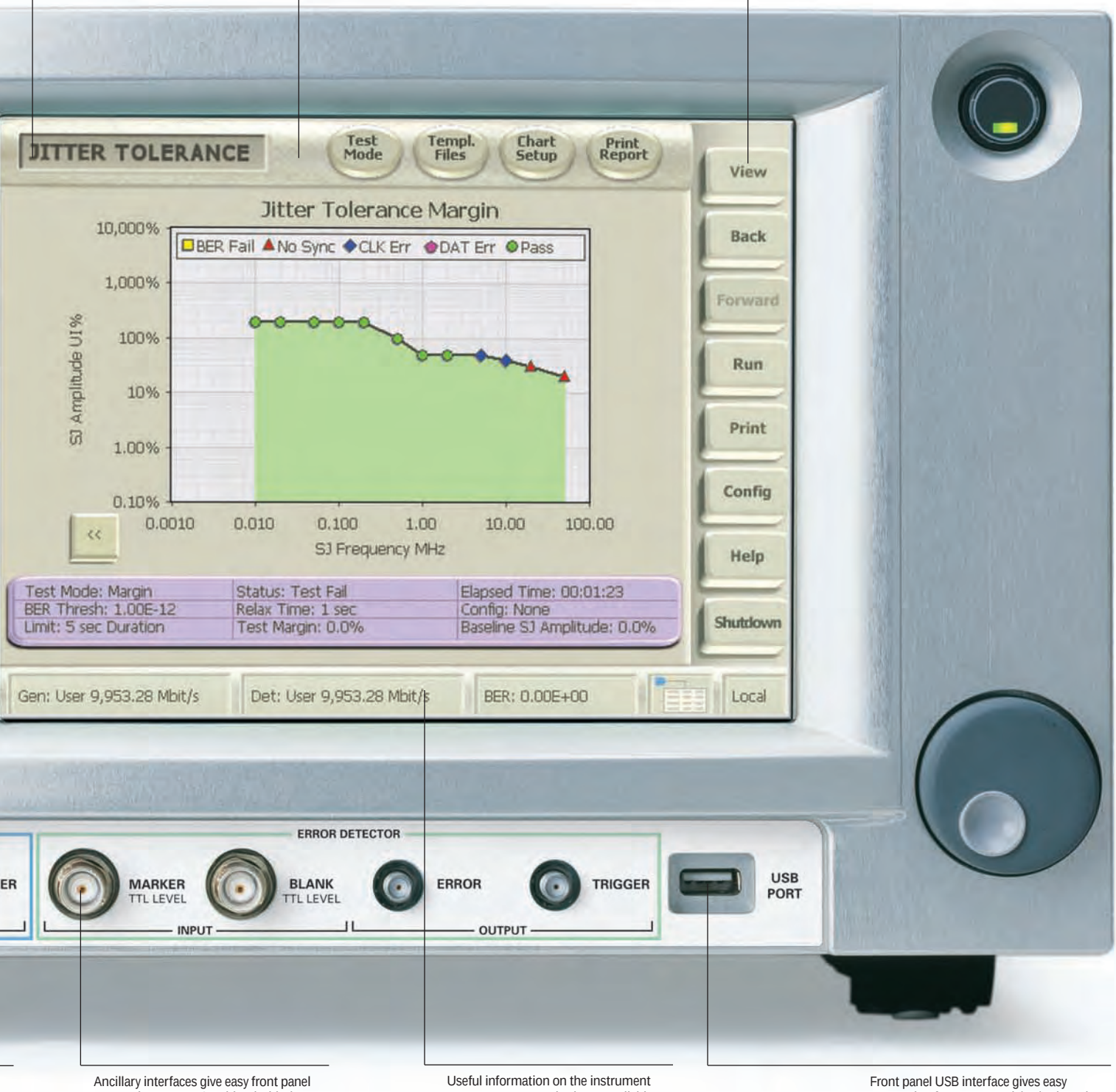
Stressed full-rate clock or unstressed, binary divided/ full-rate clock

Planar Crown is a registered trademark of Aeroflex/ Weinschel, www.aeroflex-weinschel.com

Jitter tolerance testing is easy, with many industry-standard templates ready to go

Acknowledged as the easiest to use bit error analyzer available – the logical and consistent user interface gives you the information you need clearly at all times. Access features using the touch screen, front panel control knob or using a keyboard and mouse. Many measurements require the touch of a single button.

Intuitive displays can be navigated easily using web browser-like buttons

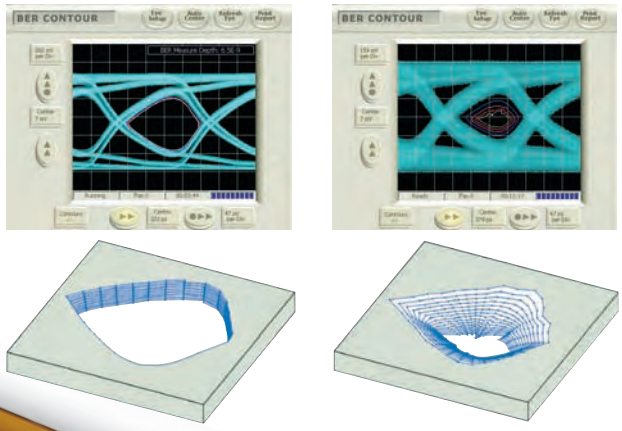


Ancillary interfaces give easy front panel connection access. Combined with the comprehensive rear-panel set, these give you impressive flexibility in instrument use.

Useful information on the instrument measurement state is always available, and the use of color-coding for non-standard conditions means you never get lost.

Front panel USB interface gives easy connection for memory sticks, keyboard and mouse or other peripherals

Channel Testing



BER Contour of a backplane operating at 4.25 Gb/s with two different patterns: CJTPAT (left) and 2^{31}-1 PRBS (right). Below each is the same data exported and plotted in 3-dimensions as an 'Eye Bowl'.

Channels take many forms, from trans-oceanic fiber links to inches of FR-4 at speeds never originally envisaged such as specified in OIF CEI and IEEE 802.3ap. They all count as hostile environments, pushing the limits of link performance. While classical fiber and satellite links tend to be noise-limited, modern bus and backplane connections are more likely to be jitter limited.

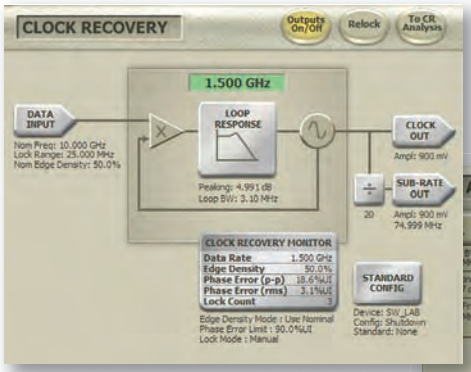
Whatever the limitation, it is often a challenge comparing real-world performance with the predictions of simulation software. For example, backplanes are often measured in S-parameter terms, but these need to be combined with transmitter parameters to be able to get an idea of the eye that a receiver will eventually see.

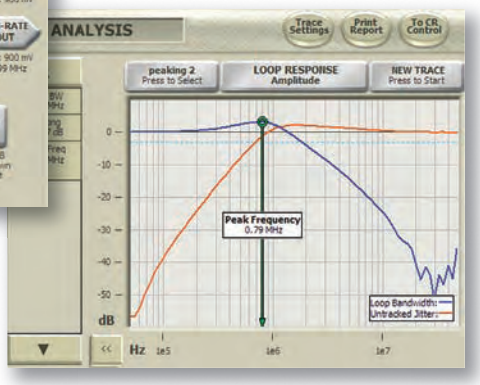
With all of the assumptions required, the role of real-world measured data becomes increasingly important. This is where BER Contour makes an intuitive link between theory and practice. It also plays a useful role in setting up the template for receiver jitter tolerance testing.

The examples shown at the top of the page are of an experimental backplane with two different patterns - CJTPAT, a Fibre Channel short jitter pattern, and 2^{31}-1 PRBS, a much longer pattern. The more aggressive nature of the PRBS pattern is readily visible, with infrequently occurring pattern combinations causing significant dispersion effects.

Add Clock Recovery

The BERTScope CR 12500A adds new levels of flexibility in compliant clock recovery. Most standards requiring jitter measurement specify the use of clock recovery, and exactly which loop bandwidth must be used. Using a different or unknown loop bandwidth will make it almost certain that you will get the wrong answer. The new clock recovery instrument enables easy and accurate measurements to be made to all of the common standards.



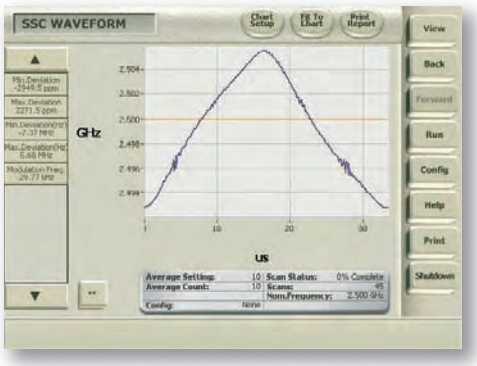


An intuitive user interface allows easy control of precise parameters. It also offers automated measurement of loop performance with graphed results. It is straightforward to employ markers for closer investigation.

The BERTScope CR and CRJ's usefulness are not just confined to BERTScope measurements. Use them standalone in the lab with your real time and sampling oscilloscopes, or with existing BERT equipment. Compliant measurements are available to you by pairing either of these versatile instruments with your existing investments.

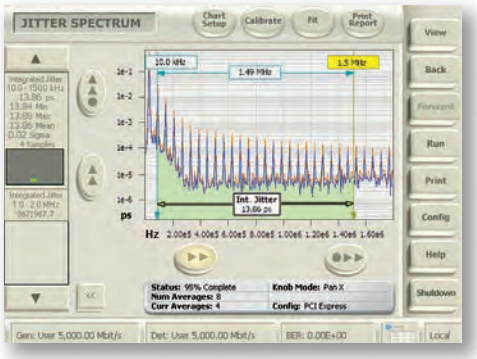
Display and Measure SSC Modulation Waveform

Spread spectrum clocking (SSC) is used by many of the latest serial busses including SATA, PCI-Express, FB-DIMM, and next generation SAS in order to reduce EMI issues in new board and system designs. The BERTScope CR and CRJ provide spread spectrum clock recovery together with the display and measurement of the SSC modulation waveform. Automated measurements include minimum and maximum frequency deviation (in MHz or ppm) and modulation frequency. Also included are display of the nominal data frequency and easy to use vertical and horizontal cursors.



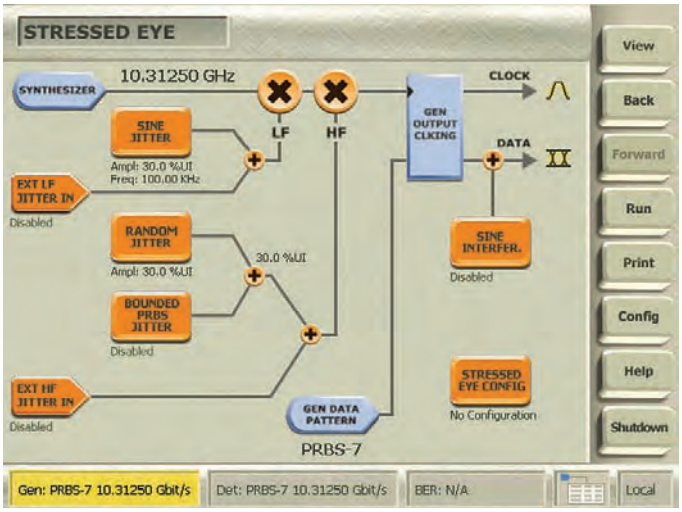
Add Jitter Analysis

Combine BERTScope CRJ 12500A with BERTScope for variable clock recovery, duty cycle distortion (DCD) measurement, and real-time jitter spectral analysis. Display jitter spectral components from 200 Hz to 90 MHz with cursor measurements of jitter and frequency. Measure band-limited integrated jitter with user-settable frequency gated measurements (pre-set band limits and integrated jitter measurement for PCI-Express Gen2 jitter spectrum in this example).

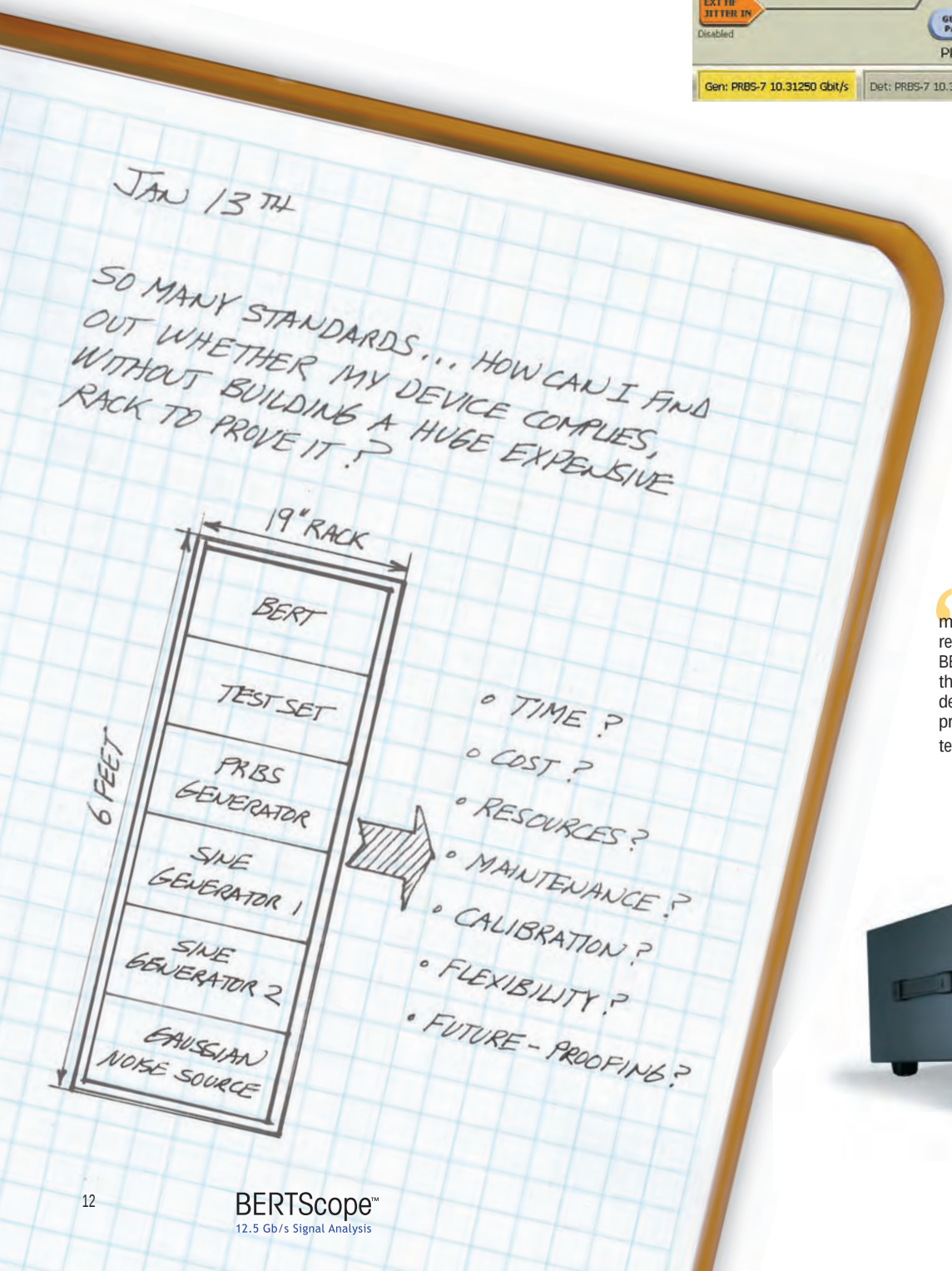


Taking the Stress out of Receiver Testing

As networks have changed, so have the challenges of testing receivers. While tests such as BER and receiver sensitivity are still important, receiver jitter tolerance has evolved to be more real-world for jitter-limited systems such as gigabits per second data over back planes and new high speed buses. Stressed Eye testing is becoming increasingly common as a compliance measurement in many standards. In addition, engineers are using it to explore the limits of their receiver performance to check margin in design and manufacturing.



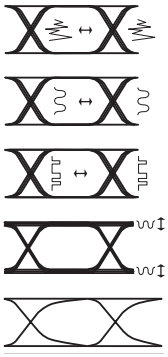
The intuitive Stress user interface of the NEW BERTScope S. The Generator Status panel (lower left) has turned yellow to be a constant reminder that you have an impairment switched in.



"In our design of leading-edge advanced memory buffers (AMB), we've significantly reduced test and validation times using the BERTScope, from hours to minutes, giving us the ability to test more parameters and more devices. We've been able to compress the project timeline with this new approach to test and measurement"

Roland Knaack
AMB Design Manager
IDT, Inc.

Flexible Stress Impairments



Random Jitter

Sinusoidal Jitter

Bounded Uncorrelated Jitter

Sinusoidal Interference

Inter-Symbol Interference

The BERTScope has high quality, calibrated sources of stress built in, including RJ, SJ, BUJ and SI. Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.

ISI is also a common ingredient in many standards. The BERTScope differential ISI board provides a wide variety of path lengths, free from switching suck-outs and anomalies.

Communications Test Examples

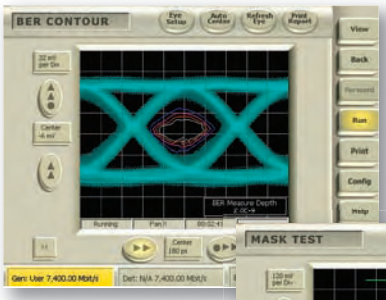
With the JDSU OPTX10, the BERTScope S provides complete optical and electrical stressed eye testing for optical transceivers such as XFP optical testing is also easy for standards such as 10 Gb Ethernet, 2X, 4X, and 10X Fibre Channel.

The BERTScope stressed eye option provides an integrated, calibrated and easy to use solution to jitter tolerance testing. Compliance test for electrical standards such as OIF-CEI, XFI, Fibre Channel, Serial-ATA II and PCI-Express. Through use of the JDSU OPTX10 optical test set, optical testing is also easy for standards such as Fibre Channel and 10 Gbit Ethernet.

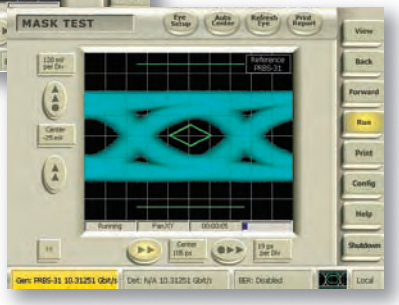
Built in flexibility allows you to explore the limits of device performance and establish the margin available to you. Mix the proportions of sinusoidal jitter, sinusoidal interference (added on data and data bar outputs either in-phase or in anti-phase), random jitter and bounded uncorrelated jitter. Simply add your own ISI filter of choice to complete the tolerance template, then automatically step through the sinusoidal jitter template required by the standard you are using. The BERTScope is designed to make it easy.

BERTScope SPG
Stressed Pattern Generator

A recently introduced member of the BERTScope family, the BERTScope SPG provides a cost effective way of adding stress generation to legacy BERT equipment, or to situations where multiple generators are needed.



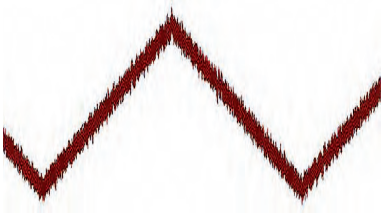
4x Fibre Channel compliant optical stressed eye



XFI compliant electrical stressed eye

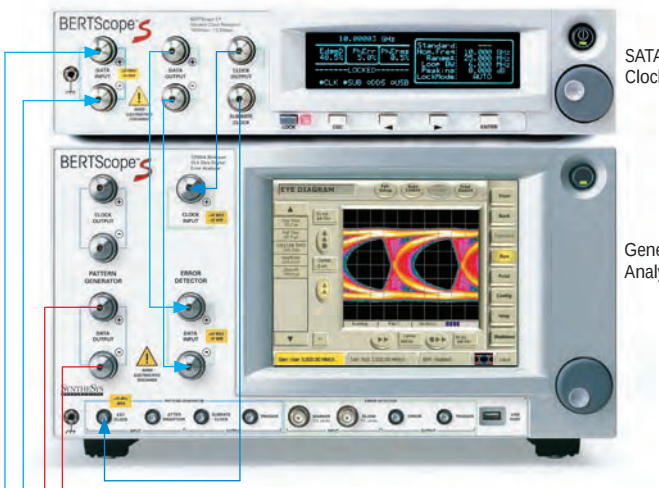
Computer and Storage Receiver Testing

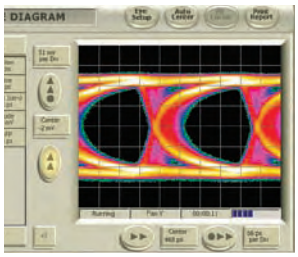
Serial buses used in computing and storage applications have some unique challenges. One is the use of clock domain matching by the insertion or deletion of fill words, which can cause problems in test. Another is the use of spread spectrum clocking (SSC). SSC involves excursions of bit rate which translate into many, many unit intervals of jitter. Providing it is tracked correctly it needn't be a problem, although test equipment frequently struggles. Use the optional SSC clock feature to generate SSC clocked data or using the external clock input to the BERTScope pattern generator, a device's own SSC may be used in testing; in combination with the BERTScope CR, CR matched cable set option and BERTScope analyzer, SSC may be correctly dealt with for proper compliance testing. Either way, the complete range of BERTScope S stresses (SJ, RJ, and BUJ) may be added to provide stressed SSC data signals.



Example: Serial ATA Receiver Compliance Testing

In this example, a disk drive is being tested using a BERTScope S and BERTScope CR. Initially the BERTScope pattern generator runs from its internal clock, supplying a data signal to the device being tested. On the output side of the drive, a clock signal is derived by the CR, and the data and clock fed to the BERTScope analyzer. The CR also supplies a clock to the pattern generator. Once set up, the device is placed in loop back mode, and the generator switched over to external clock, recovered from the drive. Now all clock domains match, and this avoids the insertion of alignment or rate matching characters by the drive. Stressing of the receiver is carried out, with errors by the receiver looped back out of the transmitter and counted by the BERTScope analyzer. The flexibility that comes from compliant clock recovery, and the ability to stress an external clock make device testing a simple setup.

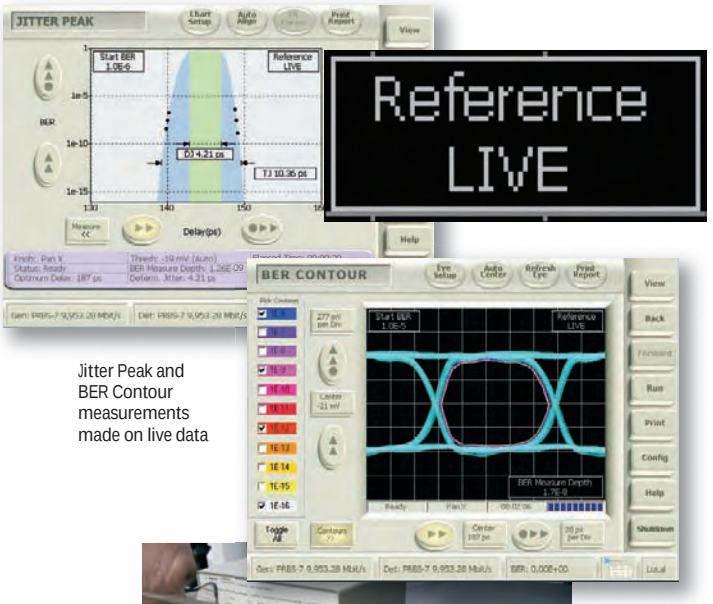




Serial ATA compliant stressed eye

Testing Interface Cards?

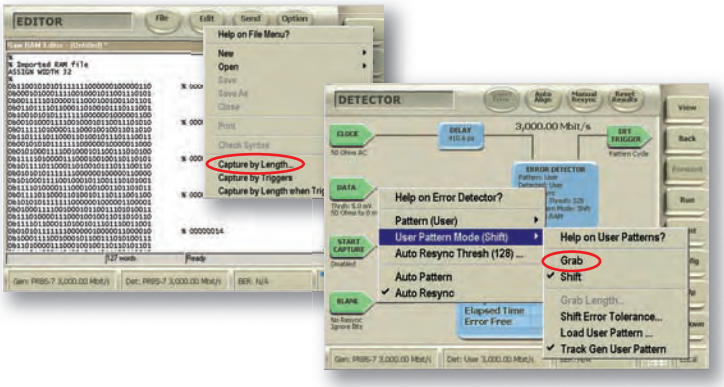
Finally a solution to the age-old problem of making physical layer measurements on high speed line cards, motherboards and live traffic – the BERTScope Live Data Analysis option. Through novel use of the dual-decision point architecture, the instrument is able to make parametric measurements such as Jitter, BER Contour and Q Factor in addition to the eye and mask measurement that are usable as standard – all that is required is a clock signal. No more frustration because the pattern is not known, predictable, or involves rate-matching word insertions. Trouble shooting is so much easier now that the one-button physical layer tests can be employed to provide unique insight.



Jitter Peak and BER Contour measurements made on live data

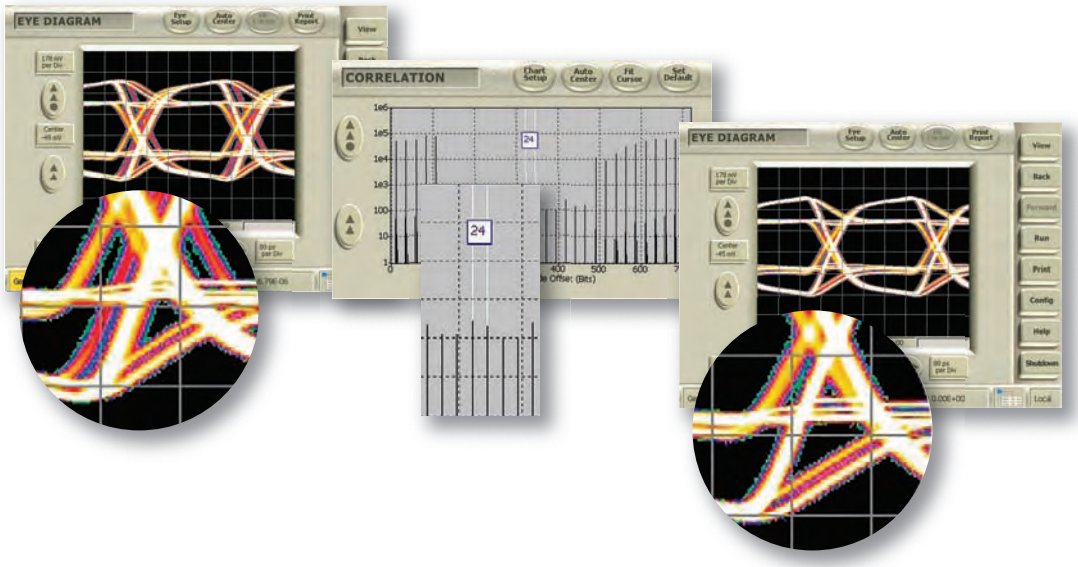
Pattern Capture

There are several options when dealing with unknown incoming data. In addition to live data analysis discussed above, a useful standard feature on all BERTScope analyzers is pattern capture. This allows the user to specify the length of a repeating pattern and then allow the analyzer to grab the specified incoming data. This can then be used as the new detector reference pattern, or edited and saved for later use.



Using the Power of Error Analysis

Customer example where eye diagram views were linked with BER to identify and solve a design issue in a memory chip controller. The eye diagram top left shows a feature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the system clock was at 1/24th of the output data rate. Redesigning the chip with greater clock path isolation gave the clean waveform of the top right eye diagram.



Our Promise to You

We have been supplying the most demanding customers for the past 15 years. We have built up long and trusting relationships with engineers working in error prone environments from aerospace defense to storage and satellite, proud to play a part in their success. We are committed to providing you with the best tools available. We are so sure that you will be delighted with the BERTScope family that we offer free technical support, a standard 1 year warranty extendable to 3 years, 1 day of start-up assistance upon system delivery, application expertise and support, responsive calibration and repair, and a library of web-based technical information. All of our instruments are upgradeable – as we advance our capabilites, we won't leave you stranded.

BERTScope™

12.5 Gb/s Signal Analysis

www.bertscope.com

BERTScope Products

	BERTScope Model				
	7500A Generator & Analyzer	**S 7500B** Stress Generator & Analyzer	**12500A** Generator & Analyzer	**S 12500B** Stress Generator & Analyzer	**SPG 12500B** Stress Generator
Features					
Maximum Bit Rate	7.5Gb/s	7.5Gb/s	12.5Gb/s	12.5Gb/s	12Gb/s
Flexible Pattern Generation	✔	✔	✔	✔	✔
BER Measurement	✔	✔	✔	✔	–
Eye Diagram, Mask Testing	✔	✔	✔	✔	–
BER Contour, Jitter Peak, Mask Testing, Compliance Contour	†	✔	†	✔	–
Stress Insertion for Jitter Tolerance Receiver Testing		✔		✔	✔
Ability to stress an external clock		✔		✔	✔
Many Sub-rate Clock Output Divide Ratios		✔		✔	✔
Jitter Tolerance Templates		✔		✔	–
Options					
Option PL - Physical Layer Test Suite: BER Contour, Jitter Peak, Compliance Contour	Option	✔	Option	✔	–
Option LDA - Live Data Analysis	Option	Option	Option	Option	–
Option SSC	–	Option	–	Option	–
Option ECC - Error correction coding analysis of error location data. Emulates ECC algorithms for 1-D, 2-D correctors	Option	✔	Option	✔	–
Option MAP - Error mapping analysis of error location data. Error mapping visualizes errors in a 2-D map using axis dividers	Option	✔	Option	✔	–
Option RACK - Rackmount Hardware. Kit includes all mounting brackets, slides and hardware necessary to mount a BERTScope into a standard 19" rack. Slides are adjustable for rack rails 17.5 to	Option	Option	Option	Option	Option
Option 3YR - Extended warranty. Adds two years to the standard one-year product warranty	Option	Option	Option	Option	Option
Option CAL - Calibration certificate	Option	Option	Option	Option	Option
BERTScope Upgrades – BERTScope 12500 xxxx unless otherwise stated					
7500A to S 7500B	Option 7A2B				
7500A to 12500A	Option UP				
7500A to S 12500B	Option UPS				
S 7500A to S 12500B		Option SUPS			
12500A to S 12500B			Option A2B		
S 12500A to S 12500B				Option SA2B	
S 12500B or S 7500B add Option SSC		Option USSC		Option USSC	
SPG to S 12500B					Option PG2B
Accessories					
BSA Differential ISI Board	Option	Option	Option	Option	Option
Option SPD - S Parameter Data	Option	Option	Option	Option	Option
BSA DEMO KIT - cables, attenuators, adapters, US power cable, USB keyboard and mouse, accessory case	Option	Option	Option	Option	Option
BSA Transit Case	Option	Option	Option	Option	Option

– - Not Available
✔ - Standard feature
† - Option available below
Option - Available by adding the listed option

For more information on this and other products:
- BERTScope™ and BERTScope™ S Signal Integrity Analyzers Technical Specifications, SR-DS014
- BERTScope ™ SPG Product Brief, SR-DS019
- BERTScope™ Differential ISI Board Product Brief, SR-DS018
- BERTScope™ CR Clock Recovery Instrument Product Brief, SR-DS016

Application information:
- Stressed Eye – Know what you are testing with, January 2006
- Constructing a 10 GbE Optical Fibre Channel Stressed Eye, January 2006
- Constructing a 4x FC Optical Stressed Eye, January 2006
- Testing the High Speed Electrical Specifications of an XFP Transceiver, July 2006
- Evaluating Stress Components Using BER-Based Jitter Measurements, September 2005

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