Fudan VLFD

Hardware Reference Manual

Version 2.00

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Table of Contents

List of Figures

List of Tables

Revision History

Version	Date	Comment
2.0	04 July, 2011	Add FPGA board figure
1.0	20 June,2011	Initial version

1. Introduction

The Fudan VLFD is an entry level FPGA development platform that connects to the host computer through USB2.0. The VLFD contains a Fudan FP3D7F FPGA. It is designed for logic design learning, and ASIC prototyping needs, including HW/SW co-development, proof-of-concept studies, IP development.

1.1 General Features

The general features of Fudan VLFD hardware board are listed as follows.

- One Fudan FDP3D7 with PQ208 package
- Data Transmission by USB 2.0
- FPGA Configuration via
  - ✓ By USB,
  - ✓ JTAG with Fudan download cable
  - ✓ A configuration mode selection
- Power supply by USB and Power Switch.
- Total 21 GIO Pins
  - ✓ Eight selectable user-defined LEDs
  - ✓ Two selectable user-defined DIP Switches
  - ✓ Two selectable user-defines Push Bottoms
- One 30MHz clock input from SMIMS Engine
- One half-size Oscillator socket
- Three Indicated LEDs

2. Hardware Board Description

In this chapter, it provides the detailed VLFD Hardware board description.

- Hardware board
- Clock
- IO Signals
- SMIMS Engine
- Status LEDs

2.1 Hardware board

Figure 1 is the top view of the Fudan VLFD board. It depicts the layout of the board and indicates the location of the connectors and key components.

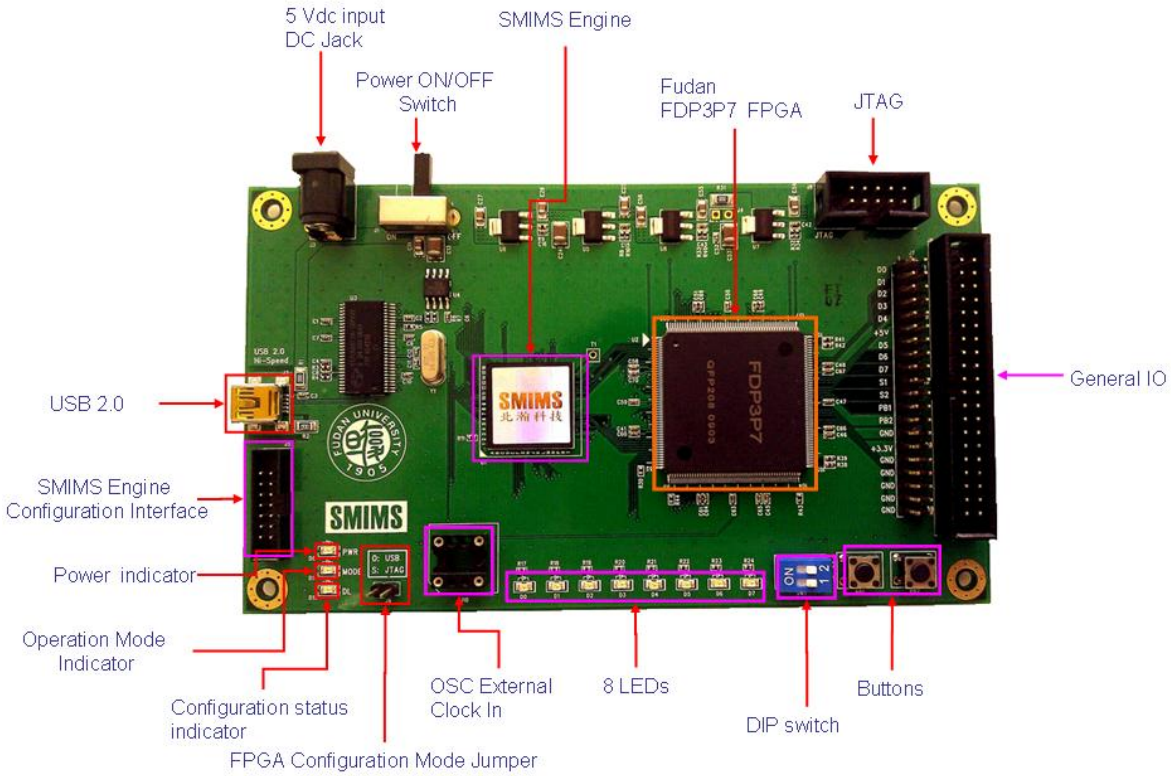


Figure 1 Top View of Fudan VLFD

Below is more detailed information regarding to those blocks.

- Fudan FP3D7F in PQ208 package
  - ✓ SMIC 0.18 um process
  - ✓ 16 4Kb dual-port memory
  - ✓ 4 Phase-locked-loops (PLLs)
- Clock inputs
  - ✓ 30 MHz clock from smims engine
  - ✓ Half-size Osc socket
- SMIMS Engine board
  - ✓ Support data transfer between PC and FPGA
  - ✓ Support FPGA configuration by USB
- Total 21 GIO
  - ✓ selectable connection to eight on-board user-defined LEDs
  - ✓ selectable connection to two on-board user-defined DIP Switches
  - ✓ selectable connection to two on-board user-defined Push Buttons
  - ✓ selectable connection to power/ground signals by jumper
- JTAG Connector
  - ✓ Support Fudan JTAG configuration
- Three System indicator LEDs
  - ✓ Voltage indicator
  - ✓ Operation mode indicator
  - ✓ Configuration done indicator
- USB Power and Power Switch

2.2 Clock

The Fudan VLFD provides a 30MHz clock from SMIMS Engine and a half-size osc socket. The 30MHz clock is also the operation clock in the VeriSDK mode. Note: VeriSDK (co-work between FPGA and C/C++) is one of verification mode.

30 MHz Clock Source	External Clock
FPGA IO Pin	FPGA IO Pin
P185	P80

Table 1. Clock Sources

2.3 I/O Signals

The Fudan VLFD contains 21 IOs. There is a 2x20pin pin header (J7) beside the GIO connector, shown as follows.

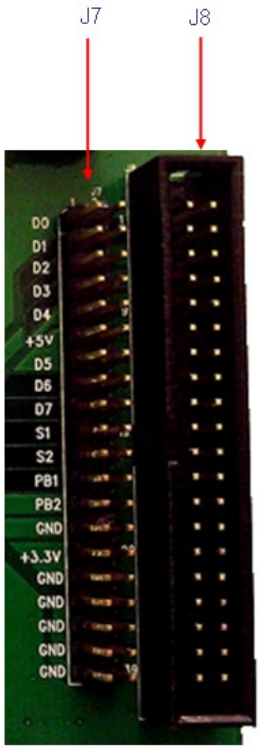


Figure 2 GIO of Fudan VLFD

If user shorts the J7.1 and J7.2 pins, it means that LED D0 will connect with GIO (J8.1), shows as follows

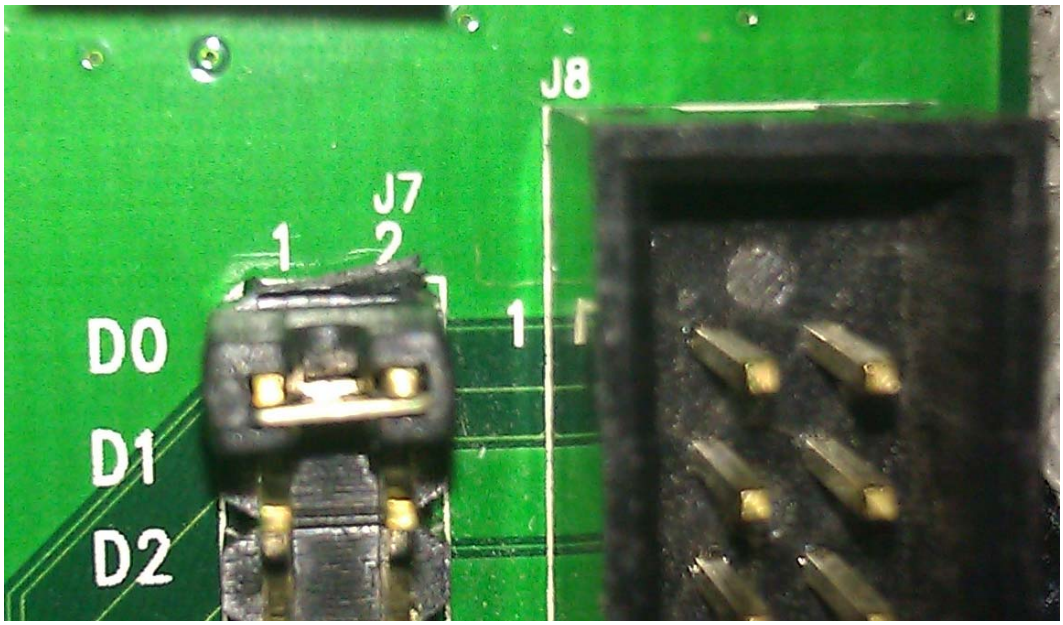


Figure 3 Connection between GIO and other device

2.4 SMIMS Engine

SMIMS Engine has a USB port to connect with PC and provides the data communication and management between PC and FPGA. SMIMS Engine provides the different interfaces which depend on using the different SMIMS software tools/operation mode.

2.5 Status LEDs

The system status indicators LEDs are shown as follows. When power on, the power status LED will be on. When the design is running in the VeriComm mode, the mode status LED will be off. When the design is running in the VeriSDK mode, the mode status LED will be on. When power on, the DL status LED will be twinkling. When FPGA programming was done, the DL status LED will be on.

System Status Indicators LEDs	
Status	**LEDs**
PWR(Power)	**D8**
MODE	**D9**
DL (Download)	**D10**

Table 2. System Status Indicators LEDs Location

3. Pin Tables

In this chapter, the FPGA pin, which connects to other devices such as I/O connectors, clocks etc, will be shown in the following tables.

3.1 Clock

30 MHz Clock Source
FPGA IO Pin
P`185

Table 3. Pin Table of 30MHz

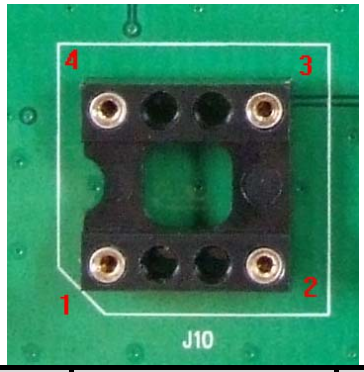
External Oscillator		
		
PCB ID	**FPGA IO Pin**	**Jumper Settings**
J10 – 1	**NC**	**None**
J10 – 2	**GND**	**None**
J10 – 3	**P80**	**None**
J10 – 4	**3.3V**	**None**

Table 4. Pin Table of External Oscillator

3.2 General IOs and Other devices

General I/O J8			
FPGA IO Pin	**Location**	**Location**	**FPGA IO Pin**
P147	**1**	**2**	**P146**
P145	**3**	**4**	**N.C.**
P141	**5**	**6**	**N.C.**
P140	**7**	**8**	**N.C.**
P139	**9**	**10**	**N.C.**
+5V	**11**	**12**	**GND**

P138	13	14	N.C.
P136	15	16	N.C.
P135	17	18	N.C.
P134	19	20	N.C.
P133	21	22	N.C.
P132	23	24	N.C.
P129	25	26	N.C.
P127	27	28	N.C.
+3.3V	29	30	GND
P126	31	32	N.C.
P125	33	34	N.C.
P123	35	36	N.C.
P122	37	38	N.C.
P121	39	40	N.C.

Table 5. Pin Table of GIOs (J8)

General I/O J7			
FPGA IO Pin	Location	Location	FPGA IO Pin
LED D0	1	2	P147
LED D1	3	4	P145
LED D2	5	6	P141
LED D3	7	8	P140
LED D4	9	10	P139
+5V	11	12	+5V
LED D5	13	14	P138
LED D6	15	16	P136
LED D7	17	18	P135
SW1.1	19	20	P134
SW1.2	21	22	P133
BT1	23	24	P132
BT2	25	26	P129
GND	27	28	P127
+3.3V	29	30	+3.3V
GND	31	32	P126
GND	33	34	P125
GND	35	36	P123
GND	37	38	P122
GND	39	40	P121

Table 6. Pin Table of GIOs (J7)

LED (Low Active)		
PCB ID	FPGA IO Pin	Jumper Settings
D0	P147	J7 Short 1-2
D1	P145	J7 Short 3-4

D2	P141	**J7 Short 5-6**
D3	P140	**J7 Short 7-8**
D4	P139	**J7 Short 9-10**
D5	P138	**J7 Short 13-14**
D6	P136	**J7 Short 15-16**
D7	P135	**J7 Short 17-18**

Switch (Low Active)		
PCB ID	**FPGA IO Pin**	**Jumper Settings**
SW1.1	P134	**J7 Short 19-20**
SW1.2	P133	**J7 Short 21-22**

Button (Low Active)		
PCB ID	**FPGA IO Pin**	**Jumper Settings**
BT1	**P132**	**J7 Short 23-24**
BT2	P129	**J7 Short 25-26**

Table 7. Pin Table of Other devices on board

3.3 Verification Mode

The following section shows the pin table in the verification mode between FPGA and SMIMS engine.

3.3.1 VeriComm/Simulink Mode

Pin Table of VerComm/Simulink Mode			
VeriComm	**FPGA IO Pins**	**VeriComm**	**FPGA IO Pins**
clk	P77		
input0	P151	Output0	P7
input1	P148	Output1	P6
input2	P150	Output2	P5
input3	P152	Output3	P4
input4	P160	Output4	P9
input5	P161	Output5	P8
input6	P162	Output6	P16
input7	P163	Output7	P15
input8	P164	Output8	P11
input9	P165	Output9	P10
input10	P166	Output10	P20
input11	P169	Output11	P18
input12	P173	Output12	P17
input13	P174	Output13	P22
input14	P175	Output14	P21
input15	P191	Output15	P23
input16	P120	Output16	P44
input17	P116	Output17	P45
input18	P115	Output18	P46
input19	P114	Output19	P43
input20	P113	Output20	P40
input21	P112	Output21	P41
input22	P111	Output22	P42
input23	P108	Output23	P33
input24	P102	Output24	P34
input25	P101	Output25	P35
input26	P100	Output26	P36
input27	P97	Output27	P30
input28	P96	Output28	P31
input29	P95	Output29	P24
input30	P89	Output30	P27
input31	P88	Output31	P29
input32	P87	Output32	P110
input33	P86	Output33	P109
input34	P81	Output34	P99
input35	P75	Output35	P98

input36	P74	Output36	P94
input37	P70	Output37	P93
input38	P69	Output38	P84
input39	P68	Output39	P83
input40	P64	Output40	P82
input41	P62	Output41	P73
input42	P61	Output42	P71
input43	P58	Output43	P63
input44	P57	Output44	P60
input45	P49	Output45	P59
input46	P47	Output46	P56
input47	P48	Output47	P55
input48	P192	Output48	P167
input49	P193	Output49	P168
input50	P199	Output50	P176
input51	P200	Output51	P187
input52	P201	Output52	P189
input53	P202	Output53	P194

Table 8. Pin Table of VeriComm/Simulink Mode

3.3.2 VeriSDK/Matlab Mode

Pin Table of VeriSDK/Matlab Mode					
VeriSDK	**FPGA IO Pins**		**VeriSDK**	**FPGA IO Pins**	
APP_CLK	P185	Input	CH[0]	P102	Input
APP_RSTN	P3	Input	CH[1]	P101	Input
APP_CS	P206	Input	CH[2]	P100	Input
APP_WR	P44	Output	CH[3]	P97	Input
APP_RD	P45	Output	CH[4]	P96	Input
APP_Full	P120	Input	CH[5]	P95	Input
APP_Empty	P115	Input	CH[6]	P89	Input
APP_AlmostFull	P116	Input	CH[7]	P88	Input
APP_AlmostEmpty	P114	Input			
APP_DI [0]	P151	Input	APP_DO [0]	P7	Output
APP_DI [1]	P148	Input	APP_DO [1]	P6	Output
APP_DI [2]	P150	Input	APP_DO [2]	P5	Output
APP_DI [3]	P152	Input	APP_DO [3]	P4	Output
APP_DI [4]	P160	Input	APP_DO [4]	P9	Output
APP_DI [5]	P161	Input	APP_DO [5]	P8	Output
APP_DI [6]	P162	Input	APP_DO [6]	P16	Output
APP_DI [7]	P163	Input	APP_DO [7]	P15	Output
APP_DI [8]	P164	Input	APP_DO [8]	P11	Output
APP_DI [9]	P165	Input	APP_DO [9]	P10	Output
APP_DI [10]	P166	Input	APP_DO [10]	P20	Output

APP_DI [11]	P169	Input	APP_DO [11]	P18	Output
APP_DI [12]	P173	Input	APP_DO [12]	P17	Output
APP_DI [13]	P174	Input	APP_DO [13]	P22	Output
APP_DI [14]	P175	Input	APP_DO [14]	P21	Output
APP_DI [15]	P191	Input	APP_DO [15]	P23	Output

Table 9. Pin Table of VeriSDK/Matlab Mode