Introduction: Connection between all stages

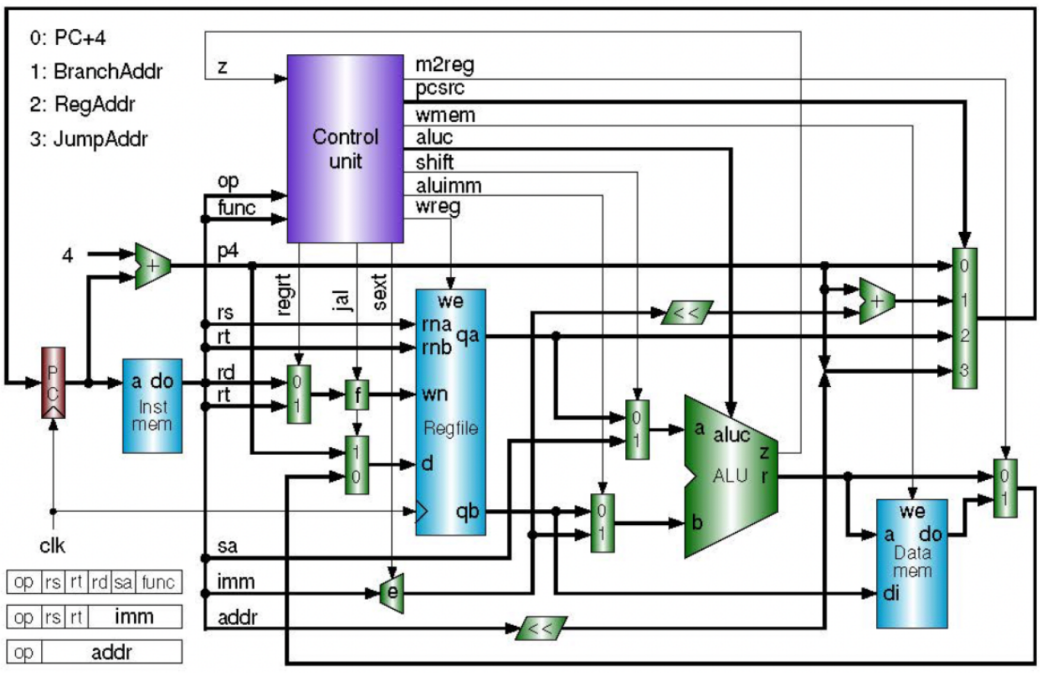


Figure 1 Block diagram of a single-cycle CPU

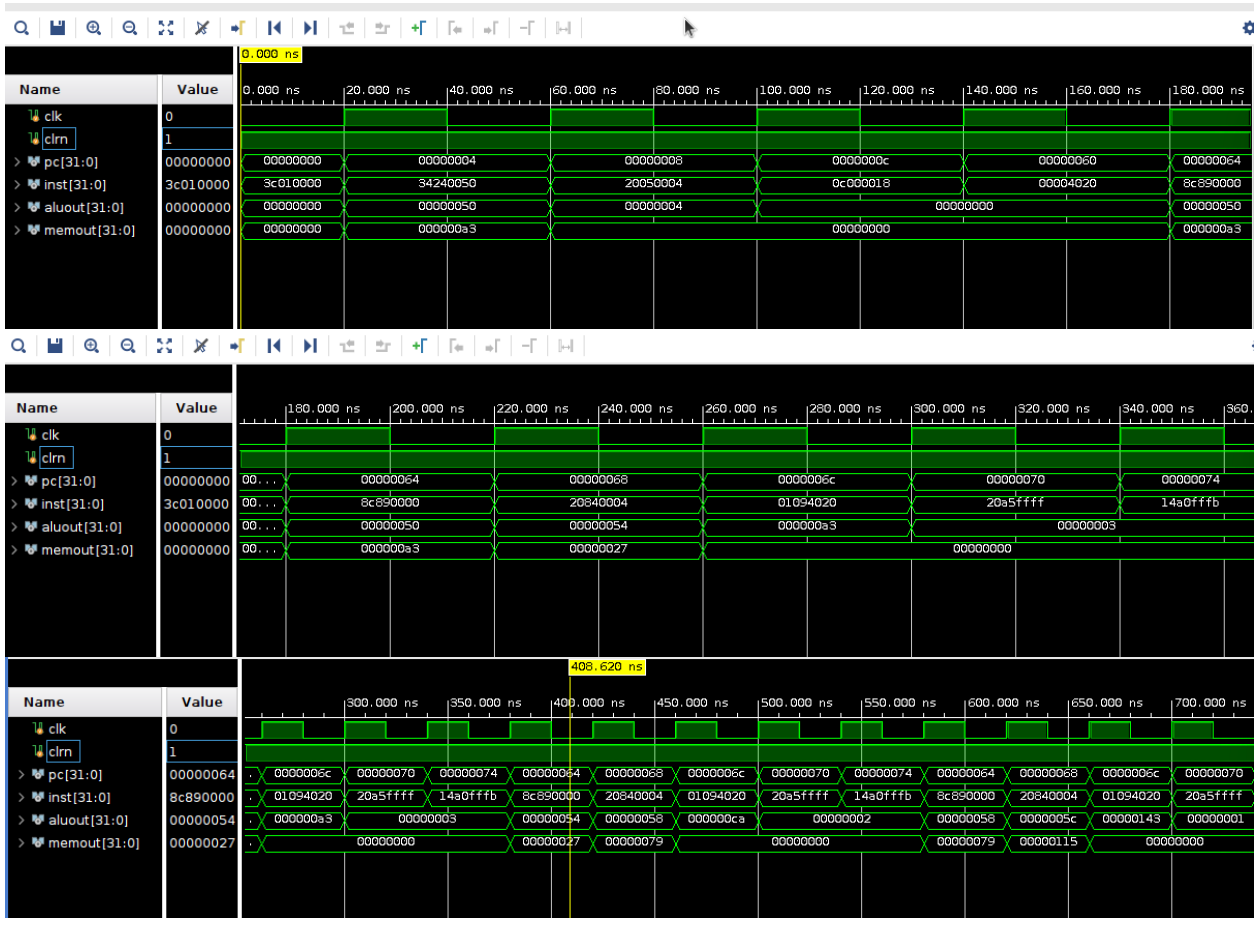
1. The connection between PC multiplexor and instruction memory is that PC multiplexor outputs pc address, and instruction memory takes it as input.
2. Instruction memory outputs instruction, and op & func fields are taken by control unit as inputs; rs, rd fields are taken by register file as inputs; sa / imm fields are taken by sign extension components; addr are taken by pc multiplexor.
3. Register file uses the inputs to fetch output qa qb, for ALU operations;
4. Control unit uses the inputs to generate control signals and send them to other parts;
5. ALU takes inputs from register files or extended immediate values, depends on the result of multiplexor; and outputs zero value and ALU results;
6. Data memory takes ALU results as the data address, and qb as the data to store at the data address;
7. If it is a lw instruction, the result from data memory will be written back to register file.
8. The PC multiplexor takes pcsrc as inputs and outputs the new pc for the next clock cycle.
The implementation uses the single clock cycle design. The benefit is that every instruction is executed in one clock cycle. It is easy to write and understand. The design also uses abstract design principal, which makes the details of each stage hidden to other stages and connect each stage with inputs and outputs only. The design makes the code easier to write and debug.

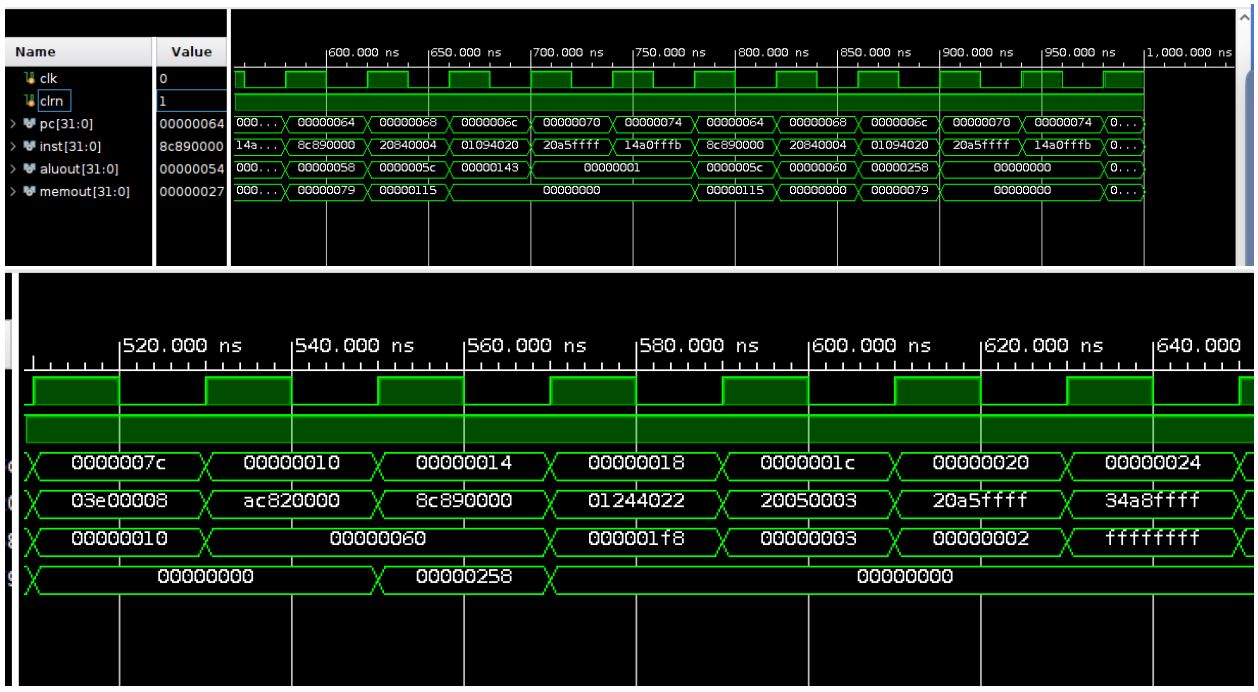
```
    CPU cpu(.clk(clk), .clrn(clrn), .pc(pc), .inst(inst), .aluout(aluout), .memout(memout));

    initial begin
        clk = 0;
        clrn = 1;
    end

    always #20 clk = !clk;
endmodule
```

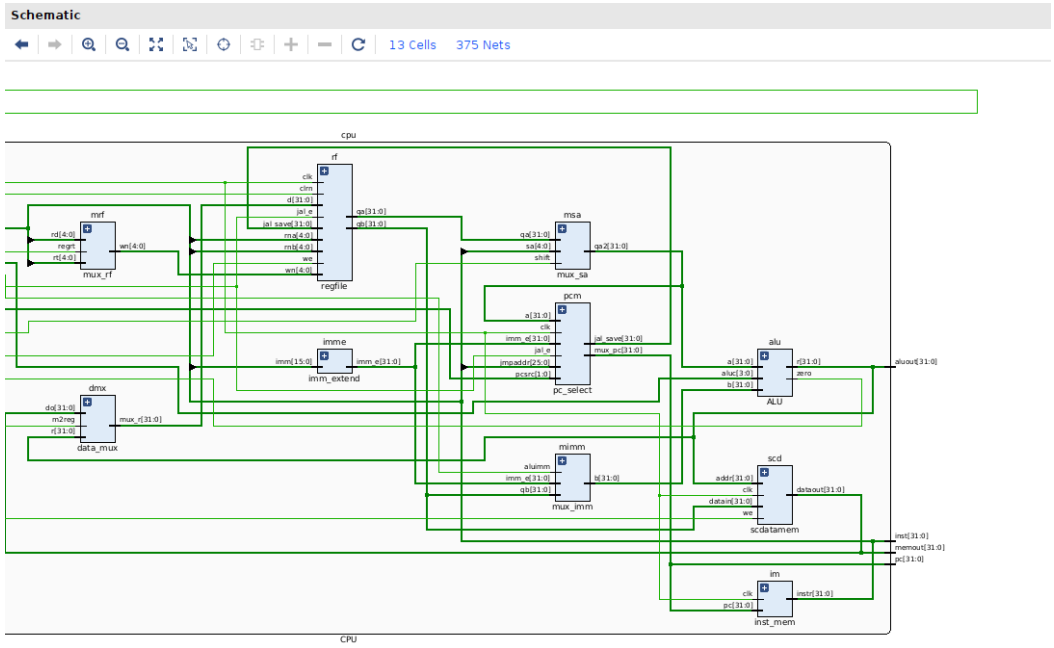
c. Waveforms



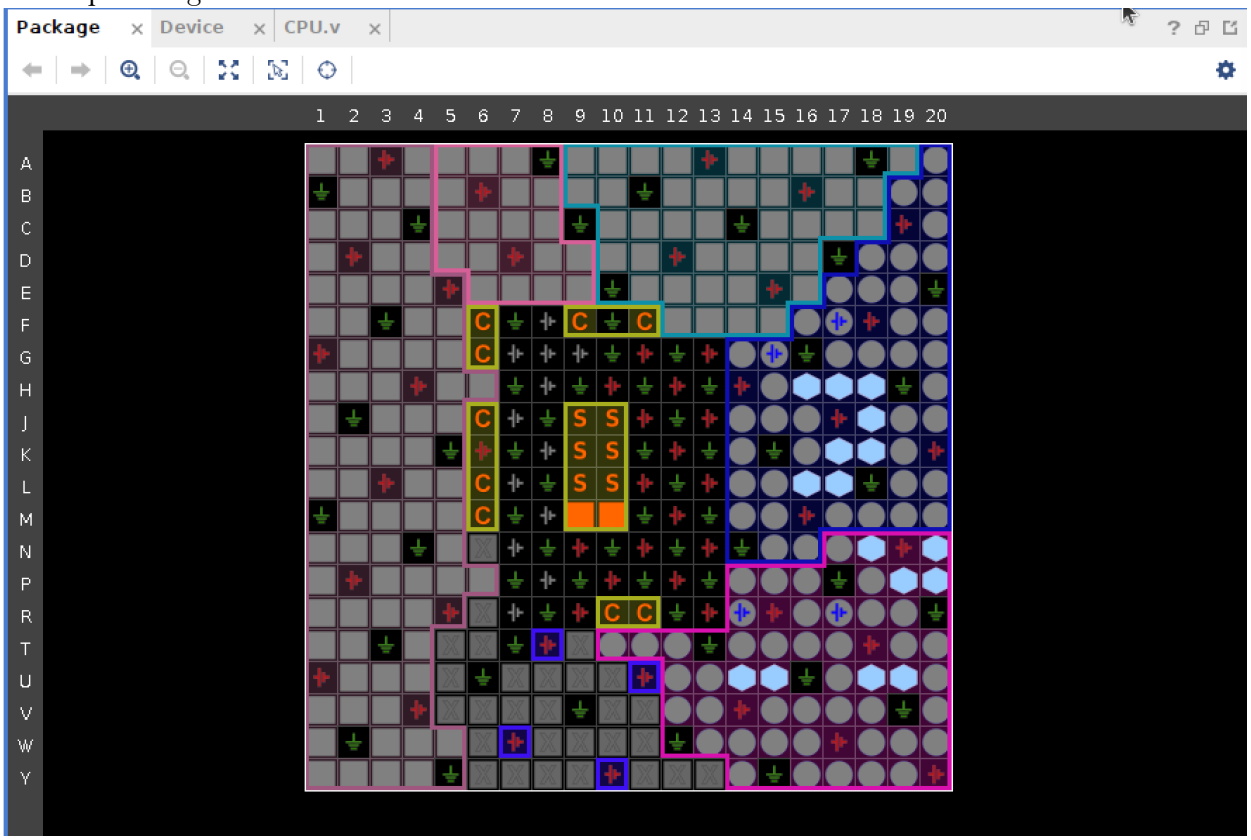


*For the last part of the waveform, I cannot generate waveform after 1000ns, so I shorten the clock period from 20ns to 10ns, and took a screen shot after 500ns, which will be equivalent to 1000-1350 ns with clock period of 20ns.

d. Schematics



e. I/O planning



f. Floor planning