DATA SHEET

SPMP8016A

Portable Multimedia Processor

Feb. 17, 2009

Version 1.0

Table of Contents

PAGE

SPMP8016A PORTABLE MULTIMEDIA PROCESSOR

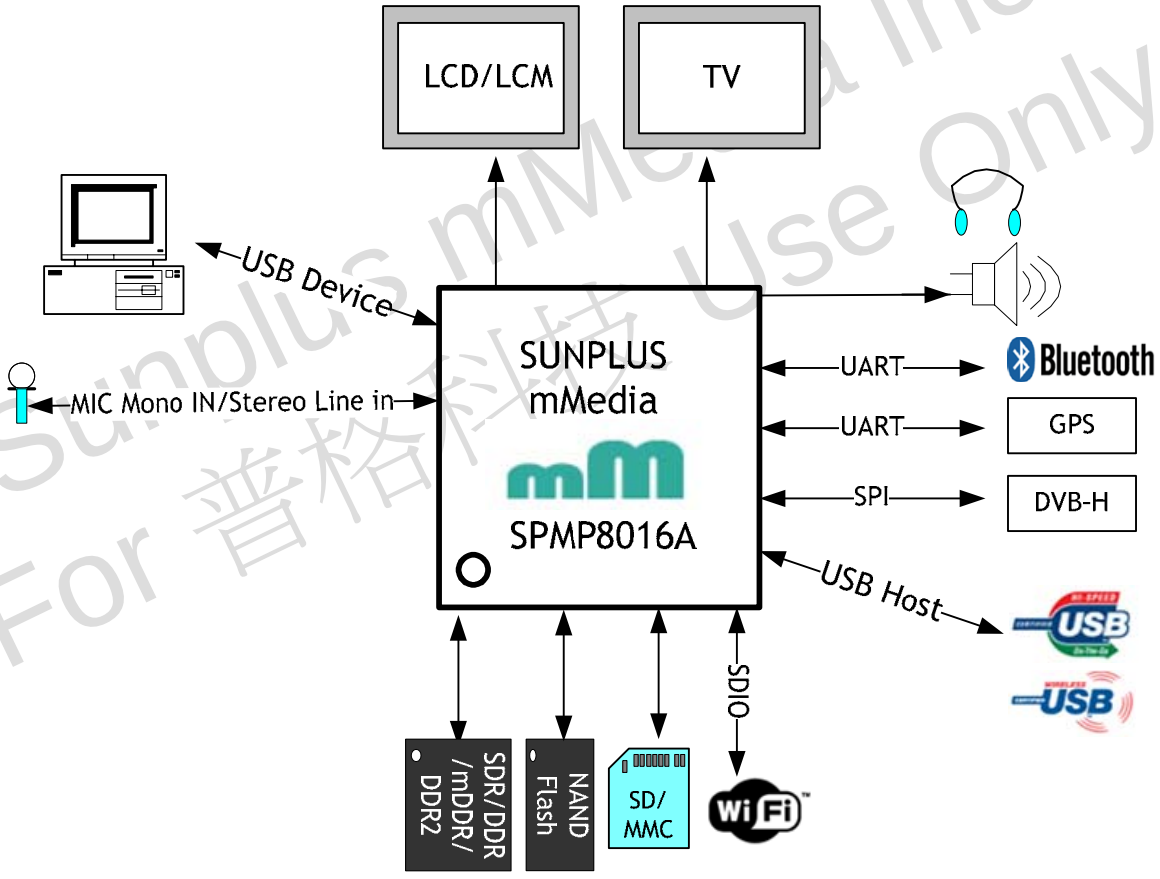
1. GENERAL DESCRIPTION

1.1. Introduction

SPMP8016A, a powerful dual-core multimedia processor, integrates an ARM926EJS CPU, a high-performance DSP, and a rich peripheral set. This makes SPMP8016A an excellent selection for multimedia applications.

The SPMP8016A has been designed with not only the latest technology but also the full service from Sunplus mMedia.

1.2. Typical Application



2. FEATURES

2.1. System

- High-performance CPU + DSP dual-core architecture
- Built-in boot 32KB ROM.
- In-System-Programming for firmware update from USB or SD card

2.2. CPU

- 32-bit ARM926EJ with 16KB instruction L1 cache and 16KB data L1 cache
- Programmable CPU operating frequency up to 270MHz
- 32KB L2 SRAM with ITCM and DTCM interface

2.3. DSP

- High-performance DSP
- Programmable operating frequency up to 324MHz

2.4. Graphics Engine

- BitBLT with 256 3-operands ROPs
- Alpha-blending, Bresebham's Line Drawing (solid and dashed line)
- Solid color pattern fill, smooth color shading fill
- Sprite color transparency with 16 color-key ROP
- Bit-plane read and write masks
- 4-bit/8-bit indexed color with color expansion

2.5. Still Image and Video Codec

- Supports multiple format decoding: JPEG, MJPEG, MPEG1, MPEG2, MPEG4 ASP, H.264, RMVB, WMV, etc
- Supports multiple format encoding: JPEG, MJPEG, MPEG4, etc.
- H.264 simple profile level-3 decoding 720x480 30fps at 3Mbps
- Video encoding up to 720x480 30fps

2.6. Audio

- Supports multiple format decoding: MP3, AAC-LC, AAC+, AMR, WMA, ADPCM, WAV, RM-Audio, OGG, APE, FLAC, etc.
- Supports multiple format encoding: MP3, WMA, etc.
- Built-in stereo audio ADC/DAC
- Stereo line-in, line-out and headphone output support
- Integrated microphone input
- Stereo speaker output with an external amplifier

2.7. Display

- Supports LCM/LCD panel resolution up to 800x600
- Supports 16-bit, 8-bit 8080/M68-MCU interface for LCM
- Supports 16/24-bit RGB, 8-bit RGB (UPS051/UPS052), CCIR601, CCIR656 interface LCD up to 16.8 million colors.
- Built-in TV encoder and DAC, providing NTSC/PAL composite video output up to 480i/576i
- LCD and TV outputs can be switched on simultaneously
- Supports OSD format RGB565, RGB1555, 8-bit index, 4-bit index, and alpha blending

2.8. USB

- USB device with EP0, BULK-IN, BULK-OUT, and INTERRUPT-IN endpoints
- OHCI/EHCI-compatible mass storage class USB host

2.9. Memory Card

- Supports SD/SDIO/microSD/MMC/MMC4.0-4bits/CE-ATA card
- Supports MS/MS-Pro/MS-Duo

2.10. DRAM

- Supports SDR/DDR/mDDR/DDR2 up-to 128MB (4 Bank organization)
- Supports operating frequency up to 133MHz for SDR and 162MHz for DDR/mDDR/DDR2

2.11. NAND Flash

- Supports SLC and MLC NAND-type Flash memory
- Built-in 8-bit ECC engine

2.12. Peripheral

- UART, SPI, I2C, I2S, RTC
- GPIO with built-in interrupt functions
- Built-in 5-channel inputs 10-bit SAR ADC
- PWM output

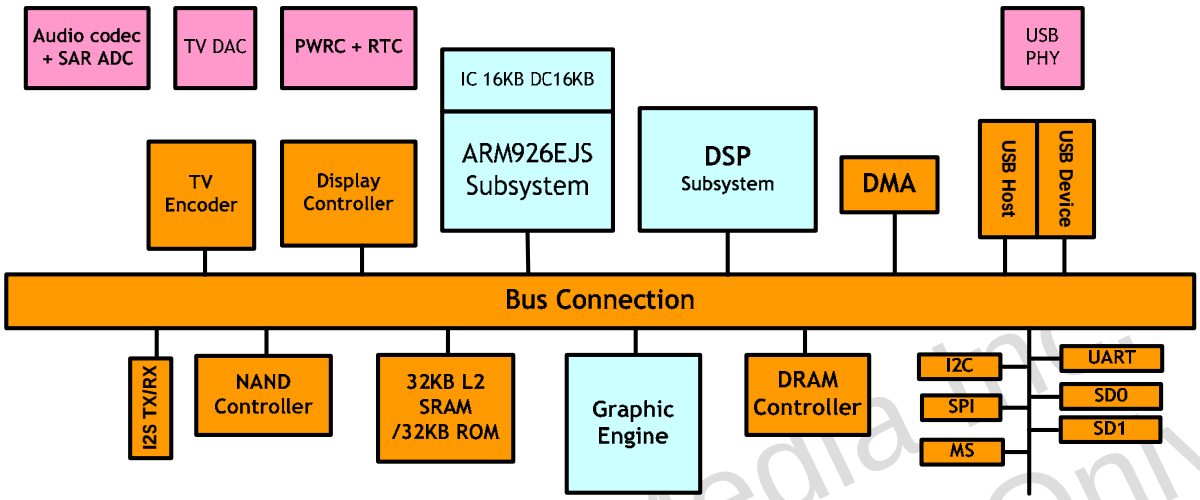
2.13. Clock

- 27MHz PLL clock input
- 32768 Hz RTC clock input

2.14. Package and Power

- 1.2V core power supply
- 1.8V ~ 3.3V IO power supply
- LQFP216-pin package

3. BLOCK DIAGRAM



4. FUNCTIONAL DESCRIPTIONS

4.1. ARM926EJS Subsystem

The ARM926EJS subsystem consists of an ARM926EJS and sub modules required for operating system implementation. The 270MHz ARM926EJS intergrates a 16KB instruction cache and a 16KB data cache. It also supports L2 access through the TCM interface. The submodules include: interrupt controller, watch dog timer, system control unit, GPIO controller, and I2C controller.

4.2. DSP Subsystem

The DSP subsystem integrates a high performance DSP and submodules (timer, interrupt controller, etc.) for maximal computation power and flexibility. The 324MHz DSP is suitable for a wide variety of applications such as multi-format audio and video codec. A software implementation shows the capability of H.264 simple profile decoding up to D1 30fps at 3Mbps.

4.3. Graphics Engine

A graphics engine provides 16-bit (RGB565/1555) operations including BitBLT with 3 ROP, alpha-blending, line drawing, pattern fill, sprite transparency with color-key ROP, bit-plane mask, and index color expansion. In addition, it accelerates GUI operation and graphics intensive applications such as GPS and games.

4.4. Display Controller

The display controller transmits both RGB data and YUV data from DRAM to LCD/LCM. In addition, it performs real time scaling up (at output stage), OSD blending, and color transformation. The display interface supports 16/24-bit (RGB), 8-bit RGB (UPS051/UPS052), and CCIR656 interfaces with resolution support up to 800x600.. An OSD engine is integrated with the display controller in order to support different format (RGB565, RGB1555, 8b/4b index) OSD functions.

In addition to the LCD/LCM output, a TV encoder is integrated for 720x480 or 720x576 480i/576i NTSC/PAL output. A embedded video DAC supports direct composite output. Furthermore, LCD and TV outputs can be switched on simultaneously.

4.5. Audio Codec and I2S Audio IF

An embedded audio codec provides high quality audio function and helps lowering the system BOM cost. Stereo line in, MIC in, headphone output, and I2S interfaces are also integrated in the SPMP8016A.

4.6. USB Device and Host

A high speed USB 2.0 device controller is integrated in SPMP8016A to support MSDC and INT class transfer. The USB device supports EP0, BULK-IN, BULK-OUT, INTERRUPT-IN endpoints. The USB host is fully OHCI- and EHCI-compatible, which supports mass storage class device at high/full speed.

4.7. NAND Controller

The NAND controller supports high speed NAND access with embedded 8-bit ECC engine for mainstream NAND technology. It also supports multiple CS for NAND with larger capacity.

4.8. DRAM Controller

The DRAM controller supports SDR, DDR, DDR2, and mDDR for higher bandwidth requirements. The maximum capacity is 64MB.

4.9. Other Components

Two SD/SDIO interfaces are integrated in the SPMP8016A. Both SD interfaces support SD/SDHC/MMC/MMC4.0 storage cards, CE-ATA storage devices, as well as SDIO devices, which enables connection to SDIO devices as well as SD storage cards. Other components in the peripheral and interface set include: SAR ADC, touch-panel interface, I2C, SPI, UART, PWM and GPIOs.

5. PIN DESCRIPTIONS

LQFP-216 Pin Description

(Dir. PG: Power/GND, A: Analog pin, B: bi-direction, I: input, O: output)

LQ	Pin name		Pull	Default	2nd Function	3rd Function
1	AVSS_APLL_VDAC	PG		Audio PLL VSS + VDAC		
2	RSET_VDAC	A		Resistor to GND		
3	CBU_VDAC	A		0.1uF to AVDD		
4	AOUT_VDAC	A		DAC current output		
5	A3V3_VDAC	PG		3.3V for VDAC		
6	HPOUTR	A		Right channel headphone output		
7	AVSS_SP	PG		Ground of A3V3_SP		
8	A3V3_SP	PG		3.3V power supply for speaker & headphone portion		
9	HPOUTL	A		Left channel headphone output		
10	AVSSAUD	PG		I/O ground for audio codec PAD		
11	AVDDAUD	PG		I/O power for audio codec PAD		
12	VREF	A		Reference voltage for ADC, DAC &SAR		
13	A3V3_CODEC	PG		3.3V power supply for ADC & DAC analog portion		
14	AVSS_CODEC	PG		GND for A3V3_CODEC		
15	LNINR	A		Right channel line in		
16	LNINL	A		Left channel line in		
17	MICINN	A		Microphone negative input		
18	MICINP	A		Microphone positive input		
19	MICBIAS	A		Buffered voltage output suitable for electro-microphone-capsule biasing. Voltage level is 0.75*AVDD33.		
20	SARIN4	A		SAR ADC input channel4		
21	TPXN	A		SAR ADC input channel (touch-panel X-)		SAR_GPIO[1]
22	TPXP	A		SAR ADC input channel (touch-panel X+)		SAR_GPIO[2]
23	TPYN	A		SAR ADC input channel (touch-panel Y-)		SAR_GPIO[0]
24	TPYP	A		SAR ADC input channel (touch-panel Y+)		SAR_GPIO[3]
25	VDD	PG		Core Power (1.2V)		
26	VSS	PG		Core + IO Gnd		
27	IOVDD	PG		IO Power (3.3V)		
28	B_DISP27	B	PD	LCD_OUT[23]	I2S_RX_DATA	GPIO1[15]
29	B_DISP26	B	PD	LCD_OUT[22]	I2S_RX_LRCK	GPIO1[14]
30	B_DISP25	B	PD	LCD_OUT[21]	I2S_RX_SCLK	GPIO1[13]
31	B_DISP24	B	PD	LCD_OUT[20]	AD_MCLK	GPIO1[12]
32	B_DISP23	B	PD	LCD_OUT[19]	I2S_TX_DATA	GPIO1[11]
33	B_DISP22	B	PD	LCD_OUT[18]	I2S_TX_LRCK	GPIO1[10]
34	B_DISP21	B	PD	LCD_OUT[17]	I2S_TX_SCLK	GPIO1[9]
35	B_DISP20	B	PD	LCD_OUT[16]	DA_MCLK	GPIO1[8]
36	B_DISP19	B	PD	LCD_OUT[15]	LCM_DAT[15]	GPIO1[7]

37	B_DISP18	B	PD	LCD_OUT[14]	LCM_DAT[14]	GPIO1[6]
38	B_DISP17	B	PD	LCD_OUT[13]	LCM_DAT[13]	GPIO1[5]
39	B_DISP16	B	PD	LCD_OUT[12]	LCM_DAT[12]	GPIO1[4]
40	B_DISP15	B	PD	LCD_OUT[11]	LCM_DAT[11]	GPIO1[3]
41	B_DISP14	B	PD	LCD_OUT[10]	LCM_DAT[10]	GPIO1[2]
42	B_DISP13	B	PD	LCD_OUT[9]	LCM_DAT[9]	GPIO1[1]
43	B_DISP12	B	PD	LCD_OUT[8]	LCM_DAT[8]	GPIO1[0]
44	IOVSS	PG		IO Gnd		
45	IOVDD	PG		IO Power (3.3V)		
46	B_DISP11	B	PD	LCD_OUT[7] (TRAP[7])	LCM_DAT[7]	
47	B_DISP10	B	PD	LCD_OUT[6] (TRAP[6])	LCM_DAT[6]	
48	B_DISP9	B	PD	LCD_OUT[5] (TRAP[5])	LCM_DAT[5]	
49	B_DISP8	B	PD	LCD_OUT[4] (TRAP[4])	LCM_DAT[4]	
50	B_DISP7	B	PD	LCD_OUT[3] (TRAP[3])	LCM_DAT[3]	
51	B_DISP6	B	PD	LCD_OUT[2] (TRAP[2])	LCM_DAT[2]	
52	B_DISP5	B	PD	LCD_OUT[1] (TRAP[1])	LCM_DAT[1]	
53	B_DISP4	B	PD	LCD_OUT[0] (TRAP[0])	LCM_DAT[0]	
54	B_DISP3	B	PD	LCD_DATA_EN	LCM_RD	
55	B_DISP2	B	PU	LCD_HSYNC	LCM_WR	
56	B_DISP1	B	PU	LCD_VSYNC	LCM_RS	
57	B_DISP0	B	PD	LCD_CLK	LCM_CS	
58	XGPIO_11	B	PD			
59	XGPIO_10	B	PD			
60	XGPIO_9	B	PD			
61	XGPIO_8	B	PD			
62	XGPIO_7	B	PD			
63	XGPIO_6	B	PD			
64	XGPIO_5	B	PD			
65	XGPIO_4	B	PD			
66	XGPIO_3	B	PD			
67	XGPIO_2	B	PD			
68	XGPIO_1	B	PD			
69	VSS	PG		IO Gnd		
70	XGPIO_0	B	PD			
71	IOVDD	PG		IO Power (3.3V)		
72	VSS	PG		Core + IO Gnd		
73	VDD	PG		Core Power (1.2V)		
74	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
75	DM_DQ15	B		DRAM DATA		
76	DM_DQ14	B		DRAM DATA		
77	DM_DQ13	B		DRAM DATA		

78	DM_DQ12	B		DRAM DATA		
79	DM_DQ11	B		DRAM DATA		
80	DM_DQ10	B		DRAM DATA		
81	DM_VSSP	PG		DRAM IO GND		
82	DM_DVSS	PG		DRAM VSS		
83	DM_DVDD	PG		DRAM VDD (1.2V)		
84	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
85	DM_DQ9	B		DRAM DATA		
86	DM_DQ8	B		DRAM DATA		
87	DM_UDQS	B		DRAM DQS		
88	DM_UDM	B		DRAM DM Byte Mask		
89	DM_CKB	O		DRAM CKB		
90	DM_CK	O		DRAM CLK		
91	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
92	DM_CKE	O		DRAM CKE		
93	DM_A12	O		DRAM ADDRESS		
94	DM_A11	O		DRAM ADDRESS		
95	DM_DVDD	PG		DRAM VDD (1.2V)		
96	DM_DVSS	PG		DRAM VSS		
97	DM_A9	O		DRAM ADDRESS		
98	DM_VSSP	PG		DRAM IO GND		
99	DM_A8	O		DRAM ADDRESS		
100	DM_A7	O		DRAM ADDRESS		
101	DM_DVDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
102	DM_A6	O		DRAM ADDRESS		
103	DM_A5	O		DRAM ADDRESS		
104	DM_A4	O		DRAM ADDRESS		
105	DM_AVSS_DLL	PG		DRAM DLL AVSS		
106	DM_A1V2_DLL_PLL	PG		DRAM DLL AVDD (1.2V)		
107	DM_AVSS_PLL	PG		DRAM PLL AVSS		
108	DM_VREF	I		DRAM VREF		
109	DM_VSSP	PG		DRAM VSS for VREF		
110	DM_A3	O		DRAM ADDRESS		
111	DM_A2	O		DRAM ADDRESS		
112	DM_A1	O		DRAM ADDRESS		
113	DM_A0	O		DRAM ADDRESS		
114	DM_DVDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
115	DM_A10	O		DRAM ADDRESS		
116	DM_BA1	O		DRAM BANK ADDRESS		
117	DM_VSSP	PG		DRAM IO GND		
118	DM_BA0	O		DRAM BANK ADDRESS		

119	DM_DVDD	PG		DRAM VDD (1.2V)		
120	DM_DVSS	PG		DRAM VSS		
121	DM_A13	O		DRAM ADDRESS		
122	DM_CSN	O		DRAM CSN		
123	DM_RAS	O		DRAM RAS		
124	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
125	DM_CAS	O		DRAM CAS		
126	DM_VSSP	PG		DRAM IO GND		
127	DM_WEN	O		DRAM WEN		
128	DM_LDM	B		DRAM DM Byte Mask		
129	DM_LDQS	B		DRAM DQS		
130	DM_DQ7	B		DRAM DATA		
131	DM_DQ6	B		DRAM DATA		
132	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
133	DM_DVDD	PG		DRAM VDD (1.2V)		
134	DM_DVSS	PG		DRAM VSS		
135	DM_VSSP	PG		DRAM IO GND		
136	DM_DQ5	B		DRAM DATA		
137	DM_DQ4	B		DRAM DATA		
138	DM_DQ3	B		DRAM DATA		
139	DM_DQ2	B		DRAM DATA		
140	DM_DQ1	B		DRAM DATA		
141	DM_DQ0	B		DRAM DATA		
142	DM_VDDP	PG		DRAM IO Power (1.8V/2.5V/3.3V)		
143	IOVDD	PG		IO Power (3.3V)		
144	VSS	PG		Core + IO Gnd		
145	VDD	PG		Core Power (1.2V)		
146	B_NAND0	B	PD	NAND_CH0_DATA[0]		
147	B_NAND1	B	PD	NAND_CH0_DATA[1]		
148	B_NAND2	B	PD	NAND_CH0_DATA[2]		
149	B_NAND3	B	PD	NAND_CH0_DATA[3]		
150	B_NAND4	B	PD	NAND_CH0_DATA[4]		
151	B_NAND5	B	PD	NAND_CH0_DATA[5]		
152	B_NAND6	B	PD	NAND_CH0_DATA[6]		
153	B_NAND7	B	PD	NAND_CH0_DATA[7]		
154	B_NAND8	B	PD	NAND_CH0_ALE		
155	B_NAND9	B	PD	NAND_CH0_CLE		
156	B_NAND10	B	PU	NAND_CH0_RD		
157	B_NAND11	B	PU	NAND_CH0_WR		
158	B_NAND12	B	PU	NAND_CH0_CS[0]		
159	B_NAND13	B	PU	NAND_CH0_RDY[0]		

160	B_NAND14	B	PU	NAND_CH0_CS[1]		
161	B_NAND15	B	PU	NAND_CH0_RDY[1]		
162	IOVSS	PG		IO Gnd		
163	IOVDD	PG		IO Power (3.3V)		
164	B_UART_BT0	B	PU	UART_BT_TX		GPIO1[22]
165	B_UART_BT1	B	PU	UART_BT_RX		GPIO1[23]
166	B_I2C0_SDA	B	PU	C_I2C_SDA	B_I2C_SDA	B&C
167	B_I2C1_SCL	B	PU	C_I2C_SCL	B_I2C_SCL	B&C
168	B_KEYSCAN7	B	PD	UART_BT_RTS*	SPI_CH0_CLK	GPIO0[7]
169	B_KEYSCAN6	B	PD	UART_BT_CTS*	SPI_CH0_DI	GPIO0[6]
170	B_KEYSCAN5	B	PD	GPIO0[5]	SPI_CH0_DO	SD_WIFI_DAT[3]
171	B_KEYSCAN4	B	PD	GPIO0[4]	SPI_CH0_CS[0]	SD_WIFI_DAT[2]
172	B_KEYSCAN3	B	PD	GPIO0[3]	SPI_CH0_CS[1]	SD_WIFI_DAT[1]
173	B_KEYSCAN2	B	PD	GPIO0[2]		SD_WIFI_DAT[0]
174	B_KEYSCAN1	B	PD	UART_MISC_RTS*	GPIO0[1]	SD_WIFI_CMD
175	B_KEYSCAN0	B	PD	UART_MISC_CTS*	GPIO0[0]	SD_WIFI_CLK
176	B_GPIO1	B	PD	GPIO_USB[0]		GPIO0[8]
177	B_PWM0	B	PD	GPIO_PWM[0]		GPIO1[18]
178	B_UART_MISC1	B	PU	UART_MISC_RX		GPIO3[12]
179	B_UART_MISC0	B	PU	UART_MISC_TX		GPIO3[11]
180	B_GPIO0	B	PD	GPIO_SD_DETECT	MS_INS	GPIO0[9]
181	B_SD_CARD5	B	PU	SD_CARD_DAT[3]	MS_BS	GPIO3[5]
182	B_SD_CARD4	B	PU	SD_CARD_DAT[2]	MS_CLK	GPIO3[4]
183	B_SD_CARD3	B	PU	SD_CARD_DAT[1]	MS_DAT[3]	GPIO3[3]
184	B_SD_CARD2	B	PU	SD_CARD_DAT[0]	MS_DAT[2]	GPIO3[2]
185	B_SD_CARD1	B	PU	SD_CARD_CMD	MS_DAT[1]	GPIO3[1]
186	B_SD_CARD0	B	PU	SD_CARD_CLK	MS_DAT[0]	GPIO3[0]
187	I_TEST_MD	I		TEST_MD		
188	IOVDD	PG		IO Power (3.3V)		
189	VSS	PG		Core + IO Gnd		
190	VDD	PG		Core Power (1.2V)		
191	XPRSTNN	I		Super reset		
192	PWRON0	I		POWERON INPUT		
193	DC2DC_EN	O		External DC2DC enable		
194	DC2DC_FB	I		DC-DC detection voltage PAD from off-chip by user decision		
195	BAT_FB	I		Battery detection voltage PAD from off-chip by user decision		
196	VDDALCD	PG		PWRC POWER		
197	PWRON1	I		USB VBUS INPUT (3.3V)		
198	OVSSRTC	PG		RTC GND		
199	XTAL_32K_O	O		RTC XTAL PAD		
200	XTAL_32K_I	I		RTC XTAL PAD		

201	OVDDRTC	PG		RTC POWER		
202	USB0_A3V3RXC	PG		USB analog power for USB core		
203	USB1_REXT	A		USB external resistor		
204	USB1_AVSSRXC	PG		USB analog ground for USB core		
205	USB1_A3V3RXC	PG		USB analog power for USB core		
206	USB1_DM	B		USB high speed D+		
207	USB1_DP	B		USB high speed D-		
208	USB1_A3V3TX	PG		USB analog power for USB core		
209	USB1_AVSSTX	PG		USB analog ground for USB core		
210	XTAL_3V3	PG		Sys PLL 3V3		
211	XTAL_VSS	PG		Sys + XTAL GND		
212	XTAL_27M_O	O		XTAL PAD		
213	XTAL_27M_I	I		XTAL PAD		
214	A1V2_APLL	PG		Audio / Sys PLL 1V2		
215	APLL_CP	A		Audio PLL Loop filter pin		
216	A3V3_APLL	PG		Audio PLL 3.3V		

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC supply voltage	A3V3_VDAC, A3V3_SP, AVDDAUD, A3V3_CODEC, IOVDD, USB0_A3V3RXC, USB1_A3V3RXC, USB1A3V3TX, XTAL_3V3	-0.3 to 3.6	V
	A1V2_APLL, VDD, DM_DVDD, DM_A1V2_DLL, DM_A1V2_PLL	-0.3 to 1.32	V
	DM_VDDP	-0.3 to 3.6	V
DC input voltage	VDDALVD	-0.3 to 4.2	V
Operating Temperature	TOPT	0 to +70	°C
Storage Temperature	TSTG	-55 to 125	°C

6.2. DC Characteristics (T_A＝25℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IOVDD	I/O supply voltage	3.0	3.3	3.6	V
VDD	Core supply voltage	1.08	1.2	1.32	V
USB0_A3V3RXC, USB1_A3V3RXC, USB1A3V3TX	USB supply voltage	3.0	3.3	3.6	V
XTAL_3V3	XTAL supply voltage	3.0	3.3	3.6	V
A3V3_VDAC	Video DAC supply voltage	3.0	3.3	3.6	V
A3V3_SP, AVDDAUD, A3V3_CODEC	Audio codec supply voltage	3.0	3.3	3.6	V
DM_VDDP	SDRAM I/O supply voltage	3.0	3.3	3.6	V
	DDR I/O supply voltage	2.25	2.5	2.75	V
	mDDR/DDR2 I/O supply voltage	1.62	1.8	1.98	V

(T_A＝25℃, IOVDD＝3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Input low voltage	-0.3	-	0.3*IOVDD	V
VIH	Input high voltage	0.7*IOVDD	-	IOVDD+10%	V
IOL	Output low current	4.4	-	8.9	mA
IOH	Output high current	10	-	21	mA
VT＋	Schmitt trigger positive-going threshold	1.48	-	1.53	V
VT－	Schmitt trigger negative-going threshold	1.28	-	1.34	V
VHYS	Hysteresis voltage for Schmitt trigger	0.19	-	0.21	V
IIL	Input leakage current	0	0	0	μA
Rd－	Pull down resistor	42K	-	44K	Ohm
Rd+	Pull up resistor	43K	-	44.5K	Ohm

6.3. Audio DAC Characteristics

(T_A =25°C, A3V3_CODEC =3.3V±10%, A1V2_APLL=1.2V±10%, Clock 12.288MHz)

Parameter	Condition	Min	Typ	Max	Unit
Output voltage	Headphone output	-	0.545*AVDD33	-	Vpp
Frequency response		20	-	19,200	Hz
Signal to noise ratio (SNR)		85	90	-	dB
Total harmonic distortion + noise (THD+N)	FIN = 1kHz, Output voltage is full swing	-	-	0.01	%
Output volume control: Gain Range Step Size Step Variation		 -46.5 - -	 - 1.5 0.15	 0 - -	 dB dB dB

■ **Headphone Audio Driver Characteristics**

(T_A=25°C, A3V3_CODEC =3.3V±10%, A1V2_APLL=1.2V±10%)

Parameter	Condition	Min	Typ	Max	Unit
Output power	FIN = 1kHz, THD+N = 0.1% RL = 16Ω RL = 32Ω		 20 10		mW
Total harmonic distortion + noise (THD+N)	FIN = 1kHz, PO = 20mW, RL = 16Ω	-	0.1	-	%

■ **Microphone Bias Electrical Characteristics**

(T_A=25°C, A3V3_CODEC =3.3V±10%, A1V2_APLL=1.2V±10%)

Parameter	Condition	Min	Typ	Max	Unit
Bias voltage			0.75*VDDAD		V
Bias current source				3	mA
Output noise voltage	1kHz~20kHz		25		nV/(Hz^0.5)

■ **Analog-to-digital converter electrical characteristics**

(T_A=25°C, A3V3_CODEC =3.3V±10%, A1V2_APLL=1.2V±10%, Clock 12.288MHz)

Parameter	Condition	Min	Typ	Max	Unit
Input voltage (MICIN)	Boost gain = 20dB PGA gain = 0dB			VDDAD/13.75	Vpp
Frequency response		20		19,200	Hz
Boost amplifier: Gain Range Step Size Step Variation		 0	 20 2	 20	 dB dB dB
PGA: Gain Range Step Size Step Variation		 -12	 1.5 0.15	 33	 dB dB dB

Signal to noise ratio (SNR)	FIN = 1kHz, Boost gain = 0dB PGA gain = 0dB		85		dB
Total harmonic distortion + noise (THD+N)	FIN = 1kHz, Boost gain =20dB PGA gain = 0dB			0.01	%

■ **General ADC Characteristics**

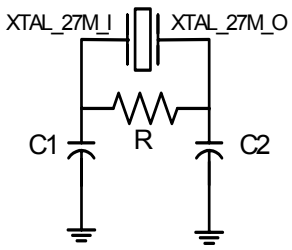
(T_A=25°C, A3V3_CODEC=3.3V±10%, A1V2_APLL=1.2V±10%)

Parameter	Condition	Min	Typ	Max	Unit
Input voltage range		0	-	3.6	V
Input capacitance		-	12	-	pf
Resolution		-	-	10	Bits
No missing codes		8	-	-	Bits
Differential Nonlinearity		-1	-	+1	LSB
Integral Nonlinearity		-2	-	+2	LSB
Schmitt-trigger: Input low level voltage Window		 - -	 0.9 400	 - -	 V mV

■ **Video-DAC Interface Characteristics**

Parameter	Condition	Min.	Typ.	Max.	Units
Power supply		3.0	3.3	3.6	V
Resolution		-	10	-	Bits
INL		-	2.5	-	LSB
DNL		-	0.5	-	LSB
Clock frequency		-	27	-	MHz
Output Voltage	Rset=1.2K	1.25	1.28	1.3	V

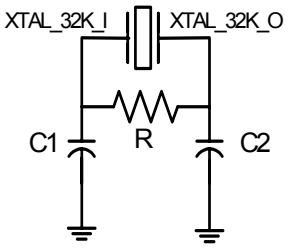
■ **27MHz XTAL Crystal Oscillation**



Parameter	Min.	Typ.	Max.	Unit
Resistor (R)	-	1	-	MΩ
Capacitor (C1)	-	22	-	pf
Capacitor (C2)	-	22	-	pf

Note: The typical value is suitable for 27M Hz crystal input.

■ **RTC Crystal Oscillation**

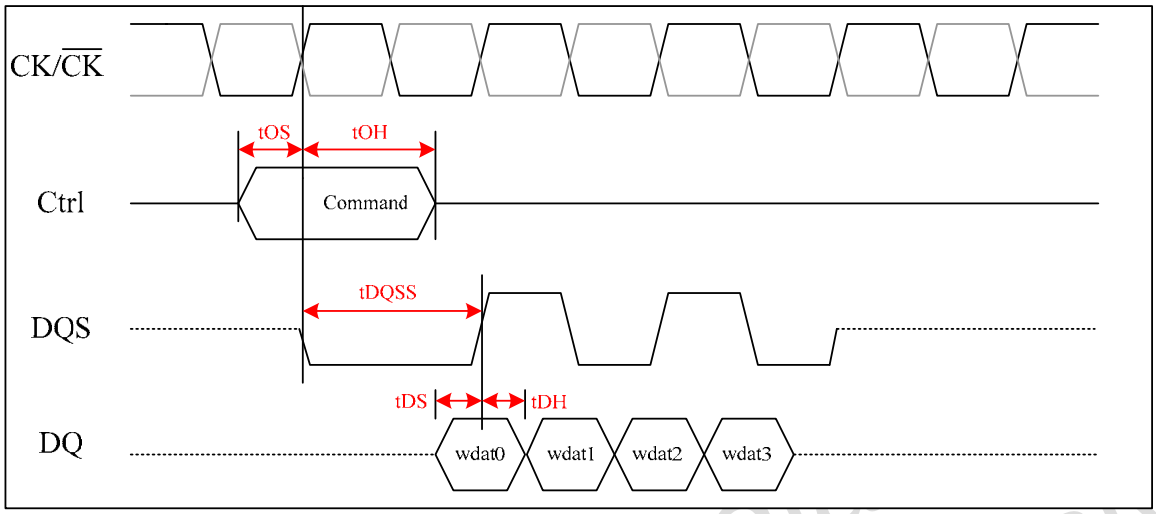


Parameter	Min.	Typ.	Max.	Unit
Resistor (R)	-	NC	-	MΩ
Capacitor (C1)	-	16	-	pf
Capacitor (C2)	-	16	-	pf

Note: The typical value is suitable for 32768Hz crystal input.

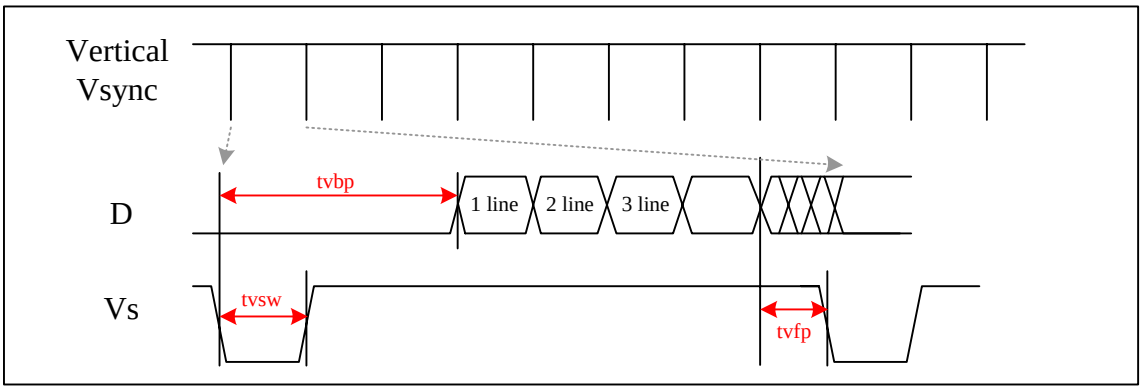
7. AC SPECIFICATIONS

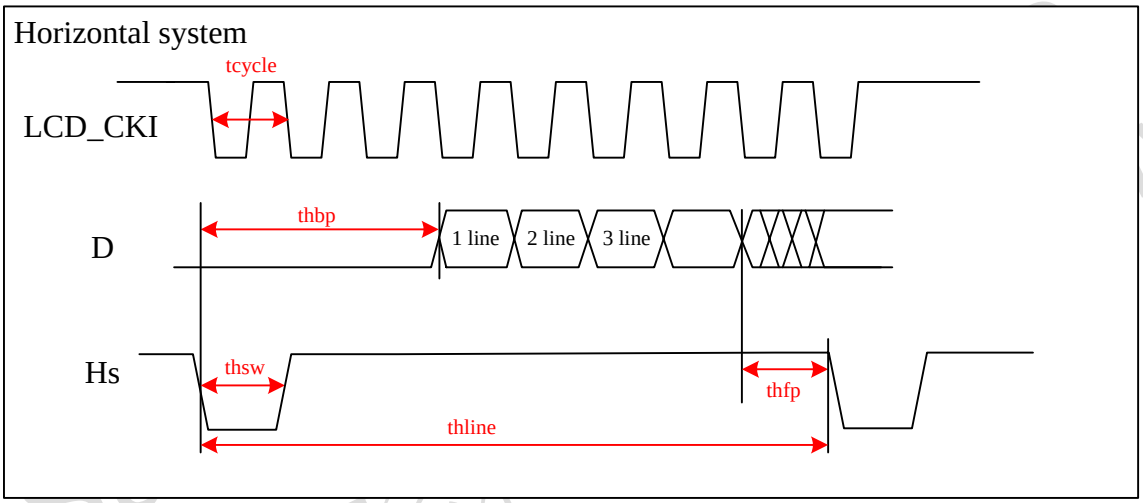
7.1. SDR/DDR/DDR2 DRAM Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
tOS	Output command setup time	0.75	-	-	ns
tOH	Output command hold time	0.75	-	-	ns
tDQSS	Write command to first DQS latching transition	0.75	-	1.25	tCK
tDS	DQ and DM output setup time	0.45	-	-	ns
tDH	DQ and DM output hold time	0.45	-	-	ns

7.2. LCD RGB Interface





Symbol	Parameter	Min.	Typ.	Max.	Unit
tml	LCD_CKI low period	25	37	111	ns
tmh	LCD_CKI high period	25	37	111	ns
thsw	Hs low width	1	-	255	tcycle
thbp	Hs back porch	1	-	1023	tcycle
thfp	Hs front porch	1	-	1023	tcycle
tvsw	Vs low width	1	-	31	thline
tvbp	Vs back porch	1	-	255	thline
tvfp	Vs front porch	1	-	255	thline

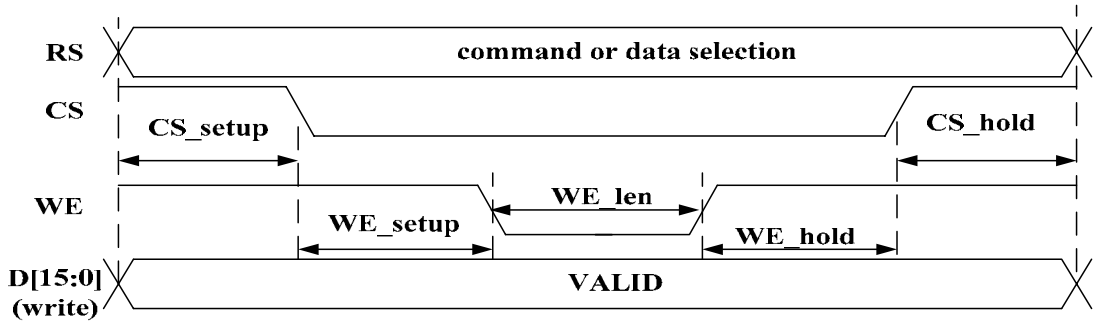
Note:

1. n is programmable.
2. LCD_CKI is programmable (derived from SPLL clock).

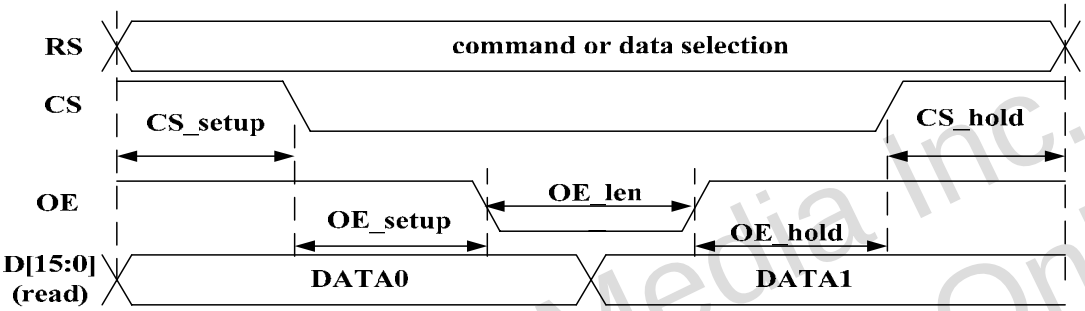
7.3. LCM (i8080 CPU) Interface

I8080 CPU interface has both command cycle and data cycle. The command cycle, the data cycle, the pulse width of CS, WE, and OE are all programmable.

8080 write AC timing is as below (RS=0 command, RS=1 data):



8080 read AC timing is as below (RS=0 command, RS=1 data):



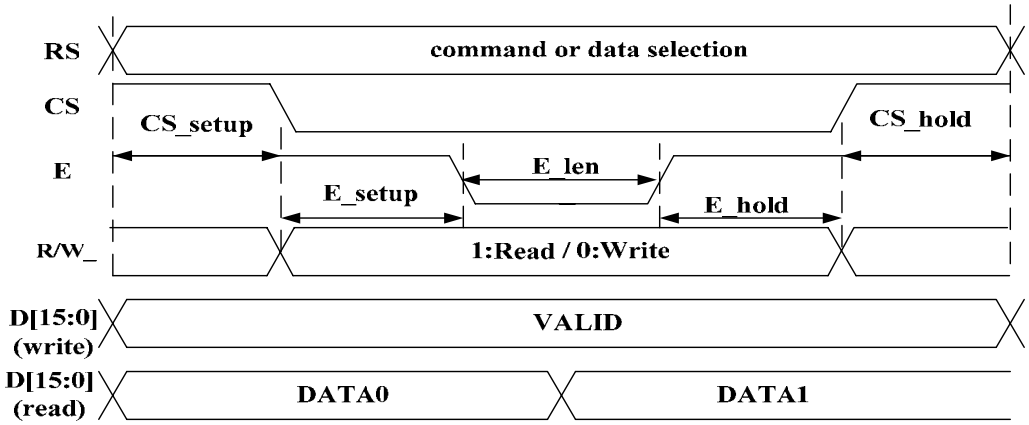
Symbol	Parameter	Min.	Typ.	Max.	Unit
CS_setup	CS setup time	1	-	15	Clk
CS_hold	CS hold time	1	-	15	Clk
WE_setup	WE setup time	1	-	15	Clk
WE_len	WE width	1	-	255	Clk
WE_hold	WE hold time	1	-	15	Clk
OE_setup	OE setup time	1	-	15	Clk
OE_len	OE width	1	-	255	Clk
OE_hold	OE hold time	1	-	15	Clk

Note:

1.Clk is the clock period of the module on which the accessing register or port is located.

2. n is programmable.

7.4. LCM (M68 CPU) read/write data selected by R/W pin



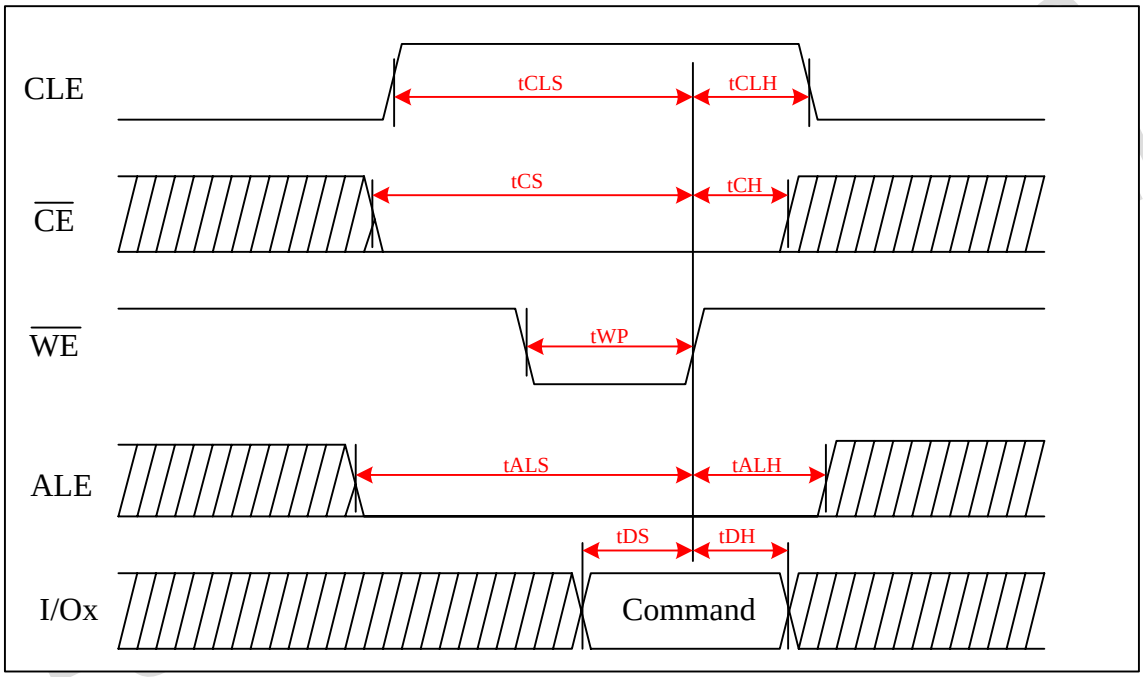
Symbol	Parameter	Min.	Typ.	Max.	Unit
CS_setup	CS setup time	1	-	15	cycle

CS_hold	CS hold time	1	-	15	ns
E_setup	E setup time	1	-	15	ns
E_len	E width	1	-	255	ns
E_hold	E hold time	1	-	15	ns

Note:
1. Clk is the clock period of the module on which the accessing register or port is located.
2. n is programmable.

7.5. NAND Flash Interface

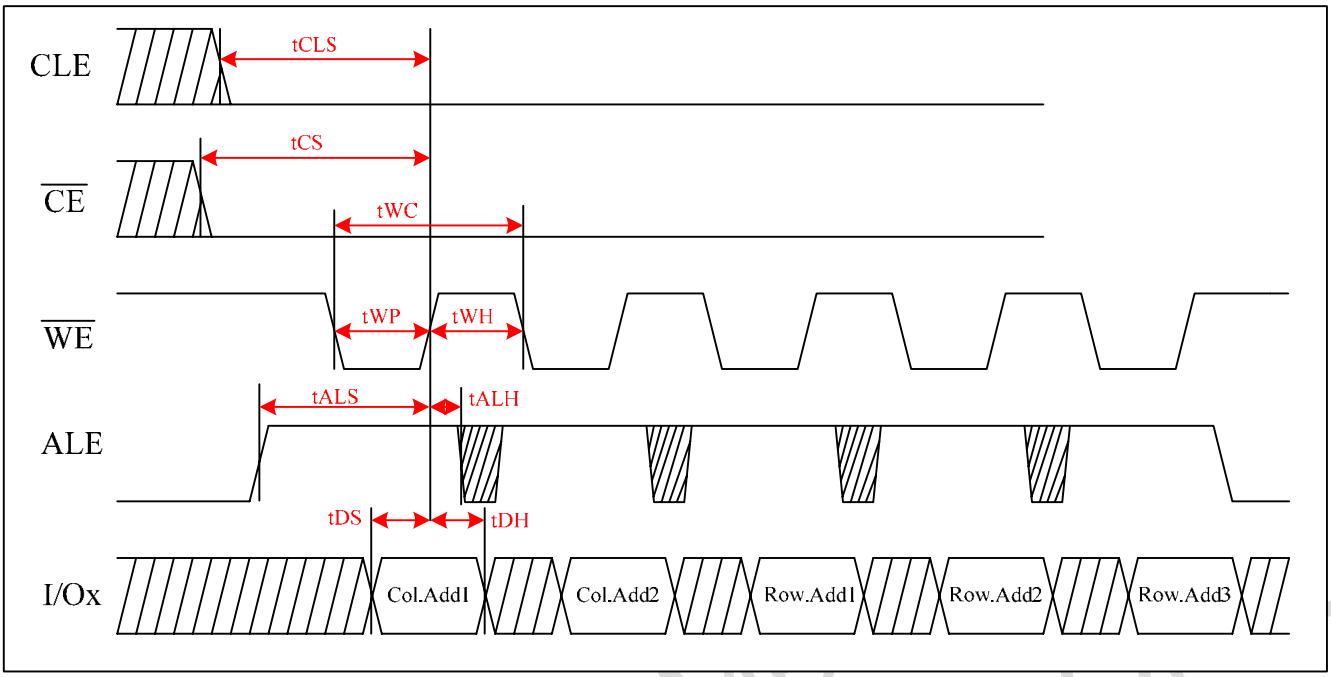
(1) Command Latch cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLS	CLE setup time	15	-	-	ns
tCLH	CLE hold time	5	-	-	ns
tCS	CEN setup time	20	-	-	ns
tCH	CEN hold time	5	-	-	ns
tWP	WEN pulse width	15	-	-	ns
tALS	ALE setup time	15	-	-	ns
tALH	ALE hold time	5	-	-	ns
tDS	Data setup time	15	-	-	ns
tDH	Data hold time	5	-	-	ns

Note: Timings are programmable

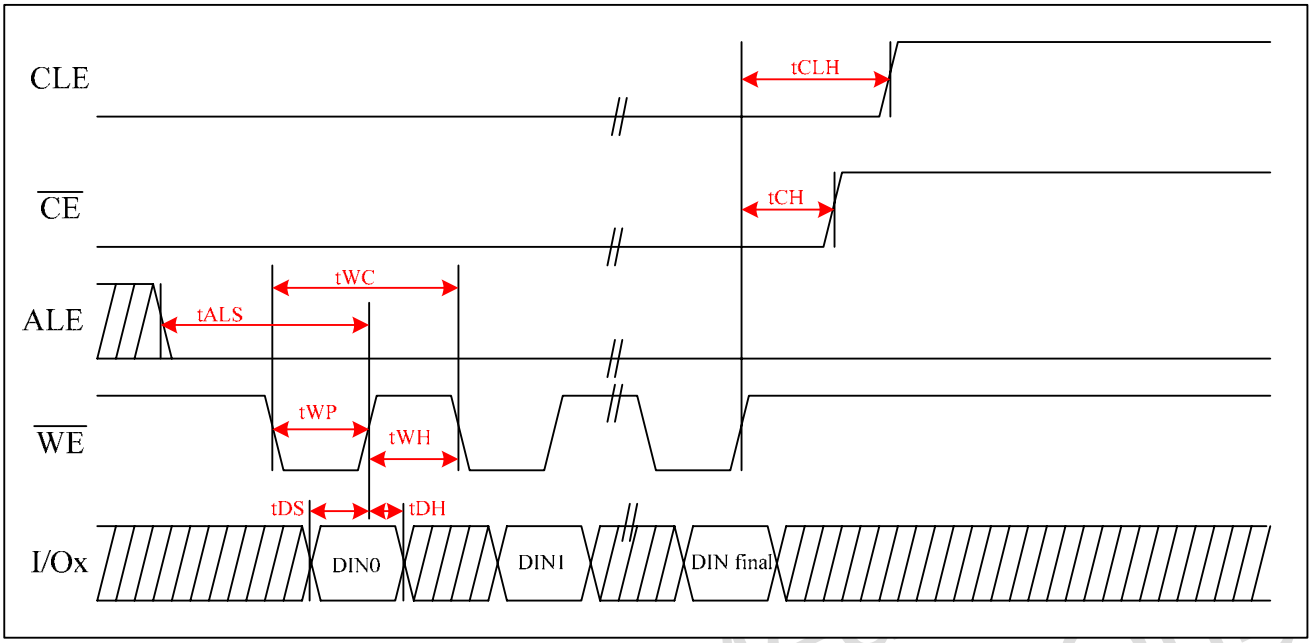
(2) Address latch cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLS	CLE setup time	15	-	-	ns
tCS	CEN setup time	20	-	-	ns
tWC	Write cycle time	30	-	-	ns
tWP	WEN pulse width	15	-	-	ns
tWH	WEN high hold time	10	-	-	ns
tALS	ALE setup time	15	-	-	ns
tALH	ALE hold time	5	-	-	ns
tDS	D[7:0] setup time	15	-	-	ns
tDH	D[7:0] hold time	5	-	-	ns

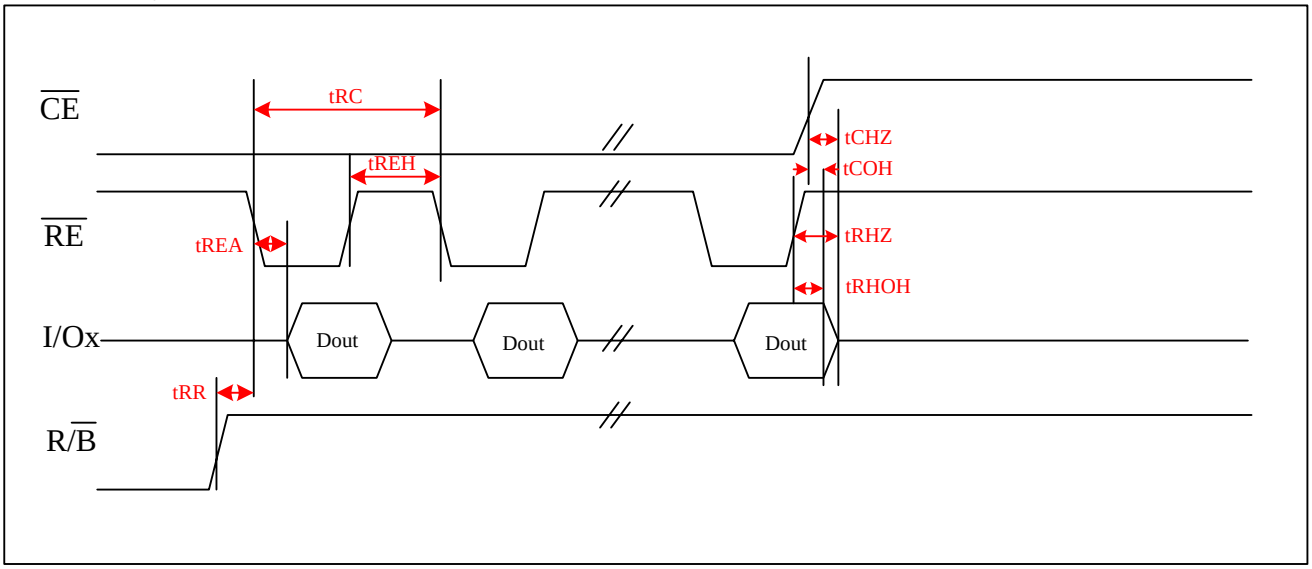
Note: Timings are programmable

(3) Input Data Latch Cycle



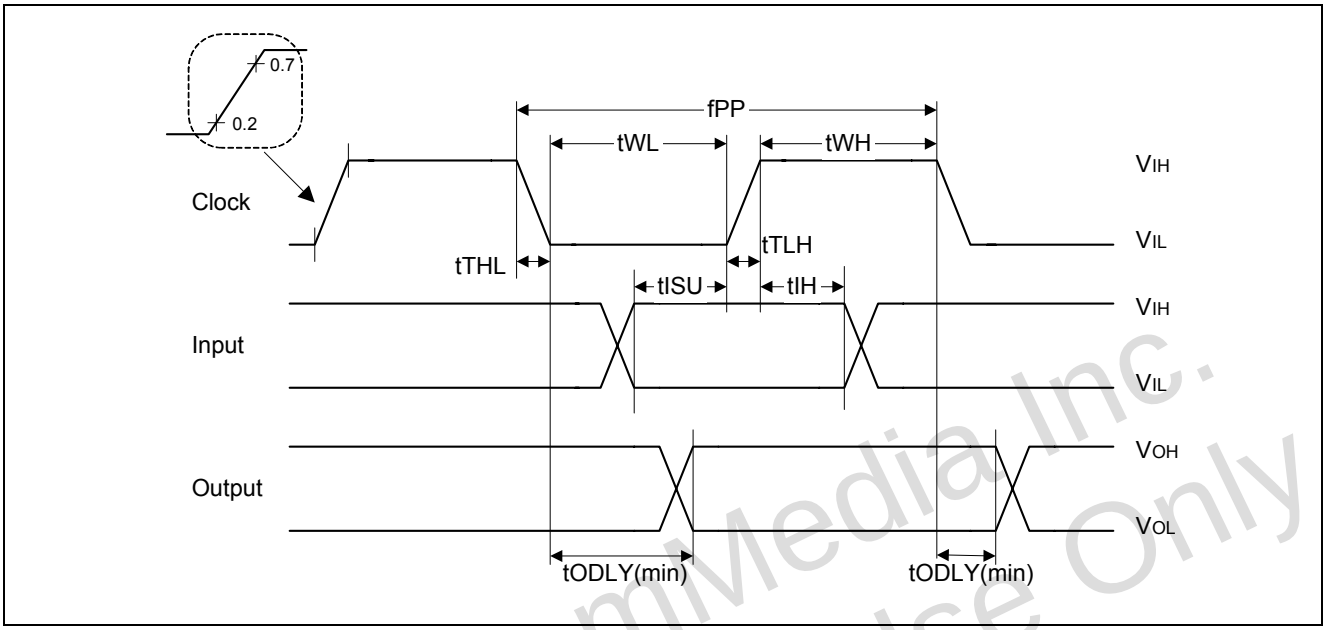
Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLH	CLE hold time	5	-	-	ns
tCH	CEN hold time	5	-	-	ns
tWC	Write cycle time	30	-	-	ns
tWP	WEN pulse width	15	-	-	ns
tWH	WEN high hold time	10	-	-	ns
tALS	ALE setup time	15	-	-	ns
tDS	D[7:0] setup time	15	-	-	ns
tDH	D[7:0] hold time	5	-	-	ns

(4) Output Data Access Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
tCHZ	CEN High to Output Hi-Z	-	-	30	ns
tRC	Read Cycle Time	30	-	-	ns
tREH	REN High Hold Time	10	-	-	ns
tREA	REN Access Time	-	-	20	ns
tRHZ	REN High to Output Hi-Z	-	-	100	ns
tOH	REN or CEN High to Output hold	15	-	-	ns
tRR	Ready to REN Low	20	-	-	ns

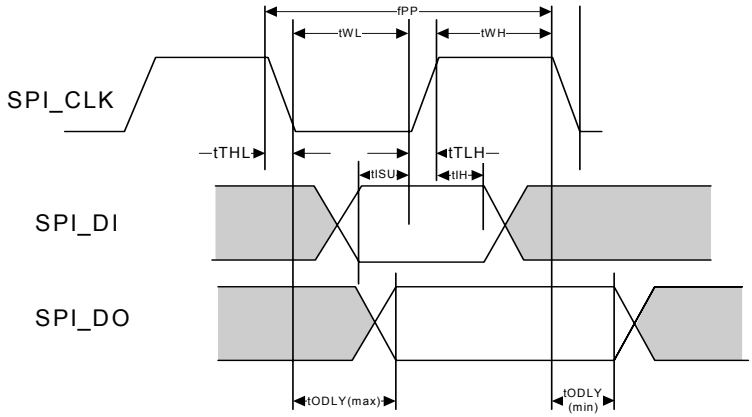
7.6. SD/SDIO Card Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Clock frequency data transfer mode	0	24.0	25	MHz
tWL	Clock low time	10	12.7	-	ns
tWH	Clock high time	10	15.6	-	ns
tTLH	Clock rise time	-	5.8	10	ns
tTHL	Clock fall time	-	7.6	10	ns
tISU	Input setup time	5	8.0	-	ns
tIH	Input hold time	5	14.4	-	ns
tODLY	Output delay time (Identification Mode)	0	7.6~8.4	50	ns
tODLY	Output delay time (Data transfer mode)	0	7.6~8.4	14	ns

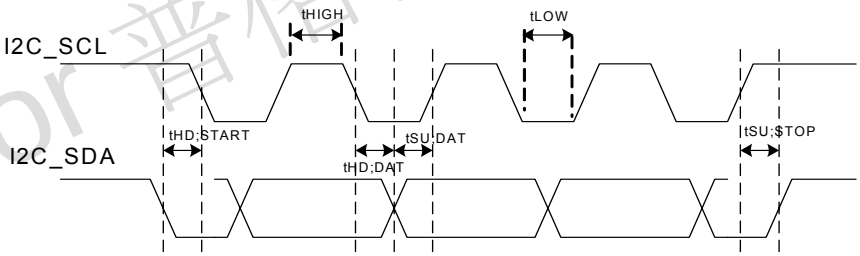
Note: ※ note CL≤100pF (7 Cards), ＊ note CL≤25pF (1 Card)

7.7. SPI Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Clock frequency data transfer mode			20	MHz
tWL	Clock low time			25	ns
tWH	Clock high time			25	ns
tTLH	Clock rise time		5		ns
tTHL	Clock fall time		5		ns
tISU	Input setup time		5		ns
tIH	Input hold time		5		ns

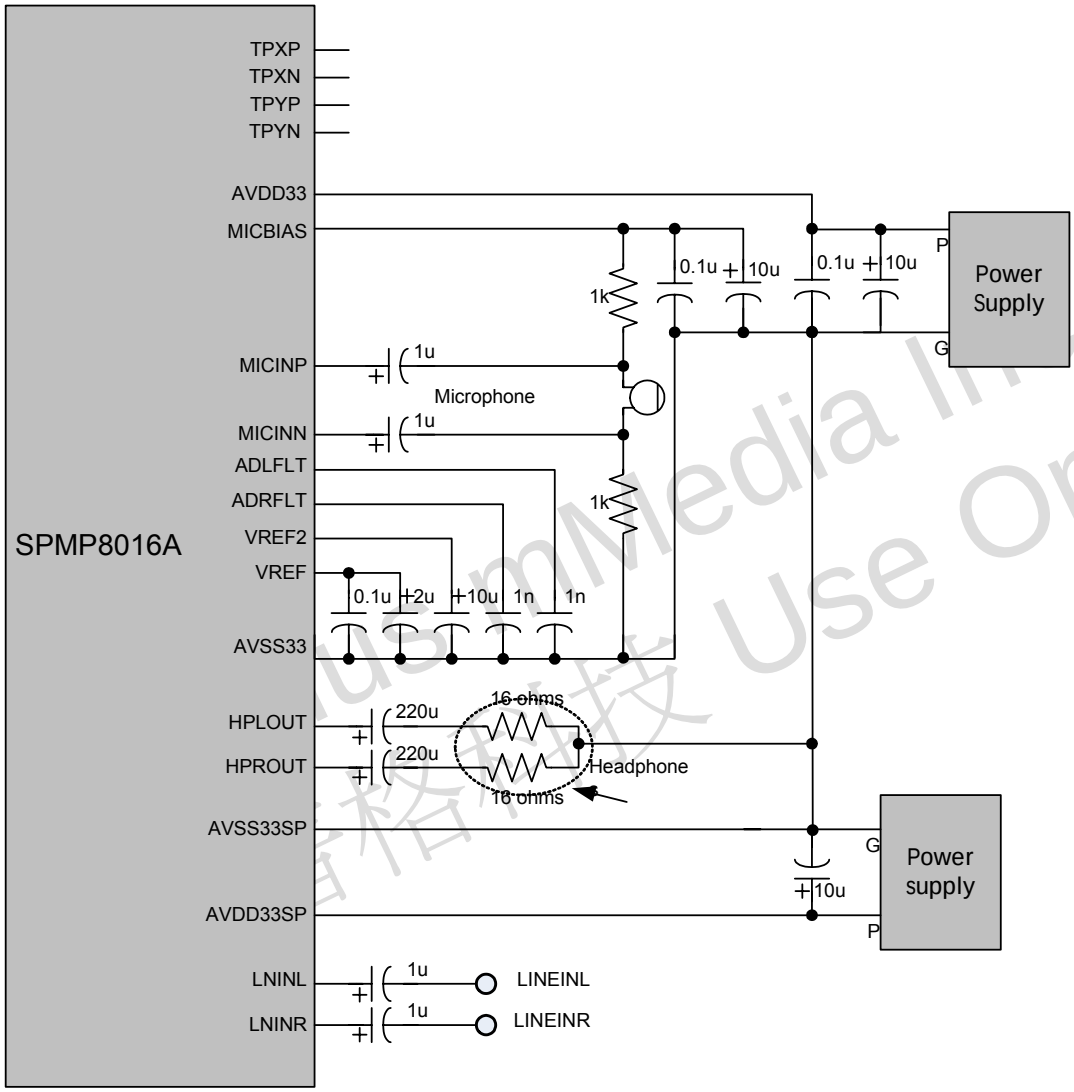
7.8. I2C Interface



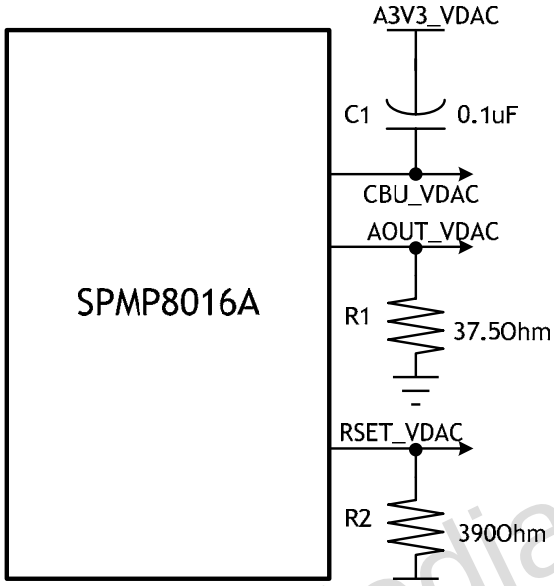
Symbol	Parameter	Min	Typ	Max	Unit
tHIGH	High period of I2C_SCL	4.0	-	-	us
tLOW	Low period of I2C_SCL	4.7	-	-	us
tHD; DAT	Data hold time	5.0	-	-	us
tSU; DAT	Data set-up time	250	-	-	ns
tHD; STA	Hold time for start condition	4.0	-	-	us
tSU; STO	Set-up time for stop condition	4.0	-	-	us

Note: Timings are programmable

7.9. Audio codec



7.10. TV-Out DAC

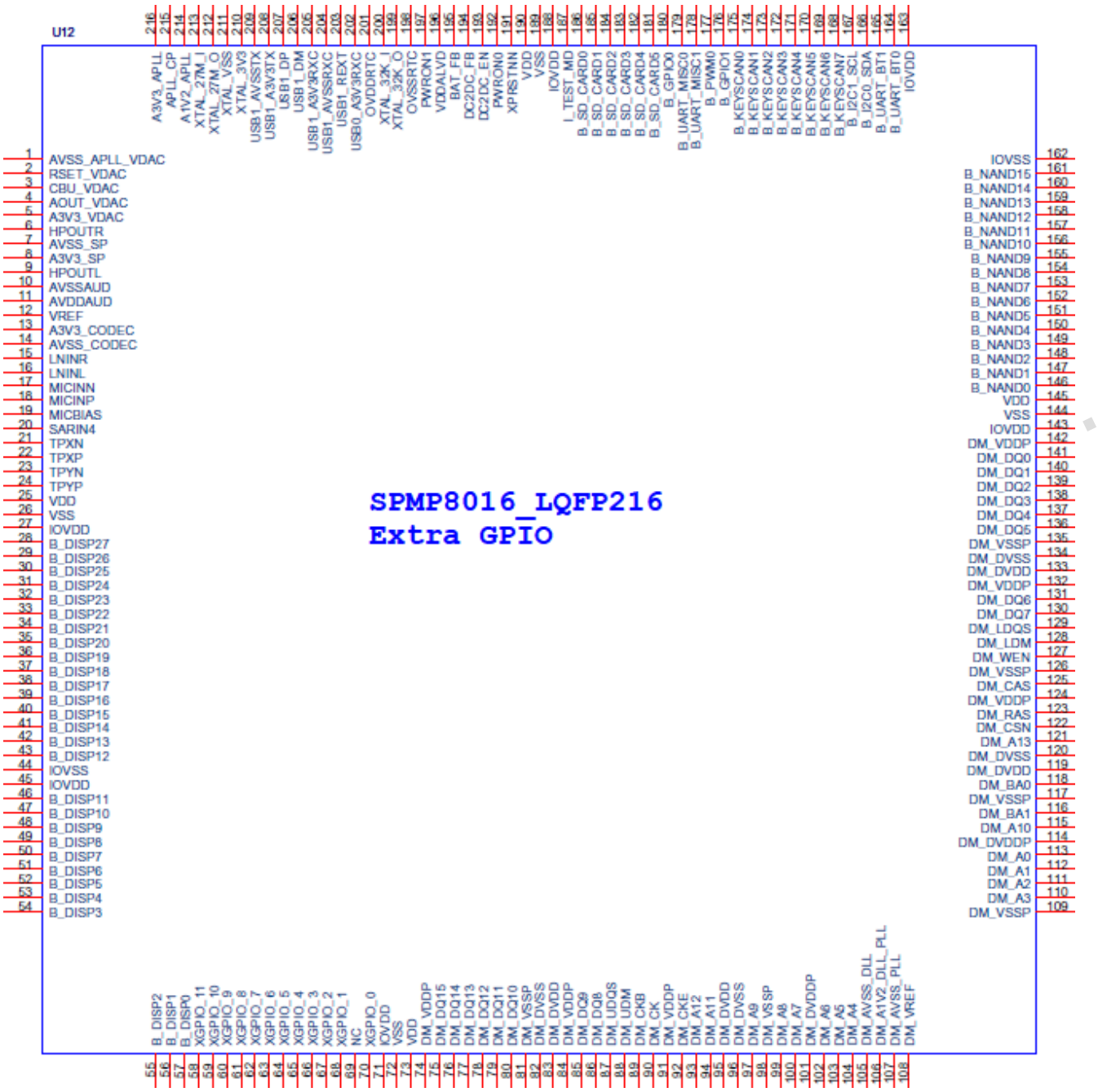


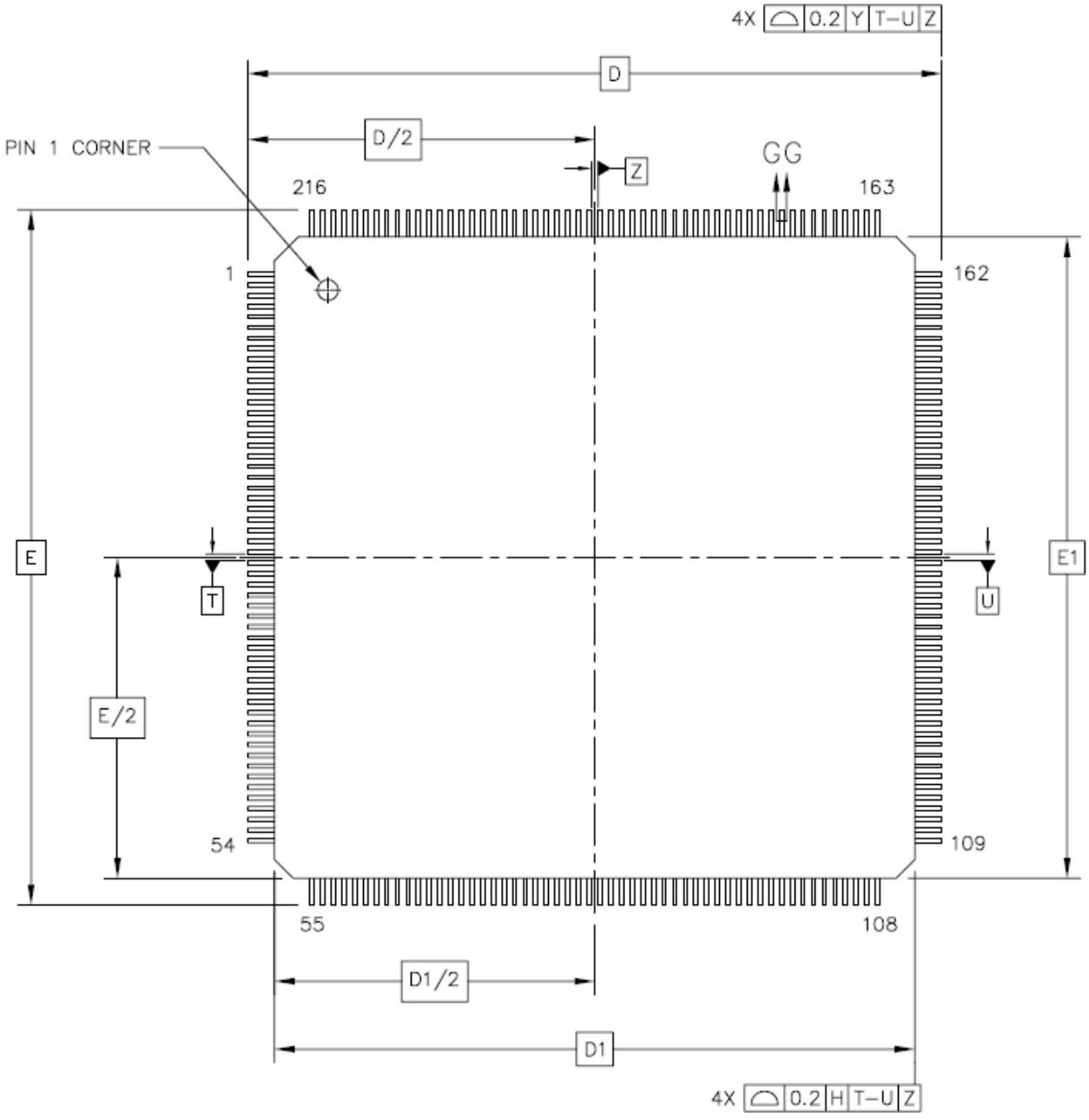
C1, R1, R2 are external components

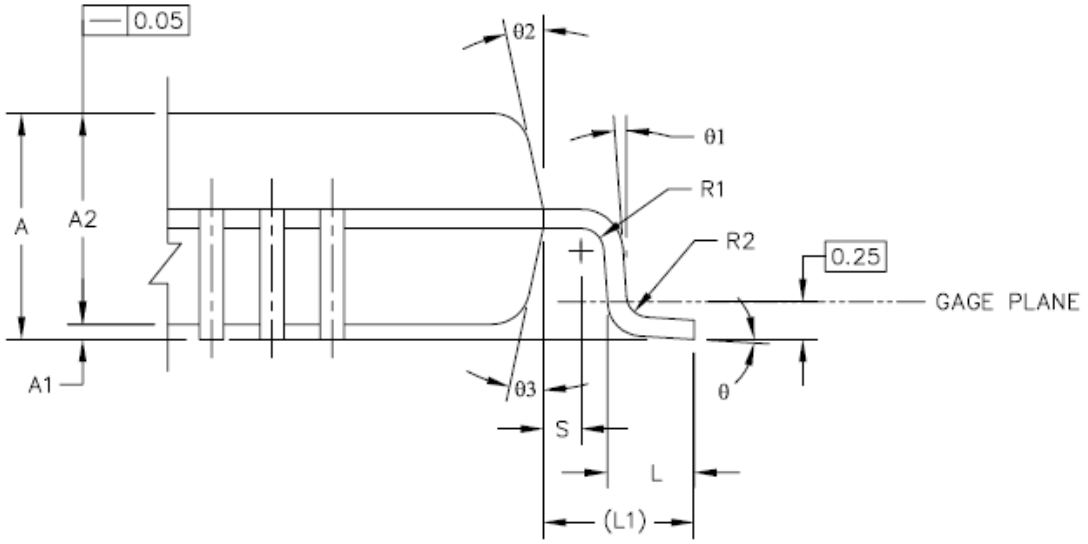
8. IO TRAP SETTING

I/O	I/O Trap Definition
B_DISPLAY10	Trap[6], DDR (0) /SDR (1), “0” for default

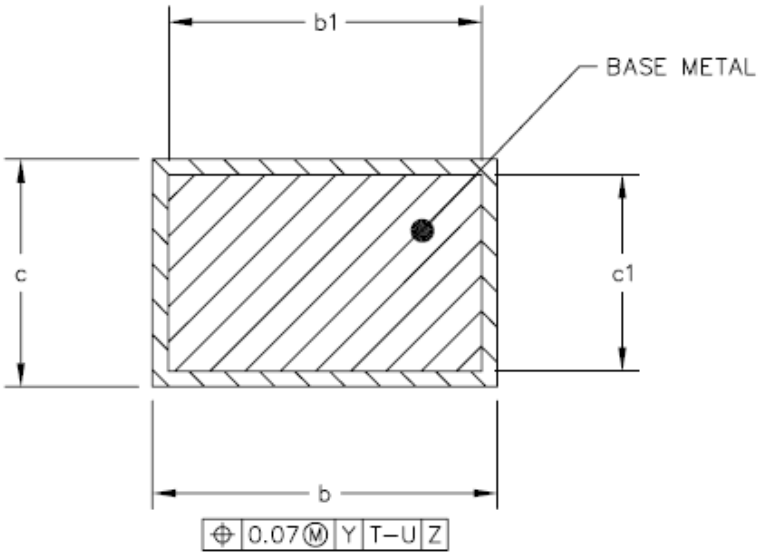
9. PACKAGE




4X 0.2 Y T-U Z
D
D/2
PIN 1 CORNER
Z
GG
216
163
1
162
E
T
U
E1
E/2
54
109
55
108
D1/2
D1
4X 0.2 H T-U Z



DETAIL F



SECTION G–G

DIM	Min.	Typ.	Max.	Note
A	-	-	1.6 mm	1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane datum H. 2. Dimension b does not include DAMBAR protrusion. DAMBAR protrusion allowable DAMBAR protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. DAMBAR can not be located on the lower radius or the foot. Minimum between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
A1	0.05 mm	-	0.15 mm	
A2	1.35 mm	1.4 mm	1.45 mm	
b	0.13 mm	0.18mm	0.23 mm	
b1	0.13 mm	0.16mm	0.19 mm	
c	0.09 mm	-	0.2 mm	
c1	0.09 mm	-	0.16 mm	
D	-	26 mm	-	
D1	-	24 mm	-	
e	-	0.4 mm	-	
E	-	26 mm	-	
E1	-	24 mm	-	
L	0.45 mm	0.6 mm	0.75mm	
L1	-	1 mm	-	
R1	0.08 mm	-	-	
R2	0.08 mm	-	-	
S	0.2 mm	-	-	
θ	0^0	3.5^0	7^0	
θ1	0^0	-	-	
θ2	11^0	12^0	13^0	
θ3	11^0	12^0	13^0	
LQFP 216 LD, 24X24X1.4 PKG, 0.4 PITCH POD, 2mm FOOTPRINT				

9.1. Ordering Information

Product Number	Package Type	Memo
TBD	LQFP 216 pins 24 x 24 x 1.4 mm	Green package in tray

9.2. Storage Condition and Period for Package

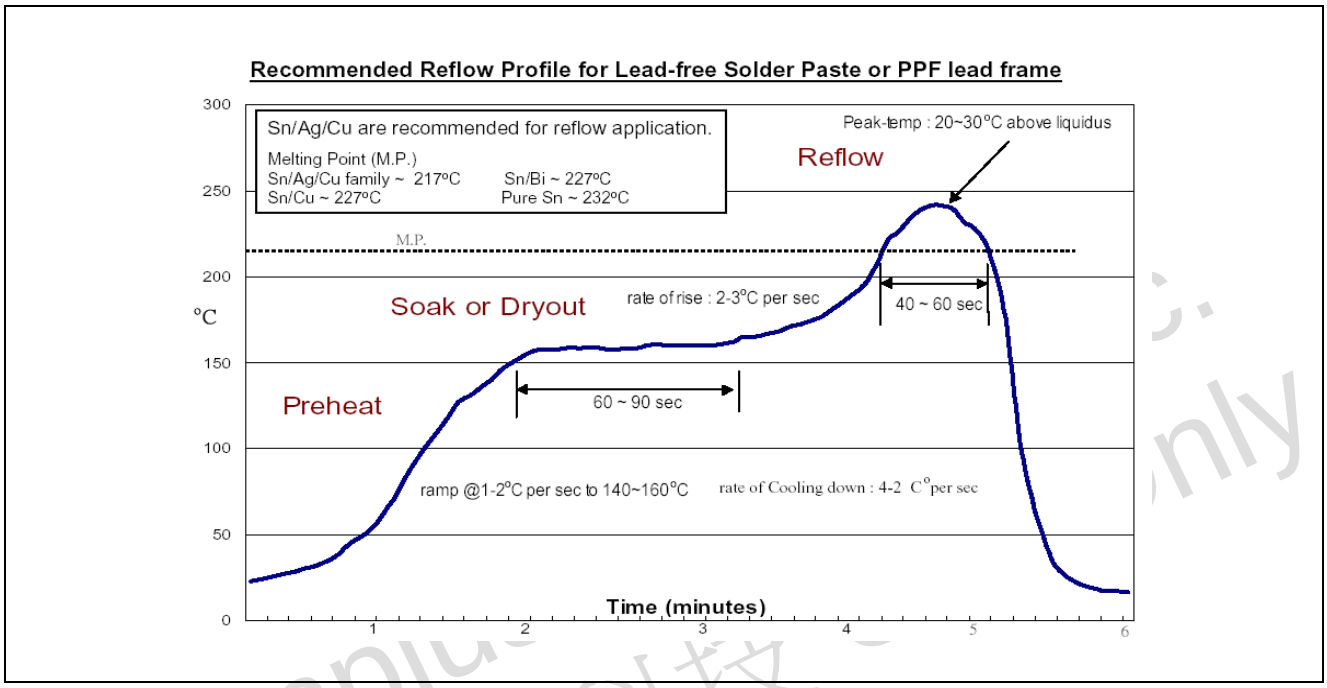
For Green Packages:

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the “CAUTION Note” on dry pack bag.

9.3. Recommended SMT Temperature Profile

This “Recommended” temperature profile is a rough guideline for SMT processing reference. Most of SUNPLUS MMEDIA leadframe-based products choose Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) products with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



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11. REVISION HISTROY

Date	Revision #	Description	Page
Feb. 17, 2009	1.0	Original	