Inter-IC Sound (I^2C) Protocol

Introduction

I^2S (Inter-IC Sound) protocol is an electrical serial bus interface standard used for connecting between digital audio devices [1]. I^2S is a synchronous, serial communication protocol [2] meant to only handle audio data with other signals such as sub-coding and control transferred separately. I^2S uses a 3-line serial bus – Continuous Serial Clock (**SCK**) line, Word Select (**WS**) line, a two time-multiplexed Serial Data (**SD**) line [3].

Serial Data (SD) [3]

Serial Data is transmitted in two's complement with the Most Significant Bit (MSB) first, such that the MSB has a fixed position while the Least Significant Bit (LSB) depends on the word length, as the transmitter and receiver may have different word lengths. Note that neither the transmitter knows how many bits the receiver can handle, nor does receiver know how many bits are being transmitted, leading to possibilities of following situations:

- System word length greater than transmitter word length

The word is truncated where least significant data bits are set to '0' for data transmission.

- Receiving more bits than receiver word length

The received bits after the word length limit will be ignored.

- Receiving less bits than receiver word length

The missing bits will be set to '0' internally on the receiver end until the LSB position.

Bits of serial data transmitted may be synchronised with either trailing (High-to-Low) or leading (Low-to-High) edge of the clock signal (SCK).

It can also be called SDATA, SDIN, SDOUT, DACDAT, ADCDAT [1].

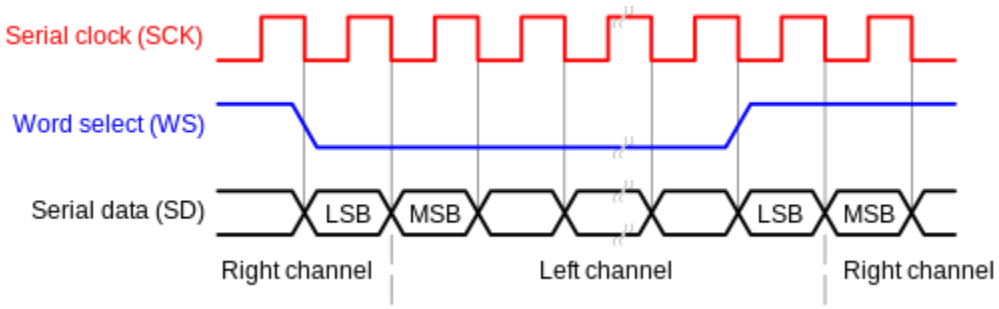
Word Select (WS)

The Word Select line indicates which channel (stereo L/R) the transmitted audio data is for. Word Select may change on either trailing or leading edge of the Serial Clock. Word Select will change 1 clock period before the MSB is transmitted, allowing the target transmitter to derive synchronous timing of the Serial Data for transmission, also to enable the receiver to store the previous word and clear its input for the next word.

- WS = 0 (Low) ; Channel 1 (Left)
- WS = 1 (High) ; Channel 2 (Right)

Serial Clock (SCK) [4]

It is often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.



Timing Diagram of I^2S [1]

Serial Bus Requirements [3]

Both the transmitter(s) and receiver(s) require the same Serial Clock signal for data transmission with the transmitter (in a one-to-one system) or a system controller (for multiple transmitters and receivers system) generating the Serial Clock and Word Select signal. In a complex system with multiple devices (transmitter or receiver), a system controller (external clock) controls the data-flow and the transmitting device acts as the **target** and the generator source is the **controller**.

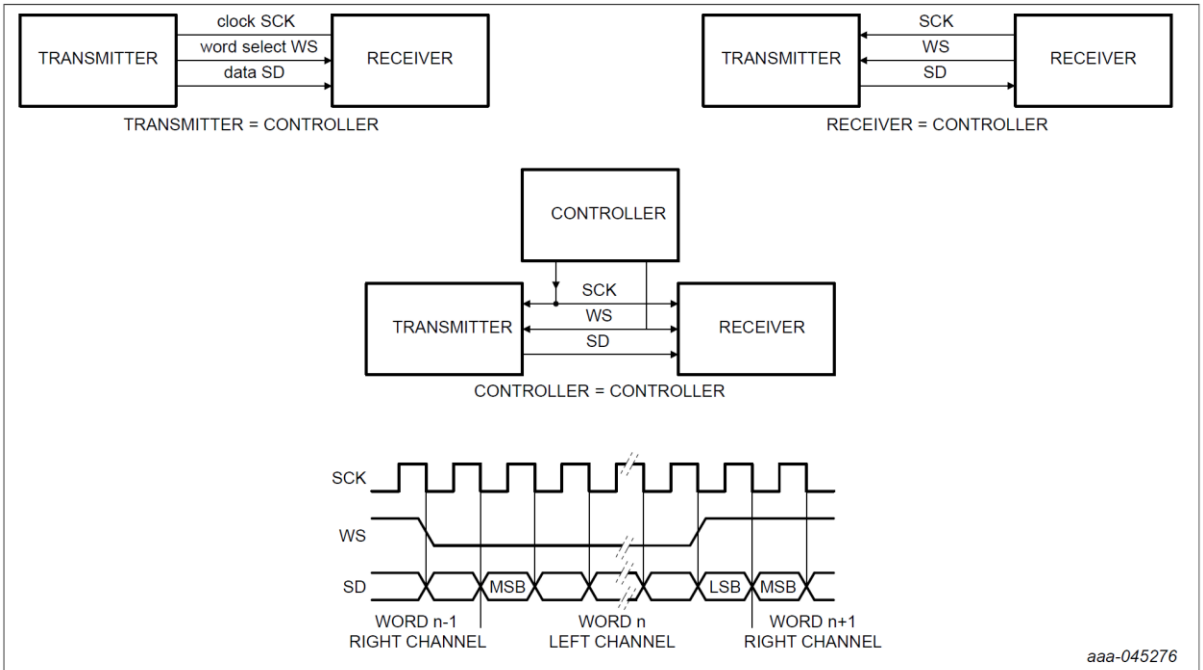


Figure 1. Simple system configurations and basic interface timing

Specifications

Protocol Features [4]

Protocol transmit Pulse-code Modulated (PCM) audio data between devices for application such as digitising audio from a microphone or playing back of .WAV audio files.

- 8 to 32 data bits per sample
- Transmit & Receive FIFO (First In First Out) Interrupt
- Supports DMA (Direct Memory Access)
- 16/32/48/64-bit Word Select period
- Simultaneous bi-directional audio streaming
- 8/16/24-bit sample width
- Various sample rates (eg. 44.1k Hz)
- Data rate up to 96k Hz through 64-bit Word Select period
- Interleaved stereo FIFOs or Independent L/R channel FIFOs
- Independent enable of Transmit or Receive

Timing [3]

Any device can act as the system controller (transmitter/receiver or external controller) by generating the necessary clock signals. A target (transmitter) will derive its internal clock signal from an external clock input.

To account for propagation delay between the controller's clock and the Serial Data and/or Word Select signals, the total delay is a sum of:

- External (controller) clock and Serial Data and/or Word Select signal; and
- Internal clock and the Serial Data and/or Word Select signal.

For inputs of Serial Data and Word Select signals, the delay between external and interna clock is of no consequences as it only lengthens the set-up time. The time margin is to accommodate the difference between the propagation delay of transmitter and set-up time of the receiver.

Voltage Level [3]

- **Output Level**

V_L	< 0.4 V
V_H	> 2.4 V

- **Input Level**

V_{IL}	0.8 V
V_{IH}	2.0 V

I²C on Infineon XMC

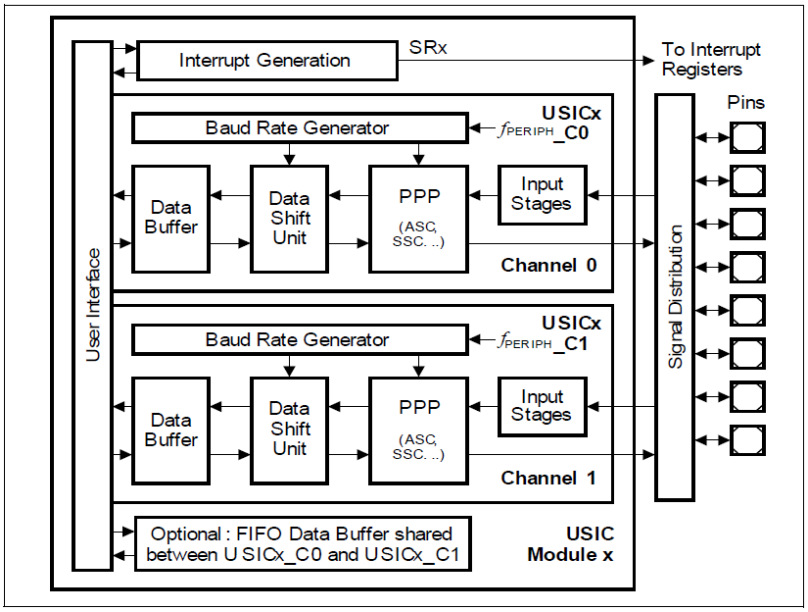
There is no dedicated module for I²C on the XMC Microcontroller instead, it uses the **Universal Serial Interface Channel** (**USIC**) module – a flexible interface module covering several serial communication protocols (UART, LIN, SSC/SPI, I²S, I²C).

Abbreviations [5, p. 922]

CTQ	Time Quanta Counter
DSU	Data Shift Unit
f_{PERIPH}	USIC module clock frequency
f_{PIN}	Input frequency to baud rate generator
MCLK	Master Clock
PPP	Protocol Pre-Processor
RSR	Receive Shift Register
TSR	Transmit Shift Register
WAIN	Word Address (a.k.a WS) Input
SCLKIN	Serial Clock In
SCLK	Serial Clock (a.k.a SCK)

Channel Structure

Each USIC module contains 2 independent communication channels named USICx_CH0 and USICx_CH1 where x is the number o the USIC module. It is user-programmable during run-time which protocol will be handled by a corresponding communication channel and pins.



Input Stages [5, pp. 927-928]

For each protocol, the number of input signals used depends on the selected protocol. Each input signal is handled by an input stage (called DXn, where n=0-5) for signal conditioning, such as input selection, polarity control, or a digital input filter.

Protocol	**Shift Data Input(s)** *[Handled by DX0, DX3, DX4, DX5]*	**Shift Clock Input** *[Handled by DX1]*	**Shift Control Input** *[Handled by DX2]*
I^2S (Master)	DIN0	Optional: External Frequency Input or Delay Compensation	Optional: Transmit data validation or Delay Compensation
I^2S (Slave)	DIN0	SCLKIN	WAIN

Output Stages [5, pp. 929-930]

Protocol	**Shift Data Output(s)** *DOUT[3:0]*	**Shift Clock Output** *SCLKOUT*	**Shift Control Outputs** *SELO[7:0]*	**Master Clock Output** *MCLKOUT*
I²S (Master)	DOUT0	Master Shift Clock	WA (or Word Select)	Optional: Master Time Base
I²S (Slave)	DOUT0	Optional: Independent Clock Output	Not used	Optional: Independent Clock Output

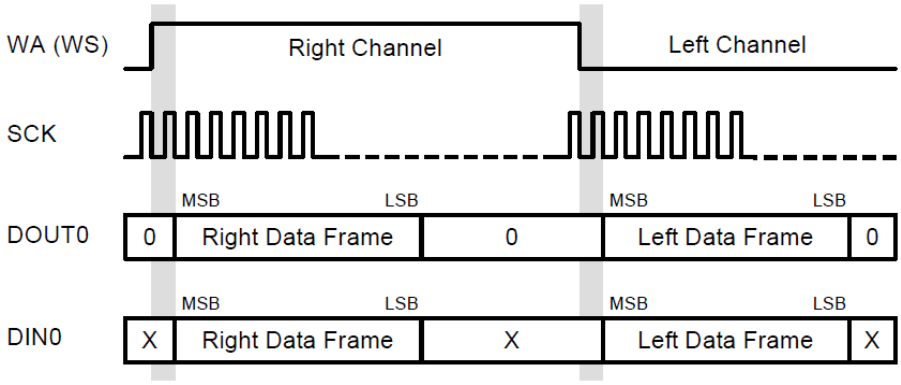
Signal Description

A typical connection between a master and slave is based on the following signals:

- **SCK** generated by the transfer master. It is permanently generated while an I²S connection is established even when no valid data bites are transferred.
- Word Address (**WA**), also known as Word Select (**WS**), generated by transfer master. It indicates the beginning of a new data word and its corresponding L/R channel. The **WA** signal is available on all ***SELOx*** outputs if **WA** generation is enabled (by PCR.WAGEN = 1 for the transfer master) and the signal changes synchronously to the falling edges of the **SCK**.
- If the transmitter is the I²S master device, it generates a master transmit slave receive data signal.
- If the transmitter is the I²S slave device, it generates a master receive slave transmit data signal. Both data changes synchronously to the falling edges of the **SCK**.

Protocol Overview [6, pp. 1057-1058]

The I²S protocol supports transfer of 2 different data frames (a length of data word) via the same data line distinguished by the **WA**/**WS** signal [see I²S Introduction]. The received data words also contains a tag identifying the **WA**/**WS** state when the data has been received.

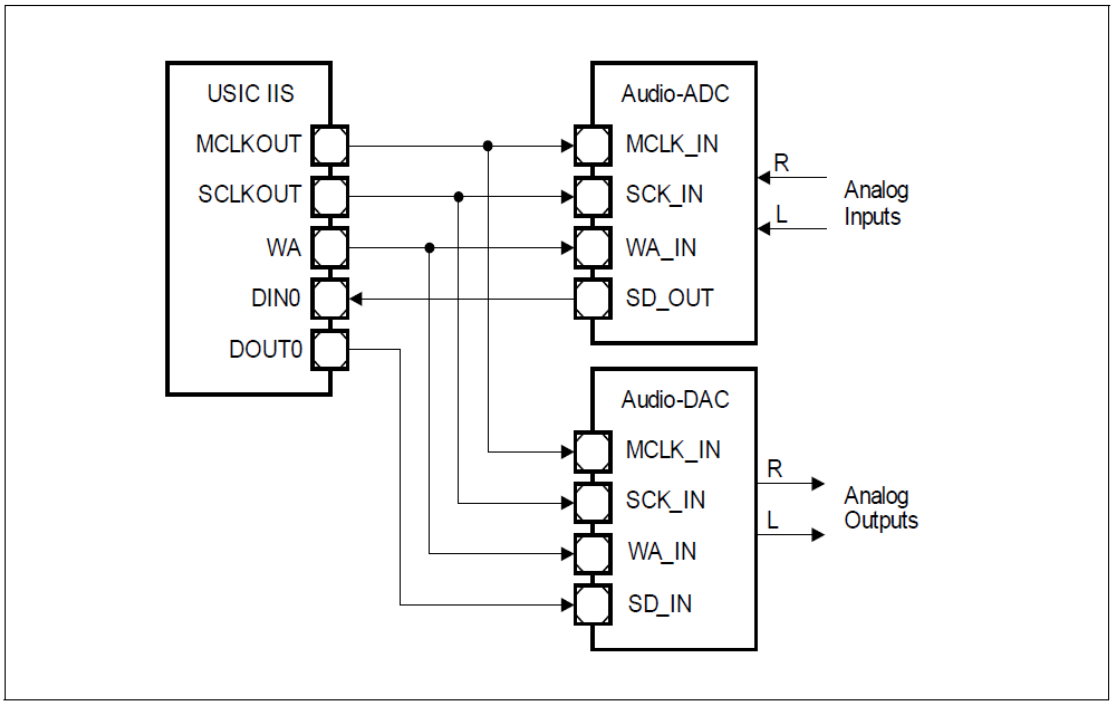


Overview of each signal during transmission

Connecting to External Audio Components [6, p. 1059]

The I²S protocol allows communication with external audio devices such as codecs or other audio data sources / destinations.

In applications especially for audio-ADCs and audio-DACs, a master clock signal is required with a fixed phase relation to the **SCK** signal. The frequency of **MCLKOUT** is a multiple o the shift frequency **SCLKOUT**. This factor defines the oversampling factor of the external device (common value of 256 or 384).



Example of connection to external audio-DAC and audio-ADC

Measurement & Verification of I2S Signal

P3.0 – SCK Signal

P2.5 – SD Signal

References

[1] Wikipedia, “I²S,” [Online]. Available: https://en.wikipedia.org/wiki/I%C2%B2S. [Accessed Mar 2024].

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[3] NXP, “UM11732 I2S bus specification,” 17 Feb 2022. [Online]. Available: https://www.nxp.com/docs/en/user-manual/UM11732.pdf. [Accessed Mar 2024].

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[5] El-Pro-Cus, “I2S Protocol: Working, Differences & Its Applications,” [Online]. Available: https://www.elprocus.com/i2s-protocol/. [Accessed Mar 2024].

[6] Infineon, “XMC4000 Family Reference Manual,” Jul 2016. [Online]. Available: https://www.infineon.com/dgdl/Infineon-xmc4100_xmc4200_rm_v1.6_2016-UM-v01_06-EN.pdf?fileId=db3a30433afc7e3e013b3c44ccd35c20.