

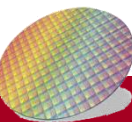


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National Cheng Kung University

HW1 traffic light Frequently asked questions

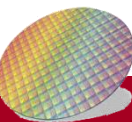
2021, Feb, 26 (Rev 1.0)





FAQ

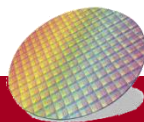
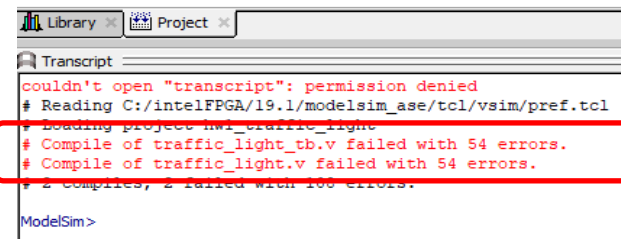
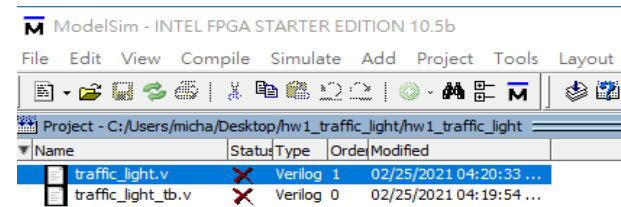
- How to debug Verilog in ModelSim?
- How to show signals in my module?
- “Real answer: $R = x, G = x, Y = x$ ” error





How to debug Verilog in ModelSim?

- Double click on the compilation error shown in the window below.





How to debug Verilog in ModelSim?

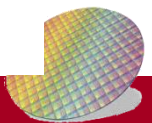
- A window will pop up and point out the error in your code.

The screenshot shows the ModelSim interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Transcript, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations and simulation. The project window shows a project named 'C:/Users/micha/Desktop/hw1_traffic_light/hw1_traffic_light' with two files: 'traffic_light.v' and 'traffic_light_tb.v', both marked with red 'X' icons indicating errors. The 'Unsuccessful Compile' window is open, displaying the following error messages:

```
log -work work -stats=none C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v
Model Technology ModelSim - Intel FPGA Edition vlog 10.5b Compiler 2016.10 Oct 5 2016
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(1): Cannot open 'include file "def.v".
-- Compiling module traffic_light
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(12): (vlog-2163) Macro `STATE_W is undefined.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(13): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(18): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(19): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(20): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(39): (vlog-2163) Macro `S_INIT is undefined.
** Error: (vlog-13069) C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(39): near "]": syntax error, un
expected ']''.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(50): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(53): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(55): (vlog-2163) Macro `COUNTER_W is undefin
ed.
** Error: C:/Users/micha/Desktop/hw1_traffic_light/traffic_light_tb.v(64): (vlog-2163) Macro `STATE_W is undefined
.
.
```

The Transcript window at the bottom shows the following output:

```
couldn't open "transcript": permission denied
# Reading C:/intelFPGA/19.1/modelsim_ase/tcl/vsim/pref.tcl
# Loading project hw1_traffic_light
# Compile of traffic_light_tb.v failed with 54 errors.
# Compile of traffic_light.v failed with 54 errors.
# 2 compiles, 2 failed with 108 errors.
ModelSim>
```





How to debug Verilog in ModelSim?

- You should make sure there aren't any error after compilation.

```
ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout

Project - C:/Users/micha/Desktop/hw1_traffic_light/hw1_traffic_light

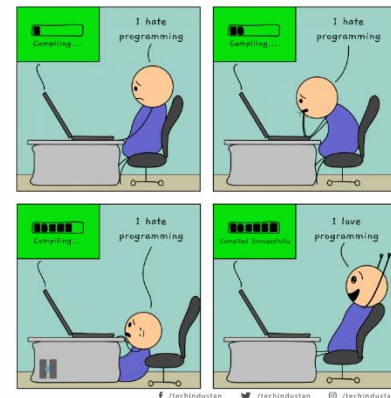
Name      Status Type  Order Modified
-----
traffic_light.v  ✓ Verilog 1  02/25/2021 04:20:33 ...
def.v          ✓ Verilog 2  02/25/2021 04:20:52 ...

Library Project

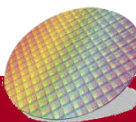
Transcript

couldn't open "transcript": permission denied
# Reading C:/intelFPGA/19.1/modelsim_ase/tcl/vsim/pref.tcl
# Loading project hw1_traffic_light
# Compile of traffic_light_tb.v failed with 54 errors.
# Compile of traffic_light.v failed with 54 errors.
# 2 compiles, 2 failed with 108 errors.
# Compile of traffic_light_tb.v was successful.
# Compile of traffic_light.v was successful.
# Compile of def.v was successful.
# 3 compiles, 0 failed with no errors.

ModelSim>
```



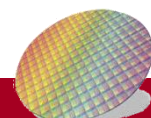
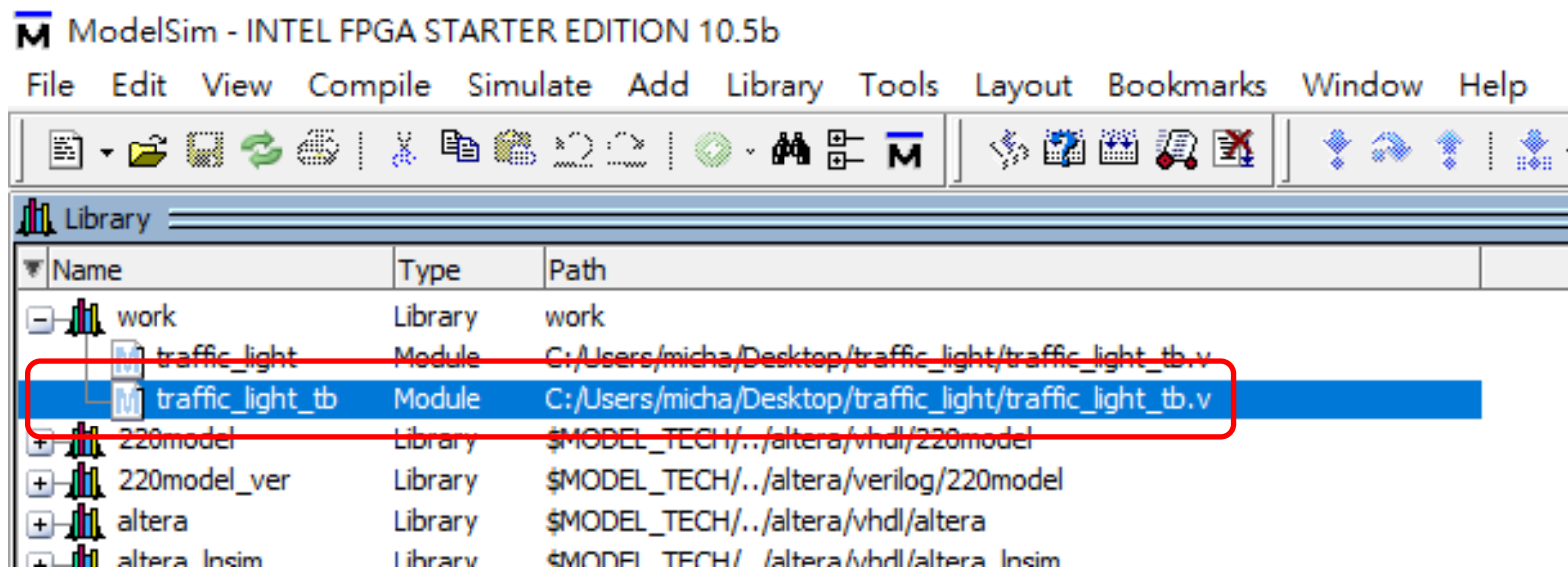
- ** Students should have 2 Verilog files (traffic_light.v and traffic_light_tb.v) only. The def.v file shown in the screenshot above is not required.





How to show signals in my module?

- Double click on work/traffic_light_tb





How to show signals in my module?

- Click on the **ul** instance.
 - This is the instance name of traffic_light module specified in traffic_light_tb.v
- Select the signal you want to debug in the “Object window”

ModelSim - INTEL FPGA STARTER EDITION 10.5b

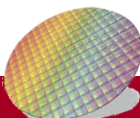
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help

sim - Default

Instance	Design unit	Design unit type	Top Category	Visibility	Total coverage
traffic_light_tb	traffic_light...	Module	DU Instance	+acc=...	
ul	traffic_light	Module	DU Instance	+acc=...	
#ALWAYS#36	traffic_light...	Process	-	+acc=...	
#INITIAL#48	traffic_light...	Process	-	+acc=...	
#INITIAL#57	traffic_light...	Process	-	+acc=...	
#INITIAL#63	traffic_light...	Process	-	+acc=...	
#INITIAL#76	traffic_light...	Process	-	+acc=...	
#ALWAYS#85	traffic_light...	Process	-	+acc=...	
#ASSIGN#90	traffic_light...	Process	-	+acc=...	
#ALWAYS#92	traffic_light...	Process	-	+acc=...	
#ALWAYS#101	traffic_light...	Process	-	+acc=...	
#ALWAYS#115	traffic_light...	Process	-	+acc=...	
#vsm_capacity#		Capacity	Statistics	+acc=...	

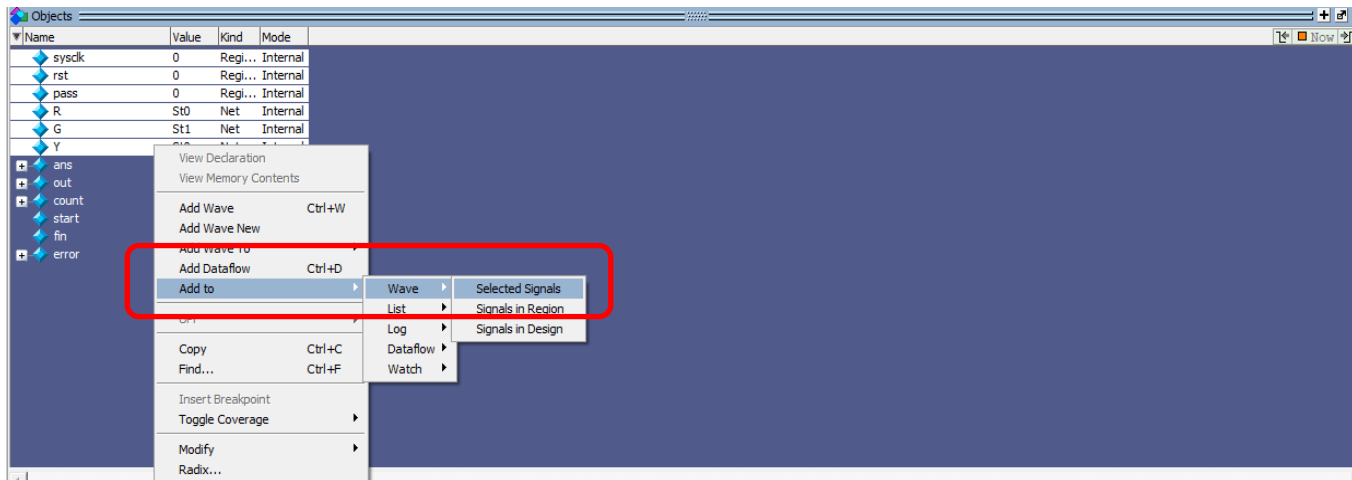
Objects

Name	Value	Kind	Mode
clk	StX	Net	In
rst	StX	Net	In
pass	StX	Net	In
R	x	Regi...	Out
G	x	Regi...	Out
Y	x	Regi...	Out
curr_state	xxxxx	Pack...	Internal
next_state	xxxxx	Pack...	Internal
cyc	xxxx...	Pack...	Internal
pass_rst	x	Regi...	Internal
pass_reg	x	Regi...	Internal
x128_4	xxxx...	Net	Internal
x128_3	xxxx...	Net	Internal
base	xxxx...	Net	Internal
init_done	StX	Net	Internal
idle_done	StX	Net	Internal
turn_yellow	StX	Net	Internal
turn_idle	StX	Net	Internal
turn_red	StX	Net	Internal

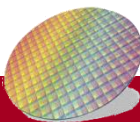
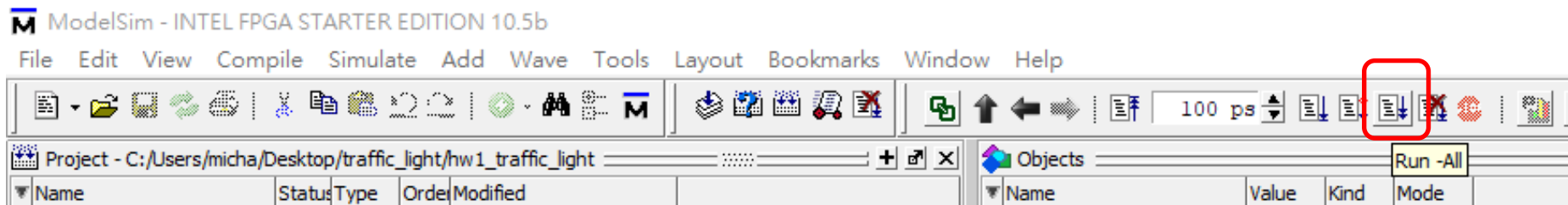


How to show signals in my module?

- Right click “Add to/Wave/Selected Signals”



- Click on the “Run all” button



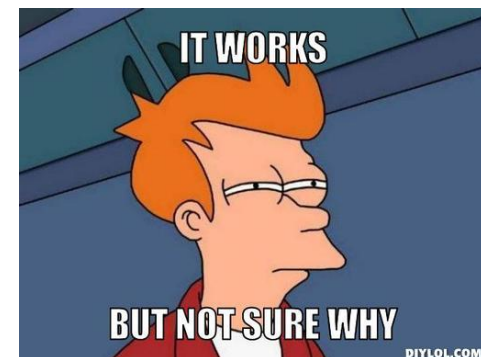


How to show signals in my module?

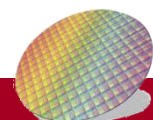
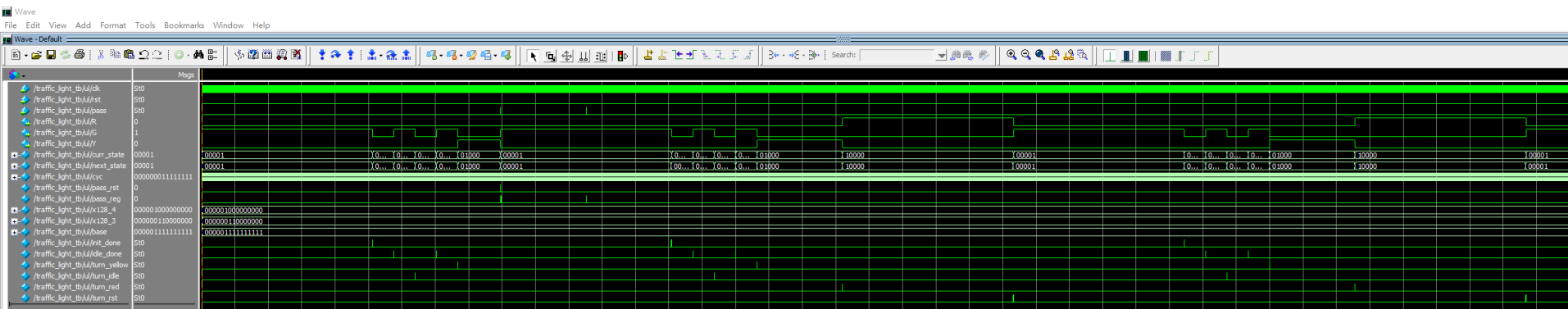
- You should see a figure if your design is correct.

```
VSIM 3> run -all

#
#
# *****
# **                               **      /|_ /|
# ** Congratulations !!          **      / 0,0 |
# **                               **      /_____|
# ** Simulation PASS!!          **      / ^ ^ ^ \ |
# **                               **      | ^ ^ ^ |w|
# **                               **      \m__m_|
# *****
#
#
# ** Note: $finish      : C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v(82)
# ** Time: 81921 ns      Iteration: 0      Instance: /traffic_light_tb
```



- Waveform of selected signals should pop up.





“Real answer: R = x ,G = x ,Y = x” error

- In the testbench file “traffic_light_tb.v”, the R,G,Y output from your module will be compared with the correct answer written in the “ans.txt” file.
- The correct answer “**ans.txt**” **MUST** be added into your project for testbench program to read it.
- In case you forgot to do so. Your output will be compared with “R = x, G = x, Y = x” and fail.

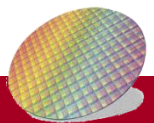
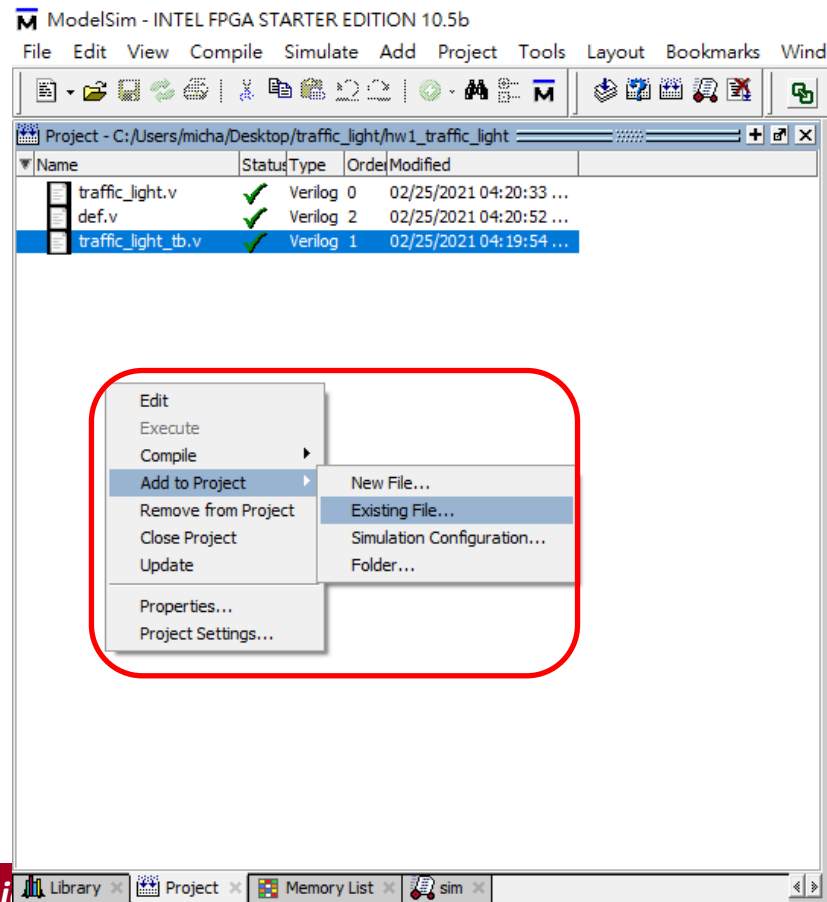
• (ノД') (╯─╯)

```
Transcript
# Error at 8187th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8188th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8189th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8190th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
#
#
# =====
# (/`n`)/ ~# There was 8191 errors in your code !!
# ----- The simulation has finished with some error, Please check it !!! -----
#
#
# ** Note: $finish      : C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v(82)
#      Time: 81921 ns  Iteration: 0  Instance: /traffic_light_tb
# 1
# Break in Module traffic_light_tb at C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v line 82
```



“Real answer: $R = x$, $G = x$, $Y = x$ ” error

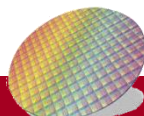
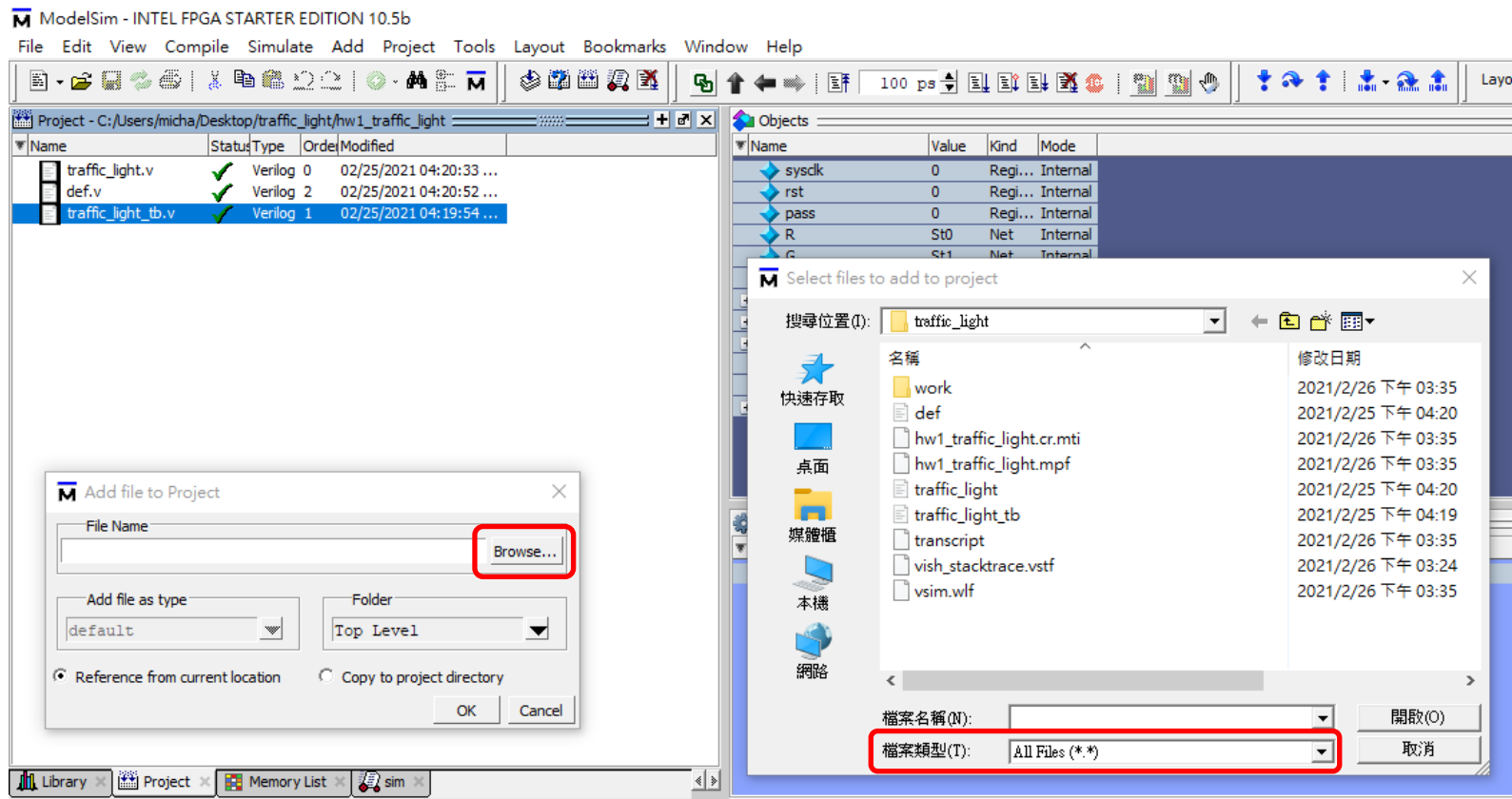
- How to add “ans.txt” to my project ?
- Right click on “Project” tab
- Click on “Add to project/Existing File”





“Real answer: $R = x, G = x, Y = x$ ” error

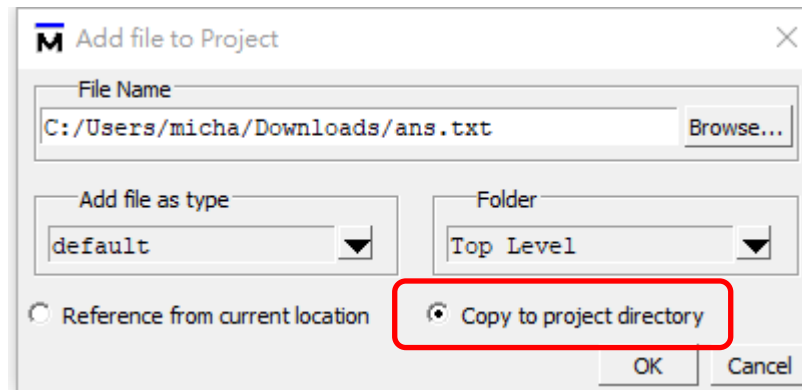
- Click “Browse” to select file
- Make sure the “File type” is set to “All Files (*.*)” and then click on “ans.txt”





“Real answer: $R = x$, $G = x$, $Y = x$ ” error

- Add file as type “Text”
- Choose “Copy to project directory” !!!
 - In case you choose “Reference from current location”. The testbench won’t be able to read “ans.txt” as input.



- You don’t have to recompile your design. Just run it again and you should be able to see the correct signals.

