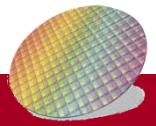
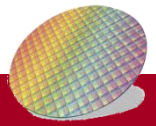
HW1 traffic light
Frequently asked questions

2021, Feb, 26 (Rev 1.0)



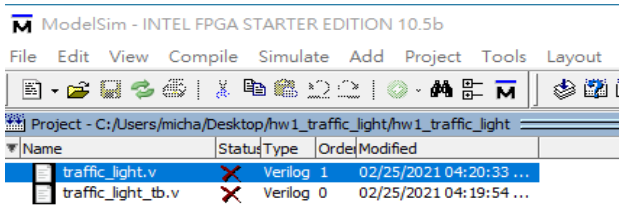
FAQ

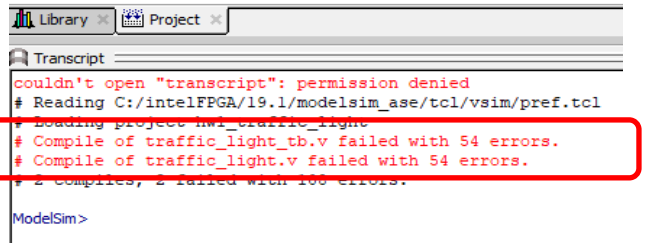
- How to debug Verilog in ModelSim?
- How to show signals in my module?
- “Real answer: R = x ,G = x ,Y = x” error



How to debug Verilog in ModelSim?

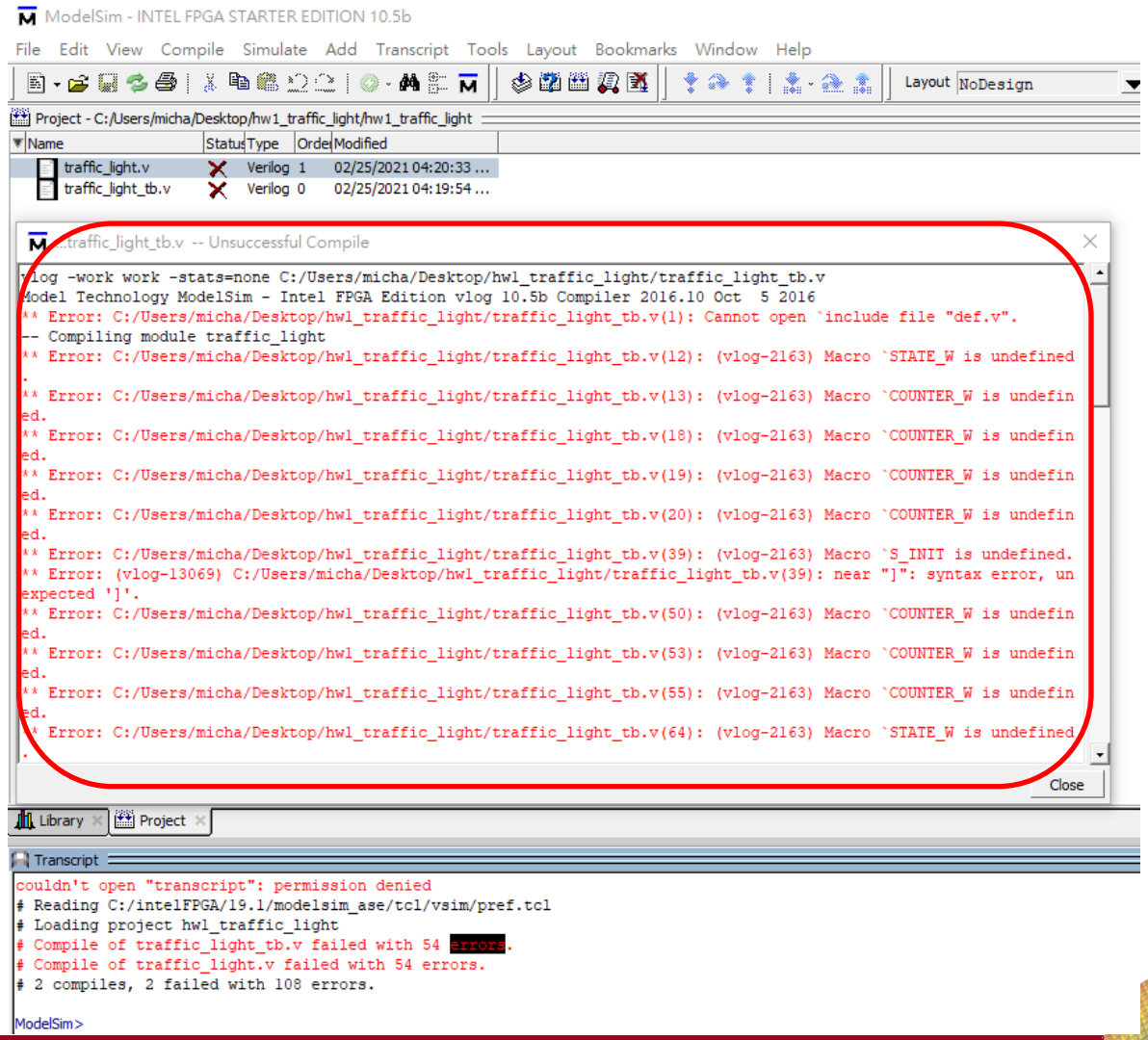
- Double click on the compilation error shown in the window below.





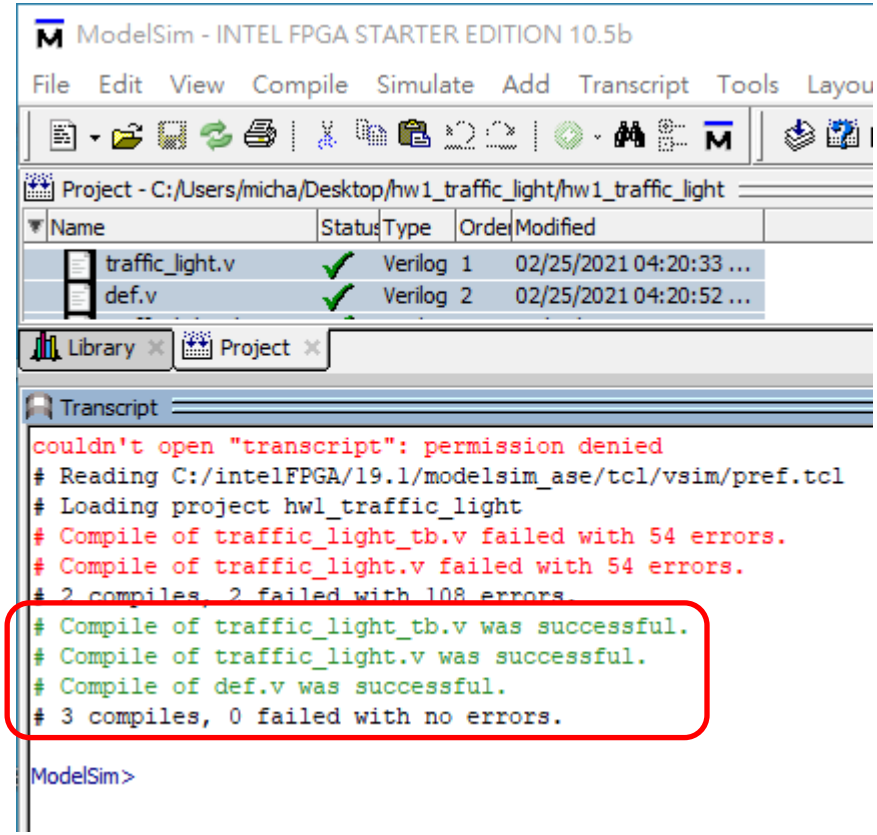
How to debug Verilog in ModelSim?

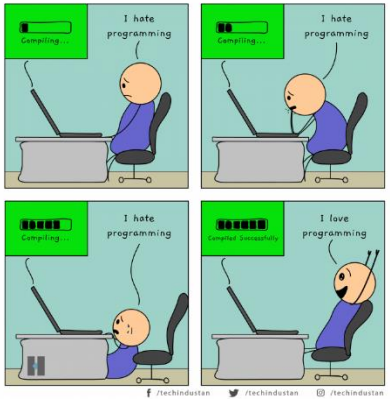
- A window will pop up and point out the error in your code.



How to debug Verilog in ModelSim?

- You should make sure there aren't any error after compilation.

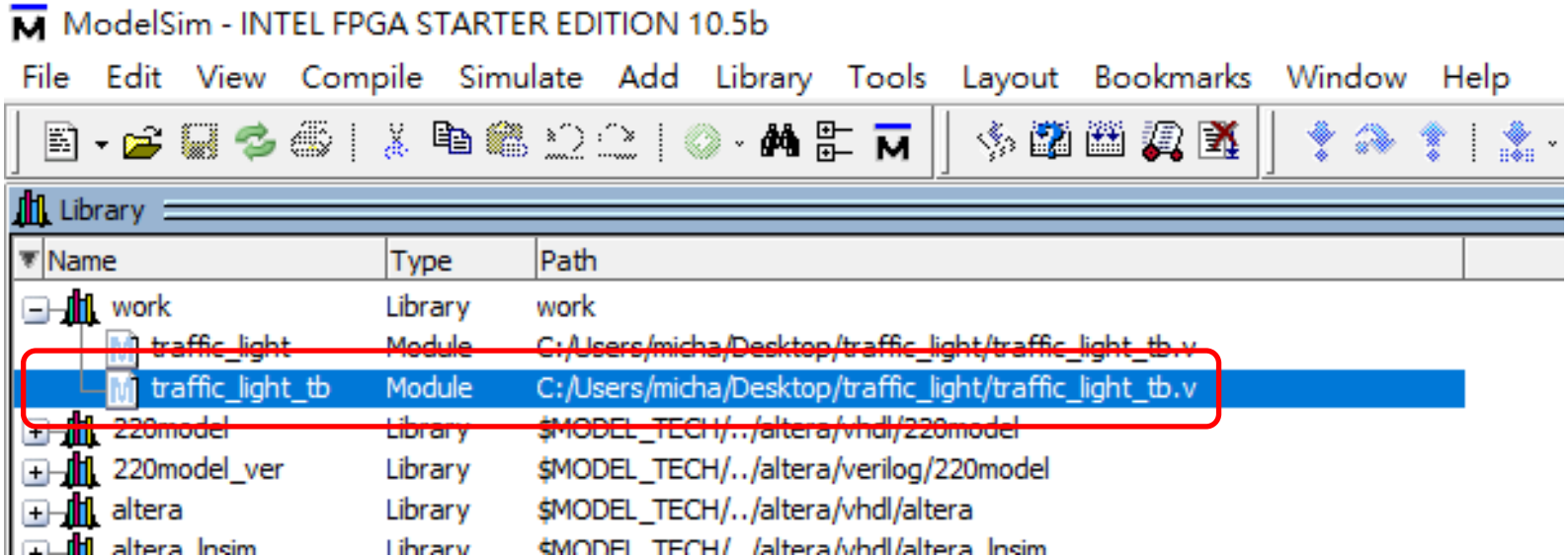




- ** Students should have 2 Verilog files (traffic_light.v and traffic_light_tb.v) only. The def.v file shown in the screenshot above is not required.

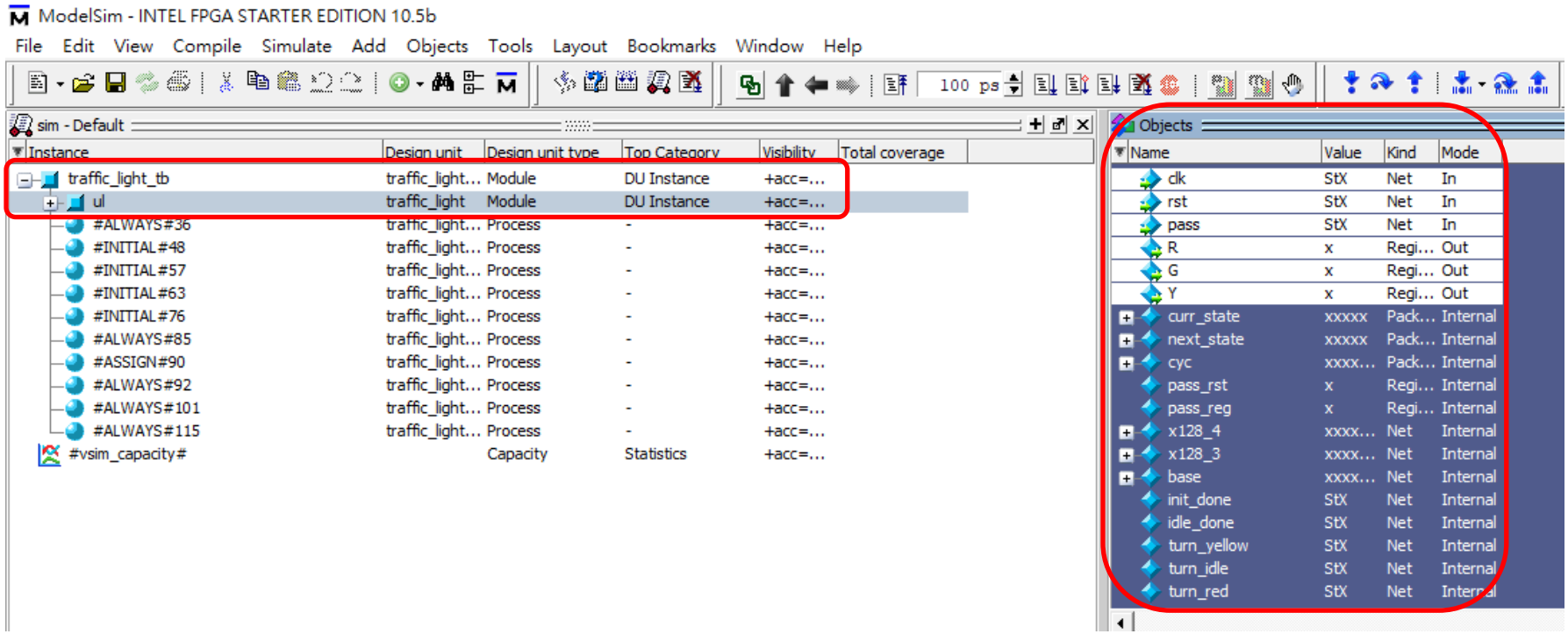
How to show signals in my module?

- Double click on work/traffic_light_tb



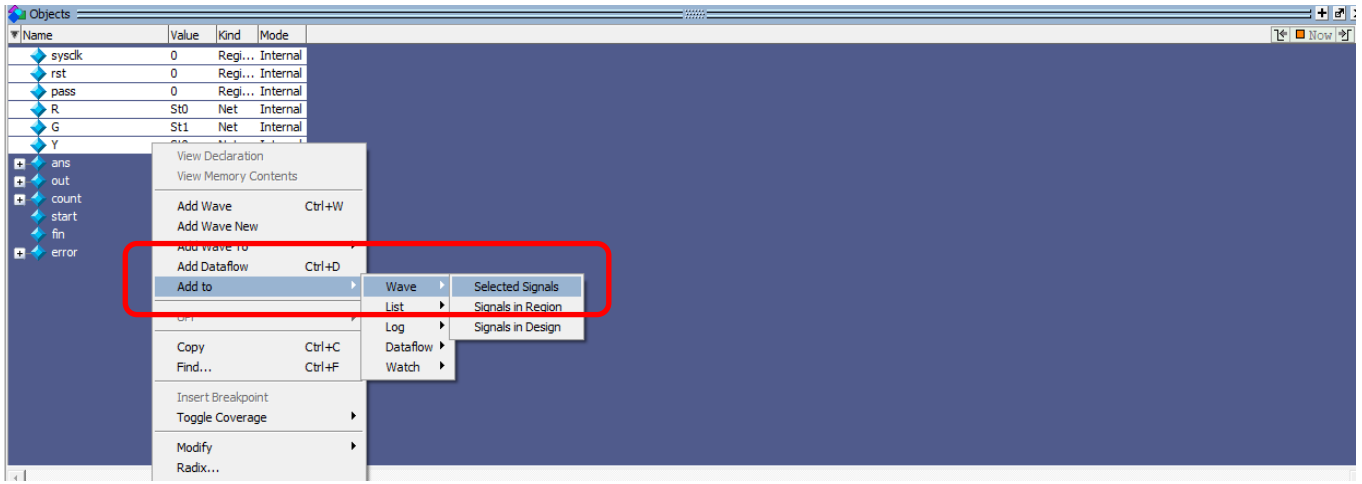
How to show signals in my module?

- Click on the ul instance.
  - This is the instance name of traffic_light module specified in traffic_light_tb.v
- Select the signal you want to debug in the “Object window”

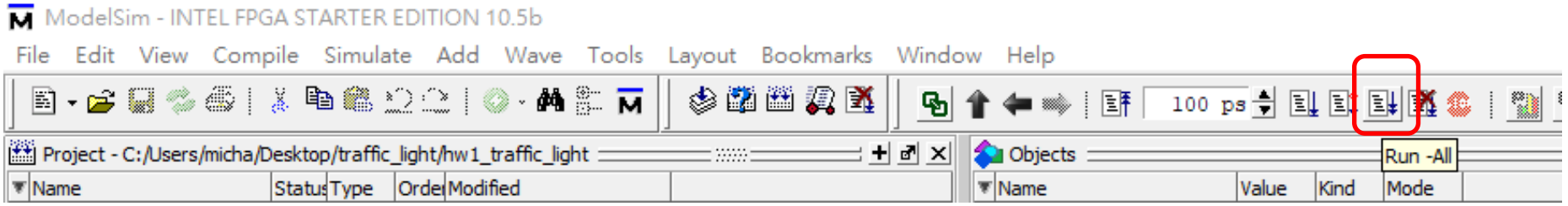


How to show signals in my module?

- Right click “Add to/Wave/Selected Signals”



- Click on the “Run all” button

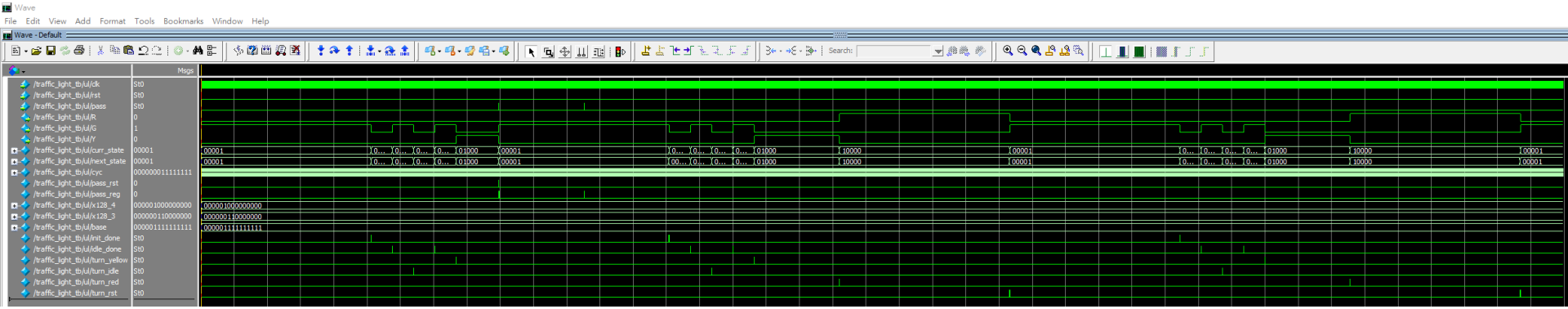


How to show signals in my module?

- You should see a figure if your design is correct.

```
VSIM 3> run -all
#
#
#          ******************************
#          **                            **        /|__/|
#          **  Congratulations !!        **       / O,O  |
#          **                            **     /_____   |
#          **  Simulation PASS!!         **    /^ ^ ^ \  |
#          **                            **   |^ ^ ^ ^ |w|
#          ****************  ************    \m___m__|_|
#
#
# ** Note: $finish    : C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v(82)
#    Time: 81921 ns  Iteration: 0  Instance: /traffic_light_tb
```

- Waveform of selected signals should pop up.



“Real answer: R = x ,G = x ,Y = x” error

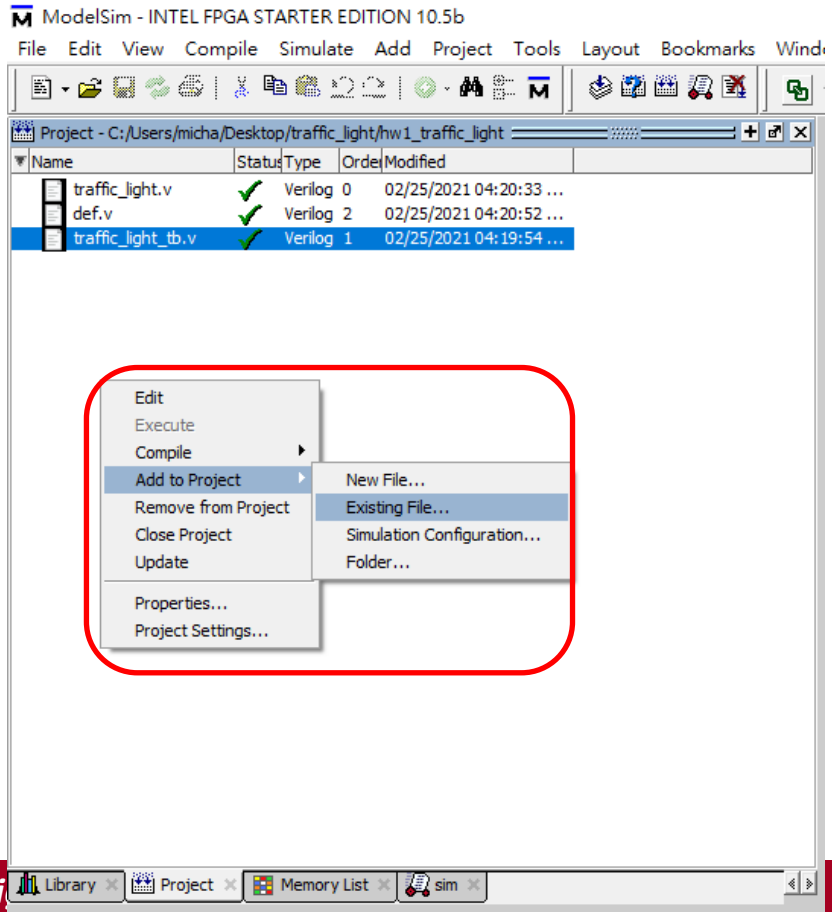
- In the testbench file “traffic_light_tb.v”, the R,G,Y output from your module will the compared with the correct answer written in the “ans.txt” file.
- The correct answer “ans.txt” **MUST** be added into your project for testbench program to read it.
- In case you forgot to do so. Your output will be compared with “R = x, G = x, Y = x” and fail.
- (ノ ゜Д゜)ノ ┻━┻

Transcript

```
# Error at 8187th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8188th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8189th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
# Error at 8190th cycle:
# Real answer: R = x ,G = x ,Y = x
# Your answer: R = 0 ,G = 1 ,Y = 0
#
#
# ================================================================================
# -------------- (/`n`)/ ~#  There was 8191 errors in your code !! ---------------------
# --------- The simulation has finished with some error, Please check it !!! ---------
# ================================================================================
#
#
# ** Note: $finish    : C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v(82)
#    Time: 81921 ns  Iteration: 0  Instance: /traffic_light_tb
# 1
# Break in Module traffic_light_tb at C:/Users/micha/Desktop/traffic_light/traffic_light_tb.v line 82
```

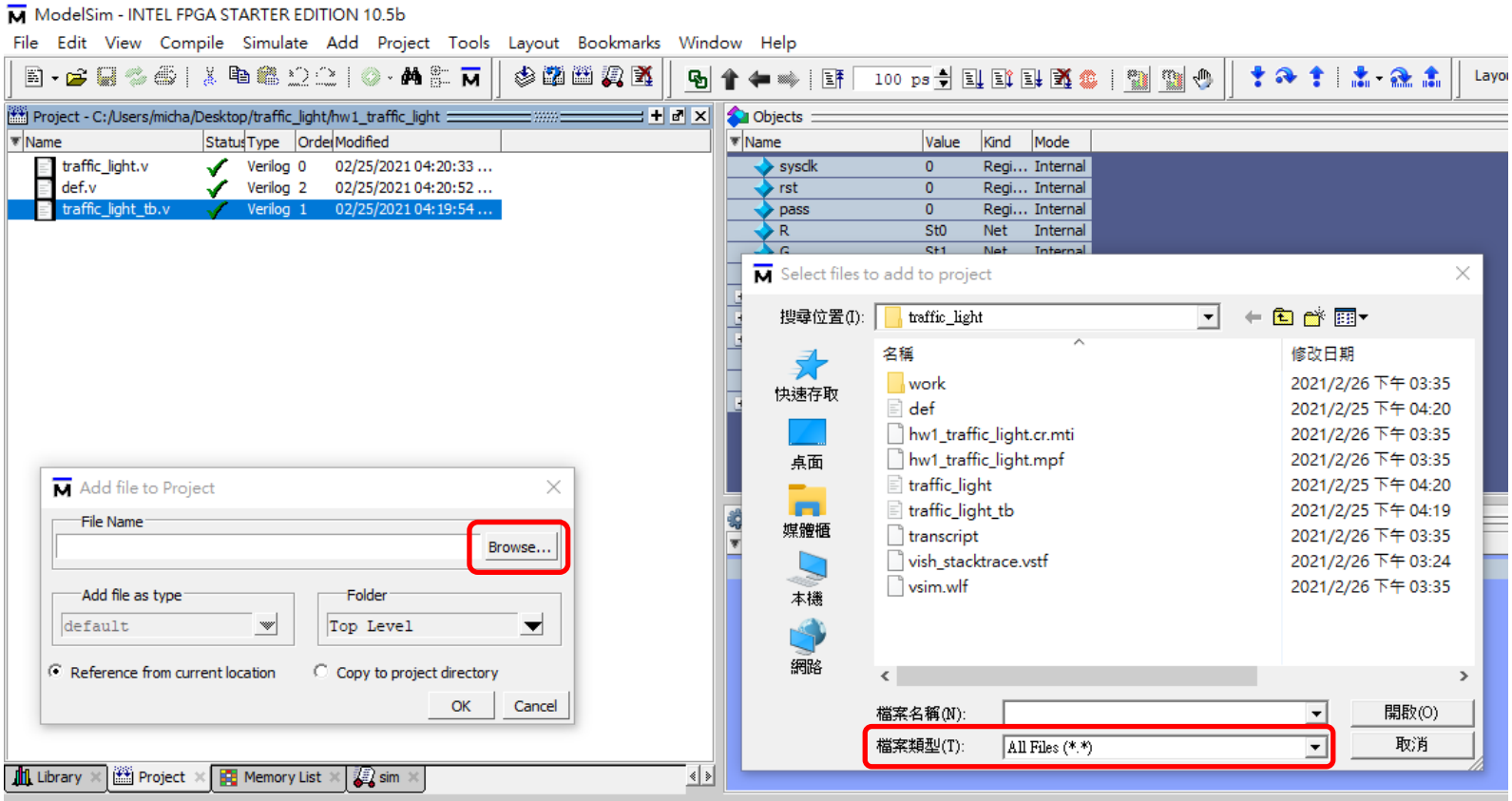
“Real answer: R = x ,G = x ,Y = x” error

- How to add “ans.txt” to my project ?
- Right click on “Project” tab
- Click on “Add to project/Existing File”



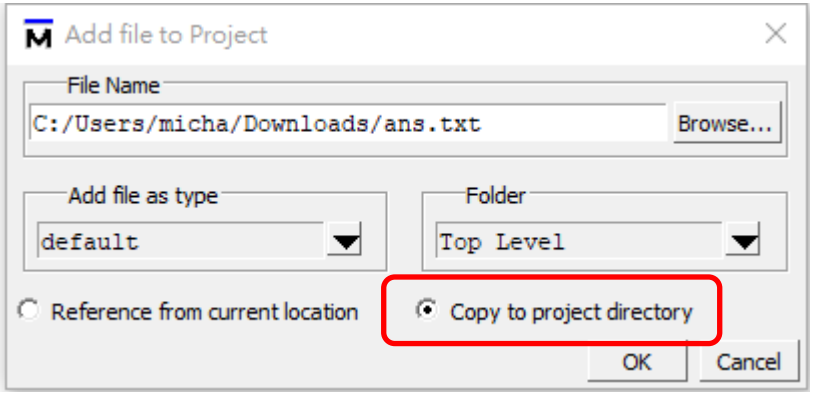
“Real answer: R = x ,G = x ,Y = x” error

- Click “Browse” to select file
- Make sure the “File type” is set to “All Files (*.*)” and then click on “ans.txt”



“Real answer: R = x ,G = x ,Y = x” error

- Add file as type “Text”
- Choose “Copy to project directory” !!!
  - In case you choose “Reference from current location”. The testbench won’t be able to read “ans.txt” as input.



- You don’t have to recompile your design. Just run it again and you should be able to see the correct signals.