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Resume Summary

Current Position : Sr Eng Process Integration in Global Foundries (Nov 2011 - Present)

Current Specialization : Engineering - Electronics/Communication

Highest Education : MSc Physics (Wafer Fabrication)

Years of Experiences : 10

Languages: English, Malay, and Japanese (spoken, written and reading)

Personal Particulars & Preferences

Date of Birth : 10 May 1977

Nationality : Malaysia

Gender : Female

Availability : After 31 Dec 2012

Employment History

Nov 2011 - Present

Global Foundries (SINGAPORE)

Position Title (Level) : Sr Eng Process Integration (Senior Executive)

Industry : Wafer Fabrication

Work Description :

- Develop custom or derivative processes to meet customer needs
- Run DOE to optimize process margins and determine process & ET specifications
- Monitor OOC, maintain good CPK for ET and monitor inline SPC parameters
- Identify and resolve process integration issues & ET related problems
- Identify yield opportunities and set preliminary yield targets
- Run prototype lots on new or derivative processes

- Liaise with Customer Engineers/Field Engineers to resolve customers' technical & yield concerns
- Develop FMEA for Custom & Derivative processes
- Document relevant information of new / derivative processes.
- Support and Implement Process change requests

Oct 2002-Nov 2011

Silterra (MALAYSIA)

Position Title (Level) : Sr Eng II Technology Development (Senior Executive)

Industry : Wafer Fabrication

Work Description:

- Develop & Qualify new & derivative processes
- Integrate of all modules processes and the respective derivatives
- Monitor inline lot movement to ensure that there is no process issues with lot
- Resolve all process integration issues by ensuring all window checks are done on critical process steps and planarization
- Write Engineering lot report for every new device & experiment
- To prepare proper transfer documents for Integration Run DOE to optimize process integration and to determine the process spec
- Develop & qualify custom or derivative processes to customer

High Voltage projects:

- 0.13-micron dual STI development
- 0.13-micron dual gate etch back center thick issue related chemical change
- 0.13-micron OTP retention with high block deposition
- 0.13-micron silicon pitting due to block etch
- Many more…

Software:

- Statistics & Analytical: Minitab, JMP, Data Power, Space, Wafer Sleuth
- Documentation: Frame Maker, Visio
- Production: Factory Works
- Microsoft Office (Word, Excel. Power Point)
- Process: K2_viewer

Oct 2002-August2006

Silterra (CALIFORNIA, USA & MALAYSIA)

Position Title (Level) : Marketing Engineer

Industry : Wafer Fabrication

Work Description:

- Exposure (short attachment) to all modules: Photolithography, Etch, Thin Film, Diffusion, Implant, Reticle (Mask), Failure Analysis and Yield.
- Market communication: marketing collaterals, web content, PR interface, trade show
- Design service: Evaluate capabilities of design service partner, EDA req. analysis.
- Market study/research-IP (Intellectual Property)

Awards:

1) Product Excellence Award 2009 by MOSTI (Display Driver Integrated Chips (DDIC): Using 0.18µm, 0.16µm and 0.13µm CMOS High Voltage technology)

2) 2009 Asia Pacific Frost & Sullivan SEA Industrial Technologies Awards

3) Silterra Long Service Award

4) Six sigma green belt

Other Activities:

Silterra Toastmaster International Club: IMP Secretary, ACB, and AL

Educational Background

Highest Education

Level: Masters of Science

Field of Study: Physics Science

Major: Semiconductor Fabrication, Dual STI Development

Institute / University: University of Science, Malaysia

Located In: Malaysia

Graduation Date: Ongoing (2008~)

Second Highest Education

Level : Professional Course

Grade : Grade A/1st Class

Field of Study : Engineering (Electrical/Electronic)

Major : Semiconductor Fabrication

Institute / University: University of California Berkeley

Located In : United States

Graduation Date: Jul 2004

Third Highest Education

Level : Bachelor's Degree

Grade : Grade A/1st Class

Field of Study : Engineering (Electrical/Electronic)

Major : Information System

Institute / University: Nagaoka University of Technology, Japan

Located In : Japan

Graduation Date: Mar 2002