Parity & Parity Generator

The **parity generating technique** is one of the most widely used **error detection techniques** for the data transmission. There are different methods for detecting the errors while the data is transmitted from source to receiver; one of them is parity generating technique. In digital systems, when binary data is transmitted and processed, the data may be subjected to **noise** and the bits can be altered. Hence **parity bit** is added to the word containing data in order to make the number of 1's either even or odd. The message containing the data bits along with the parity bit is transmitted from the source to the receiver. At the receiving end, the number of 1's in the message is counted and if it doesn't match with the transmitted one, then it means there is an error in the data.

A **parity generator** is a combinational logic circuit that generates the parity bit in the transmitter. A circuit that checks the parity in the receiver end is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

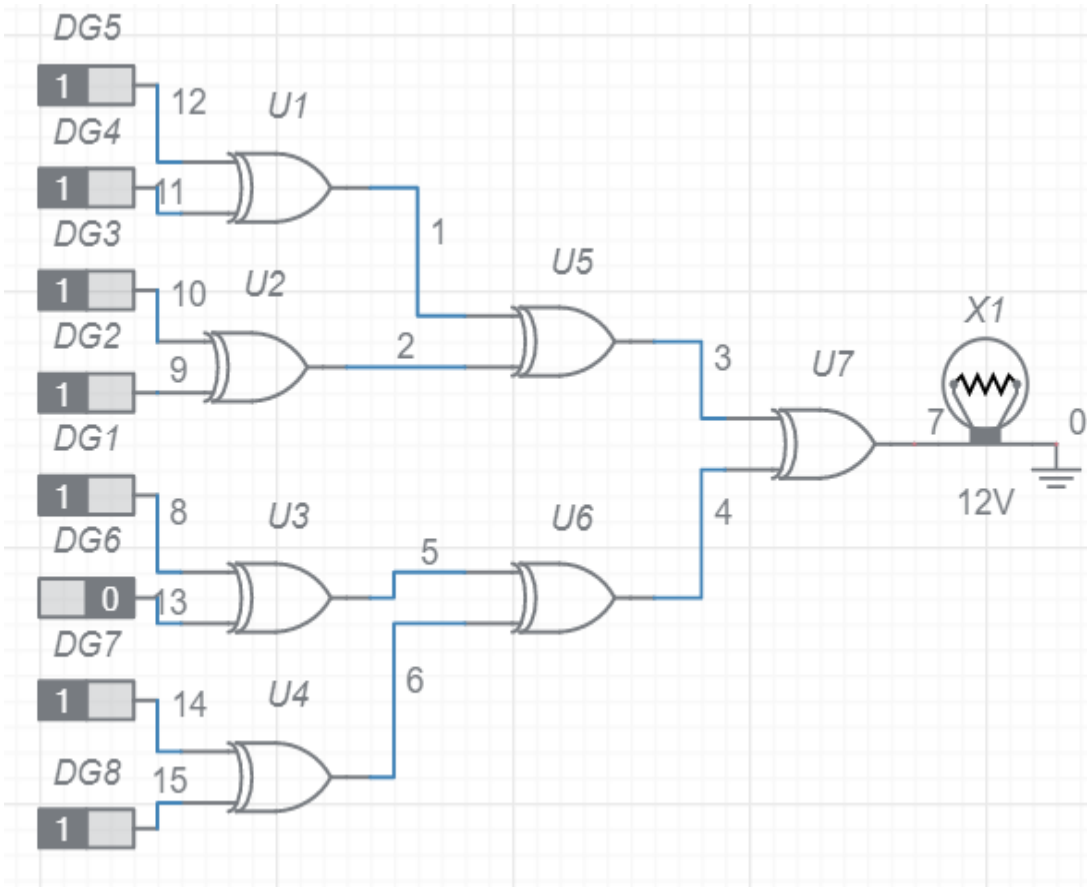
Types:

There are two types based on the number of 1s. They are:

1) Even parity

In even parity, the added parity bit will make the total number of 1s an even.

Such error detecting and correction circuits can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of 1's inputs).



In this image an 8-bit even parity generator circuit is shown it is designed using basic 2-input Ex-or logic gates only. We can use IC's also or some other logic gates but I feel it is simple and efficient.

2) Odd parity

In odd parity the added parity bit will make the total number of 1s odd amount.

Such error detecting and correction circuits can be implemented by using Ex-NOR gates (since Ex-NOR gate produce zero output when there are odd number of 1's inputs).

Parity Generator:

A combinational circuit that accepts an (n-1) bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit.

In even parity bit scheme, the parity bit is 0 if there are even numbers of 1s in the data stream and the parity bit is 1 if there are odd numbers of 1s in the data stream.

In odd parity bit scheme, the parity bit is 1 if there are even numbers of 1s in the data stream and the parity bit is 0 if there are odd numbers of 1s in the data stream.

Parity Checker:

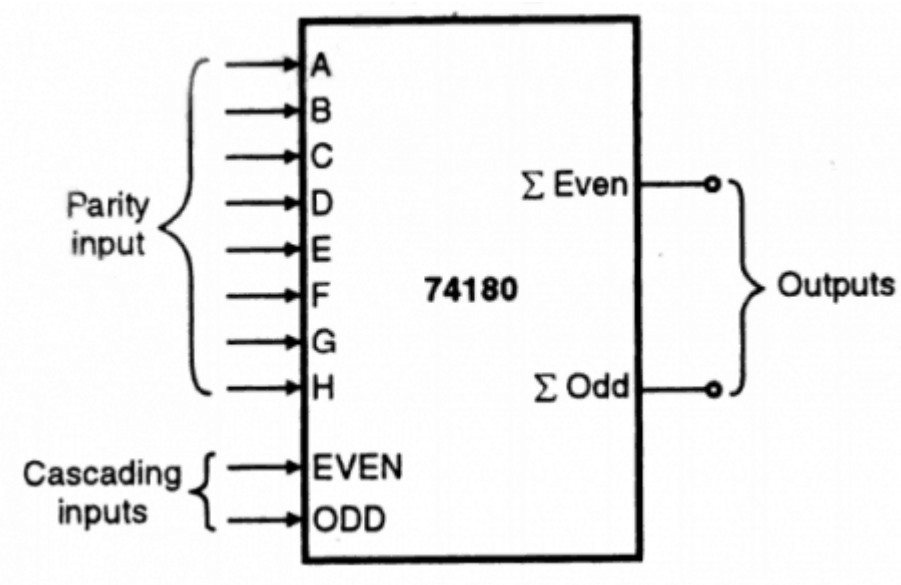
A combinational logic circuit that checks for possible errors in transmission is known as Parity Checker. This circuit is of two types; an even parity checker and an odd parity checker depending on the parity generator at the transmission end.

When this circuit is used as even parity checker, the number of input bits must always be even. If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check). The PEC is 1 if the number of 1's in the transmitted data along with the parity bit is odd.

When this circuit is used as odd parity checker, the number of input bits must always be odd. If any error occurs, the received message consists of even number of 1s. The output of the parity checker is denoted by PEC (parity error check). The PEC is 1 if the number of 1's in the transmitted data along with the parity bit is even.

Parity Generator/Checker ICs:

There are different types of parity generator /checker ICs are available with different input configurations such as 5-bit, 4-bit, 9-bit, 12-bit, etc. A most commonly used and standard type of parity generator/checker IC is 74180. It is a 9-bit parity generator or checker (8 bit data and 1 parity bit) used to detect errors in high speed data transmission or data retrieval systems. The figure below shows the pin diagram of 74180 IC.



The IC contains of 14 pins in which 8 parity inputs pins labelled as A, B, C, D, E, F, G and H from pin 8 to 13 and pin 1 and two cascading inputs labelled as even and odd at the pin 3 and 4. Pin 7 is ground and Pin 14 is Vcc. Pins 5 and 6 are output pins.

Note:

A parity bit can also be changed or affected due to interference. There is a different case for this in Error detection and correction scheme.

References:

https://www.electronicshub.org/parity-generator-and-parity-check/

A report by **Jyotsana Sampatharao**