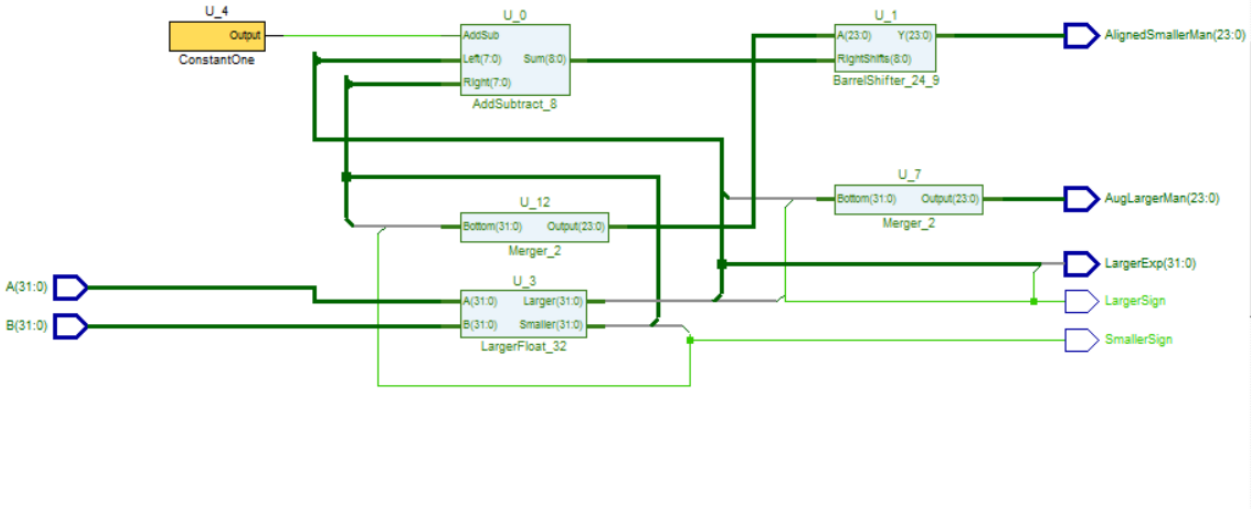
Jeffery You (jy9vm)

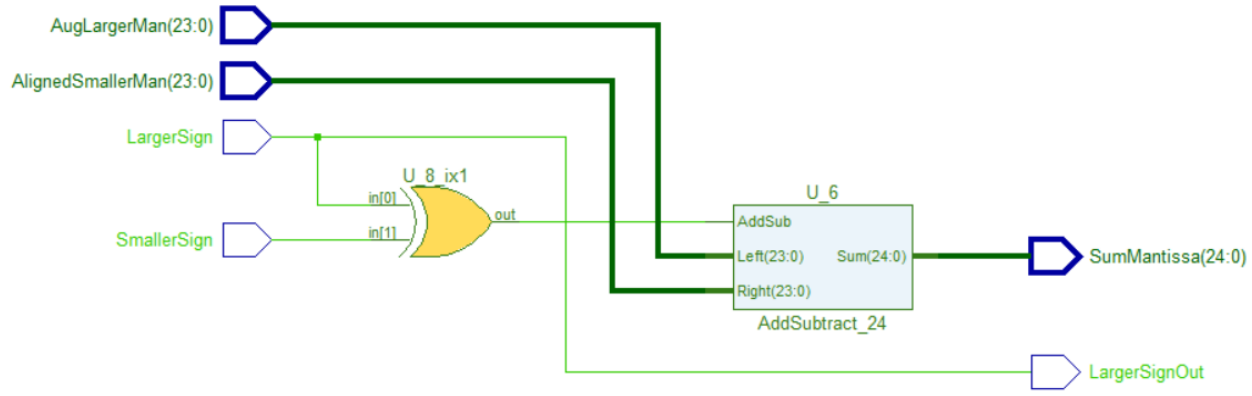
Lab #7 Report

Combinational Subtask #1



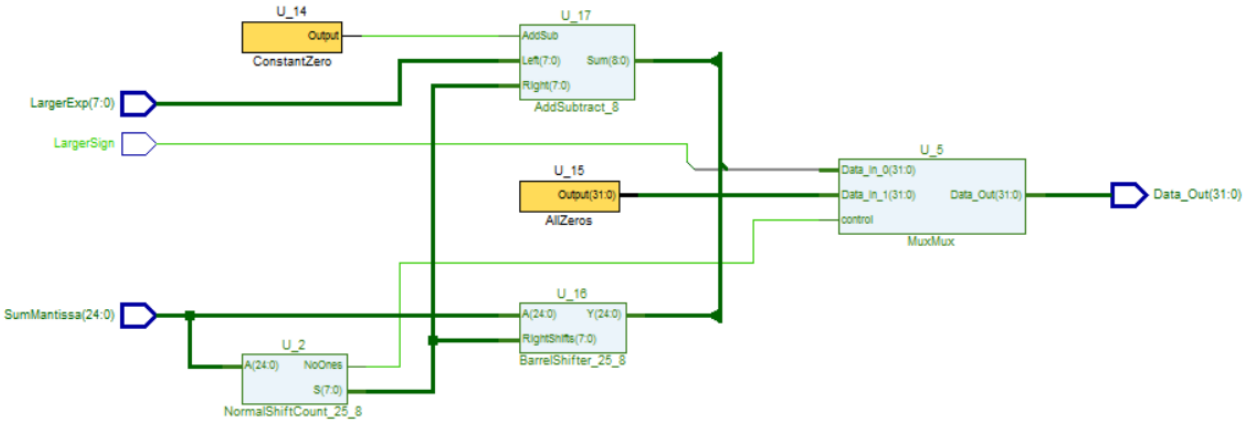
Schematic of the first Combinational Subtask block.

Combinational Subtask #2



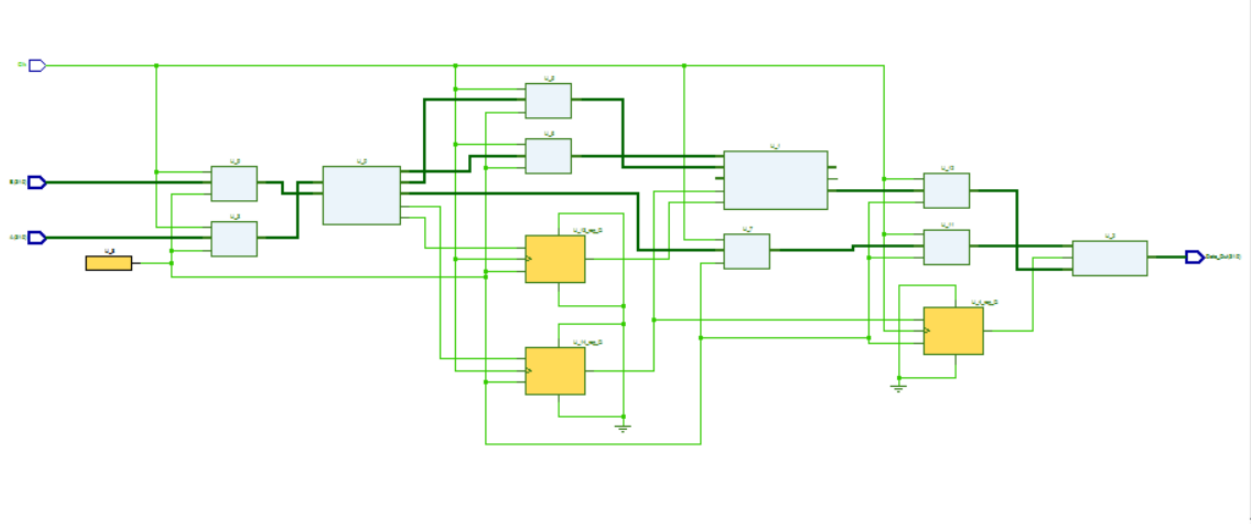
Schematic of the second Combinational Subtask block.

Combinational Subtask #3



Schematic of the third Combinational Subtask block.

Pipelining with All Pieces Together



Schematic of the entire pipelining schematic.

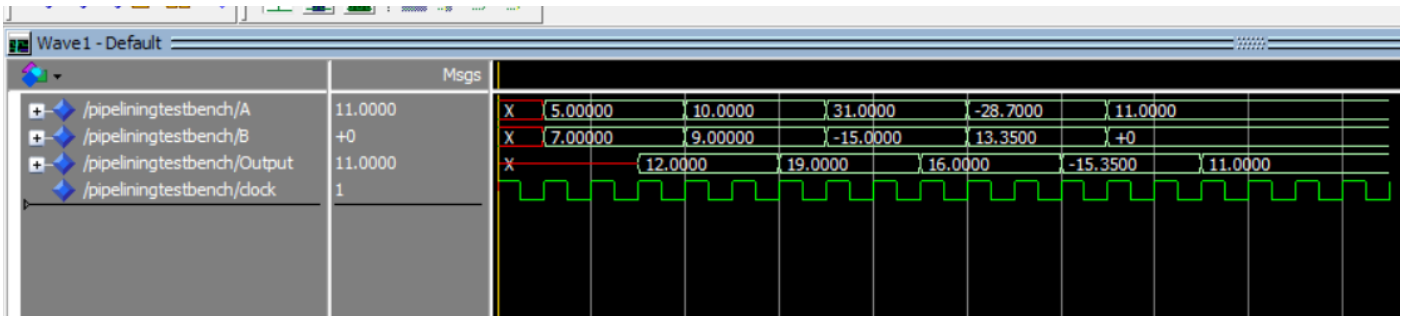
TestBench VHDL Code:

```
10  LIBRARY ieee;
11  USE ieee.std_logic_1164.all;
12  USE ieee.std_logic_arith.all;
13
14  ENTITY PipeliningTestBench IS
15  END ENTITY PipeliningTestBench;
16
17  --
18  ARCHITECTURE Behavior OF PipeliningTestBench IS
19     SIGNAL clock : std_logic;
20    Signal A, B, Output: std_logic_vector(31 DOWNTO 0);
21  BEGIN
22     DUT: ENTITY work.PipelineTogether(Struct)
23      PORT MAP(A=>A, B=>B, Data_Out=>Output, clk=>clock);
24    PROCESS
25      BEGIN
26        clock <= '1';
27        WAIT FOR 50 ns;
28        clock <= '0';
29        WAIT FOR 50 ns;
30      END PROCESS;
31    PROCESS
32      BEGIN
33        WAIT FOR 100 ns;
34        A<="01000000101000000000000000000000";
35        B<="01000000111000000000000000000000";
36        WAIT FOR 275 ns;
37        assert (Output = "01000001010000000000000000000000")
38          report "Test 1 Failure";
39        WAIT FOR 25 ns;
```

```
40
41          A<="01000001001000000000000000000000";
42          B<="01000001000100000000000000000000";
43          WAIT FOR 275 ns;
44          assert (Output = "01000001100110000000000000000000")
45            report "Test 2 Failure";
46          WAIT FOR 25 ns;
47
48          A<="01000001111110000000000000000000";
49          B<="11000001011100000000000000000000";
50          WAIT FOR 275 ns;
51          assert (Output = "01000001100000000000000000000000")
52           report "Test 3 Failure";
53          WAIT FOR 25 ns;
54
55          A<="11000001111001011001100110011010";
56          B<="01000001010101011001100110011010";
57          WAIT FOR 275 ns;
58          assert (Output = "11000001011101011001100110011010")
59            report "Test 4 Failure";
60          WAIT FOR 25 ns;
61
62          A<="01000001001100000000000000000000";
63          B<="00000000000000000000000000000000";
64          WAIT FOR 275 ns;
65          assert (Output = "01000001001100000000000000000000")
66            report "Test 5 Failure";
67          WAIT FOR 25 ns;
68          WAIT;
69      END PROCESS;
70  END ARCHITECTURE Behavior;
71
```

A 100 ns clock period is initially made. 5 different test cases were created. The program first WAITS 100 ns before inserting the first set of inputs to make sure they are correctly registered. Assertion is made within the 3rd clock cycle but before the 3rd cycle is completed.

TestBench Results:



This is the result of the testbench. Notice that the correct result for the floating point numbers A and B is outputted on the 3rd clock cycle after every time the two inputs changes.