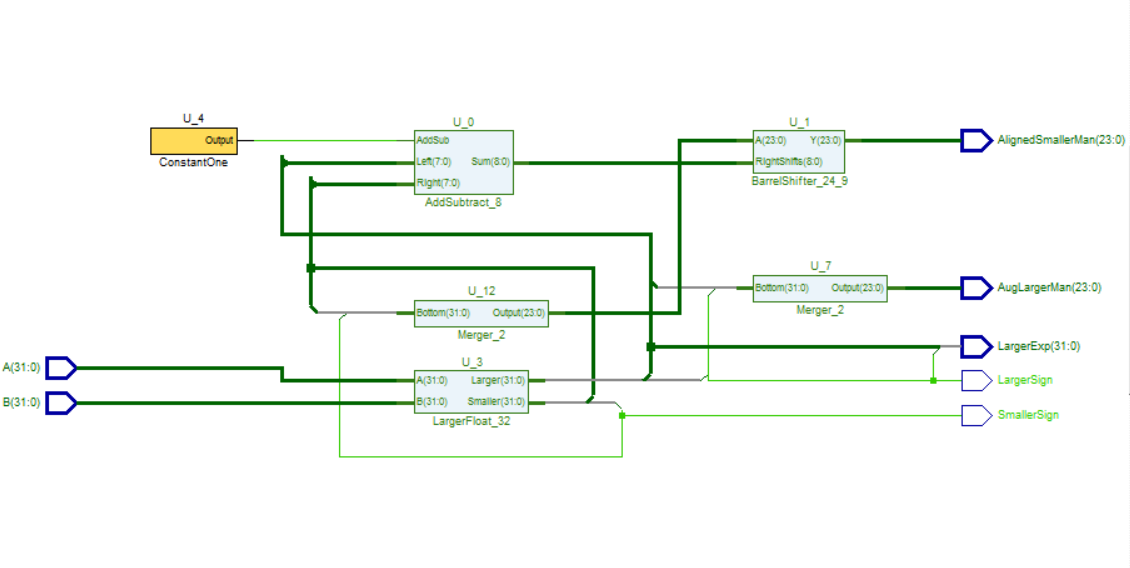
Jeffery You (jy9vm)

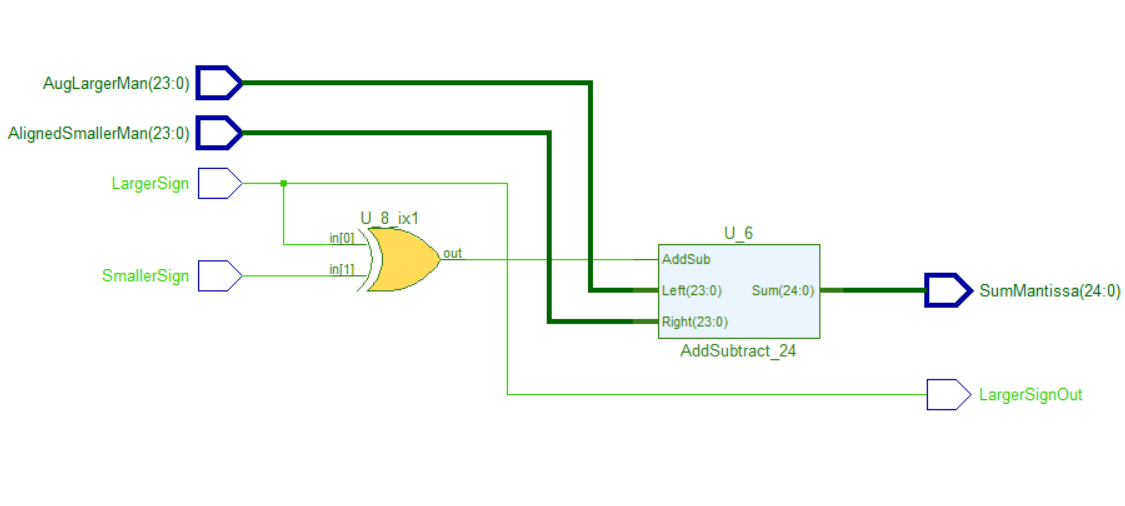
Lab #7 Report

*Combinational Subtask #1*



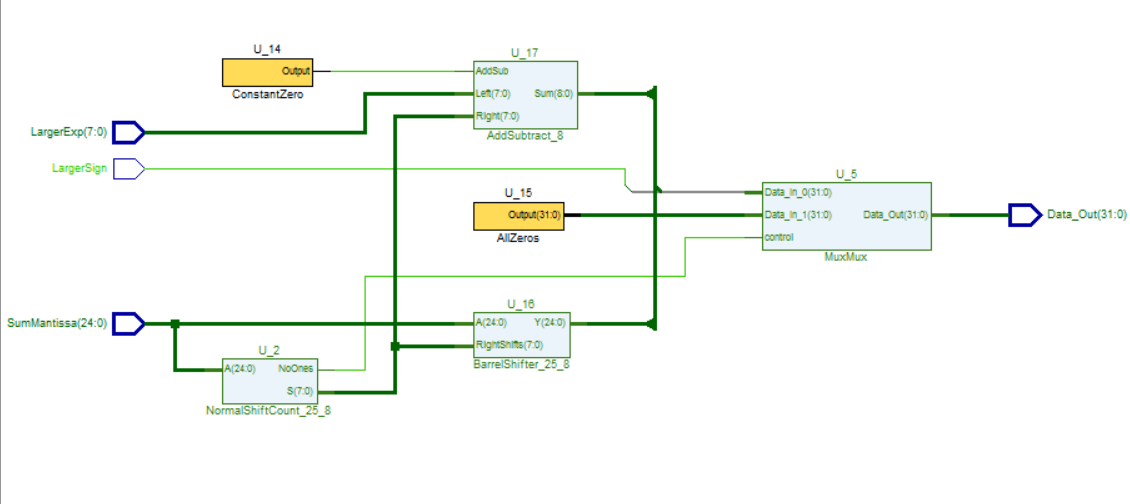
Schematic of the first Combinational Subtask block.

*Combinational Subtask #2*



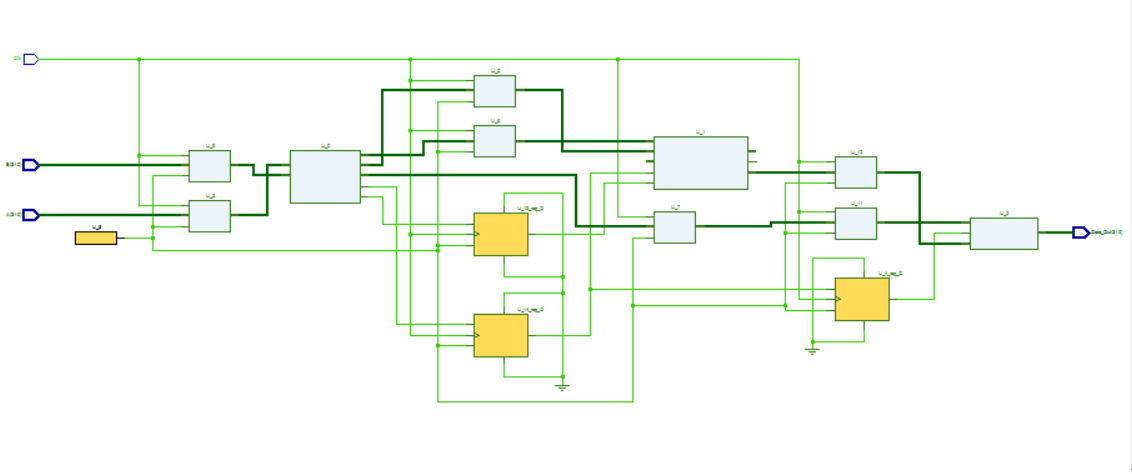
Schematic of the second Combinational Subtask block.

*Combinational Subtask #3*



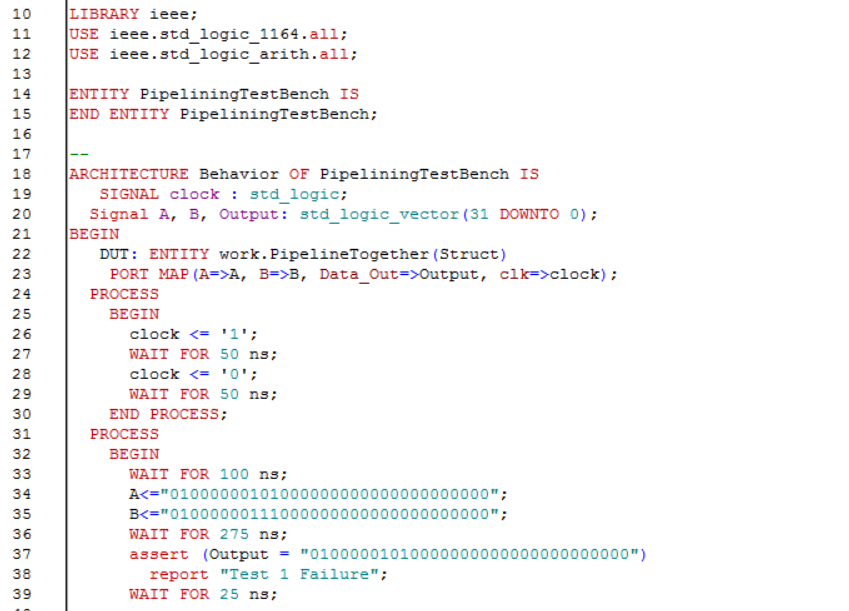
Schematic of the third Combinational Subtask block.

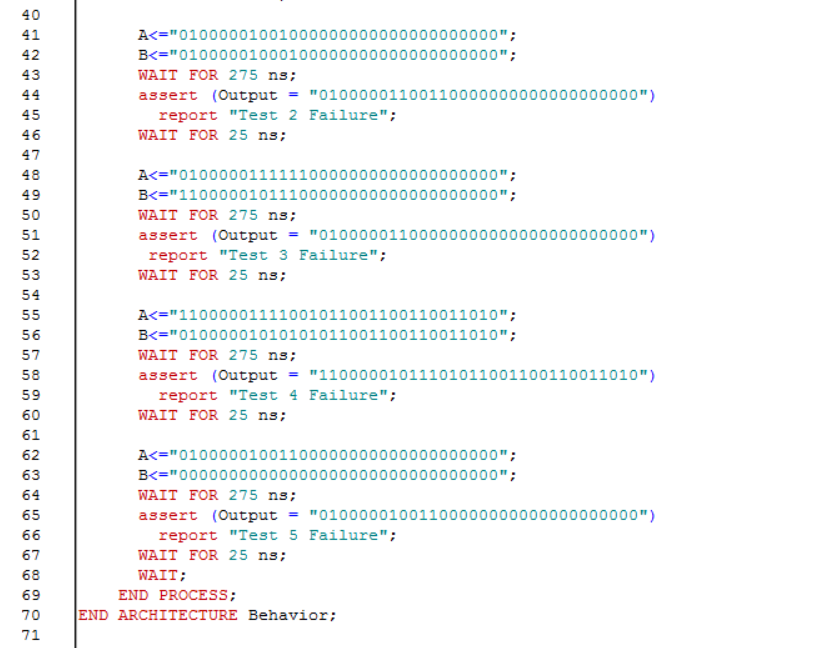
*Pipelining with All Pieces Together*



Schematic of the entire pipelining schematic.

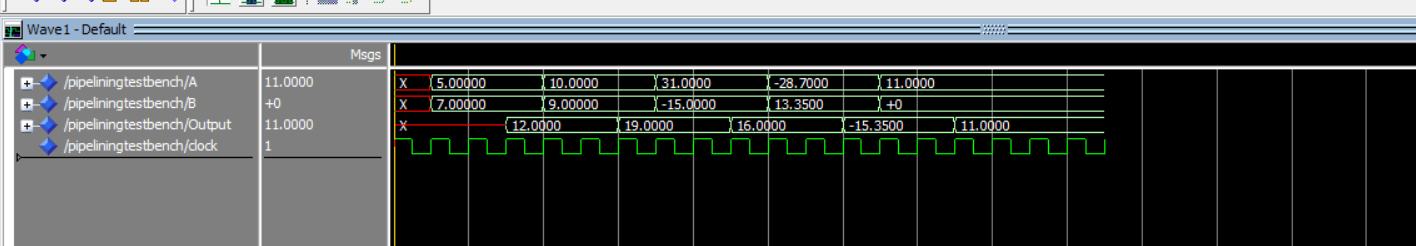
*TestBench VHDL Code:*





A 100 ns clock period is initially made. 5 different test cases were created. The program first WAITS 100 ns before inserting the first set of inputs to make sure they are correctly registered. Assertion is made within the 3rd clock cycle but before the 3rd cycle is completed.

*TestBench Results:*



This is the result of the testbench. Notice that the correct result for the floating point numbers A and B is outputted on the 3rd clock cycle after every time the two inputs changes.