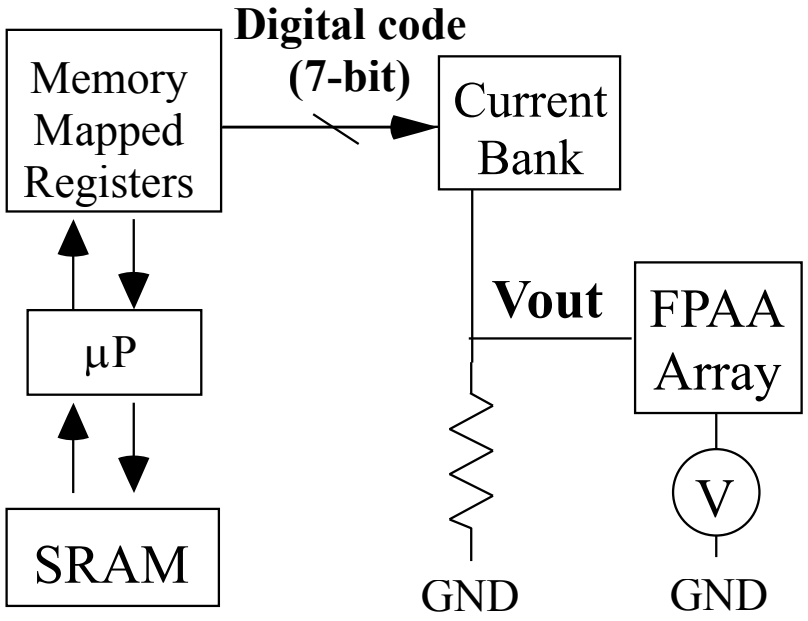
Block name: GENARB_f

Number of inputs: 0

Number of outputs: 1

Parameter list: Waveform Variable name, Sample rate

Block description: Arb Waveform (Arbitrary waveform generator) blocks, consisting of a current bank and a resistor, interface with the μP through memory mapped registers. The input is compiled as a vector on the SRAM. Run mode assembly code sends the input vector uploaded on SRAM to a memory mapped register at a given frequency.



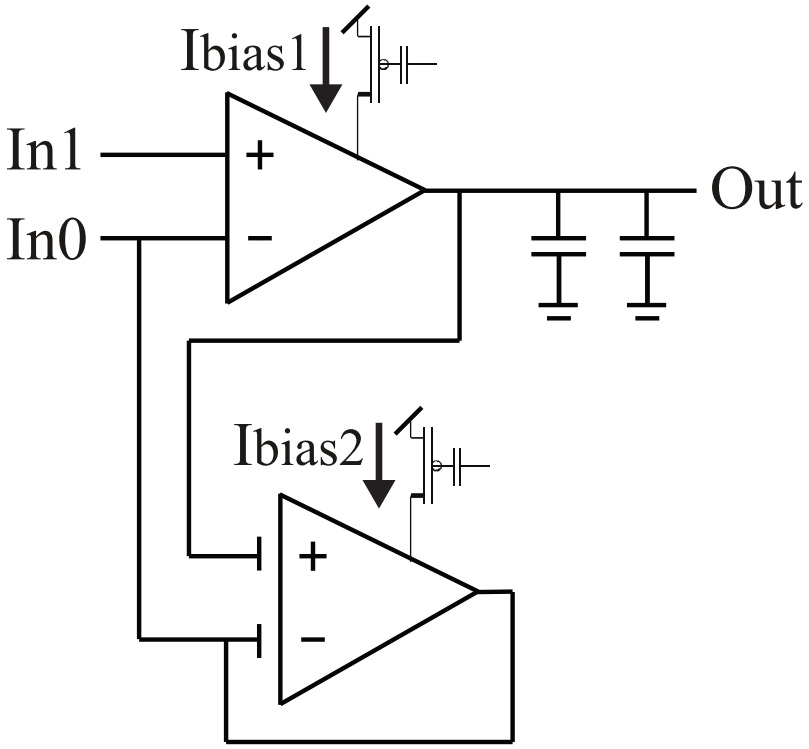
Block name: I_SenseAmp

Number of inputs: 2

Number of outputs: 1

Parameter list: I_SenseAmp_ota0_ibias, I_SenseAmp_fgota0_ibias, I_SenseAmp_fgota0_pbias, I_SenseAmp_fgota0_nibias, I_SenseAmp_cap0, I_SenseAmp_cap1

Block description: A Current Sense Amplifier block using an OTA, an FG OTA, and two capacitors. Ibias1 is I_SenseAmp_ota0_ibias, which has a default value of 2μA. Ibias2 is I_SenseAmp_fgota0_ibias, which has a default value of 2μA. The FGOTA's pbias is I_SenseAmp_fgota0_pbias, which has a default value of 2μA. The FGOTA's nbias is I_SenseAmp_fgota0_nbias, which has a default value of 2μA. It has two capacitor variables, which are I_SenseAmp_cap0 and I_SenseAmp_cap1.



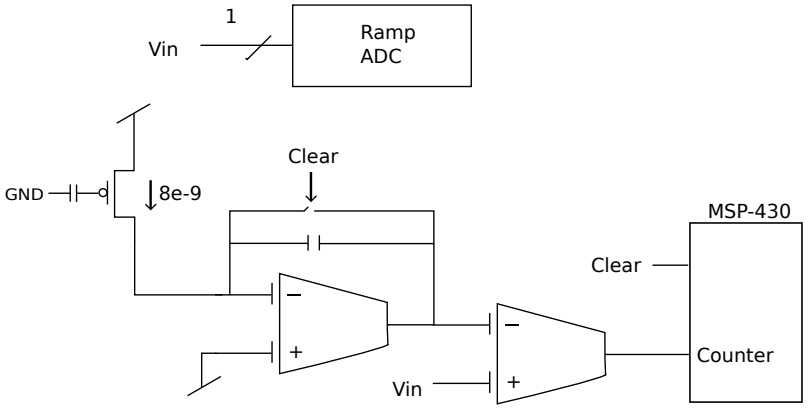
Block name: Ramp_ADC

Number of inputs: 1

Number of outputs: 0

Parameter list: NA

Block description: Single slope Analog to digital Converter. The input is to a FG comparator, which allows for higher dynamic range. The input current to the integrator is via a FG transistor and is set to 8nA. Advanced users could change this from inside the block defination to change number of bits and speed of the ADC. The counter is implemented on the processor on-chip. Take DATA button is used to get the output of the Ramp ADC. The output is stored in a .csv file called Results.csv. One can use the command Out=csvRead('Results.csv') to store it in a variable inside scilab. RAMP ADC performs data acquisition with a fixed sampling rate depending on the input voltage (100us maximum time between samples). Hence the sampling rate of the system will be determined by the sampling rate of the DAC (ARB GEN block).



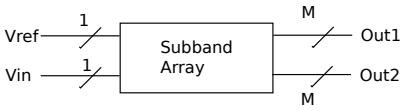
Block name: SubbandArray

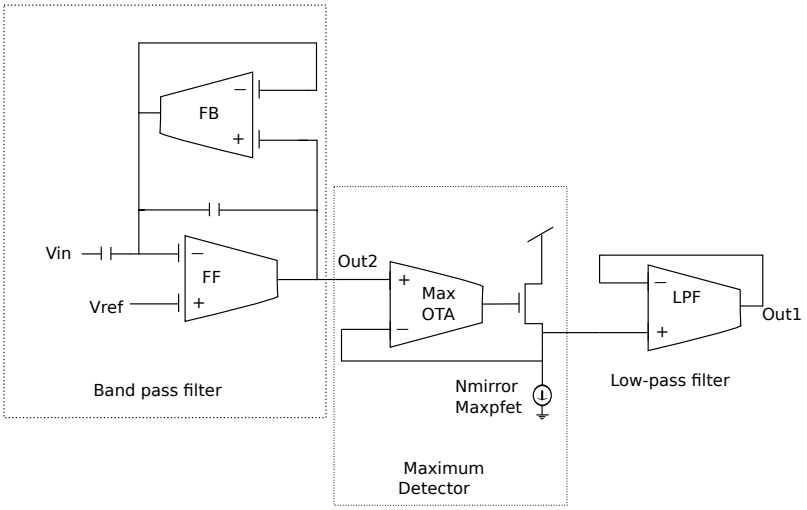
Number of inputs: 2

Number of outputs: 2

Parameter list: num_of_blk,SubbandArray_Maxpfet, SubbandArray_FBbias,SubbandArray_FBpbias,SubbandArray_FBnbias, SubbandArray_FFbias,SubbandArray_FFpbias,SubbandArray_FFnbias, SubbandArray_Maxota,SubbandArray_LPF,SubbandArray_FFcap, SubbandArray_FBcap

Block description: Analog Front-end used to extract frequency spectrum of a signal. The block consists of band-pass filter, maximum detector and Low-pass filter. Inputs are all connected to one node. Outputs are vectorized to have M.





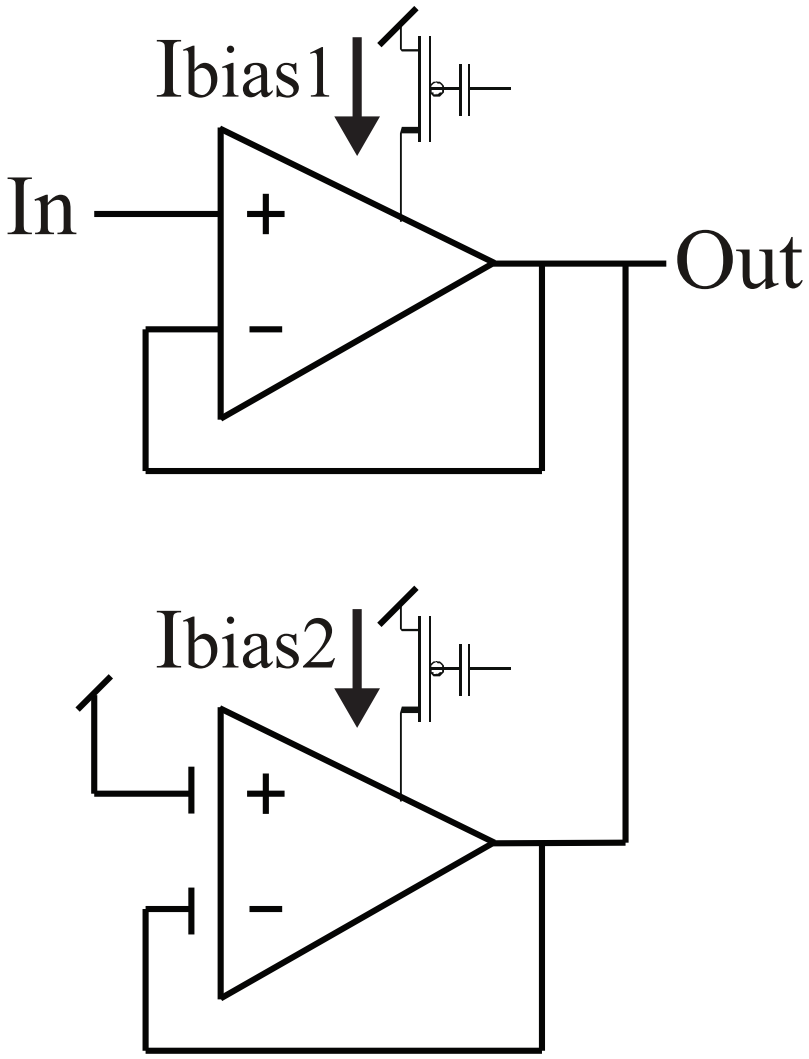
Block name: VolDivide1

Number of inputs: 1

Number of outputs: 1

Parameter list: VolDivide1_ota0_ibias, VolDivide1_fgota0_ibias, VolDivide1_fgota0_pbias, VolDivide1_fgota0_nbias

Block description: A Voltage divider block using an OTA and an FG OTA. Ibias1 is VolDivide1_ota0_ibias, which has a default value of 2μA. Ibias2 is VolDivide1_fgota0_ibias, which has a default value of 2μA. The FGOTA's pbias is VolDivide1_fgota0_pbias, which has a default value of 2μA. The FGOTA's nbias is VolDivide1_fgota0_nbias, which has a default value of 2μA.



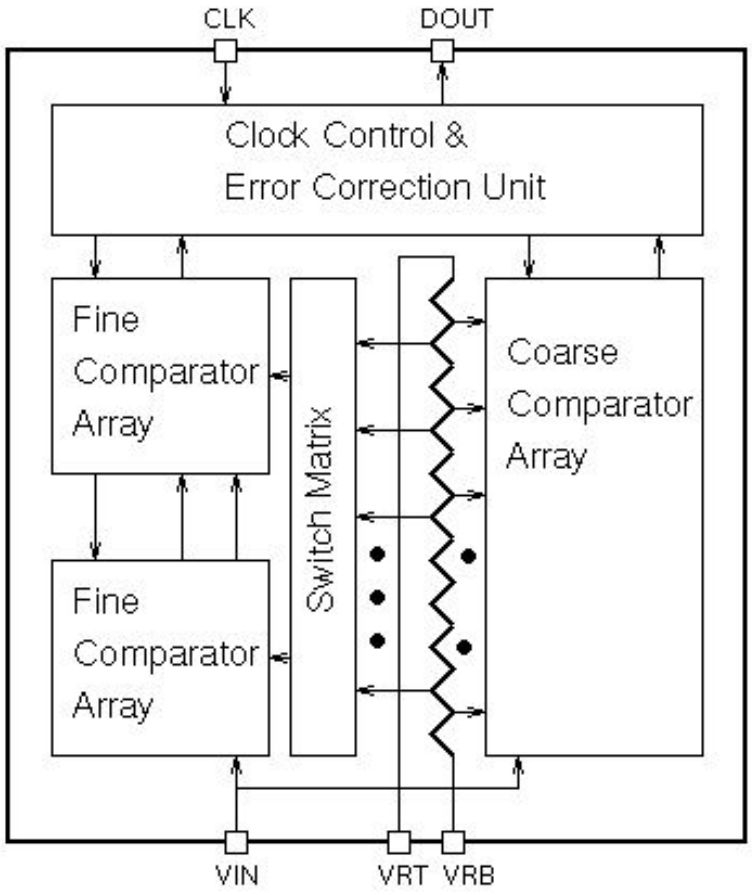
Block name: adc_ip

Number of inputs: 1

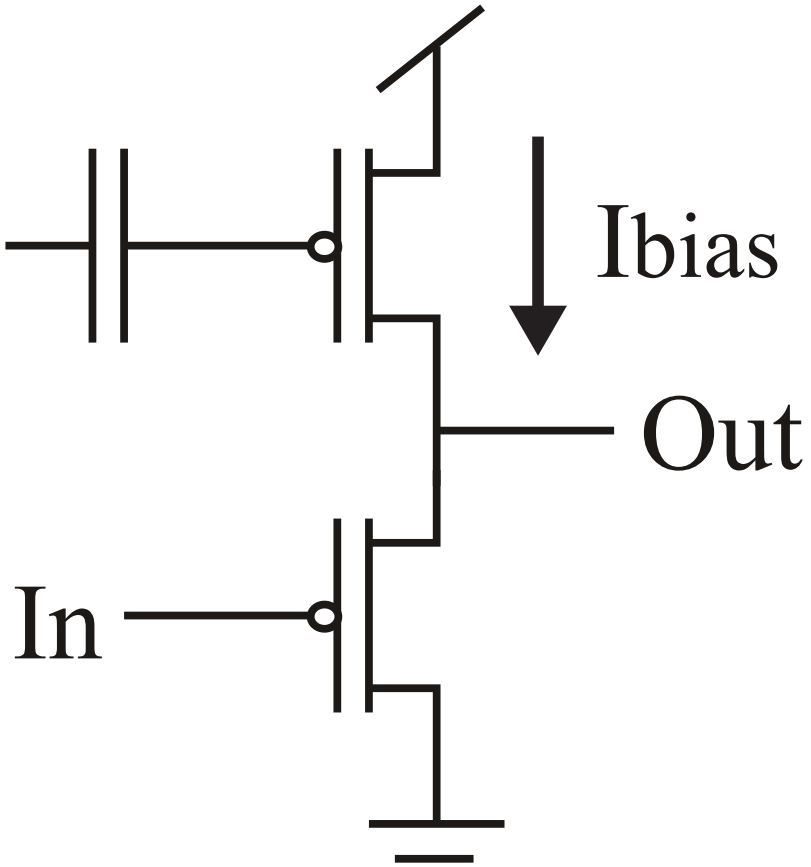
Number of outputs: 0

Parameter list: none

Block description: ADC (8bit 20MHz) is an 8-bit CMOS A/D converter (TAD3308A), which is a TSMC IP blcok. The cell receives analog input signal and decodes to digital output signals. Sampling rate is controlled by the clock input signal.



Block name: common_drain
Number of inputs: 1
Number of outputs: 1
Parameter list: common_drain_fgswc_ibias
Block description: A common drain circuit using a pFET and FG device. The parameter, common_drain_fgswc_bias, sets the bias current, which has a default value of 50nA.



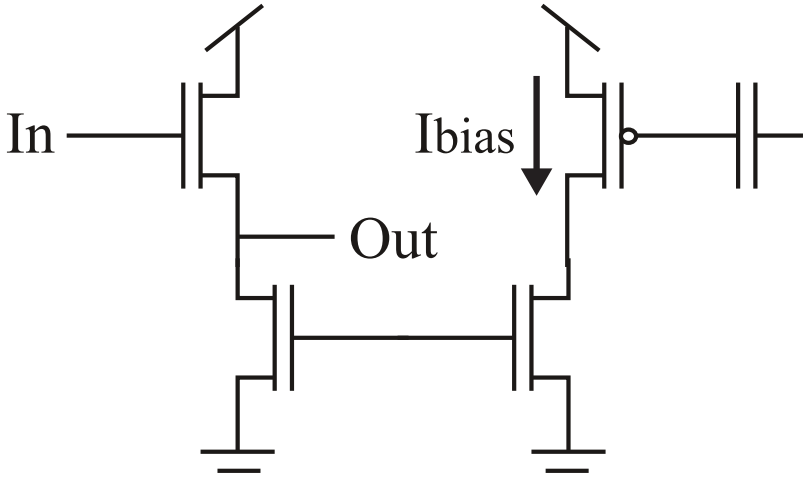
Block name: common_drain_nfet

Number of inputs: 1

Number of outputs: 1

Parameter list: common_drain_nfet_ibias

Block description: A common drain circuit using a nfet and a current mirror with a FG device setting the bias current. The parameter, common_drain_nfet_ibias, sets the bias current, which has a default value of 50nA.



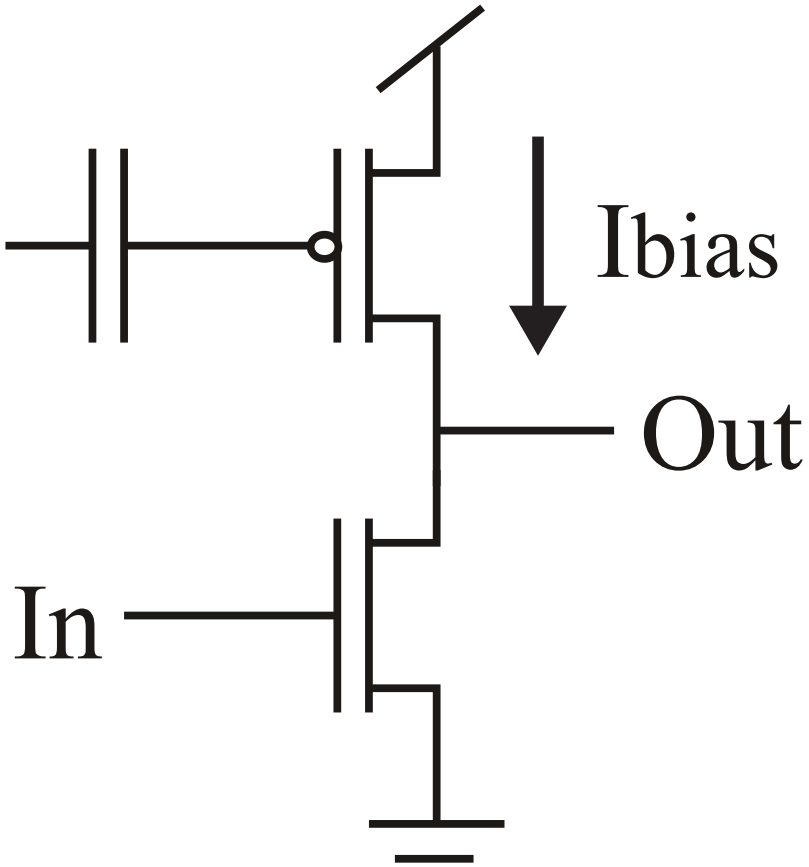
Block name: common_source

Number of inputs: 1

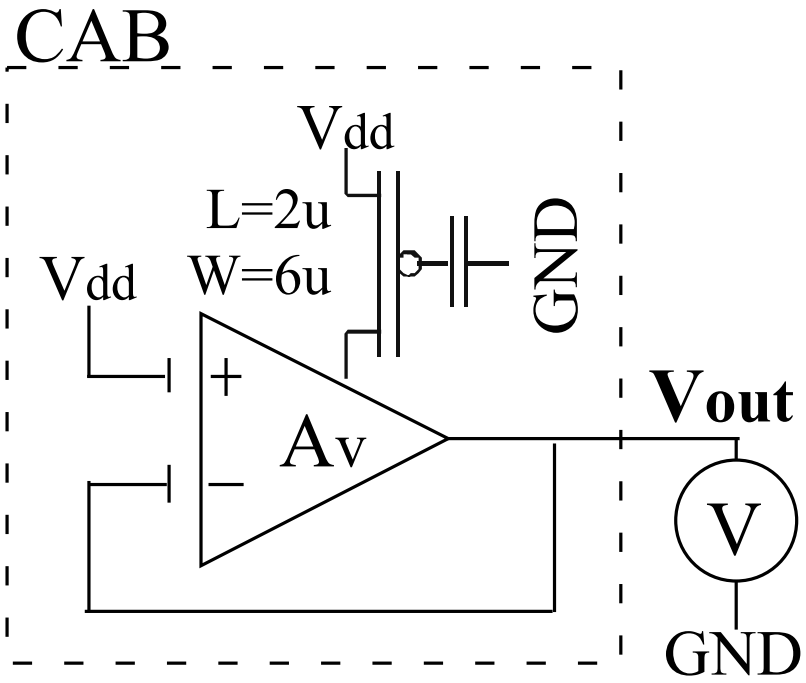
Number of outputs: 1

Parameter list: common_source_ibias

Block description: A common source circuit using a nFET and FG device. The parameter, common_source_ibias, sets the bias current, which has a default value of 50nA.



Block name: dc_in
Number of inputs: 0
Number of outputs: 1
Parameter list: DC Value
Block description: DC Voltage: A compiled block in a CAB to set a DC voltage, comprises of an FG OTA in a unity-gain follower configuration.



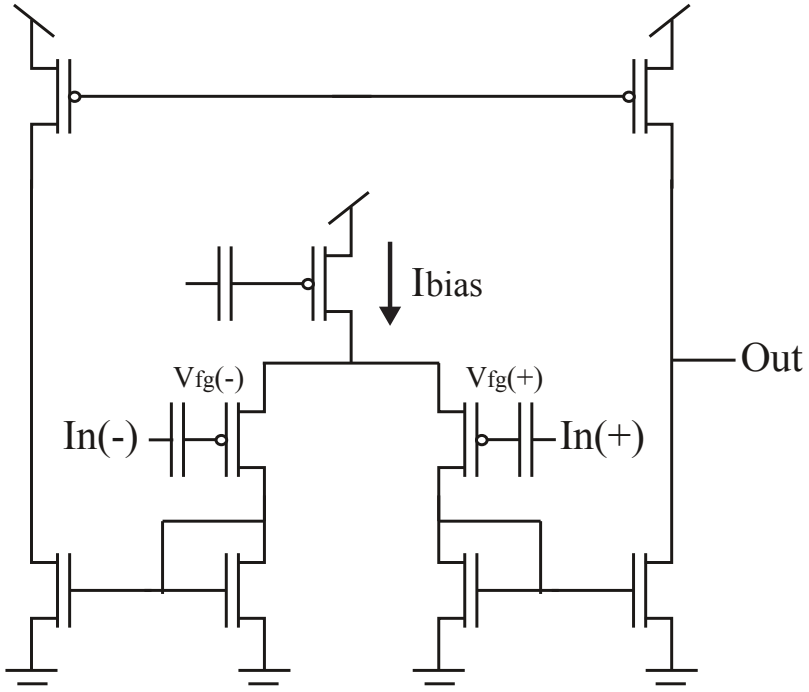
Block name: fgota

Number of inputs: 2

Number of outputs: 1

Parameter list: Ibias, Vfg_n, Vfg_n, small_cap

Block description: A nine transistor OTA block with input FG devices, which is one analog element blocks. Ibias controls the bais current. Vfg_n and Vfg_p define input FG pFET's floated node voltage, respectively.



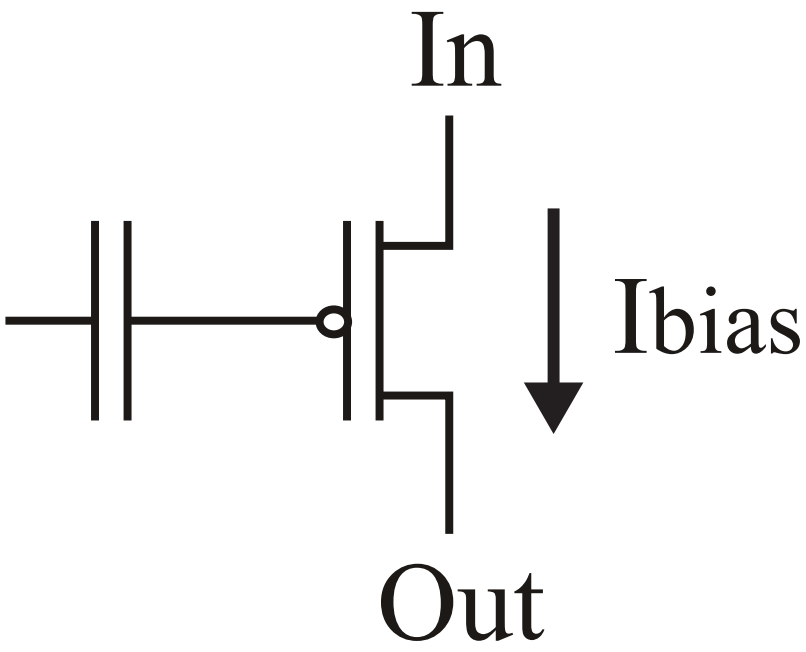
Block name: fgswitch

Number of inputs: 1

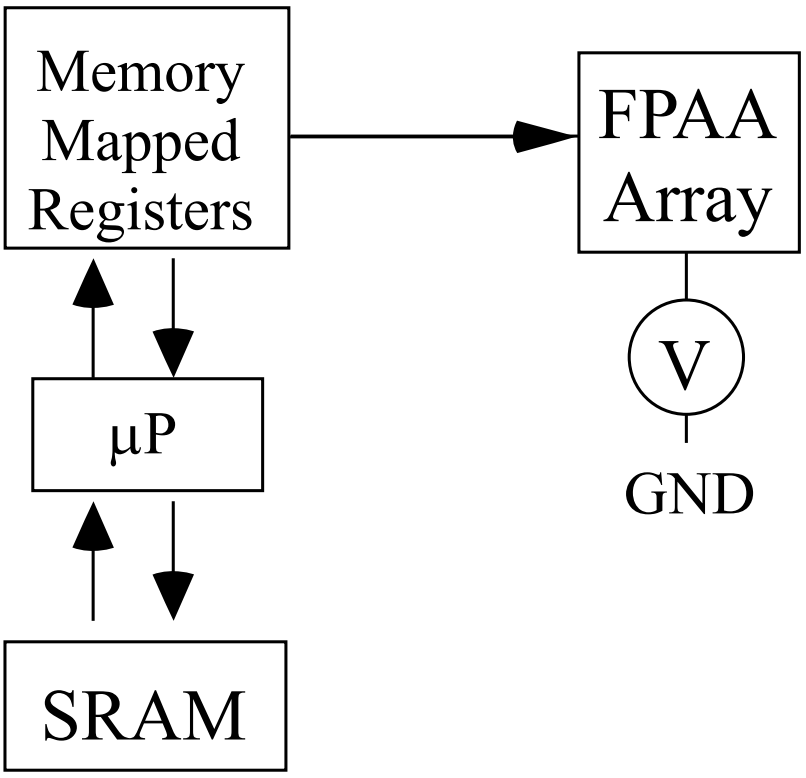
Number of outputs: 1

Parameter list: fgswitch_fgswc_ibias

Block description: An FG switch. fgswitch_fgswc_ibias controls the bais current.



Block name: gpio_in
Number of inputs: 0
Number of outputs: 1
Parameter list: GPIO IN Variable name, sample rate
Block description: Digital In blocks interfacing with the μP through memory mapped registers.



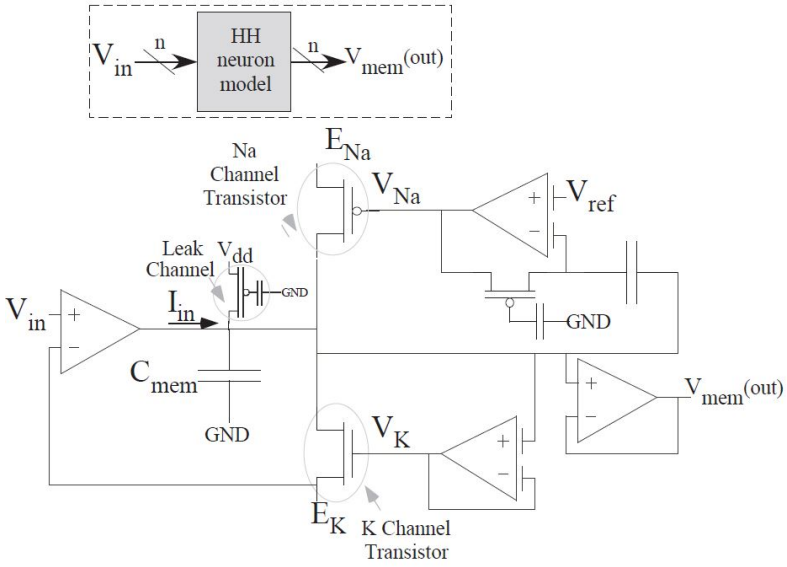
Block name: hhn

Number of inputs: 4

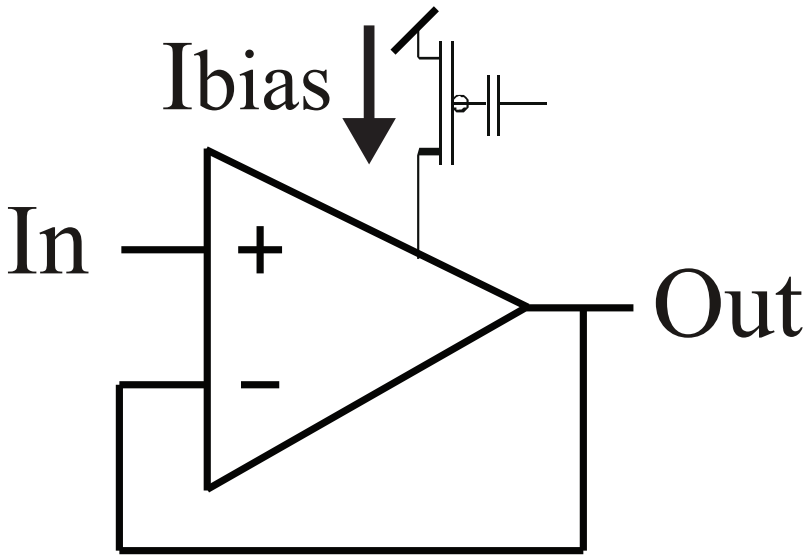
Number of outputs: 1

Parameter list: hhn_fgswc_ibias, hhn_fgota1_ibias, hhn_fgota1_pbias, hhn_fgota1_nbias, hhn_fgota0_ibias, hhn_fgota0_pbias, hhn_fgota0_nbias, hhn_ota0_ibias, hhn_ota1_ibias, hhn_cap0

Block description: a Hodgkin Huxley neuron circuit.



Block name: lpfota
Number of inputs: 1
Number of outputs: 1
Parameter list: Cutoff_freq
Block description: A low pass filter block using an OTA. The default value of cutoff frequency is set to 21.7 Hz.



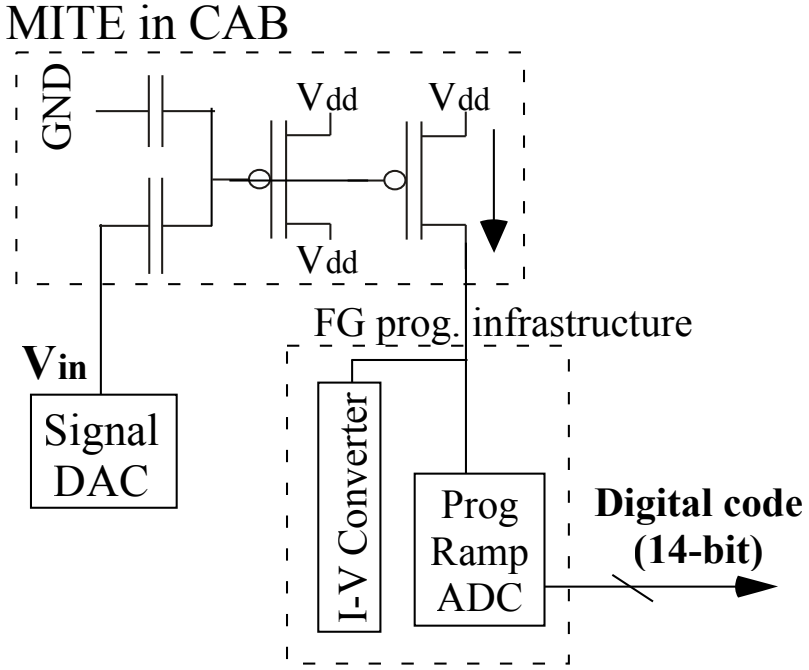
Block name: meas_volt

Number of inputs: 1

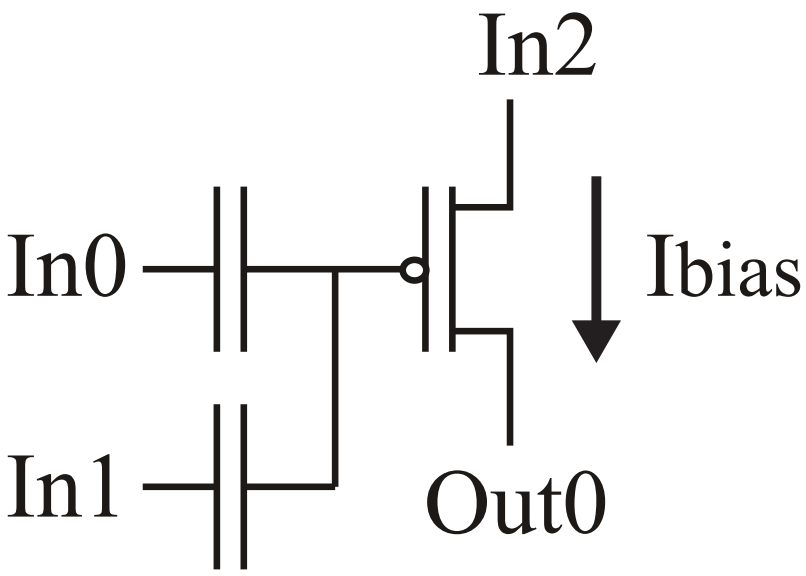
Number of outputs: 0

Parameter list: Variable name, sample rate

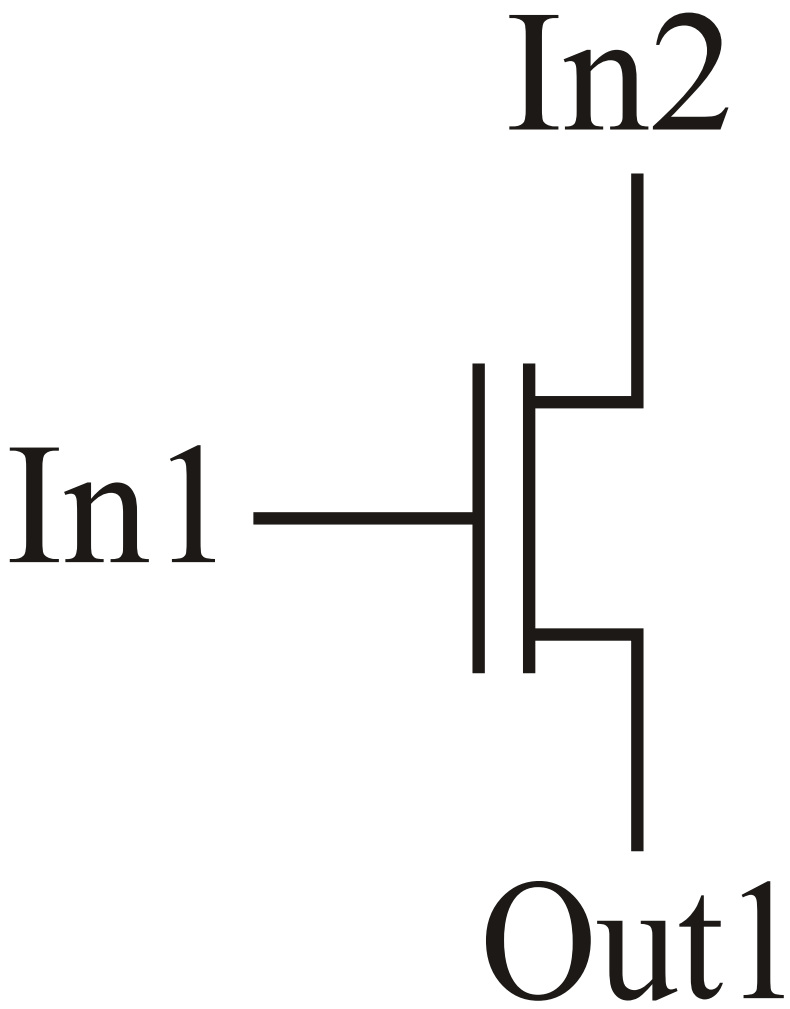
Block description: An ADC block using a Multiple-Input Translinear Element (MITE) device in a CAB couples , which is measured by a pFET diode I-V converter and a 14-bit ramp ADC in the program infrastructure.



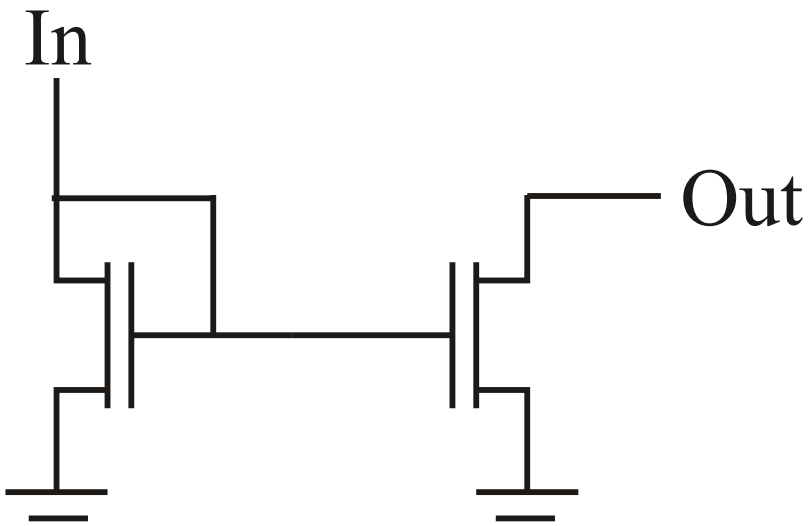
Block name: mite_FG
Number of inputs: 3
Number of outputs: 1
Parameter list: MITE_current
Block description: A MITE (Multiple-Input Translinear Element) block. MITE_current controls the bais current.



Block name: nfet
Number of inputs: 2
Number of outputs: 1
Parameter list: No.
Block description: n-type MOSFET.



Block name: nmirror
Number of inputs: 1
Number of outputs: 1
Parameter list: none
Block description: An nmirror circuit element in CAB.



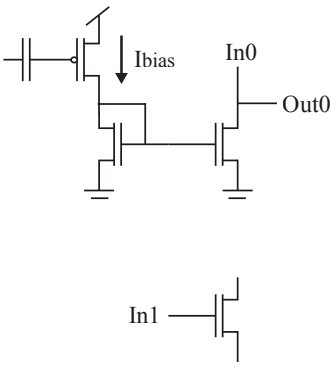
Block name: nmirror_w_bias

Number of inputs: 2

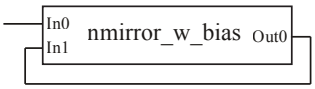
Number of outputs: 1

Parameter list: nmirror_w_bias_ibias

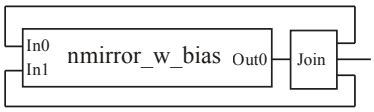
Block description: An nmirror circuit with a FG bias current. Ibias is nmirror_w_bias_ibias, which has a default value of 50 nA.



When input is in use:



When output is in use:



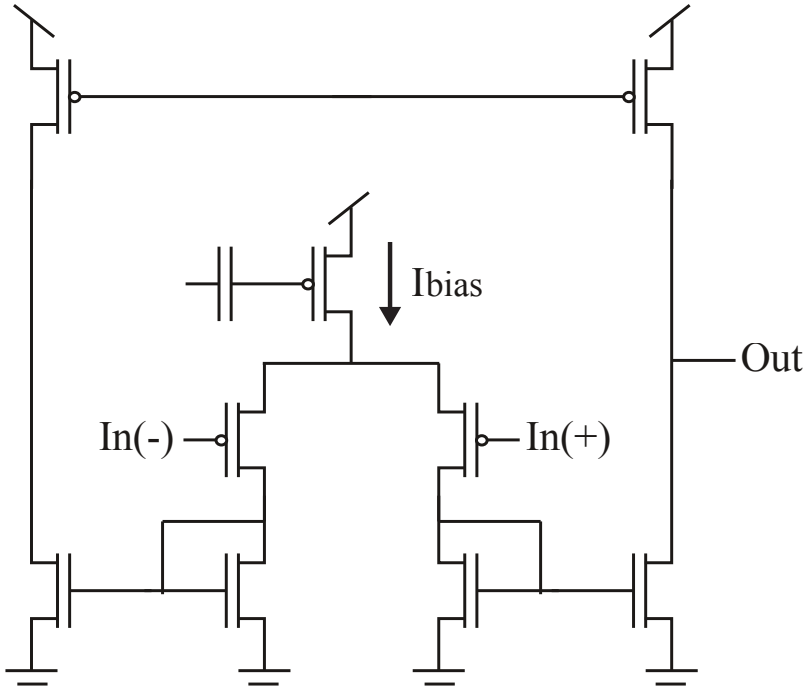
Block name: ota

Number of inputs: 2

Number of outputs: 1

Parameter list: ibias

Block description: A nine transistor OTA block, which is one analog element blocks. Ibias controls the bais current.



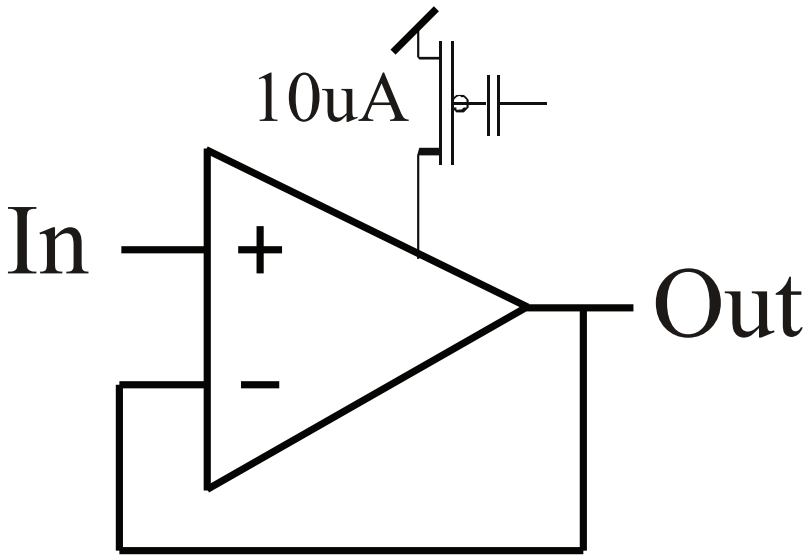
Block name: ota_buf

Number of inputs: 1

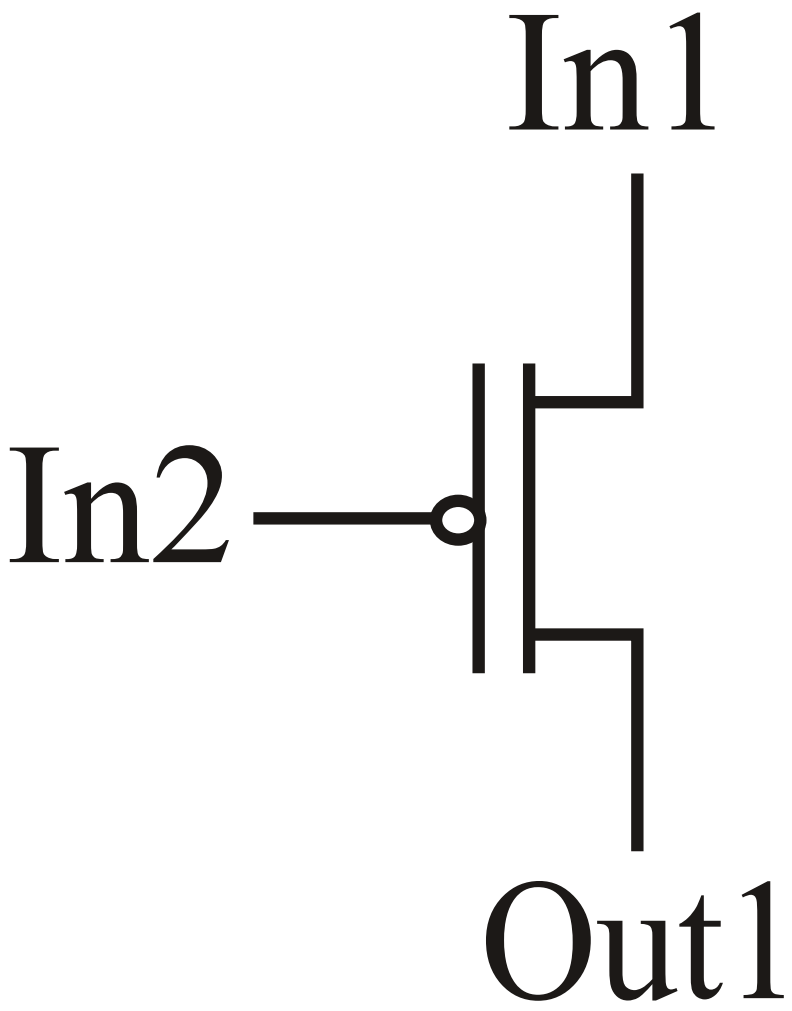
Number of outputs: 1

Parameter list: none

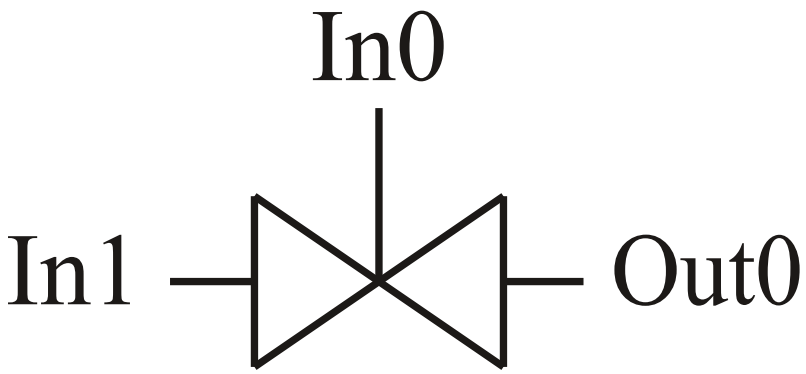
Block description: An analog buffer using an OTA. The bias current is set to 10μA.



Block name: pfet
Number of inputs: 2
Number of outputs: 1
Parameter list: no
Block description: p-type MOSFET.



Block name: tgate
Number of inputs: 2
Number of outputs: 1
Parameter list: none
Block description: A T-gate element in CAB.



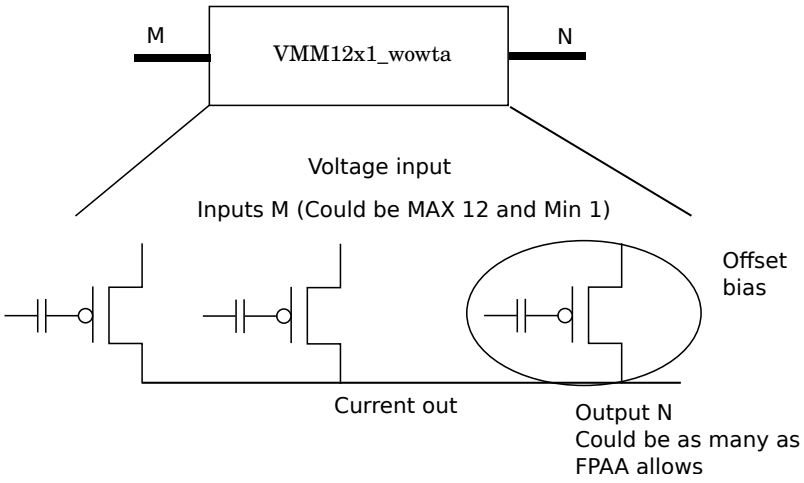
Block name: vmm12×1_wowta

Number of inputs: 12

Number of outputs: 1

Parameter list: Input_Dimensions, Weight_Matrix, Offset_bias

Block description: This is a Vector Matrix Multiplie circuit built using Floating Gate (FG) pFET transistors. There are 12 input FG pFET transistors and an offset FG transistor. Input_Dimensions has row and column depending on inputs for your VMM one can have minimum of 1 input to maximum of 12 inputs. Output columns can be as many allowed by FPAA. Each VMM block will sit in a different CAB. The inputs and outputs are vectorized.



Block name: wta_new

Number of inputs: 3

Number of outputs: 1

Parameter list: number of blocks, wta_new_buf_bias, wta_new_wta_bias

Block description: A vectorized version of WTA circuit. Classic work on winner take all circuit (*https* : *//papers.nips.cc/paper/*151 − *winner* − *take* − *all* − *networks* − *of* − *on* − *complexity.pdf*) please read it before attempting to compile. This WTA has a FG pFET load (wta_new_wta_bias) at the output. Its output is voltage and input is current (usually used with VMM12x1_wowta). The output is buffered using ota in a follower configuration (wta_new_buf_bias). The first input and the output are vectorized where as the second and third input are common.