Canny Edge Detector

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This project will create an ASIC that is capable of accurately performing Canny edge detection. The input to the chip will be image files in their original form. The output of the chip will be modified image files that have been created using the Canny edge detection process on the original image. The edge detection process will consist of five major steps: image smoothing, gradient magnitude calculation, directional non-maximum suppression, threshold calculation, and hysteresis thresholding.

Many people are very interested in various kinds of image processing. Image processing can transform original images into images that are much more interesting to look at. The Canny edge detection algorithm offers a kind of image processing that highlights the edges in pictures and makes these edges much easier for the viewer to see. Potential users of this ASIC include both people simply looking to make rather plain images into something more exciting to look at as well as people wanting to identify the distinct edges within an image for some kind of analytical purpose.

This design is more appropriate for an ASIC rather than a microprocessor for several reasons. First of all, high-speed performance is necessary in order for the edge detection process to run in a reasonable amount of time for an average size image. The performance offered by a microprocessor is simply not enough to satisfy this requirement. Also, with an ASIC it is possible to take advantage of parallel processing which will again help with speed and will make the mathematical operations necessary for Canny edge detection much easier to implement.

BLOCK DIAGRAM of the Canny Edge Detection Algorithm